芯颖科技有限公司
CHIP WEALTH TECHNOLOGY LTD.

CH13613

480RGB x 480 dot
AMOLED Mobile Single Chip Driver

1 DESCRIPTION

The CH13613 device is a single-chip solution for LTPS AMOLED that incorporates gate drivers and is capable of 480RGBx480, 454RGBx454, 400RGBx400, 360RGBx360, 320RGBx480, 320RGBx360, 320RGBx320, 320RGBx290, 300RGBx300, 272RGBx340, 272RGBx480, 264RGBx296, 240RGBx240, 240RGBx320, 240RGBx720, 180RGBx360, 180RGBx540 with internal GRAM. It includes a 2,764,800 bits internal memory, a timing controller with glass interface level-shifters and a glass power supply circuit.

The CH13613 supports MIPI Interface, serial peripheral interfaces (SPI), dual serial peripheral interfaces (Dual-SPI) and quad serial peripheral interfaces (Quad-SPI). The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The CH13613 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores 480-RGB x 480-dot 16.77M-color images. A deep standby mode is also supported for lower power consumption. This LSI is suitable for wearable device applications, including I-watch and smart band.

2 Features

■ Single chip AMOLED Controller/driver.

■ 240 channels source driver.

■ Display Resolutions

- 480RGB x (100+2NL)
- 454RGB x (100+2NL)
- 420RGB x (100+2NL)
- 400RGB x (100+2NL)
- 360RGB x (100+2NL)
- 320RGB x (100+2NL)
- 300RGB x (100+2NL)
- 272RGB x (100+2NL)
- 264RGB x (100+2NL)
- 240RGB x (100+2NL)
- 180RGB x (100+2NL)

■ Display data frame memory

- RAM size: 2,764,800 bits (480 x 480 x 24 bits*1/2)

■ Display mode (Color mode)

- Full color mode: 16.7M colors
- Reduce color mode: 262K colors
- Reduce color mode: 65K colors
- Reduce color mode: 4096 colors
- Idle mode: 16.7M colors, 262K colors , 65K colors , 4096 colors , 8 colors

■ Interface

- Serial peripheral interface (SPI)
- Dual serial peripheral interface (Dual-SPI)
- Quad serial peripheral interface (Quad-SPI)
- MIPI Display Serial Interface (1 clock and 2 data lane pairs)
  - ➢ Support 1lane/2lane (1lane: 500Mbps)
  - ➢ Maximum total bit rate is 500Mbps of 24-bit data format/ 360Mbps of 18-bit data format/320Mbps of 16-bit data format

■ Display features:

- Built-in digital R/G/B separate gamma correct circuit
- Source output mirror function
- Source support MUX1:6,1:9,1:12
- Partial display function
- Deep standby function

■ Supply voltage range

- Regulator and I/O power supply for VDDIO,VDDR: 1.65 ~ 3.6V
- Analog power supply for VDDA,VDDB: 2.7 ~ 3.6V

■ Output voltage range

- Step-up output voltage range for AVDD:4.5 ~ 6.5V(2*VDDB,3*VDDB)
- Step-up output voltage range for AVEE: -1*VDDB,-2*VDDB
- gamma highest voltage range for VGM: 2.0V ~ 6.3V (10mV/step,max:AVDD-0.2)
- gamma lowest voltage range for VGS: 0,0.2V ~ 4.5V(10mV/step)
- Positive gate driver voltage range for VGH: AVDD, AVDD+VDDB,2AVDD
- Negative gate driver voltage range for VGL: AVEE,AVEE-VDDB,AVEE-AVDD
- Positive gate driver voltage range for VGHO : 3.0V ~ 10V(0.5V/step)

- Negative gate driver voltage range for VGLO: -10V ~ -3.0V (0.5V/step)
- Pixel reset voltage range for VREFP: 0.5V ~ 5.0V (0.1V/step, max:AVDD-0.2)
- Pixel reset voltage range for VREFN: -5.0V ~ -0.2V(0.1V/step, max:AVEE+0.2)
- Step-up output positive voltage for ELVDD(VEP): 2.0V~5V(0.1V/step)
- Step-up output negative voltage for ELVSS(VEN):0,-0.2V~-5V(0.1V/step)

■ On chip:

- Brightness control
- Support HBM function(High brightness mode)
- Support Sunlight Readability enhancement function
- Support circular edge optimization algorithm
- Support oblique line optimization algorithm
- Support notch algorithm
- Support AOD function
- Support De-burn-in function
- Support Dynamic ELVSS
- Support gate control signals to gate driver on the panel
- Internal oscillator for display clock
- Support OTP for adjusting gamma/timing parameters

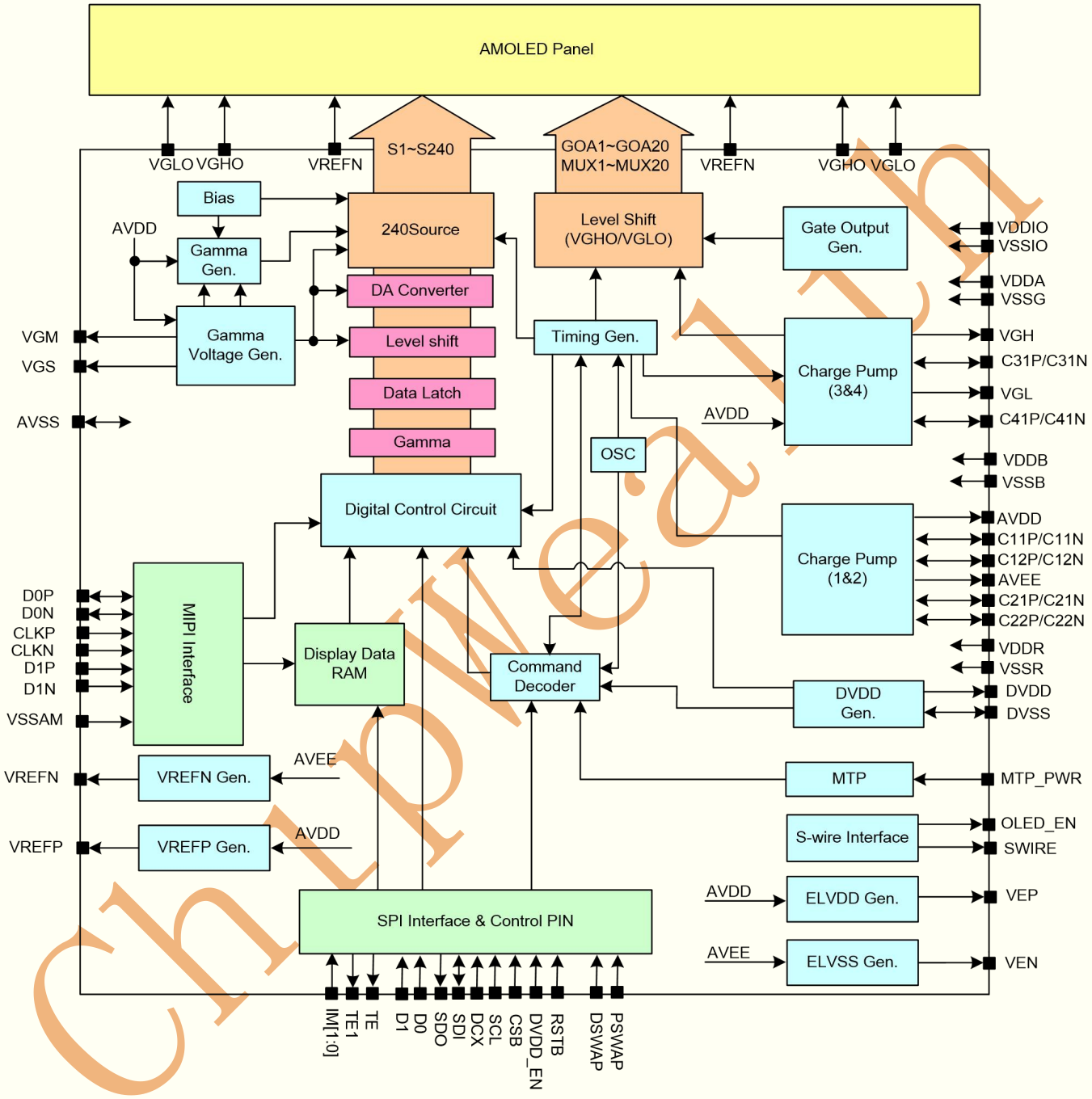
■ PKG

- COF/COG

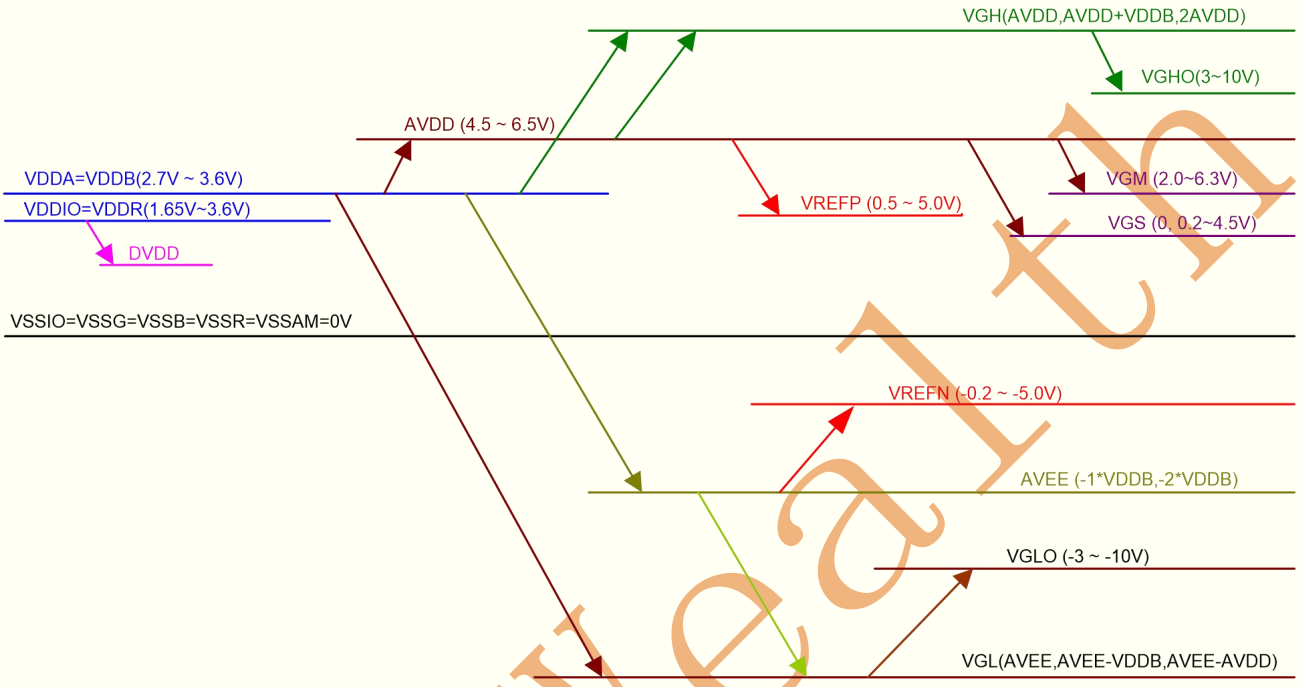
■ Chip size: 8300um x 1580um

3 Device Over View

3.1 Block Diagram



3.2 POWER GENERATION CIRCUIT



3.3 EXTERNAL COMPONENTS CONNECTION

Pad Name	Connection	Typical Value
VDDIO/ VDDR	Connect to Capacitor (Max 6V): VDDIO/ VDDR ------||------ GND	2.2μF
VDDA/ VDDB	Connect to Capacitor (Max 6V): VDDA/ VDDB ------||------ GND	2.2μF
DVDD	Connect to Capacitor (Max 6V): DVDD------||------ GND	2.2μF
VSSIO	Interface ground(Connect to GND)	-
VSSR	Regulator ground(Connect to GND)	-
VSSAM	MIPI ground (Connect to GND)	-
VSSB	Pump ground (Connect to GND)	-
DVSS	Digital logic ground (Connect to GND)	-
VSSG	Analog gray ground (Connect to GND)	-
AVSS	Source OP ground (Connect to GND)	-
C11P, C11N	Connect to Capacitor (Max 10V): C11P ------||------ C11N	1.0μF
C12P, C12N	Connect to Capacitor (Max 10V): C12P ------||------ C12N	1.0μF
C21P, C21N	Connect to Capacitor (Max 10V): C21P------||------ C21N	1.0μF
C22P, C22N	Connect to Capacitor (Max 10V): C22P ------||------ C22N	1.0μF
C31P, C31N	Connect to Capacitor (Max 16V): V31P ------||------ C31N	1.0μF
C41P, C41N	Connect to Capacitor (Max 16V): V41P ------||------ C41N	1.0μF
AVDD	Connect to Capacitor (Max 10V): AVDD ------||------ GND	2.2μF
AVEE	Connect to Capacitor (Max 10V): AVEE ------||------ GND	2.2μF
VGH	Connect to Capacitor (Max 16V): VGH ------||------ GND	1.0μF
VGL	Connect to Capacitor (Max 16V): VGL --------||-------- GND └----►|------ GND	2.2μF D1(Note 1)
VREFP	Connect to Capacitor (Max 10V): VREFP ------||------ GND	2.2μF(Note 2)
VREFN	Connect to Capacitor (Max 10V): VREFN ------||------ GND	2.2μF
VEP	Connect to Capacitor (Max 10V): VEP ------||------ GND	2.2uF(Note 2)
VEN	Connect to Capacitor (Max 10V): VEN ------||------ GND	2.2μF(Note 2)
VGHO	Connect to Capacitor (Max 16V): VGHO ------||------ GND	1.0μF
VGLO	Connect to Capacitor (Max 16V): VGLO ------||------ GND	1.0μF
VREF	Connect to Capacitor (Max 6V): VREF ------||------ GND	2.2μF
VGM	No Capacitor is needed	-
VGS	No Capacitor is needed	-

Note 1: The recommended component: Schottky RB521CS-30 (VF=0.35V@10mA and VR=30V).
Note 2: Leave VREFP/VEP/VEN open if this voltage is not in use.

3.4 MAXIMUM SERIES RESISTANCE

The driver will operate in “Chip on Glass” applications with series Resistances (due to ITO track Resistance). Voltages are specified at module I/O assuming maximum values as in below table.

Name	Type	Maximum Series Resistance	Unit
VDDIO	Power supply	10	Ω
VDDR	Power supply	5	Ω
VDDA	Power supply	5	Ω
VDDB	Power supply	5	Ω
VSSIO	Power supply	10	Ω
VSSR	Power supply	5	Ω
VSSAM	Power supply	5	Ω
VSSB	Power supply	5	Ω
VSSG	Power supply	5	Ω
AVSS	Power supply	5	Ω
DVSS	Power supply	5	Ω
IM[1:0] ,PSWAP,DSWAP	Input	100	Ω
DVDD_EN	Input	50	Ω
RSTB, CSB,SCL,DCX,D[1:0]	Input	50	Ω
SDI	Input/Output	50	Ω
CLKP/N, D1P/N	Input	10	Ω
D0P/N	Input/Output	10	Ω
SDO, OLED_EN,SWIRE	Output	50	Ω
DVDD,VREF	Power output	5	Ω
VGM,VGS,VEP,VEN,VREFP,VREFN	Power output	5	Ω
AVDD,AVEE	Power output	5	Ω
C11P/N,C12P/N,C21P/N,C22P/N,C31P/N,C41P/N	Capacitor connection	5	Ω
VGH,VGL,VGHO,VGLO	Power output	10	Ω
MTP_PWR	Power supply	10	Ω

4 Pin description

Symbol	Name	Description
Power Supply Pins		
VDDIO	I/O Power	Power supply for interface system except MIPI interface.
VDDR	Regulator Power	Power supply for regulator system.
VDDA	MIPI Power	Power supply for analog system.
VDDB	Analog Power	Power supply for DC/DC converter.
VSSIO	I/O GND	System ground for interface system except MIPI interface.
VSSR	Regulator GND	System ground for regulator.
VSSAM	MIPI GND	System ground for internal MIPI analog system.
VSSB	Pump GND	System ground for pump circuit system.
VSSG	Analog gray GND	System ground for analog gray system.
AVSS	Source OP GND	System ground for source OP.
DVSS	Digital GND	System ground for digital circuit system.
MTP_PWR	MTP Power	OTP programming power supply pin. Must open it for normal operation.
DC/DC Converter Pins		
AVDD	O	Output voltage from step-up circuit 1.generated from VDDB. Connect a capacitor for stabilization.
AVEE	O	Output voltage from internal step-up circuit 2, generated from VDDB. Connect a capacitor for stabilization.
VGH	O	Output voltage from step-up circuit 3. Connect a capacitor for stabilization.
VGL	O	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
C11P,C11N C12P,C12N	O	Capacitor connection pins for the step-up circuit which generate AVDD. Connect capacitor as requirement. When not in used, please open these pins.
C21P,C21N C22P,C22N	O	Capacitor connection pins for the step-up circuit which generate AVEE. Connect capacitor as requirement.
C31P,C31N	O	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitors as required, if not used open these pins.
C41P,C41N	O	Capacitor connection pins for the step-up circuit which generate VGL. Connect capacitors as required, if not used open these pins.
VGM	O	Output voltage generated from AVDD. LDO output for gamma's highest reference voltage.
VGS	O	Output voltage generated from AVDD. LDO output for gamma's lowest reference voltage.
VEP	O	Output voltage generated from AVDD. LDO output positive voltage for panel ELVDD.
VEN	O	Output voltage generated from AVEE. LDO output negative voltage for panel ELVSS.
VREF	O	Regulator output for internal reference voltage, Connect a capacitor for stabilization.
DVDD	O	Regulator output for logic system power, Connect a capacitor for stabilization.

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">SPI Interface Pins connect with Host</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pin in SPI I/F.
If not used, please connect to VDDIO.</td></tr>
<tr><td>SCL</td><td>I</td><td>Synchronous clock signal in SPI I/F.
If not used, please connect to VSSIO.</td></tr>
<tr><td>DCX</td><td>I</td><td>Display data/command selection in 8 bit SPI I/F.
DCX = “0” : Command;
DCX = “1” : Display data or Parameter;
If not used, please connect to VSSIO.</td></tr>
<tr><td>SDI</td><td>I/O</td><td>Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal.
If not used, please open this pin.</td></tr>
<tr><td>SDO</td><td>O</td><td>Serial outputs signal in SPI I/F. The data is output on the edge of the SCL signal.
If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together.
If not used, please open this pin.</td></tr>
<tr><td>D0,D1</td><td>I</td><td>Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal.
If not used, please connect to VSSIO.</td></tr>
<tr><td colspan="3">MIPI Interface Pins</td></tr>
<tr><td>CLKP
CLKN</td><td>I</td><td>-These pins are DSI-CLK+/- differential clock signals if MIPI interface is used.
- CLKP/N are differential small amplitude signals.
Ensure the trace length is shortest so that the COF Resistance is less than 3 ohm.
-If not used, please connect these pins to VSSAM.
-When Driver IC enters to ULPM or Deep Standby Mode, please keep these pins low.</td></tr>
<tr><td>D0P
D0N</td><td>I/O</td><td>-These pins are DSI-D0+/- differential data signals if MIPI interface is used.
- D0P/N are differential small amplitude signals.
Ensure the trace length is shortest so that the COF Resistance is less than 3 ohm.
-If not used, please connect these pins to VSSAM.
-When Driver IC enters to ULPM or Deep Standby Mode, please keep these pins low.</td></tr>
<tr><td>D1P
D1N</td><td>I</td><td>-These pins are DSI-D1+/- differential data signals if MIPI interface is used.
- D1P/N are differential small amplitude signals.
Ensure the trace length is shortest so that the COF Resistance is less than 3 ohm.
-If not used, please connect these pins to VSSAM.
-When Driver IC enters to ULPM or Deep Standby Mode, please keep these pins low.</td></tr>
<tr><td>PSWAP
DSWAP</td><td>I</td><td>Input pin to select D0 P/N、D1 P/N data lane sequence and polarity in high speed interface only.
<table>
<tr><th>PSWAP</th><th>DSWAP</th><th>D0P</th><th>D0N</th><th>CLKP</th><th>CLKN</th><th>D1P</th><th>D1N</th></tr>
<tr><td>0</td><td>0</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td></tr>
<tr><td>0</td><td>1</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td></tr>
<tr><td>1</td><td>0</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td></tr>
<tr><td>1</td><td>1</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td></tr>
</table>
If not used, please connect to VSSAM.</td></tr>
</table>

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Interface Logic Pins</td></tr>
<tr><td>RSTB</td><td>I</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>IM[1:0]</td><td>I</td><td>Interface type selection.
<table>
<tr><th>IM[1:0]</th><th>Display Data</th><th>Command</th></tr>
<tr><td>00</td><td>MIPI DSI / 9 bit SPI</td><td>MIPI DSI / 9 bit SPI</td></tr>
<tr><td>01</td><td>MIPI DSI / 8 bit SPI</td><td>MIPI DSI / 8 bit SPI</td></tr>
<tr><td>10</td><td>MIPI DSI / Quad-SPI</td><td>MIPI DSI / Quad-SPI</td></tr>
<tr><td>11</td><td>MIPI DSI</td><td>MIPI DSI / 16 bit rising SPI</td></tr>
</table>
Please connect to VDDIO or VSSIO.</td></tr>
<tr><td>TE</td><td>O</td><td>Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command.
When this pin is not activated, this pin is output low.
If not used, please open this pin.</td></tr>
<tr><td>TE1</td><td>O</td><td>This signal is used for noise sensing of TP and generated per scan line.
The output voltage level of TE1 pin is determined by VDDIO.
The TE1 pin can select to output other control signals via register setting as well.
If not used, please open this pin.</td></tr>
<tr><td>DVDD_EN</td><td>I</td><td>Set generation of DVDD.
DVDD_EN=0, disable generation of DVDD.
DVDD_EN=1, enable generation of DVDD.
This pin internal pull high.</td></tr>
</table>

Symbol	I/O	Description
Output Driver Pins		
S1~ S240	O	Pixel electrode driving output.
GOA1~GOA20 MUX1~MUX20	O	Gate driver output pins. The swing voltage level is VGHO to VGLO.
VGHO	O	High voltage level for gate control signals and gate circuit of panel.
VGLO	O	Low voltage level for gate control signals and gate circuit of panel.
VREFP	O	Pixel Reset Voltage. Connect a capacitor for stabilization. If not used, please open this pin.
VREFN	O	Pixel Reset Voltage. Connect a capacitor for stabilization. If not used, please open this pin.
External Power Control Pins		
OLED_EN	O	Power IC enable control pin. If not used, please open this pin.
SWIRE	O	S-wire protocol setting pin of power IC. If not used, please open this pin.
Test Pins		
DUMMY	-	-These pins are dummy with Hi-Z in driver IC (not have any function inside). -Signal traces can pass through on glass under these pads.
ATESTOUT[1:0]	O	Test pins, not accessible to user. If not used, please open this pin.
DTEST[12:0]	I/O	Test pins, not accessible to user. Please connect to VSSIO.

5 Command Description

User Command set list

Instr.	ACT	R/W	Address		Parameter								Function
			MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	Dir	W	00h	0000h	No Argument								No Operation
SWRESET	Dir	W	01h	0100h	No Argument								Software Reset
RDDID	Dir	R	04h	0400h	ID1[7:0]								Read display ID
				0401h	ID2[7:0]								
				0402h	ID3[7:0]								
RDNUMED	Dir	R	05h	0500h	D7	D6	D5	D4	D3	D2	D1	D0	Read No. of the errors on DSI only
RDDPM	Dir	R	0Ah	0A00h	D7	D6	D5	D4	D3	D2	-	-	Read display power mode
RDDMADCTR	Dir	R	0Bh	0B00h	MY	MX	MV	ML	RGB	-	RSMX	RSMY	Read display MADCTR
RDDCOLMO	Dir	R	0Ch	0C00h	-	-	-	-	-	IFPF[2:0]			Read display pixel format
RDDIM	Dir	R	0Dh	0D00h	-	-	D5	D4	D3	-	-	-	Read display image mode
RDDSM	Dir	R	0Eh	0E00h	D7	D6	D5	-	-	-	-	D0	Read display signal mode
RDDSDR	Dir	R	0Fh	0F00h	-	-	-	-	-	D2	D1	D0	Read display Self-diagnostic
SLPIN	DVS	W	10h	1000h	No Argument								Sleep in & booster off
SLPOUT	Dir	W	11h	1100h	No Argument								Sleep out & booster on
PTLON	DVS	W	12h	1200h	No Argument								Partial display mode on
NORON	DVS	W	13h	1300h	No Argument								Normal display mode on
INVOFF	DVS	W	20h	2000h	No Argument								Display inversion off (normal)
INVON	DVS	W	21h	2100h	No Argument								Display inversion on
ALLPOFF	DVS	W	22h	2200h	No Argument								All pixel off (black)
ALLPON	DVS	W	23h	2300h	No Argument								All pixel on (white)
DISPOFF	DVS	W	28h	2800h	No Argument								Display off
DISPON	DVS	W	29h	2900h	No Argument								Display on
CASET	Dir	R/W	2Ah	2A00h	-	-	-	-	-	-	-	SC8	Set column start address
				2A01h	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
				2A02h	-	-	-	-	-	-	-	EC8	
				2A03h	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	
RASET	Dir	R/W	2Bh	2B00h	-	-	-	-	-	-	SP9	SP8	Set row start address
				2B01h	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
				2B02h	-	-	-	-	-	-	EP9	EP8	
				2B03h	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	
RAMW	Dir	W	2Ch	2C00h	D7	D6	D5	D4	D3	D2	D1	D0	Write RAM start
				2C01h	D7	D6	D5	D4	D3	D2	D1	D0	
				2C02h	D7	D6	D5	D4	D3	D2	D1	D0	

				:	:	:	:	:	:	:	:	:	
RAMR	Dir	R	2Eh	2E00h	D7	D6	D5	D4	D3	D2	D1	D0	Read RAM start
				2E01h	D7	D6	D5	D4	D3	D2	D1	D0	
				2E02h	D7	D6	D5	D4	D3	D2	D1	D0	
				:	:	:	:	:	:	:	:	:	
HPTLAR	DVS	R/W	30h	3000h	-	-	-	-	-	-	PSR[9]	PSR[8]	Horizontal Partial area
				3001h	PSR[7]	PSR[6]	PSR[5]	PSR[4]	PSR[3]	PSR[2]	PSR[1]	PSR[0]	
				3002h	-	-	-	-	-	-	PER[9]	PER[8]	
				3003h	PER[7]	PER[6]	PER[5]	PER[4]	PER[3]	PER[2]	PER[1]	PER[0]	
VPTLAR	DVS	R/W	31h	3100h	-	-	-	-	-	-	-	PSC[8]	Vertical Partial area
				3101h	PSC[7]	PSC[6]	PSC[5]	PSC[4]	PSC[3]	PSC[2]	PSC[1]	PSC[0]	
				3102h	-	-	-	-	-	-	-	PEC[8]	
				3103h	PEC[7]	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]	
TEOFF	DVS	W	34h	3400h	No Argument								Tearing effect line off
TEON	DVS	W	35h	3500h	-	-	-	-	-	-	TE_M	TELOM	Tearing effect mode set & on
SDC	Dir	R/W	36h	3600h	MY	MX	MV	ML	RGB	-	RSMX	RSMY	Scan direction control
IDMOFF	DVS	W	38h	3800h	No Argument								Idle mode off
IDMON	DVS	W	39h	3900h	No Argument								Idle mode on
IPF	Dir	R/W	3Ah	3A00h	-	-	-	-	-	IFPF[2:0]			Interface Pixel Format
RAMWC	Dir	W	3Ch	3C00h	D7	D6	D5	D4	D3	D2	D1	D0	Write RAM Continuous
				3C01h	D7	D6	D5	D4	D3	D2	D1	D0	
				3C02h	D7	D6	D5	D4	D3	D2	D1	D0	
				:	:	:	:	:	:	:	:	:	
RAMRDC	Dir	R	3Eh	3E00h	D7	D6	D5	D4	D3	D2	D1	D0	Read RAM Continuous
				3E01h	D7	D6	D5	D4	D3	D2	D1	D0	
				3E02h	D7	D6	D5	D4	D3	D2	D1	D0	
				:	:	:	:	:	:	:	:	:	
STESL	DVS	W	44h	4400h	N15	N14	N13	N12	N11	N10	N9	N8	Set tearing effect scan line
				4401h	N7	N6	N5	N4	N3	N2	N1	N0	
GSL	Dir	R	45h	4500h	N15	N14	N13	N12	N11	N10	N9	N8	Get scan line
				4501h	N7	N6	N5	N4	N3	N2	N1	N0	
RAMW	Dir	W	4Ch	4C00h	D7	D6	D5	D4	D3	D2	D1	D0	Write AOD RAM start
				4C01h	D7	D6	D5	D4	D3	D2	D1	D0	
				4C02h	D7	D6	D5	D4	D3	D2	D1	D0	
				4C03h	:	:	:	:	:	:	:	:	
DSTBON	Dir	W	4Fh	4F00h	-	-	-	-	-	-	-	DSTB	Deep standby mode on
WDB	DVS	W	51h	5100h	DBV[7:0]								Write display brightness
RDB	DVS	R	52h	5200h	DBV[7:0]								read display brightness

HBMSEL	DVS	W	53h	5300h	HBM_EN[7:0]								Select HBM mode
RHBM	Dir	R	54h	5400h	HBM_EN[7:0]								Read HBM mode
NEM	DVS	R/W	55h	5500h	NOR_WIDTH[7:0]								Set EM Width for Normal mode
IEM	DVS	R/W	56h	5600h	IDLE_WIDTH[7:0]								Set EM Width for Idle mode
HEM	DVS	R/W	57h	5700h	HBM_WIDTH[7:0]								Set EM Width for HBM mode
RAMWC	Dir	W	5Ch	5C00h	D7	D6	D5	D4	D3	D2	D1	D0	Write AOD RAM continuous
				5C01h	D7	D6	D5	D4	D3	D2	D1	D0	
				5C02h	D7	D6	D5	D4	D3	D2	D1	D0	
				5C03h	:	:	:	:	:	:	:	:	
BACTR	Dir	R/W	60h	6000h	EM_M	EM_DIM_EN	HMS_DIM_EN	IMS_DIM_EN	-	BC_LINEAR	BC_DIM_M	BC_DIM_EN	Dimming Control
DECTR	DVS	R/W	62h	6200h	-	-	-	D_DIM_EN	-	IDLE_DELVSS_EN	DELVSSM[1:0]		Dynamic ELVSS Function Control
SRECTR	DVS	R/W	63h	6300h	-	-	-	SRE_EN	-	-	SRE_SIZE[1:0]		SRE Mode Control
GACMSET	DVS	R/W	64h	6400h	-	-	GAM_HBM[1:0]		GAM_IDLE[1:0]		GAM_NOR[1:0]		Gamma and Color Mode set
SPIRDC	Dir	W	65h	6500h	SPI_CNT[7:0]								SPI read manufacture
CICEN	DVS	R/W	67h	6700h	-	-	UD_POS[1:0]		-	-	-	R_O_EN	circular edgeenable
OLOAEN	DVS	R/W	68h	6800h	-	-	OBL_Y	OBL_X	-	-	-	OBL_EN	Oblique Lineenable
NOTCHEN	DVS	R/W	69h	6900h	-	-	-	-	-	-	-	Notch_EN	Notch algorithm enable
INCIREN	DVS	R/W	6Ah	6A00h	-	-	-	-	-	-	-	R_I_EN	Inside CircularAlgorithm Enable
SWIREMANU	DVS	R/W	6Ch	6C00h	SMANU_CTL[7:0]								Swire Manual Control
SPIRDC	Dir	W	6Dh	6D00h	-	-	-	-	-	-	-	SPI_READ_EN	SPI read manufacture command Enable
AODCLKS	Dir	R/W	82h	8200h	AOD_EN	CLOCKM	HOURM	TIMEM	DCLKMEN	-	-	-	AOD clock setting
AODTIME	Dir	R/W	83h	8300h	Hour[7:0]								AOD time setting
				8301h	Minute[7:0]								
				8301h	Second[7:0]								
AODSECCAL	Dir	R/W	84h	8400h	No Argument								AOD second hand calibration
AODSYNCP	Dir	R/W	85h	8500h	SECOND_OFFSET[9:8]		-	CALB_EN	-	-	CALB_CYCLE[1:0]		AOD Synchronization cycle setting
				8501h	SECOND_OFFSET[7:0]								

				8502h	SECOND_COUNT[23:16]		
				8503h	SECOND_COUNT[15:8]		
				8504h	SECOND_COUNT[7:0]		
DCLKF SIZE	Dir	R/W	86h	8600h	-	NUMSize_R[6:0]	Digital clock Font size
				8601h	-	NUMSize_C[6:0]	
				8602h	-	MARKSize_C[6:0]	
DHCOL ORR	Dir	R/W	87h	8700h	DH_Color_R0[7:0]		Hour color setting
				8701h	DH_Color_R1[7:0]		
				8702h	DH_Color_ R2[7:0]		
				…	…		
				87FEh	DH_Color_R254[7:0]		
				87FFh	DH_Color_R255[7:0]		
DHCOL ORG	Dir	R/W	88h	8800h	DH_Color_G0[7:0]		
				8801h	DH_Color_G1[7:0]		
				8802h	DH_Color_ G2[7:0]		
				…	…		
				88FEh	DH_Color_G254[7:0]		
				88FFh	DH_Color_G255[7:0]		
DHCOL ORB	Dir	R/W	89h	8900h	DH_Color_B0[7:0]		
				8901h	DH_Color_B1[7:0]		
				8902h	DH_Color_ B2[7:0]		
				…	…		
				89FEh	DH_Color_B254[7:0]		
				89FFh	DH_Color_B255[7:0]		
DHCOL ORA	Dir	R/W	8Ah	8A00h	DH_Color_A0[7:0]		
				8A01h	DH_Color_A1[7:0]		
				8A02h	DH_Color_ A2[7:0]		
				…	…		
				8AFEh	DH_Color_A254[7:0]		
				8AFFh	DH_Color_A255[7:0]		
DMCOL ORR	Dir	R/W	8Bh	8B00h	DM_Color_R0[7:0]		Minute color setting
				8B01h	DM_Color_R1[7:0]		
				8B02h	DM_Color_ R2[7:0]		
				…	…		
				8BFEh	DM_Color_R254[7:0]		
				8BFFh	DM_Color_R255[7:0]		
DMCOL ORG	Dir	R/W	8Ch	8C00h	DM_Color_G0[7:0]		
				8C01h	DM_Color_G1[7:0]		
				8C02h	DM_Color_ G2[7:0]		
				…	…		
				8CFEh	DM_Color_G254[7:0]		
				8CFFh	DM_Color_G255[7:0]		
DMCOL	Dir	R/W	8Dh	8D00h	DM_Color_B0[7:0]		

ORB				8D01h	DM_Color_B1[7:0]									
				8D02h	DM_Color_ B2[7:0]									
				…	…									
				8DFEh	DM_Color_B254[7:0]									
				8DFFh	DM_Color_B255[7:0]									
DMCOLORA	Dir	R/W	8Eh	8E00h	DM_Color_A0[7:0]									
				8E01h	DM_Color_A1[7:0]									
				8E02h	DM_Color_ A2[7:0]									
				…	…									
				8EFEh	DM_Color_A254[7:0]									
				8EFFh	DM_Color_A255[7:0]									
DCCOLOR	Dir	R/W	8Fh	8F00h	-	-	-	-	-	-	-	DC_CHOOSE		Digital clock colon color setting
DCLKHC	Dir	R/W	90h	9000h	-	-	-	DClockC[8]	-	-	DClockR[9:8]			Host send digital clock position
				9001h	DClockR[7:0]									
				9002h	DClockC[7:0]									
DCLKOCS	Dir	R/W	91h	9100h	DClockY4[9:8]		DClockY3[9:8]		DClockY2[9:8]		DClockY1[9:8]			Digital clock offset coordinate setting
				9101h	-	-	-	-	-	-	DClockY5[9:8]			
				9102h	-	-	-	DClockX5[8]	DClockX4[8]	DClockX3[8]	DClockX2[8]	DClockX1[8]		
				9103h	DClockY1[7:0]									
				9104h	DClockX1[7:0]									
				9105h	DClockY2[7:0]									
				9106h	DClockX2[7:0]									
				9107h	DClockY3[7:0]									
				9108h	DClockX3[7:0]									
				9109h	DClockY4[7:0]									
				910Ah	DClockX4[7:0]									
				910Bh	DClockY5[7:0]									
				910Ch	DClockX5[7:0]									
ACLKSET	Dir	R/W	92h	9200h	-	-	-	-	-	ACLKSQ_EN	ACLKSEC_EN	ACLKMIN_EN		Analog clock setting
ACLKRCC	Dir	R/W	93h	9300h	MINUTE_ROTATE_R[7:0]									Analog clock rotate center coordinate setting
				9301h	-	-	MINUTE_ROTATE_C[5:0]							
				9302h	SECOND_ROTATE_R[7:0]									
				9303h	-	-	-	SECOND_ROTATE_C[4:0]						
ACLKCLS	Dir	R/W	94h	C300h	-	-	-	-	-	-	-	AClockR[8]		Analog clock center location setting
				C301h	AClockR[7:0]									
				C302h	AClockC[7:0]									
DEBURNSET	Dir	R/W	95h	9500h	-	-	-	DE_BURN_EN	-	-	SP_AOD			AOD De-burn-in setting
				9501h	-	DE_BURNSMS			-	DE_BURNSMP				
				9502h	-	SP_X								
				9503h	-	SP_Y								
DEBUR	Dir	R/W	96h	9600h	X2Dir[1:0]		Y2Dir[1:0]		X1Dir[1:0]		Y1Dir[1:0]			AOD De-burn-in

NDIR_LSB				9601h	X4Dir[1:0]		Y4Dir[1:0]		X3Dir[1:0]		Y3Dir[1:0]		direction of each step setting
				9602h	X6Dir[1:0]		Y6Dir[1:0]		X5Dir[1:0]		Y5Dir[1:0]		
				9603h	X8Dir[1:0]		Y8Dir[1:0]		X7Dir[1:0]		Y7Dir[1:0]		
				9604h	X10Dir[1:0]		Y10Dir[1:0]		X9Dir[1:0]		Y9Dir[1:0]		
				9605h	X12Dir[1:0]		Y12Dir[1:0]		X11Dir[1:0]		Y11Dir[1:0]		
				9606h	X14Dir[1:0]		Y14Dir[1:0]		X13Dir[1:0]		Y13Dir[1:0]		
				9607h	X16Dir[1:0]		Y16Dir[1:0]		X15Dir[1:0]		Y15Dir[1:0]		
				9608h	X18Dir[1:0]		Y18Dir[1:0]		X17Dir[1:0]		Y17Dir[1:0]		
				9609h	X20Dir[1:0]		Y20Dir[1:0]		X19Dir[1:0]		Y19Dir[1:0]		
				960Ah	X22Dir[1:0]		Y22Dir[1:0]		X21Dir[1:0]		Y21Dir[1:0]		
				960Bh	X24Dir[1:0]		Y24Dir[1:0]		X23Dir[1:0]		Y23Dir[1:0]		
				960Ch	X26Dir[1:0]		Y26Dir[1:0]		X25Dir[1:0]		Y25Dir[1:0]		
				960Dh	X28Dir[1:0]		Y28Dir[1:0]		X27Dir[1:0]		Y27Dir[1:0]		
				960Eh	X30Dir[1:0]		Y30Dir[1:0]		X29Dir[1:0]		Y29Dir[1:0]		
				960Fh	X32Dir[1:0]		Y32Dir[1:0]		X31Dir[1:0]		Y31Dir[1:0]		
DEBURNDIR_MSB	Dir	R/W	97h	9700h	X34Dir[1:0]		Y34Dir[1:0]		X33Dir[1:0]		Y33Dir[1:0]		AOD De-burn-in direction of each step setting
				9701h	X36Dir[1:0]		Y36Dir[1:0]		X35Dir[1:0]		Y35Dir[1:0]		
				9702h	X38Dir[1:0]		Y38Dir[1:0]		X37Dir[1:0]		Y37Dir[1:0]		
				9703h	X40Dir[1:0]		Y40Dir[1:0]		X39Dir[1:0]		Y39Dir[1:0]		
				9704h	X42Dir[1:0]		Y42Dir[1:0]		X41Dir[1:0]		Y41Dir[1:0]		
				9705h	X44Dir[1:0]		Y44Dir[1:0]		X43Dir[1:0]		Y43Dir[1:0]		
				9706h	X46Dir[1:0]		Y46Dir[1:0]		X45Dir[1:0]		Y45Dir[1:0]		
				9707h	X48Dir[1:0]		Y48Dir[1:0]		X47Dir[1:0]		Y47Dir[1:0]		
				9708h	X50Dir[1:0]		Y50Dir[1:0]		X49Dir[1:0]		Y49Dir[1:0]		
				9709h	X52Dir[1:0]		Y52Dir[1:0]		X51Dir[1:0]		Y51Dir[1:0]		
				970Ah	X54Dir[1:0]		Y54Dir[1:0]		X53Dir[1:0]		Y53Dir[1:0]		
				970Bh	X56Dir[1:0]		Y56Dir[1:0]		X55Dir[1:0]		Y55Dir[1:0]		
				970Ch	X58Dir[1:0]		Y58Dir[1:0]		X57Dir[1:0]		Y57Dir[1:0]		
				970Dh	X60Dir[1:0]		Y60Dir[1:0]		X59Dir[1:0]		Y59Dir[1:0]		
				970Eh	X62Dir[1:0]		Y62Dir[1:0]		X61Dir[1:0]		Y61Dir[1:0]		
				970Fh	X64Dir[1:0]		Y64Dir[1:0]		X63Dir[1:0]		Y63Dir[1:0]		
RDID1	Dir	R	DAh	DA00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1
RDID2	Dir	R	DBh	DB00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	Read ID2
RDID3	Dir	R	DCh	DC00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	Read ID3

Notes:

1. The following description is indicates the executing time of instructions.

No.	Symbol	Executing time
1	Dir (Direct)	At the received a completed instruction and parameter
2	DVS (Display Vertical Sync.)	Synchronized with the next frame

2. The 8-bit Command code in above table and following command description means MIPI.

NOP(0000h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
00h	0000h	No Argument								N/A
Description		This command is empty command. It does not have effect on the display module. However it can be used to terminate parameter write commands.								
Restriction		-								

SWRESET: Software Reset (0100h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
01h	0100h	No Argument								N/A
Description		When the software reset command is written, it causes software reset. It resets the commands and parameters to their S/W reset default values. (See default tables in each command description). The display is blank immediately.								
Restriction		It will be necessary to wait 5 msec before sending new command following software reset. The display module loads all display suppliers factory default values to the registers during this 5 msec. If software reset is applied during sleep out mode, it will be necessary to wait 120 msec before sending sleep out command. Software reset command cannot be sent during sleep out sequence.								

RDDID: Read Display ID (0400h~0402h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
04h	0400h	ID1[7:0]								00h
	0401h	ID2[7:0]								80h
	0402h	ID3[7:0]								00h
Description		This read byte returns 24-bit display identification information. The 1st parameter (ID1): the module's manufacture ID. The 2nd parameter (ID2): the module/driver version ID. The 3rd parameter (ID3): the module/driver ID. Note: Commands RDID1/2/3 (DAh, DBh, DCh) read data correspond to the parameter 1, 2, 3 of the command 04h, respectively								
Restriction		-								

RDNUMED: Read Number of Errors on DSI (0500h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
05h	0500h	D7	D6	D5	D4	D3	D2	D1	D0	00h
Description		The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below. D[6..0] bits are telling a number of the parity errors. D[7] is set to “1” if there is overflow with P[6..0] bits. D[7..0] bits are set to “0”s (as well as RDDSM(0Eh)’s D0 are set “0” at the same time) after there is sent the first parameter information (= The read function is completed). See also section “Acknowledge with Error Report (AwER)” and command RDDSM 0Eh. This command is used for MIPI DSI only. It is no function for others interface operation.								
Restriction		-								

RDDPM: Read display power mode (0A00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Ah</td><td>0A00h</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>-</td><td>-</td><td>08h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Booster Voltage Status</td><td>“1”=Booster On, “0”=Booster Off</td></tr>
<tr><td>D6</td><td>Idle Mode On/Off</td><td>“1”=Idle Mode On, “0”= Idle Mode Off</td></tr>
<tr><td>D5</td><td>Partial mode On/Off</td><td>“1”=Partial Mode On, “0”= Partial Mode Off</td></tr>
<tr><td>D4</td><td>Sleep In/Out</td><td>“1”=Sleep Out Mode, “0”=Sleep In Mode</td></tr>
<tr><td>D3</td><td>Display Normal Mode On/Off</td><td>“1”=Display Normal On, “0”=Display Normal Off</td></tr>
<tr><td>D2</td><td>Display On/Off</td><td>“1”=Display On, “0”=Display Off</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

RDDMADCTR: Read Display MADCTR (0B00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Bh</td><td>0B00h</td><td>MY</td><td>MX</td><td>MV</td><td>ML</td><td>RGB</td><td>-</td><td>RSMX</td><td>RSMY</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command indicates the current status of the display as described in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>MY</td><td>Row Address Increment</td><td>“0” = Increasing in vertical;
“1” = Decreasing in vertical</td></tr>
<tr><td>MX</td><td>Column Address Increment</td><td>“0” = Increasing in horizontal;
“1” = Decreasing in horizontal</td></tr>
<tr><td>MV</td><td>Row/Column Order</td><td>“0” =Normal;
“1” = Row/column exchange</td></tr>
<tr><td>ML</td><td>Vertical Refresh Order</td><td>“0” =Panel Refresh Top to Bottom;
“1” = Panel Refresh Bottom to Top;</td></tr>
<tr><td>RGB</td><td>RGB/BGR Order</td><td>“0” =RGB;
“1” = BGR</td></tr>
<tr><td>RSMX</td><td>Horizontal Flip</td><td>“0” =Normaldisplay;
“1” = Flipped display</td></tr>
<tr><td>RSMY</td><td>Vertical Flip</td><td>“0” =Normaldisplay;
“1” = Flipped display</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

RDDCOLMOD: Read Display Pixel Format (0C00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Ch</td><td>0C00h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td colspan="3">IFPF[2:0]</td><td>07h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>IFPF[2:0]</th><th>DBI pixel format</th></tr>
<tr><td>001</td><td>SPI 1-1-1</td></tr>
<tr><td>010</td><td>SPI 8bit/pixel(256 colors);SPI 3-3-2</td></tr>
<tr><td>011</td><td>SPI 8bit/pixel(256 colors);SPI 256Gray</td></tr>
<tr><td>101</td><td>16bit/pixel(65,536 colors)</td></tr>
<tr><td>110</td><td>18bit/pixel(262,144 colors)</td></tr>
<tr><td>111</td><td>24bit/pixel(16.7M colors)</td></tr>
<tr><td>Others</td><td>reserved</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

RDDIM: Read Display Image Mode (0D00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Dh</td><td>0D00h</td><td>-</td><td>-</td><td>D5</td><td>D4</td><td>D3</td><td>-</td><td>-</td><td>-</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D5</td><td>Inversion On/Off</td><td>“1” = Inversion On, “0” = Inversion Off</td></tr>
<tr><td>D4</td><td>All Pixel On</td><td>“1” = White display, “0” = Normal display</td></tr>
<tr><td>D3</td><td>All Pixel Off</td><td>“1” = Black display, “0” = Normal display</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

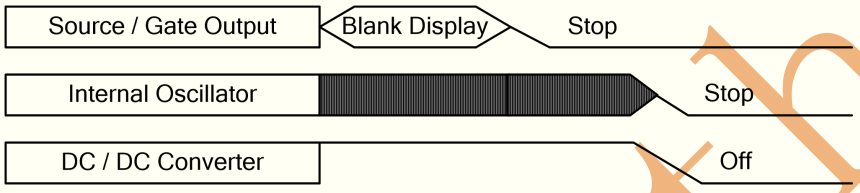
RDDSM: Read Display Signal Mode (0E00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Eh</td><td>0E00h</td><td>D7</td><td>D6</td><td>D5</td><td>-</td><td>-</td><td>-</td><td>-</td><td>D0</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Tearing Effect Line On/Off</td><td>“1” = On, “0” = Off</td></tr>
<tr><td>D6</td><td>Tearing Effect Mask Mode</td><td>“1” = TE Mask Mode
“0” = TE Non-mask Mode</td></tr>
<tr><td>D5</td><td>Tearing Effect Line Mode</td><td>“1” = V-Blanking & H-Blinking Mode
“0” = V-Blanking Mode</td></tr>
<tr><td>D0</td><td>Error on DSI(SOT sync error, SOT error, HS time out, Multi-bit ECC error, single-bit ECC error(需要设计增加);CRC error)</td><td>“1”=error, “0”=no error</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

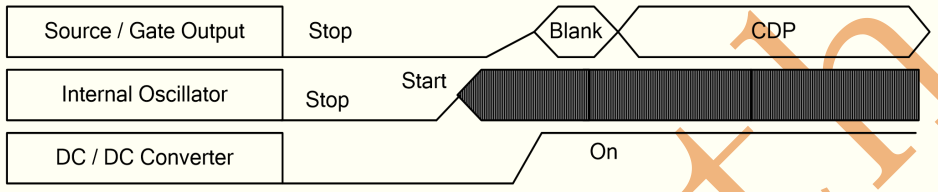
RDDSDR: Read Display Self-Diagnostic Result (0F00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Fh</td><td>0F00h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>D2</td><td>D1</td><td>D0</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>value</th></tr>
<tr><td>D2</td><td>fill ok flag反馈标志位</td><td>“1”=fill ok flag, “0”=not fill ok flag</td></tr>
<tr><td>D1</td><td>RGB Timing off detection flag</td><td>“1”=External RGB timing off,
“0”=External RGB timing on</td></tr>
<tr><td>D0</td><td>Checksum Status</td><td>“1”=Checksum abnormal, “0”=
Checksum normal</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

SLPIN: Sleep In (1000h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
10h	1000h	No Argument								Sleep in mode
Description		This command causes the AMOLED module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, internal display oscillator is stopped, and panel scanning is stopped.  Control Interface, display data and registers are still working. User can send RGB Timing for blank display after Sleep In command and this information is invalid during 2 frames after Sleep In command if there is used Normal Mode On in Sleep Out-mode. Dimming function does not work when there is changing mode from Sleep Out to Sleep In.								
Restriction		This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.								

SLPOUT: Sleep Out (1100h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
11h	1100h	No Argument								Sleep out mode
Description		This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.  User can start to send RGB Timing before Sleep Out command driver IC will do sequence control about gate control signals when sleep out.								
Restriction		Sleep Out Mode can only be exit by the Sleep In Command (10h), S/W Reset command (01h) or H/W Reset. It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. Driver IC loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the driver IC is already Sleep Out mode. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.								

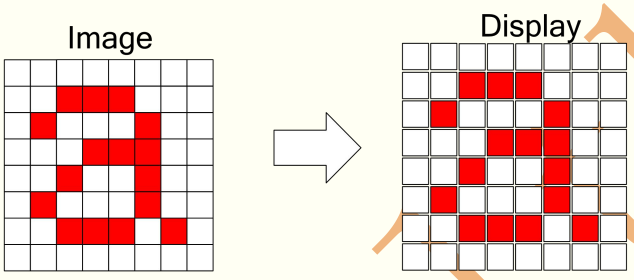
PTLON: Partial Display Mode On(1200h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
12h	1200h	No Argument								Partial Mode On
Description		This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the Partial Area (30h/31h) command. To leave Partial Display Mode, the Normal Display Mode On (13h) command should be written. The host processor continues to send PCLK, HS and VS information to display modules for two frames after this command is sent when the display module is in Normal Display Mode.								
Restriction		This command has no effect when Partial Display Mode is active.								

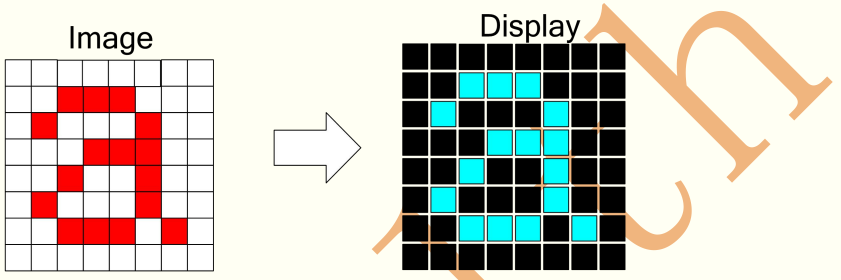
NORON: Normal Display Mode on (1300h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
13h	1300h	No Argument								Normal Mode On
Description		This command returns the display to normal mode.								
Restriction		This command has no effect when Normal Display Mode is active.								

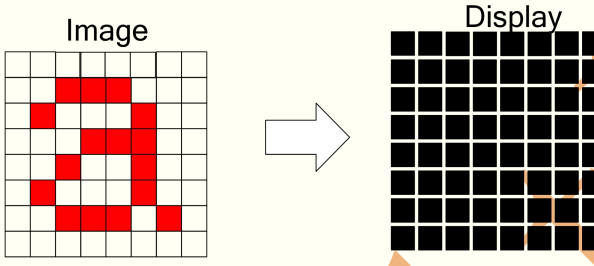
INVOFF: Display Inversion Off (2000h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
20h	2000h	No Argument								Display inversion off
Description		This command is used to recover from display inversion mode. This command does not change any other status. Example: 								
Restriction		This command has no effect when module is already in inversion off mode.								

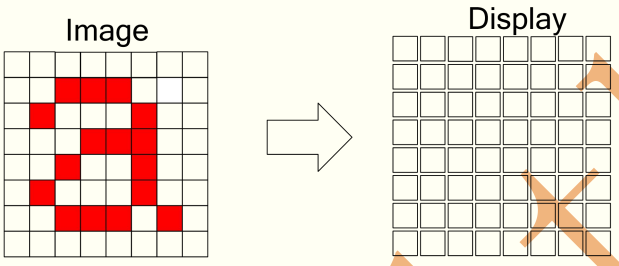
INVON: Display Inversion On (2100h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
21h	2100h	No Argument								Display inversion on
Description		This command is used to enter display inversion mode. This command does not change any other status. To exit from Display Inversion On, the Display Inversion Off command (20h) should be written. Example:  …								
Restriction		This command has no effect when module is already in Inversion On mode.								

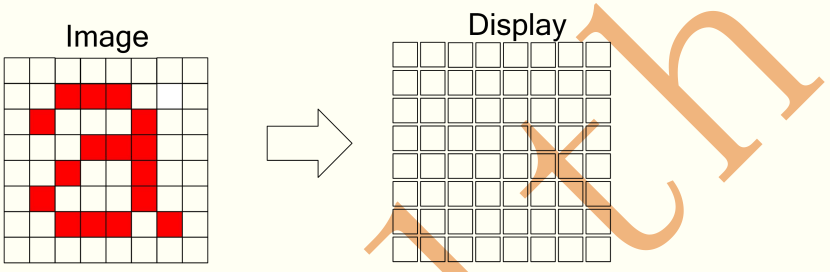
ALLPOFF: All Pixel Off (2200h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
22h	2200h	No Argument								All pixel off
Description		This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status. Example:  "All Pixels On" or "Normal Display Mode On" commands are used to leave this mode. The display panel shows the display data after "Normal Display On" command.								
Restriction		This command has no effect when module is already in All Pixel Off mode.								

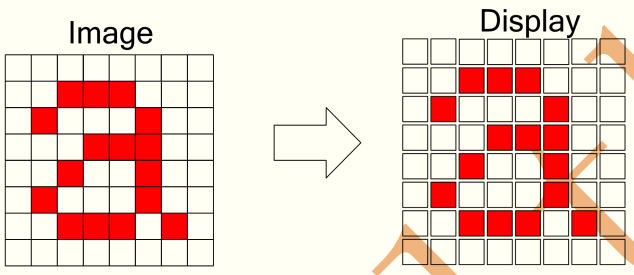
ALLPON: All Pixel On (2300h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
23h	2300h	No Argument								All pixel on
Description		This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status. Example:  "All Pixels Off" or "Normal Display Mode On" commands are used to leave this mode. The display panel is showing the display data after "Normal Display On" command.								
Restriction		This command has no effect when module is already in All Pixel ON mode.								

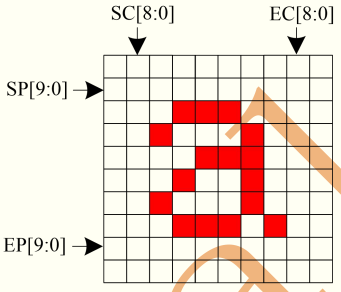
DISPOFF: Display Off (2800h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
28h	2800h	No Argument								Display off
Description		This command is used to enter into Display Off mode. In this mode, the display data is disabled and the blank page is inserted. This command does not change any other status. There will be no abnormal visible effect on the display. Example:  …								
Restriction		This command has no effect when module is already in display off mode.								

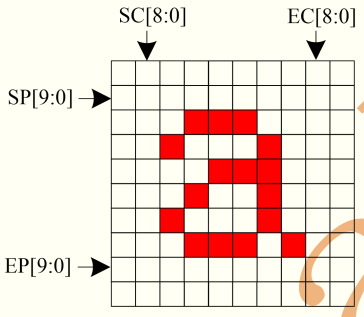
DISPON: Display On (2900h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
29h	2900h	No Argument								Display on
Description		This command is used to recover from DISPLAY OFF mode. Output from display data is enabled. This command does not change any other status. Example:  …								
Restriction		This command has no effect when module is already in Display On mode.								

CASET: Set Column Start Address(2A00h~2A03h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
2Ah	2A00h	-	-	-	-	-	-	-	SC8	00h
	2A01h	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00h
	2A02h	-	-	-	-	-	-	-	EC8	01h
	2A03h	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	C5h
Description		This command defines the column extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. This command makes no change on theother driver status. The values of SC[8:0] and EC[8:0] are referred when RAMWR command comes.  								
Restriction		When partial update,The SC[8:0] and EC[8:0]-SC[8:0]+1 must can be divisible by 2.								

RASET: Set Row Start Address(2B00h~2B03h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
2Bh	2B00h	-	-	-	-	-	-	SP9	SP8	00h
	2B01h	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00h
	2B02h	-	-	-	-	-	-	EP9	EP8	01h
	2B03h	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	C5h
Description		This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. This command makes no change on theother driver status. The values of SP[9:0] and EP[9:0] are referred when RAMWR command comes.  								
Restriction		When partial update,The SP[9:0] and EC[9:0]-SC[9:0]+1 must can be divisible by 2.								

RAMW: Write memory Start (2Ch)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
2Ch	2C00h	D7	D6	D5	D4	D3	D2	D1	D0	Contents of memory is set randomly
	2C01h	D7	D6	D5	D4	D3	D2	D1	D0	
	2C02h	D7	D6	D5	D4	D3	D2	D1	D0	
	:	:	:	:	:	:	:	:	:	
Description		This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. Please use MIPI HS format to write image data. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command.								
Restriction		A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.								

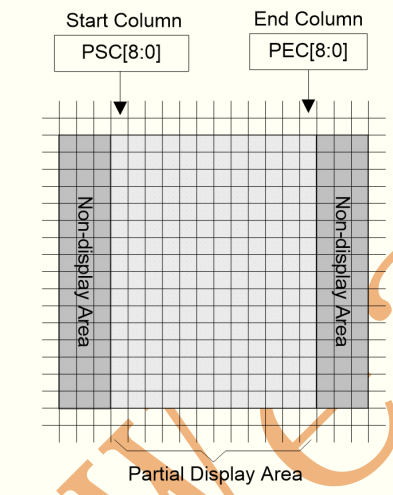
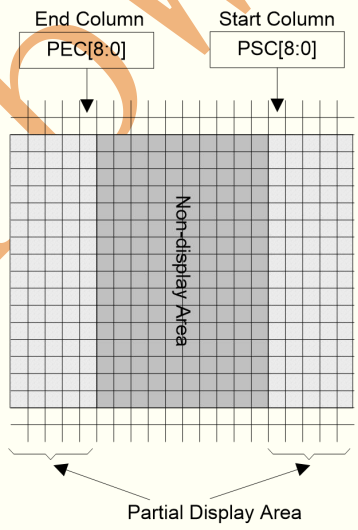
RAMR: Read memory (2Eh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
2Eh	2E00h	D7	D6	D5	D4	D3	D2	D1	D0	Contents of memory is set randomly
	2E01h	D7	D6	D5	D4	D3	D2	D1	D0	
	2E02h	D7	D6	D5	D4	D3	D2	D1	D0	
	:	:	:	:	:	:	:	:	:	
Description		This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.								
Restriction		There is no restriction on length of parameters.								

HPTLAR: Horizontal Partial Area (3000h~3003h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
30h	3000h	-	-	-	-	-	-	PSR[9]	PSR[8]	00h
	3001h	PSR[7]	PSR[6]	PSR[5]	PSR[4]	PSR[3]	PSR[2]	PSR[1]	PSR[0]	00h
	3002h	-	-	-	-	-	-	PER[9]	PER[8]	01h
	3003h	PER[7]	PER[6]	PER[5]	PER[4]	PER[3]	PER[2]	PER[1]	PER[0]	C5h
Description		This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. If End Row> Start Row: Start Row PSR[9:0] Non-display Area Partial Display Area End Row PER[9:0] Non-display Area If End Row< Start Row : End Row PER[9:0] Non-display Area Partial Display Area Start Row PSR[9:0] If End Row = Start Row Then the Partial Area will be one row deep.								
Restriction		PSR[9:0] and PER[9:0] settings should be within max available Display Area.								

VPTLAR:Vertical Partial Area (3100h~3101h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
31h	3100h	-	-	-	-	-	-	-	PSC[8]	00h
	3101h	PSC[7]	PSC[6]	PSC[5]	PSC[4]	PSC[3]	PSC[2]	PSC[1]	PSC[0]	00h
	3102h	-	-	-	-	-	-	-	PEC[8]	01h
	3103h	PEC[7]	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]	C5h
Description		This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Column (SC) and the second the End Column (EC), as illustrated in the following figure. If End Column> Start Column:  If End Column< Start Column:  If End Column = Start Column then the partial Area will be one column deep.									
Restriction		PSC[8:0] and PEC[8:0] settings should be within max available Display Area.								

TEOFF: TE Signal OFF (3400h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
34h	3400h	No Argument								TE off
Description		This command is used to turn OFF (Active Low) the output signal from the TE signal line.								
Restriction		This command has no effect when TE output is already OFF.								

TEON: TE Signal ON (3500h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
35h	3500h	-	-	-	-	-	-	TE_M	TELOM	TE on

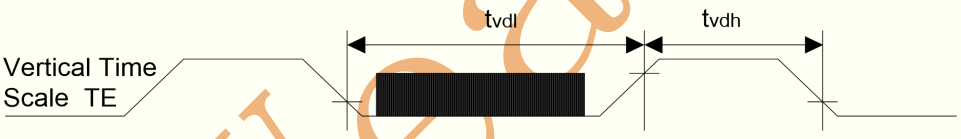
Description

This command is used to turn ON the output signal from the TE signal line. The TE On has one parameter, which describes the mode of Output Line. ("-"means don't care).

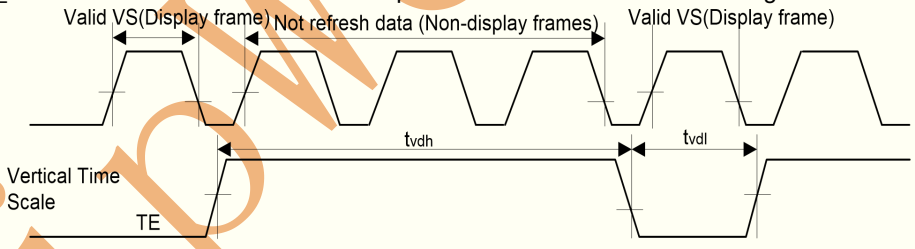
TE_M	Function
0	Output mode of TE signal set
1	Output mode of TE signal set (Mask TE signal during non-display Frame)

When TE_M = "0" & TELOM = "0": The TE Output line consists of V-Blanking information only.

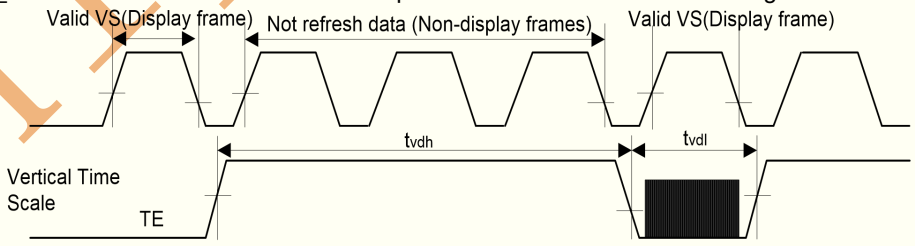
When TE_M = "0" & TELOM = "1": The TE Output line consists of both V-Blanking and H-Blinking information.



When TE_M = "1" & TELOM = "0": The TE Output line consists of Valid V-Blanking information.



When TE_M = "1" & TELOM = "1": The TE Output line consists of Valid V-Blanking information.



Note: 1. During Sleep In Mode with TE Line On, TE Output pin will be active Low.
2. When 35h=01h, TE output high during non-display frame.

Restriction: This command has no effect when Tearing Effect output is already ON.

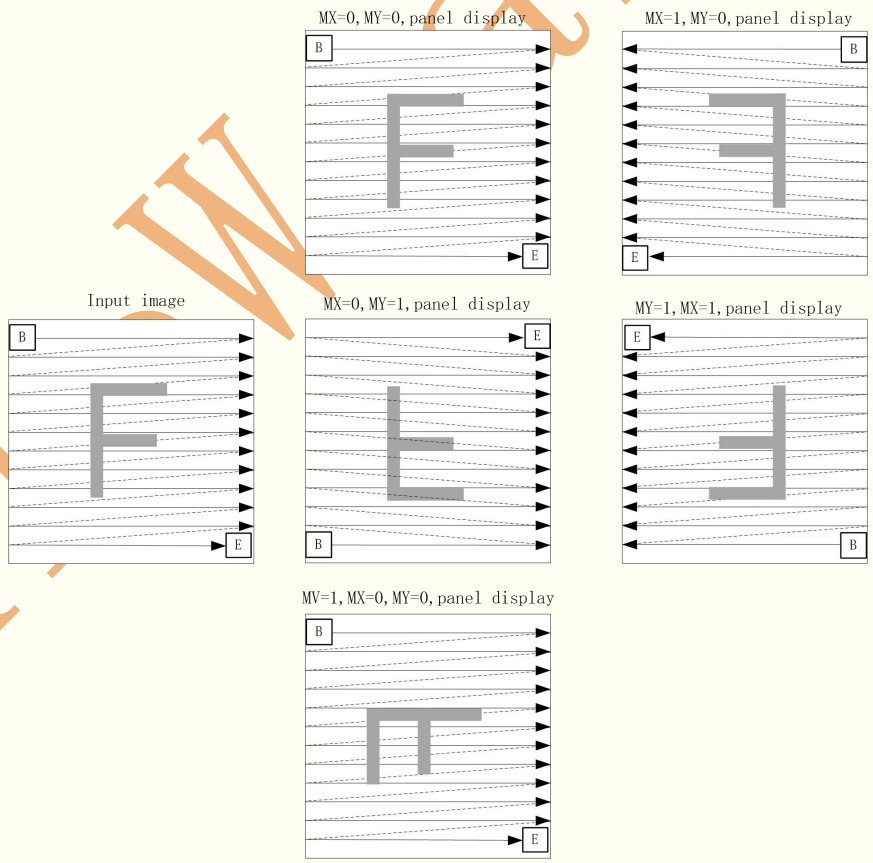
SDC: ScanDirectionControl (3600h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
36h	3600h	MY	MX	MV	ML	RGB	-	RSMX	RSMY	00h

Description

This command defines the scan direction of Source and Gate Driver. This command makes no change on the other driver status.

Bit	Description	Value
MY	Row Address Increment	“0” = Increasing in vertical “1” = Decreasing in vertical
MX	Column Address Increment	“0” = Increasing in horizontal “1” = Decreasing in horizontal
MV	Row/Column Order	“0” = Normal “1” = Row/column exchange
ML	Vertical Refresh Order	“0” = Panel Refresh Top to Bottom “1” = Panel Refresh Bottom to Top
RGB	RGB/BGR Order	“0” = RGB “1” = BGR
RSMX	Horizontal Flip	“0” = Normaldisplay “1” = Flipped display
RSMY	Vertical Flip	“0” = Normaldisplay “1” = Flipped display



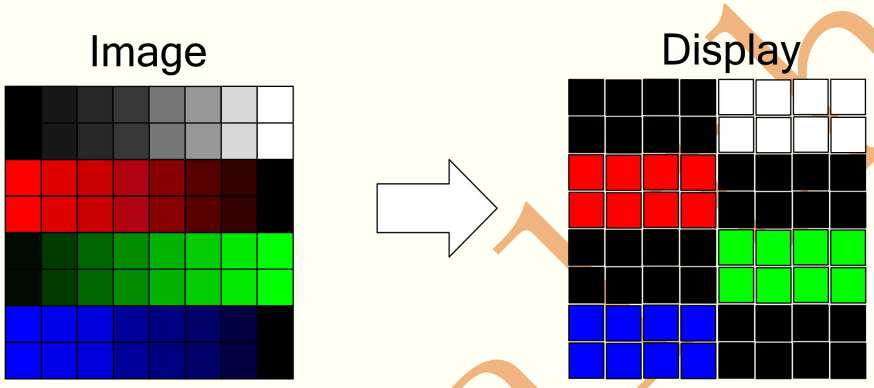
Note:1:MV转置功能设计只保证需要转置的图片在panel的有效显示区域内，转置后出现部分画面转出屏体的case设计不做特殊处理
2:其中MY/MX/MV/RGB为Dir，ML/RSMX/RSMY为DVS

Restriction	-

IDMOFF: Idle Mode Off (3800h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
38h	3800h	No Argument								Idle Mode off
Description		This command is used to recover from idle mode on. In the idle off mode, display panel can display maximum 16.7M colors.								
Restriction		This command has no effect when module is already in Idle Off Mode.								

IDMON: Idle mode On (3900h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>39h</td><td>3900h</td><td colspan="8">No Argument</td><td>Idle Mode on</td></tr>
<tr><td>Description</td><td colspan="9">This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G, and B, 8 color depth data is displayed.
 

<table>
<tr><th colspan="4">Image Contents VS. Display Colors</th></tr>
<tr><th></th><th>R7R6R5R4R3R2R1R0</th><th>G7G6G5G4G3G2G1G0</th><th>B7B6B5B4B3B2B1B0</th></tr>
<tr><td>Black</td><td>0XXXXXXX</td><td>0 XXXXXXX</td><td>0 XXXXXXX</td></tr>
<tr><td>Blue</td><td>0 XXXXXXX</td><td>0 XXXXXXX</td><td>1 XXXXXXX</td></tr>
<tr><td>Red</td><td>1 XXXXXXX</td><td>0 XXXXXXX</td><td>0 XXXXXXX</td></tr>
<tr><td>Magenta</td><td>1 XXXXXXX</td><td>0 XXXXXXX</td><td>1 XXXXXXX</td></tr>
<tr><td>Green</td><td>0 XXXXXXX</td><td>1 XXXXXXX</td><td>0 XXXXXXX</td></tr>
<tr><td>Cyan</td><td>0 XXXXXXX</td><td>1 XXXXXXX</td><td>1 XXXXXXX</td></tr>
<tr><td>Yellow</td><td>1 XXXXXXX</td><td>1 XXXXXXX</td><td>0 XXXXXXX</td></tr>
<tr><td>White</td><td>1 XXXXXXX</td><td>1 XXXXXXX</td><td>1 XXXXXXX</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="9">This command has no effect when module is already in Idle On Mode.</td></tr>
</table>

IPF: Interface Pixel Format(3A00h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
3Ah	3A00h	-	-	-	-	-	IFPF[2:0]			07h

Description

This command sets the pixel format for the RGB image data used by the interface.
IFPF[2:0] : Pixel Format Definition.
If not used DPI interface, then the corresponding bits in the parameter are ignored.

IFPF[2:0]	Control Interface Color Format
001	SPI 1-1-1
010	SPI 8bit/pixel(256 colors);SPI 3-3-2
011	SPI 8bit/pixel(256 colors);SPI 256Gray
101	16bit/pixel(65,536 colors)
110	18bit/pixel(262,144 colors)
111	24bit/pixel(16.7M colors)
Others	reserved

SPI 1-1-1

RGB 1-1-1 bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1,2RAMD Data Write	1	x	x	P1[2]	P1[1]	P1[0]	P2[2]	P2[1]	P2[0]	1,2pixel Data Write
3,4RAMD Data Write	1	x	x	P3[2]	P3[1]	P3[0]	P4[2]	P4[1]	P4[0]	3,4pixel Data Write
5,6RAMD Data Write	1	x	x	P5[2]	P5[1]	P5[0]	P6[2]	P6[1]	P6[0]	5,6pixel Data Write
So on…										

RGB 1-1-1 bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1,2RAMD Data Write	1	x	P1[2]	P1[1]	P1[0]	x	P2[2]	P2[1]	P2[0]	1,2pixel Data Write
3,4RAMD Data Write	1	x	P3[2]	P3[1]	P3[0]	x	P4[2]	P4[1]	P4[0]	3,4pixel Data Write
5,6RAMD Data Write	1	x	P5[2]	P5[1]	P5[0]	x	P6[2]	P6[1]	P6[0]	5,6pixel Data Write
So on…										

RGB 1-1-1 bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1,2RAMD	1	P1[3]	P1[2]	P1[1]	P1[0]	P2[3]	P2[2]	P2[1]	P2[0]	1,2pixel

Data Write										Data Write
3,4RAMD Data Write	1	P3[3]	P3[2]	P3[1]	P3[0]	P4[3]	P4[2]	P4[1]	P4[0]	3,4pixel Data Write
5,6RAMD Data Write	1	P5[3]	P5[2]	P5[1]	P5[0]	P6[3]	P6[2]	P6[1]	P6[0]	5,6pixel Data Write
So on…										

SPI 3-3-2

RGB 3-3-2 bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st RAMD Data Write	1	R1[2]	R1[1]	R1[0]	G1[2]	G1[1]	G1[0]	B1[1]	B1[0]	1st pixel Data Write
2st RAMD Data Write	1	R2[2]	R2[1]	R2[0]	G2[2]	G2[1]	G2[0]	B2[1]	B2[0]	2st pixel Data Write
3st RAMD Data Write	1	R3[2]	R3[1]	R3[0]	G3[2]	G3[1]	G3[0]	B3[1]	B3[0]	3st pixel Data Write
So on…										

SPI 3-3-2 SPI 256 Gray

RGB 3-3-2 bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st RAMD Data Write	1	P1[7]	P1[6]	P1[5]	P1[4]	P1[3]	P12]	P1[1]	P1[0]	1st pixel Data Write
2st RAMD Data Write	1	P2[7]	P2[6]	P2[5]	P2[4]	P2[3]	P2[2]	P2[1]	P2[0]	2st pixel Data Write
3st RAMD Data Write	1	P3[7]	P3[6]	P3[5]	P3[4]	P3[3]	P3[2]	P3[1]	P3[0]	3st pixel Data Write
So on…										

Restriction	-

RAMWC: Write memory Continue (3Ch)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
3Ch	3C00h	D7	D6	D5	D4	D3	D2	D1	D0	Contents of memory is set randomly
	3C01h	D7	D6	D5	D4	D3	D2	D1	D0	
	3C02h	D7	D6	D5	D4	D3	D2	D1	D0	
	:	:	:	:	:	:	:	:	:	
Description		This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Please use MIPI HS format to write image data. If MV(36h-B5) = 0: Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. If MV(36h-B5) = 1: Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.								
Restriction		A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.								

RAMRDC: Memory Continuous Read (3Eh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
3Eh	3E00h	D7	D6	D5	D4	D3	D2	D1	D0	Contents of memory is set randomly
	3E01h	D7	D6	D5	D4	D3	D2	D1	D0	
	3E02h	D7	D6	D5	D4	D3	D2	D1	D0	
	:	:	:	:	:	:	:	:	:	
Description		This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands. If MV(36h-B5) = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If MV(36h-B5) = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.								
Restriction		There is no restriction on length of parameters.								

STESL: Set tearing effect scan line (4400h~4401h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
44h	4400h	N15	N14	N13	N12	N11	N10	N9	N8	00h
	4401h	N7	N6	N5	N4	N3	N2	N1	N0	00h
Description		This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The Tearing Effect Line On has parameter, which describes the mode of the Tearing Effect Output Line Mode. The Tearing Effect Output line consists of V-Blanking information only.  Note that STESL with N[15:0]="0000h" is equivalent to TEON with M="0" The Tearing Effect Output line shall be active low when the display module is in sleep in mode. This command takes effect on the frame following the current frame. Therefore, if the TE output is already on, the TE output shall continue to operate as programmed by the previous "TEON(35h)" or "STESL(44h) command" until the end of the frame.								
Restriction		-								

GSL: Get Scan Line (4500h~4501h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
45h	4500h	N15	N14	N13	N12	N11	N10	N9	N8	00h
	4501h	N7	N6	N5	N4	N3	N2	N1	N0	00h
Description		This command returns the current scan line, N, used to update the display module. The total number of scan lines on display is defined as VSYNC+VBP+VADR+VFP. The first scan line is defined as the first line of V Sync and is denoted as Line 0. When in Sleep in mode, the returned value is undefined.								
Restriction		-								

RAMW: Write AOD RAM Start (4Ch)

Write to the AOD RAM according to the digital or analog clock graphics, please refer to register 82h CLOCKM setting.
The order in which the analog clock is written to the AOD RAM is the minute hand、second hand and center square.
Please use MIPI HS format to write image data.
RAM Size: Minute hand = 240x40x8x4 bit
Second hand = 240x20x8x4 bit
Center square = 50x50x8x4 bit

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
4Ch	4C00h	D7	D6	D5	D4	D3	D2	D1	D0	Write RAM start
	4C01h	D7	D6	D5	D4	D3	D2	D1	D0	
	4C02h	D7	D6	D5	D4	D3	D2	D1	D0	
	:	:	:	:	:	:	:	:	:	
Description		This command is used for AOD.								
Restriction		When writing data to AOD ram, the number of data byte must be divisible by 3.								

DSTBON: Deep Standby Mode On (4F00h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
4Fh	4F00h	-	-	-	-	-	-	-	DSTB	00h
Description		This command is used to enter deep standby mode. DSTB="1", enter deep standby mode. Notes: 1. Before setting this command, enter Sleep In Mode (10h) and Display Off (28h) first. User cannot write this register in Sleep-Out and Display-On mode. 2. It cannot exit Deep Standby Mode while setting bit DSTB from "1" to "0". 3. To exit Deep Standby Mode, input low pulse more than 1 msec to pin RSTB. 4. When Driver IC in Deep Standby Mode, the lane status of DSI must keep to LP-00.								
Restriction		-								

WDB: Write Display Brightness (5100h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
51h	5100h	DBV[7:0]								FFh
Description		This command is used to adjust brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.								
Restriction		-								

RDB: Read Display Brightness (5200h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
52h	5200h	DBV[7:0]								FFh
Description		This command is used to return the brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.								
Restriction		-								

HBMSEL: High Brightness Mode Selection (5300h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>53h</td><td>5300h</td><td colspan="8">HBM_EN[7:0]</td><td>5Ah</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to select high brightness mode.
HBM_EN:used to enable or disablehigh brightness mode.
<table><tr><th>HBM_EN</th><th>Function</th></tr><tr><td>5Ah</td><td>Disable HBM</td></tr><tr><td>A5h</td><td>Enable HBM</td></tr></table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

RHBM: Read High Brightness Mode (5400h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>54h</td><td>5400h</td><td colspan="8">HBM_EN[7:0]</td><td>5Ah</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to select high brightness mode.
HBM_EN: the status of high brightness mode.

<table><tr><th>HBM_EN</th><th>Function</th></tr><tr><td>5Ah</td><td>Disable HBM</td></tr><tr><td>A5h</td><td>Enable HBM</td></tr></table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

NEM: Emission Width for Normal Mode (5500h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>55h</td><td>5500h</td><td colspan="8">NOR_WIDTH[7:0]</td><td>05h</td></tr>
<tr><td>Description</td><td colspan="9">This command is used to configure the emission for Normal mode.
NOR_WIDTH[7:0]: the initial EM width for idle mode.

<table><tr><th>NOR_WIDTH[7:0]</th><th>Function</th></tr><tr><td>00h</td><td>0 h-syncs</td></tr><tr><td>01h</td><td>1 h-syncs</td></tr><tr><td>02h</td><td>2 h-syncs</td></tr><tr><td>…</td><td>1 h-sync/step</td></tr><tr><td>05h</td><td>5 h-syncs</td></tr><tr><td>…</td><td>1 h-sync/step</td></tr><tr><td>FFh</td><td>255 h-syncs</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="9">-</td></tr>
</table>

Note:检测写动作，即写了此寄存器后，待DVS生效时，将55h寄存器值写入或将值的作用体现在GOA的STE信号

IEM: Emission Width for Idle mode (5600h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>56h</td><td>5600h</td><td colspan="8">IDLE_WIDTH[7:0]</td><td>05h</td></tr>
<tr><td>Description</td><td colspan="9">This command is used to configure the emission for Idle mode.
IDLE_WIDTH[7:0]: the initial EM width for idle mode.

<table><tr><th>IDLE_WIDTH[7:0]</th><th>Function</th></tr><tr><td>00h</td><td>0 h-syncs</td></tr><tr><td>01h</td><td>1 h-syncs</td></tr><tr><td>02h</td><td>2 h-syncs</td></tr><tr><td>…</td><td>1 h-sync/step</td></tr><tr><td>05h</td><td>5 h-syncs</td></tr><tr><td>…</td><td>1 h-sync/step</td></tr><tr><td>FFh</td><td>255 h-syncs</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="9">-</td></tr>
</table>

Note:检测写动作，即写了此寄存器后，待DVS生效时，将56h寄存器值写入或将值的作用体现在GOA的STE信号上

HEM: Emission Width for HBM mode (5700h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>57h</td><td>5700h</td><td colspan="8">HBM_WIDTH[7:0]</td><td>05h</td></tr>
<tr><td>Description</td><td colspan="9">This command is used to configure the emission for HBM mode.
HBM_WIDTH[7:0]: the initial EM width for HBM mode.

<table><tr><th>HBM_WIDTH[7:0]</th><th>Function</th></tr><tr><td>00h</td><td>0 h-syncs</td></tr><tr><td>01h</td><td>1 h-syncs</td></tr><tr><td>02h</td><td>2 h-syncs</td></tr><tr><td>…</td><td>1 h-sync/step</td></tr><tr><td>05h</td><td>5 h-syncs</td></tr><tr><td>…</td><td>1 h-sync/step</td></tr><tr><td>FFh</td><td>255 h-syncs</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="9">-</td></tr>
</table>

Note:检测写动作，即写了此寄存器后，待DVS生效时，将57h寄存器值写入或将值的作用体现在GOA的STE信号上

RAMWC: Write AOD RAM Continue (5Ch)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
5Ch	5C00h	D7	D6	D5	D4	D3	D2	D1	D0	Write RAM Continuous
	5C01h	D7	D6	D5	D4	D3	D2	D1	D0	
	5C02h	D7	D6	D5	D4	D3	D2	D1	D0	
	:	:	:	:	:	:	:	:	:	
Description		This command is used for AOD. Please use MIPI HS format to write image data.								
Restriction		When writing data to AOD ram, the number of data byte must be divisible by 3.								

BACTR: Brightness Adjustment Control (6000h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
60h	6000h	EM_M	EM_DIM_EN	HMS_DIM_EN	IMS_DIM_EN	-	BC_LINEAR	BC_DIM_M	BC_DIM_EN	01h

Description

This command is used to configure the dimming for 51h and mode switch.
BC_DIM_EN: enable or disable the 51h dimming.

BC_DIM_EN	Function
0	Disable 51h dimming
1	Enable 51h dimming

BC_DIM_M: set the 51h dimming mode.

BC_DIM_M	Function
0	fixed time
1	fixed step

BC_LINEAR: set the brightness curve trend.

BC_LINEAR	Function
0	2.2
1	1.0

IMS_DIM_EN/HBM_DIM_EN: enable or disable the dimming of mode switch.

IMS_DIM_EN/HMS_DIM_EN	Function
0	Disable mode switch dimming
1	Enable mode switch dimming

EM_DIM_EN: enable or disable the dimming for changing emission ratio.

EM_DIM_EN	Function
0	Disable change emission ratio dimming
1	Enable change emission ratio dimming

EM_M: select the mode of Emission width.

EM_M	Function
0	Reference emission width from STV1
1	Reference emission width from 55h

Restriction	-

Note1：Idle和HBM dimming mode独立使能原因为：如果DGC调节Normal和Idle，高亮可能不调节DGC，通过STE实现；
Note2：BC_LINEAR通过Data Ratio查找表或51h设定的值转换为对应的Data Ratio实现线性1.0和2.2。
Note3：EM_DIM_EN控制的dimming参数详见Page4B1h寄存器

DECTR: Dynamic ELVSS Function Control (6200h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>62h</td><td>6200h</td><td>-</td><td>-</td><td>-</td><td>D_DIM_EN</td><td>-</td><td>IDLE_DELVSS_EN</td><td colspan="2">DELVSSM[1:0]</td><td>04h</td></tr>
<tr><td>Description</td><td colspan="9">This command is used to select the dynamic elvss(VEN) level.
DELVSSM [1:0]: different level.
<table><tr><th>DELVSSM[1:0]</th><th>Function</th></tr><tr><td>00</td><td>Close Dynamic Elvss</td></tr><tr><td>01</td><td>Mode1</td></tr><tr><td>10</td><td>Mode2</td></tr><tr><td>11</td><td>Mode3</td></tr></table>IDLE_DELVSS_EN: Enable or Disable Dynamic ELVSS function in idle mode.
<table><tr><th>IDLE_DELVSS_EN</th><th>Function</th></tr><tr><td>0</td><td>Close Dynamic ELVSS</td></tr><tr><td>1</td><td>Same to normal mode</td></tr></table>D_DIM_EN: Enable or Disable Dynamic ELVSS Dimming function.
<table><tr><th>D_DIM_EN</th><th>Function</th></tr><tr><td>0</td><td>Dimming function disable</td></tr><tr><td>1</td><td>Dimming function enable</td></tr></table>Note: Mode1: DBV+AVR ; Mode2:DBV ; Mode3:AVR</td></tr>
<tr><td>Restriction</td><td colspan="9">-</td></tr>
</table>

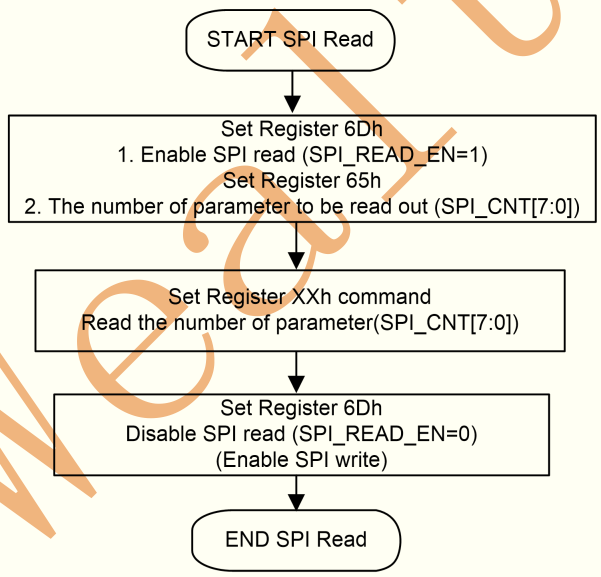
SRECTR:Sunlight Readable Enhance Function Control (6300h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>63h</td><td>6300h</td><td>-</td><td>-</td><td>-</td><td>SRE_EN</td><td>-</td><td>-</td><td colspan="2">SRE_SIZE[1:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to set the SRE function.
SRE_EN: Sunlight Readable Enhance functions enable control.
<table>
<tr><th>SRE_EN</th><th>Function</th></tr>
<tr><td>0</td><td>SRE function disable</td></tr>
<tr><td>1</td><td>SRE function enable</td></tr>
</table>
SRE_SIZE[1:0]: Sunlight Readable Enhance function level set, while level0 is the lowest and level2 is the highest.
<table>
<tr><th>SRE_SIZE[1:0]</th><th>Function</th></tr>
<tr><td>00</td><td>SRE level0</td></tr>
<tr><td>01</td><td>SRE level1</td></tr>
<tr><td>10</td><td>SRE level2</td></tr>
<tr><td>11</td><td>SRE level0</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

GACMSET: Gamma Set and Color ModeSet (6400h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>64h</td><td>6400h</td><td>-</td><td>-</td><td colspan="2">GAM_HBM[1:0]</td><td colspan="2">GAM_IDLE[1:0]</td><td colspan="2">GAM_NOR[1:0]</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to select the Gamma and Color Mode.
GAM_HBM[1:0]/ GAM_IDLE[1:0]/ GAM_NOR[1:0]: select the gamma for HBM/Idle/normal mode.
<table><tr><th>GAM_HBM[1:0]/ GAM_IDLE[1:0]/ GAM_NOR[1:0]</th><th>Gamma</th></tr><tr><td>00h</td><td>Gamma1</td></tr><tr><td>01h</td><td>Gamma2</td></tr><tr><td>10h</td><td>Gamma3</td></tr><tr><td>11h</td><td>Gamma1</td></tr></table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

SPIRDC:SPI read manufacture command control (6500h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>65h</td><td>6500h</td><td colspan="8">SPI_CNT[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="9">This command is used to set the number of parameter to be read out from R/W command in SPI interface.
It must set SPI_READ_EN is enable(6Dh) before reading command.
<table>
<tr><th>SPI_CNT[7:0]</th><th>The number of parameter to be read out</th></tr>
<tr><td>00h</td><td>1</td></tr>
<tr><td>01h</td><td>2</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>FFh</td><td>256</td></tr>
</table>
SPI_CNT[7:0]: The number of parameter to be read out

</td></tr>
<tr><td>Restriction</td><td colspan="9">Note:65h only support SPI write</td></tr>
</table>

CICEN: Circular Edge Optimization Algorithm Enable(6700h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>67h</td><td>6700h</td><td>-</td><td>-</td><td colspan="2">UD_POS[1:0]</td><td>-</td><td>-</td><td>-</td><td>R_O_EN</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">R_O_EN:Out circular edge optimization algorithm enable.
<table>
<tr><th>R_O_EN</th><th>function</th></tr>
<tr><td>0</td><td>disable</td></tr>
<tr><td>1</td><td>enable</td></tr>
</table>
UD_POS[1:0]:The mode config of out circular.
<table>
<tr><th>UD_POS[1:0]</th><th>Mode config</th></tr>
<tr><td>00</td><td>Both big circle</td></tr>
<tr><td>01</td><td>UP big，Down small</td></tr>
<tr><td>10</td><td>UP small，Down big</td></tr>
<tr><td>11</td><td>Both small circle</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

OLOAEN: Oblique Line Optimization Algorithm Enable (6800h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
68h	6800h	-	-	OBL_Y	OBL_X	-	-	-	OBL_EN	01h
Description		OBL_EN：The Oblique Line Optimization Algorithm Enable. OBL_X/ OBL_Y:Mirror select.								
Restriction										

OBL_EN	function
0	“0”=disable
1	“1”= enable

OBL_X	OBL_Y	function
0	0	normal
1	0	X Mirror
0	1	Y Mirror
1	1	180 degreereversal

NOTCHEN: Notch AlgorithmEnable(6900h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>69h</td><td>6900h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>Notch_EN</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">Notch_EN:Notch algorithm enable.
<table><tr><th>Notch_EN</th><th>function</th></tr><tr><td>0</td><td>disable</td></tr><tr><td>1</td><td>enable</td></tr></table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9"></td></tr>
</table>

INCIREN: Inside CircularAlgorithmEnable(6A00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>6Ah</td><td>6A00h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>R_I_EN</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">R_I_EN:Inside circular edge optimization algorithm enable.
<table><tr><th>R_I_EN</th><th>function</th></tr><tr><td>0</td><td>disable</td></tr><tr><td>1</td><td>enable</td></tr></table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9"></td></tr>
</table>

SWIREMANU: SWIRE manual control (6C00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>6Ch</td><td>6C00h</td><td colspan="8">SMANU_CTL[7:0]</td><td>5Ah</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">SMANU_CTL [7:0]:SWIRE Manual control
<table><tr><th>SMANU_CTL[7:0]</th><th>SWIRE manual control</th></tr><tr><td>5Ah</td><td>ELVDD/ELVSS power Off</td></tr><tr><td>A5h</td><td>ELVDD/ELVSS power On</td></tr><tr><td>Others</td><td>ELVDD/ELVSS power Off</td></tr></table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

SPIRDC:SPI read manufacture command Enable (6D00h)

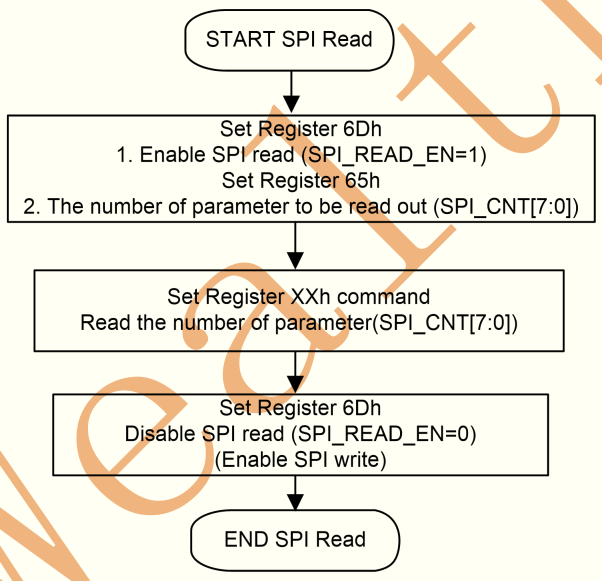
Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
6Dh	6D00h	-	-	-	-	-	-	-	SPI_READ_EN	00h

Description

This command is used to enable/disable SPI read R/W command
SPI_READ_EN: 8bit/9bit/Quad SPI read R/W command enable

SPI_READ_EN	Function
0	8bit/9bit/Quad SPI read R/W command Disable
1	8bit/9bit/Quad SPI read R/W command Enable

SPI_CNT[7:0]: The number of parameter to be read out



Restriction	Note:6Dh only support SPI write

AODCLKS: AOD clock setting (8200h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
82h	8200h	AOD_EN	CLOCKM	HOURM	TIMEM	DCLKM_EN	-	-	-	00h

Description

This command is used to set clock mode.
AOD_EN: AOD enable.

AOD_EN	AOD mode enable / disable when 39h send
0	AOD Disable，Enter Idle mode after 39h take effect
1	AOD Enable，Enter AOD mode after 39h take effect

CLOCKM: clock mode selection.

CLOCKM	AOD Clock mode selection
0	Digital clock
1	Analog clock

HOURM: hour mode selection.

HOURM	Hour mode selection
0	24-hour clock
1	12-hour clock

TIMEM: AOD time mode selection.

TIMEM	AOD time mode selection
0	Mode0 （eg:0x0A,0x08,0x0F means 10:08:15）
1	Mode1 （eg:0x10,0x08,0x15 means 10:08:15）

DCLKM_EN: Digital clock mark enable selection.

DCLKM_EN	Digital Clock mark display enable
0	disable （eg 10 08）
1	enable（eg 10：08）

Restriction: -

AODTIME: AOD Time setting (8300h~8302h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="3">83h</td><td>8300h</td><td colspan="8">Hour[7:0]</td><td>10h</td></tr>
<tr><td>8301h</td><td colspan="8">Minute[7:0]</td><td>08h</td></tr>
<tr><td>8302h</td><td colspan="8">Second[7:0]</td><td>05h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to set the AOD time defined by TIMEM.
<table><tr><th>TIMEM</th><th>AOD time mode selection</th></tr><tr><td>0</td><td>Mode0 （eg:0x0A,0x08,0x0F means 10:08:15）</td></tr><tr><td>1</td><td>Mode1 （eg:0x10,0x08,0x15 means 10:08:15）</td></tr></table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

AODSECCAL: AOD second hand calibration method (8400h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
84h	8400h	No Argument								AOD second hand calibration
Description		This command is used to calibrate second hand time, a total of 5 times need to be sent for calibration. Please refer to register 85h CALB_CYCLE[1:0] to set the calibration interval.								
Restriction										

AODSYNCP: AOD synchronization cycle setting (8500h~8504h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
85h	8500h	SECOND_OFFSET[9:8]		-	CALB_EN	-	-	CALB_CYCLE[1:0]		01h
	8501h	SECOND_OFFSET[7:0]								00h
	8502h	SECOND_COUNT[23:16]								29h
	8503h	SECOND_COUNT[15:8]								F6h
	8504h	SECOND_COUNT[7:0]								30h

Description

This command is used to set synchronization cycle.

CALB_EN: Calibration enable/disable.

CALB_EN	Calibration enable / disable
0	Disable
1	Enable

CALB_CYCLE[1:0]: Calibration cycle setting,
The command of 84h is used to calibrate second hand time.

CALB_CYCLE[1:0]	Calibration cycle
00	16.67ms
01	33.33ms
10	66.67ms
11	100ms

SECOND_COUNT: The number of clock contained in 1s. (1clock=osc/8 ; osc=22MHz)

SECOND_OFFSET[7:0]: SECOND_CONUT offset value. (1clock=osc/8 ; osc=22MHz)
As second hand time compensation, avoid DDIC time faster than Host.

SECOND_OFFSET[9:0]	SECOND_COUNT offset value
000h	0 clock
001h	1 clock
010h	2 clock
…	…
3FE	1022 clock
3FF	1023 clock

Restriction	-

DCLKFSIZE: Digital clock font size setting (8600h~8602h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="3">86h</td><td>8600h</td><td>-</td><td colspan="7">NUMSize_R[6:0]</td><td>20h</td></tr>
<tr><td>8601h</td><td>-</td><td colspan="7">NUMSize_C[6:0]</td><td>17h</td></tr>
<tr><td>8602h</td><td>-</td><td colspan="7">MARKSize_C[6:0]</td><td>0Bh</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to set the digital clock font size.
<table>
<tr><th>NUMSize_R[6:0]</th><th>Row</th><th>xxxSize_C[6:0]</th><th>Column</th></tr>
<tr><td>00h~11h</td><td>reserve</td><td>00h~0Ch</td><td>reserve</td></tr>
<tr><td>12h</td><td>18 line</td><td>0Dh</td><td>13 column</td></tr>
<tr><td>13h</td><td>19 line</td><td>0Eh</td><td>14 column</td></tr>
<tr><td>14h</td><td>20 line</td><td>0Fh</td><td>15 column</td></tr>
<tr><td>……</td><td>……</td><td>……</td><td>……</td></tr>
<tr><td>30h</td><td>48 line</td><td>21h</td><td>33 column</td></tr>
<tr><td>31h</td><td>49 line</td><td>22h</td><td>34 column</td></tr>
<tr><td>32h</td><td>50 line</td><td>23h</td><td>35 column</td></tr>
<tr><td>……</td><td>……</td><td>……</td><td>……</td></tr>
<tr><td>5F</td><td>95 line</td><td>47h</td><td>71 column</td></tr>
<tr><td>60h~7Fh</td><td>96 line</td><td>48h~7Fh</td><td>72 column</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

说明：冒号的行数和数字的行数相同，故不用单独设定。

DHCOLORR: Digital clock Hour color setting (8700h~87FFh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
87h	8700h	DH_Color_R0[7:0]								00h
	8701h	DH_Color_R1[7:0]								01h
	8702h	DH_Color_R2[7:0]								02h
	8703h	DH_Color_R3[7:0]								03h
	8704h	DH_Color_R4[7:0]								04h
	8705h	DH_Color_R5[7:0]								05h
	8706h	DH_Color_R6[7:0]								06h
	8707h	DH_Color_R7[7:0]								07h
	8708h	DH_Color_R8[7:0]								08h
	8709h	DH_Color_R9[7:0]								09h
	870Ah	DH_Color_R10[7:0]								0Ah
	870Bh	DH_Color_R11[7:0]								0Bh
	870Ch	DH_Color_R12[7:0]								0Ch
	870Dh	DH_Color_R13[7:0]								0Dh
	870Eh	DH_Color_R14[7:0]								0Eh
	870Fh	DH_Color_R15[7:0]								0Fh
	8710h	DH_Color_R16[7:0]								10h
	8711h	DH_Color_R17[7:0]								11h
	8712h	DH_Color_R18[7:0]								12h
	8713h	DH_Color_R19[7:0]								13h
	8714h	DH_Color_R20[7:0]								14h
	8715h	DH_Color_R21[7:0]								15h
	8716h	DH_Color_R22[7:0]								16h
	8717h	DH_Color_R23[7:0]								17h
	8718h	DH_Color_R24[7:0]								18h
	8719h	DH_Color_R25[7:0]								19h
	871Ah	DH_Color_R26[7:0]								1Ah
	871Bh	DH_Color_R27[7:0]								1Bh
	871Ch	DH_Color_R28[7:0]								1Ch
	871Dh	DH_Color_R29[7:0]								1Dh
	871Eh	DH_Color_R30[7:0]								1Eh
	871Fh	DH_Color_R31[7:0]								1Fh
	8720h	DH_Color_R32[7:0]								20h
	8721h	DH_Color_R33[7:0]								21h
	8722h	DH_Color_R34[7:0]								22h
	8723h	DH_Color_R35[7:0]								23h
	8724h	DH_Color_R36[7:0]								24h
	8725h	DH_Color_R37[7:0]								25h
	8726h	DH_Color_R38[7:0]								26h

	8727h	DH_Color_R39[7:0]	27h
	8728h	DH_Color_R40[7:0]	28h
	8729h	DH_Color_R41[7:0]	29h
	872Ah	DH_Color_R42[7:0]	2Ah
	872Bh	DH_Color_R43[7:0]	2Bh
	872Ch	DH_Color_R44[7:0]	2Ch
	872Dh	DH_Color_R45[7:0]	2Dh
	872Eh	DH_Color_R46[7:0]	2Eh
	872Fh	DH_Color_R47[7:0]	2Fh
	8730h	DH_Color_R48[7:0]	30h
	8731h	DH_Color_R49[7:0]	31h
	8732h	DH_Color_R50[7:0]	32h
	8733h	DH_Color_R51[7:0]	33h
	8734h	DH_Color_R52[7:0]	34h
	8735h	DH_Color_R53[7:0]	35h
	8736h	DH_Color_R54[7:0]	36h
	8737h	DH_Color_R55[7:0]	37h
	8738h	DH_Color_R56[7:0]	38h
	8739h	DH_Color_R57[7:0]	39h
	873Ah	DH_Color_R58[7:0]	3Ah
	873Bh	DH_Color_R59[7:0]	3Bh
	873Ch	DH_Color_R60[7:0]	3Ch
	873Dh	DH_Color_R61[7:0]	3Dh
	873Eh	DH_Color_R62[7:0]	3Eh
	873Fh	DH_Color_R63[7:0]	3Fh
	8740h	DH_Color_R64[7:0]	40h
	8741h	DH_Color_R65[7:0]	41h
	8742h	DH_Color_R66[7:0]	42h
	8743h	DH_Color_R67[7:0]	43h
	8744h	DH_Color_R68[7:0]	44h
	8745h	DH_Color_R69[7:0]	45h
	8746h	DH_Color_R70[7:0]	46h
	8747h	DH_Color_R71[7:0]	47h
	8748h	DH_Color_R72[7:0]	48h
	8749h	DH_Color_R73[7:0]	49h
	874Ah	DH_Color_R74[7:0]	4Ah
	874Bh	DH_Color_R75[7:0]	4Bh
	874Ch	DH_Color_R76[7:0]	4Ch
	874Dh	DH_Color_R77[7:0]	4Dh
	874Eh	DH_Color_R78[7:0]	4Eh
	874Fh	DH_Color_R79[7:0]	4Fh
	8750h	DH_Color_R80[7:0]	50h

	8751h	DH_Color_R81[7:0]	51h
	8752h	DH_Color_R82[7:0]	52h
	8753h	DH_Color_R83[7:0]	53h
	8754h	DH_Color_R84[7:0]	54h
	8755h	DH_Color_R85[7:0]	55h
	8756h	DH_Color_R86[7:0]	56h
	8757h	DH_Color_R87[7:0]	57h
	8758h	DH_Color_R88[7:0]	58h
	8759h	DH_Color_R89[7:0]	59h
	875Ah	DH_Color_R90[7:0]	5Ah
	875Bh	DH_Color_R91[7:0]	5Bh
	875Ch	DH_Color_R92[7:0]	5Ch
	875Dh	DH_Color_R93[7:0]	5Dh
	875Eh	DH_Color_R94[7:0]	5Eh
	875Fh	DH_Color_R95[7:0]	5Fh
	8760h	DH_Color_R96[7:0]	60h
	8761h	DH_Color_R97[7:0]	61h
	8762h	DH_Color_R98[7:0]	62h
	8763h	DH_Color_R99[7:0]	63h
	8764h	DH_Color_R100[7:0]	64h
	8765h	DH_Color_R101[7:0]	65h
	8766h	DH_Color_R102[7:0]	66h
	8767h	DH_Color_R103[7:0]	67h
	8768h	DH_Color_R104[7:0]	68h
	8769h	DH_Color_R105[7:0]	69h
	876Ah	DH_Color_R106[7:0]	6Ah
	876Bh	DH_Color_R107[7:0]	6Bh
	876Ch	DH_Color_R108[7:0]	6Ch
	876Dh	DH_Color_R109[7:0]	6Dh
	876Eh	DH_Color_R110[7:0]	6Eh
	876Fh	DH_Color_R111[7:0]	6Fh
	8770h	DH_Color_R112[7:0]	70h
	8771h	DH_Color_R113[7:0]	71h
	8772h	DH_Color_R114[7:0]	72h
	8773h	DH_Color_R115[7:0]	73h
	8774h	DH_Color_R116[7:0]	74h
	8775h	DH_Color_R117[7:0]	75h
	8776h	DH_Color_R118[7:0]	76h
	8777h	DH_Color_R119[7:0]	77h
	8778h	DH_Color_R120[7:0]	78h
	8779h	DH_Color_R121[7:0]	79h
	877Ah	DH_Color_R122[7:0]	7Ah

	877Bh	DH_Color_R123[7:0]	7Bh
	877Ch	DH_Color_R124[7:0]	7Ch
	877Dh	DH_Color_R125[7:0]	7Dh
	877Eh	DH_Color_R126[7:0]	7Eh
	877Fh	DH_Color_R127[7:0]	7Fh
	8780h	DH_Color_R128[7:0]	80h
	8781h	DH_Color_R129[7:0]	81h
	8782h	DH_Color_R130[7:0]	82h
	8783h	DH_Color_R131[7:0]	83h
	8784h	DH_Color_R132[7:0]	84h
	8785h	DH_Color_R133[7:0]	85h
	8786h	DH_Color_R134[7:0]	86h
	8787h	DH_Color_R135[7:0]	87h
	8788h	DH_Color_R136[7:0]	88h
	8789h	DH_Color_R137[7:0]	89h
	878Ah	DH_Color_R138[7:0]	8Ah
	878Bh	DH_Color_R139[7:0]	8Bh
	878Ch	DH_Color_R140[7:0]	8Ch
	878Dh	DH_Color_R141[7:0]	8Dh
	878Eh	DH_Color_R142[7:0]	8Eh
	878Fh	DH_Color_R143[7:0]	8Fh
	8790h	DH_Color_R144[7:0]	90h
	8791h	DH_Color_R145[7:0]	91h
	8792h	DH_Color_R146[7:0]	92h
	8793h	DH_Color_R147[7:0]	93h
	8794h	DH_Color_R148[7:0]	94h
	8795h	DH_Color_R149[7:0]	95h
	8796h	DH_Color_R150[7:0]	96h
	8797h	DH_Color_R151[7:0]	97h
	8798h	DH_Color_R152[7:0]	98h
	8799h	DH_Color_R153[7:0]	99h
	879Ah	DH_Color_R154[7:0]	9Ah
	879Bh	DH_Color_R155[7:0]	9Bh
	879Ch	DH_Color_R156[7:0]	9Ch
	879Dh	DH_Color_R157[7:0]	9Dh
	879Eh	DH_Color_R158[7:0]	9Eh
	879Fh	DH_Color_R159[7:0]	9Fh
	87A0h	DH_Color_R160[7:0]	A0h
	87A1h	DH_Color_R161[7:0]	A1h
	87A2h	DH_Color_R162[7:0]	A2h
	87A3h	DH_Color_R163[7:0]	A3h
	87A4h	DH_Color_R164[7:0]	A4h

	87A5h	DH_Color_R165[7:0]	A5h
	87A6h	DH_Color_R166[7:0]	A6h
	87A7h	DH_Color_R167[7:0]	A7h
	87A8h	DH_Color_R168[7:0]	A8h
	87A9h	DH_Color_R169[7:0]	A9h
	87AAh	DH_Color_R170[7:0]	AAh
	87ABh	DH_Color_R171[7:0]	ABh
	87ACh	DH_Color_R172[7:0]	ACh
	87ADh	DH_Color_R173[7:0]	ADh
	87AEh	DH_Color_R174[7:0]	AEh
	87AFh	DH_Color_R175[7:0]	AFh
	87B0h	DH_Color_R176[7:0]	B0h
	87B1h	DH_Color_R177[7:0]	B1h
	87B2h	DH_Color_R178[7:0]	B2h
	87B3h	DH_Color_R179[7:0]	B3h
	87B4h	DH_Color_R180[7:0]	B4h
	87B5h	DH_Color_R181[7:0]	B5h
	87B6h	DH_Color_R182[7:0]	B6h
	87B7h	DH_Color_R183[7:0]	B7h
	87B8h	DH_Color_R184[7:0]	B8h
	87B9h	DH_Color_R185[7:0]	B9h
	87BAh	DH_Color_R186[7:0]	BAh
	87BBh	DH_Color_R187[7:0]	BBh
	87BCh	DH_Color_R188[7:0]	BCh
	87BDh	DH_Color_R189[7:0]	BDh
	87BEh	DH_Color_R190[7:0]	BEh
	87BFh	DH_Color_R191[7:0]	BFh
	87C0h	DH_Color_R192[7:0]	C0h
	87C1h	DH_Color_R193[7:0]	C1h
	87C2h	DH_Color_R194[7:0]	C2h
	87C3h	DH_Color_R195[7:0]	C3h
	87C4h	DH_Color_R196[7:0]	C4h
	87C5h	DH_Color_R197[7:0]	C5h
	87C6h	DH_Color_R198[7:0]	C6h
	87C7h	DH_Color_R199[7:0]	C7h
	87C8h	DH_Color_R200[7:0]	C8h
	87C9h	DH_Color_R201[7:0]	C9h
	87CAh	DH_Color_R202[7:0]	CAh
	87CBh	DH_Color_R203[7:0]	CBh
	87CCh	DH_Color_R204[7:0]	CCh
	87CDh	DH_Color_R205[7:0]	CDh
	87CEh	DH_Color_R206[7:0]	CEh

	87CFh	DH_Color_R207[7:0]	CFh
	87D0h	DH_Color_R208[7:0]	D0h
	87D1h	DH_Color_R209[7:0]	D1h
	87D2h	DH_Color_R210[7:0]	D2h
	87D3h	DH_Color_R211[7:0]	D3h
	87D4h	DH_Color_R212[7:0]	D4h
	87D5h	DH_Color_R213[7:0]	D5h
	87D6h	DH_Color_R214[7:0]	D6h
	87D7h	DH_Color_R215[7:0]	D7h
	87D8h	DH_Color_R216[7:0]	D8h
	87D9h	DH_Color_R217[7:0]	D9h
	87DAh	DH_Color_R218[7:0]	DAh
	87DBh	DH_Color_R219[7:0]	DBh
	87DCh	DH_Color_R220[7:0]	DCh
	87DDh	DH_Color_R221[7:0]	DDh
	87DEh	DH_Color_R222[7:0]	DEh
	87DFh	DH_Color_R223[7:0]	DFh
	87E0h	DH_Color_R224[7:0]	E0h
	87E1h	DH_Color_R225[7:0]	E1h
	87E2h	DH_Color_R226[7:0]	E2h
	87E3h	DH_Color_R227[7:0]	E3h
	87E4h	DH_Color_R228[7:0]	E4h
	87E5h	DH_Color_R229[7:0]	E5h
	87E6h	DH_Color_R230[7:0]	E6h
	87E7h	DH_Color_R231[7:0]	E7h
	87E8h	DH_Color_R232[7:0]	E8h
	87E9h	DH_Color_R233[7:0]	E9h
	87EAh	DH_Color_R234[7:0]	EAh
	87EBh	DH_Color_R235[7:0]	EBh
	87ECh	DH_Color_R236[7:0]	ECh
	87EDh	DH_Color_R237[7:0]	EDh
	87EEh	DH_Color_R238[7:0]	EEh
	87EFh	DH_Color_R239[7:0]	EFh
	87F0h	DH_Color_R240[7:0]	F0h
	87F1h	DH_Color_R241[7:0]	F1h
	87F2h	DH_Color_R242[7:0]	F2h
	87F3h	DH_Color_R243[7:0]	F3h
	87F4h	DH_Color_R244[7:0]	F4h
	87F5h	DH_Color_R245[7:0]	F5h
	87F6h	DH_Color_R246[7:0]	F6h
	87F7h	DH_Color_R247[7:0]	F7h
	87F8h	DH_Color_R248[7:0]	F8h

	87F9h	DH_Color_R249[7:0]	F9h
	87FAh	DH_Color_R250[7:0]	FAh
	87FBh	DH_Color_R251[7:0]	FBh
	87FCh	DH_Color_R252[7:0]	FCh
	87FDh	DH_Color_R253[7:0]	FDh
	87FEh	DH_Color_R254[7:0]	FEh
	87FFh	DH_Color_R255[7:0]	FFh
Description		This command is used to set digital clock hour color.	
Restriction		-	

DHCOLORG: Digital clock Hour color setting (8800h~88FFh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
88h	8800h	DH_Color_G0[7:0]								00h
	8801h	DH_Color_G1[7:0]								01h
	8802h	DH_Color_G2[7:0]								02h
	8803h	DH_Color_G3[7:0]								03h
	8804h	DH_Color_G4[7:0]								04h
	8805h	DH_Color_G5[7:0]								05h
	8806h	DH_Color_G6[7:0]								06h
	8807h	DH_Color_G7[7:0]								07h
	8808h	DH_Color_G8[7:0]								08h
	8809h	DH_Color_G9[7:0]								09h
	880Ah	DH_Color_G10[7:0]								0Ah
	880Bh	DH_Color_G11[7:0]								0Bh
	880Ch	DH_Color_G12[7:0]								0Ch
	880Dh	DH_Color_G13[7:0]								0Dh
	880Eh	DH_Color_G14[7:0]								0Eh
	880Fh	DH_Color_G15[7:0]								0Fh
	8810h	DH_Color_G16[7:0]								10h
	8811h	DH_Color_G17[7:0]								11h
	8812h	DH_Color_G18[7:0]								12h
	8813h	DH_Color_G19[7:0]								13h
	8814h	DH_Color_G20[7:0]								14h
	8815h	DH_Color_G21[7:0]								15h
	8816h	DH_Color_G22[7:0]								16h
	8817h	DH_Color_G23[7:0]								17h
	8818h	DH_Color_G24[7:0]								18h
	8819h	DH_Color_G25[7:0]								19h
	881Ah	DH_Color_G26[7:0]								1Ah
	881Bh	DH_Color_G27[7:0]								1Bh
	881Ch	DH_Color_G28[7:0]								1Ch
	881Dh	DH_Color_G29[7:0]								1Dh
	881Eh	DH_Color_G30[7:0]								1Eh
	881Fh	DH_Color_G31[7:0]								1Fh
	8820h	DH_Color_G32[7:0]								20h
	8821h	DH_Color_G33[7:0]								21h
	8822h	DH_Color_G34[7:0]								22h
	8823h	DH_Color_G35[7:0]								23h
	8824h	DH_Color_G36[7:0]								24h
	8825h	DH_Color_G37[7:0]								25h
	8826h	DH_Color_G38[7:0]								26h

	8827h	DH_Color_G39[7:0]	27h
	8828h	DH_Color_G40[7:0]	28h
	8829h	DH_Color_G41[7:0]	29h
	882Ah	DH_Color_G42[7:0]	2Ah
	882Bh	DH_Color_G43[7:0]	2Bh
	882Ch	DH_Color_G44[7:0]	2Ch
	882Dh	DH_Color_G45[7:0]	2Dh
	882Eh	DH_Color_G46[7:0]	2Eh
	882Fh	DH_Color_G47[7:0]	2Fh
	8830h	DH_Color_G48[7:0]	30h
	8831h	DH_Color_G49[7:0]	31h
	8832h	DH_Color_G50[7:0]	32h
	8833h	DH_Color_G51[7:0]	33h
	8834h	DH_Color_G52[7:0]	34h
	8835h	DH_Color_G53[7:0]	35h
	8836h	DH_Color_G54[7:0]	36h
	8837h	DH_Color_G55[7:0]	37h
	8838h	DH_Color_G56[7:0]	38h
	8839h	DH_Color_G57[7:0]	39h
	883Ah	DH_Color_G58[7:0]	3Ah
	883Bh	DH_Color_G59[7:0]	3Bh
	883Ch	DH_Color_G60[7:0]	3Ch
	883Dh	DH_Color_G61[7:0]	3Dh
	883Eh	DH_Color_G62[7:0]	3Eh
	883Fh	DH_Color_G63[7:0]	3Fh
	8840h	DH_Color_G64[7:0]	40h
	8841h	DH_Color_G65[7:0]	41h
	8842h	DH_Color_G66[7:0]	42h
	8843h	DH_Color_G67[7:0]	43h
	8844h	DH_Color_G68[7:0]	44h
	8845h	DH_Color_G69[7:0]	45h
	8846h	DH_Color_G70[7:0]	46h
	8847h	DH_Color_G71[7:0]	47h
	8848h	DH_Color_G72[7:0]	48h
	8849h	DH_Color_G73[7:0]	49h
	884Ah	DH_Color_G74[7:0]	4Ah
	884Bh	DH_Color_G75[7:0]	4Bh
	884Ch	DH_Color_G76[7:0]	4Ch
	884Dh	DH_Color_G77[7:0]	4Dh
	884Eh	DH_Color_G78[7:0]	4Eh
	884Fh	DH_Color_G79[7:0]	4Fh
	8850h	DH_Color_G80[7:0]	50h

	8851h	DH_Color_G81[7:0]	51h
	8852h	DH_Color_G82[7:0]	52h
	8853h	DH_Color_G83[7:0]	53h
	8854h	DH_Color_G84[7:0]	54h
	8855h	DH_Color_G85[7:0]	55h
	8856h	DH_Color_G86[7:0]	56h
	8857h	DH_Color_G87[7:0]	57h
	8858h	DH_Color_G88[7:0]	58h
	8859h	DH_Color_G89[7:0]	59h
	885Ah	DH_Color_G90[7:0]	5Ah
	885Bh	DH_Color_G91[7:0]	5Bh
	885Ch	DH_Color_G92[7:0]	5Ch
	885Dh	DH_Color_G93[7:0]	5Dh
	885Eh	DH_Color_G94[7:0]	5Eh
	885Fh	DH_Color_G95[7:0]	5Fh
	8860h	DH_Color_G96[7:0]	60h
	8861h	DH_Color_G97[7:0]	61h
	8862h	DH_Color_G98[7:0]	62h
	8863h	DH_Color_G99[7:0]	63h
	8864h	DH_Color_G100[7:0]	64h
	8865h	DH_Color_G101[7:0]	65h
	8866h	DH_Color_G102[7:0]	66h
	8867h	DH_Color_G103[7:0]	67h
	8868h	DH_Color_G104[7:0]	68h
	8869h	DH_Color_G105[7:0]	69h
	886Ah	DH_Color_G106[7:0]	6Ah
	886Bh	DH_Color_G107[7:0]	6Bh
	886Ch	DH_Color_G108[7:0]	6Ch
	886Dh	DH_Color_G109[7:0]	6Dh
	886Eh	DH_Color_G110[7:0]	6Eh
	886Fh	DH_Color_G111[7:0]	6Fh
	8870h	DH_Color_G112[7:0]	70h
	8871h	DH_Color_G113[7:0]	71h
	8872h	DH_Color_G114[7:0]	72h
	8873h	DH_Color_G115[7:0]	73h
	8874h	DH_Color_G116[7:0]	74h
	8875h	DH_Color_G117[7:0]	75h
	8876h	DH_Color_G118[7:0]	76h
	8877h	DH_Color_G119[7:0]	77h
	8878h	DH_Color_G120[7:0]	78h
	8879h	DH_Color_G121[7:0]	79h
	887Ah	DH_Color_G122[7:0]	7Ah

	887Bh	DH_Color_G123[7:0]	7Bh
	887Ch	DH_Color_G124[7:0]	7Ch
	887Dh	DH_Color_G125[7:0]	7Dh
	887Eh	DH_Color_G126[7:0]	7Eh
	887Fh	DH_Color_G127[7:0]	7Fh
	8880h	DH_Color_G128[7:0]	80h
	8881h	DH_Color_G129[7:0]	81h
	8882h	DH_Color_G130[7:0]	82h
	8883h	DH_Color_G131[7:0]	83h
	8884h	DH_Color_G132[7:0]	84h
	8885h	DH_Color_G133[7:0]	85h
	8886h	DH_Color_G134[7:0]	86h
	8887h	DH_Color_G135[7:0]	87h
	8888h	DH_Color_G136[7:0]	88h
	8889h	DH_Color_G137[7:0]	89h
	888Ah	DH_Color_G138[7:0]	8Ah
	888Bh	DH_Color_G139[7:0]	8Bh
	888Ch	DH_Color_G140[7:0]	8Ch
	888Dh	DH_Color_G141[7:0]	8Dh
	888Eh	DH_Color_G142[7:0]	8Eh
	888Fh	DH_Color_G143[7:0]	8Fh
	8890h	DH_Color_G144[7:0]	90h
	8891h	DH_Color_G145[7:0]	91h
	8892h	DH_Color_G146[7:0]	92h
	8893h	DH_Color_G147[7:0]	93h
	8894h	DH_Color_G148[7:0]	94h
	8895h	DH_Color_G149[7:0]	95h
	8896h	DH_Color_G150[7:0]	96h
	8897h	DH_Color_G151[7:0]	97h
	8898h	DH_Color_G152[7:0]	98h
	8899h	DH_Color_G153[7:0]	99h
	889Ah	DH_Color_G154[7:0]	9Ah
	889Bh	DH_Color_G155[7:0]	9Bh
	889Ch	DH_Color_G156[7:0]	9Ch
	889Dh	DH_Color_G157[7:0]	9Dh
	889Eh	DH_Color_G158[7:0]	9Eh
	889Fh	DH_Color_G159[7:0]	9Fh
	88A0h	DH_Color_G160[7:0]	A0h
	88A1h	DH_Color_G161[7:0]	A1h
	88A2h	DH_Color_G162[7:0]	A2h
	88A3h	DH_Color_G163[7:0]	A3h
	88A4h	DH_Color_G164[7:0]	A4h

	88A5h	DH_Color_G165[7:0]	A5h
	88A6h	DH_Color_G166[7:0]	A6h
	88A7h	DH_Color_G167[7:0]	A7h
	88A8h	DH_Color_G168[7:0]	A8h
	88A9h	DH_Color_G169[7:0]	A9h
	88AAh	DH_Color_G170[7:0]	AAh
	88ABh	DH_Color_G171[7:0]	ABh
	88ACh	DH_Color_G172[7:0]	ACh
	88ADh	DH_Color_G173[7:0]	ADh
	88AEh	DH_Color_G174[7:0]	AEh
	88AFh	DH_Color_G175[7:0]	AFh
	88B0h	DH_Color_G176[7:0]	B0h
	88B1h	DH_Color_G177[7:0]	B1h
	88B2h	DH_Color_G178[7:0]	B2h
	88B3h	DH_Color_G179[7:0]	B3h
	88B4h	DH_Color_G180[7:0]	B4h
	88B5h	DH_Color_G181[7:0]	B5h
	88B6h	DH_Color_G182[7:0]	B6h
	88B7h	DH_Color_G183[7:0]	B7h
	88B8h	DH_Color_G184[7:0]	B8h
	88B9h	DH_Color_G185[7:0]	B9h
	88BAh	DH_Color_G186[7:0]	BAh
	88BBh	DH_Color_G187[7:0]	BBh
	88BCh	DH_Color_G188[7:0]	BCh
	88BDh	DH_Color_G189[7:0]	BDh
	88BEh	DH_Color_G190[7:0]	BEh
	88BFh	DH_Color_G191[7:0]	BFh
	88C0h	DH_Color_G192[7:0]	C0h
	88C1h	DH_Color_G193[7:0]	C1h
	88C2h	DH_Color_G194[7:0]	C2h
	88C3h	DH_Color_G195[7:0]	C3h
	88C4h	DH_Color_G196[7:0]	C4h
	88C5h	DH_Color_G197[7:0]	C5h
	88C6h	DH_Color_G198[7:0]	C6h
	88C7h	DH_Color_G199[7:0]	C7h
	88C8h	DH_Color_G200[7:0]	C8h
	88C9h	DH_Color_G201[7:0]	C9h
	88CAh	DH_Color_G202[7:0]	CAh
	88CBh	DH_Color_G203[7:0]	CBh
	88CCh	DH_Color_G204[7:0]	CCh
	88CDh	DH_Color_G205[7:0]	CDh
	88CEh	DH_Color_G206[7:0]	CEh

	88CFh	DH_Color_G207[7:0]	CFh
	88D0h	DH_Color_G208[7:0]	D0h
	88D1h	DH_Color_G209[7:0]	D1h
	88D2h	DH_Color_G210[7:0]	D2h
	88D3h	DH_Color_G211[7:0]	D3h
	88D4h	DH_Color_G212[7:0]	D4h
	88D5h	DH_Color_G213[7:0]	D5h
	88D6h	DH_Color_G214[7:0]	D6h
	88D7h	DH_Color_G215[7:0]	D7h
	88D8h	DH_Color_G216[7:0]	D8h
	88D9h	DH_Color_G217[7:0]	D9h
	88DAh	DH_Color_G218[7:0]	DAh
	88DBh	DH_Color_G219[7:0]	DBh
	88DCh	DH_Color_G220[7:0]	DCh
	88DDh	DH_Color_G221[7:0]	DDh
	88DEh	DH_Color_G222[7:0]	DEh
	88DFh	DH_Color_G223[7:0]	DFh
	88E0h	DH_Color_G224[7:0]	E0h
	88E1h	DH_Color_G225[7:0]	E1h
	88E2h	DH_Color_G226[7:0]	E2h
	88E3h	DH_Color_G227[7:0]	E3h
	88E4h	DH_Color_G228[7:0]	E4h
	88E5h	DH_Color_G229[7:0]	E5h
	88E6h	DH_Color_G230[7:0]	E6h
	88E7h	DH_Color_G231[7:0]	E7h
	88E8h	DH_Color_G232[7:0]	E8h
	88E9h	DH_Color_G233[7:0]	E9h
	88EAh	DH_Color_G234[7:0]	EAh
	88EBh	DH_Color_G235[7:0]	EBh
	88ECh	DH_Color_G236[7:0]	ECh
	88EDh	DH_Color_G237[7:0]	EDh
	88EEh	DH_Color_G238[7:0]	EEh
	88EFh	DH_Color_G239[7:0]	EFh
	88F0h	DH_Color_G240[7:0]	F0h
	88F1h	DH_Color_G241[7:0]	F1h
	88F2h	DH_Color_G242[7:0]	F2h
	88F3h	DH_Color_G243[7:0]	F3h
	88F4h	DH_Color_G244[7:0]	F4h
	88F5h	DH_Color_G245[7:0]	F5h
	88F6h	DH_Color_G246[7:0]	F6h
	88F7h	DH_Color_G247[7:0]	F7h
	88F8h	DH_Color_G248[7:0]	F8h

	88F9h	DH_Color_G249[7:0]	F9h
	88FAh	DH_Color_G250[7:0]	FAh
	88FBh	DH_Color_G251[7:0]	FBh
	88FCh	DH_Color_G252[7:0]	FCh
	88FDh	DH_Color_G253[7:0]	FDh
	88FEh	DH_Color_G254[7:0]	FEh
	88FFh	DH_Color_G255[7:0]	FFh
Description		This command is used to set digital clock hour color.	
Restriction		-	

DHCOLORB: Digital clock Hour color setting (8900h~89FFh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
89h	8900h	DH_Color_B0[7:0]								00h
	8901h	DH_Color_B1[7:0]								01h
	8902h	DH_Color_B2[7:0]								02h
	8903h	DH_Color_B3[7:0]								03h
	8904h	DH_Color_B4[7:0]								04h
	8905h	DH_Color_B5[7:0]								05h
	8906h	DH_Color_B6[7:0]								06h
	8907h	DH_Color_B7[7:0]								07h
	8908h	DH_Color_B8[7:0]								08h
	8909h	DH_Color_B9[7:0]								09h
	890Ah	DH_Color_B10[7:0]								0Ah
	890Bh	DH_Color_B11[7:0]								0Bh
	890Ch	DH_Color_B12[7:0]								0Ch
	890Dh	DH_Color_B13[7:0]								0Dh
	890Eh	DH_Color_B14[7:0]								0Eh
	890Fh	DH_Color_B15[7:0]								0Fh
	8910h	DH_Color_B16[7:0]								10h
	8911h	DH_Color_B17[7:0]								11h
	8912h	DH_Color_B18[7:0]								12h
	8913h	DH_Color_B19[7:0]								13h
	8914h	DH_Color_B20[7:0]								14h
	8915h	DH_Color_B21[7:0]								15h
	8916h	DH_Color_B22[7:0]								16h
	8917h	DH_Color_B23[7:0]								17h
	8918h	DH_Color_B24[7:0]								18h
	8919h	DH_Color_B25[7:0]								19h
	891Ah	DH_Color_B26[7:0]								1Ah
	891Bh	DH_Color_B27[7:0]								1Bh
	891Ch	DH_Color_B28[7:0]								1Ch
	891Dh	DH_Color_B29[7:0]								1Dh
	891Eh	DH_Color_B30[7:0]								1Eh
	891Fh	DH_Color_B31[7:0]								1Fh
	8920h	DH_Color_B32[7:0]								20h
	8921h	DH_Color_B33[7:0]								21h
	8922h	DH_Color_B34[7:0]								22h
	8923h	DH_Color_B35[7:0]								23h
	8924h	DH_Color_B36[7:0]								24h
	8925h	DH_Color_B37[7:0]								25h
	8926h	DH_Color_B38[7:0]								26h

	8927h	DH_Color_B39[7:0]	27h
	8928h	DH_Color_B40[7:0]	28h
	8929h	DH_Color_B41[7:0]	29h
	892Ah	DH_Color_B42[7:0]	2Ah
	892Bh	DH_Color_B43[7:0]	2Bh
	892Ch	DH_Color_B44[7:0]	2Ch
	892Dh	DH_Color_B45[7:0]	2Dh
	892Eh	DH_Color_B46[7:0]	2Eh
	892Fh	DH_Color_B47[7:0]	2Fh
	8930h	DH_Color_B48[7:0]	30h
	8931h	DH_Color_B49[7:0]	31h
	8932h	DH_Color_B50[7:0]	32h
	8933h	DH_Color_B51[7:0]	33h
	8934h	DH_Color_B52[7:0]	34h
	8935h	DH_Color_B53[7:0]	35h
	8936h	DH_Color_B54[7:0]	36h
	8937h	DH_Color_B55[7:0]	37h
	8938h	DH_Color_B56[7:0]	38h
	8939h	DH_Color_B57[7:0]	39h
	893Ah	DH_Color_B58[7:0]	3Ah
	893Bh	DH_Color_B59[7:0]	3Bh
	893Ch	DH_Color_B60[7:0]	3Ch
	893Dh	DH_Color_B61[7:0]	3Dh
	893Eh	DH_Color_B62[7:0]	3Eh
	893Fh	DH_Color_B63[7:0]	3Fh
	8940h	DH_Color_B64[7:0]	40h
	8941h	DH_Color_B65[7:0]	41h
	8942h	DH_Color_B66[7:0]	42h
	8943h	DH_Color_B67[7:0]	43h
	8944h	DH_Color_B68[7:0]	44h
	8945h	DH_Color_B69[7:0]	45h
	8946h	DH_Color_B70[7:0]	46h
	8947h	DH_Color_B71[7:0]	47h
	8948h	DH_Color_B72[7:0]	48h
	8949h	DH_Color_B73[7:0]	49h
	894Ah	DH_Color_B74[7:0]	4Ah
	894Bh	DH_Color_B75[7:0]	4Bh
	894Ch	DH_Color_B76[7:0]	4Ch
	894Dh	DH_Color_B77[7:0]	4Dh
	894Eh	DH_Color_B78[7:0]	4Eh
	894Fh	DH_Color_B79[7:0]	4Fh
	8950h	DH_Color_B80[7:0]	50h

	8951h	DH_Color_B81[7:0]	51h
	8952h	DH_Color_B82[7:0]	52h
	8953h	DH_Color_B83[7:0]	53h
	8954h	DH_Color_B84[7:0]	54h
	8955h	DH_Color_B85[7:0]	55h
	8956h	DH_Color_B86[7:0]	56h
	8957h	DH_Color_B87[7:0]	57h
	8958h	DH_Color_B88[7:0]	58h
	8959h	DH_Color_B89[7:0]	59h
	895Ah	DH_Color_B90[7:0]	5Ah
	895Bh	DH_Color_B91[7:0]	5Bh
	895Ch	DH_Color_B92[7:0]	5Ch
	895Dh	DH_Color_B93[7:0]	5Dh
	895Eh	DH_Color_B94[7:0]	5Eh
	895Fh	DH_Color_B95[7:0]	5Fh
	8960h	DH_Color_B96[7:0]	60h
	8961h	DH_Color_B97[7:0]	61h
	8962h	DH_Color_B98[7:0]	62h
	8963h	DH_Color_B99[7:0]	63h
	8964h	DH_Color_B100[7:0]	64h
	8965h	DH_Color_B101[7:0]	65h
	8966h	DH_Color_B102[7:0]	66h
	8967h	DH_Color_B103[7:0]	67h
	8968h	DH_Color_B104[7:0]	68h
	8969h	DH_Color_B105[7:0]	69h
	896Ah	DH_Color_B106[7:0]	6Ah
	896Bh	DH_Color_B107[7:0]	6Bh
	896Ch	DH_Color_B108[7:0]	6Ch
	896Dh	DH_Color_B109[7:0]	6Dh
	896Eh	DH_Color_B110[7:0]	6Eh
	896Fh	DH_Color_B111[7:0]	6Fh
	8970h	DH_Color_B112[7:0]	70h
	8971h	DH_Color_B113[7:0]	71h
	8972h	DH_Color_B114[7:0]	72h
	8973h	DH_Color_B115[7:0]	73h
	8974h	DH_Color_B116[7:0]	74h
	8975h	DH_Color_B117[7:0]	75h
	8976h	DH_Color_B118[7:0]	76h
	8977h	DH_Color_B119[7:0]	77h
	8978h	DH_Color_B120[7:0]	78h
	8979h	DH_Color_B121[7:0]	79h
	897Ah	DH_Color_B122[7:0]	7Ah

	897Bh	DH_Color_B123[7:0]	7Bh
	897Ch	DH_Color_B124[7:0]	7Ch
	897Dh	DH_Color_B125[7:0]	7Dh
	897Eh	DH_Color_B126[7:0]	7Eh
	897Fh	DH_Color_B127[7:0]	7Fh
	8980h	DH_Color_B128[7:0]	80h
	8981h	DH_Color_B129[7:0]	81h
	8982h	DH_Color_B130[7:0]	82h
	8983h	DH_Color_B131[7:0]	83h
	8984h	DH_Color_B132[7:0]	84h
	8985h	DH_Color_B133[7:0]	85h
	8986h	DH_Color_B134[7:0]	86h
	8987h	DH_Color_B135[7:0]	87h
	8988h	DH_Color_B136[7:0]	88h
	8989h	DH_Color_B137[7:0]	89h
	898Ah	DH_Color_B138[7:0]	8Ah
	898Bh	DH_Color_B139[7:0]	8Bh
	898Ch	DH_Color_B140[7:0]	8Ch
	898Dh	DH_Color_B141[7:0]	8Dh
	898Eh	DH_Color_B142[7:0]	8Eh
	898Fh	DH_Color_B143[7:0]	8Fh
	8990h	DH_Color_B144[7:0]	90h
	8991h	DH_Color_B145[7:0]	91h
	8992h	DH_Color_B146[7:0]	92h
	8993h	DH_Color_B147[7:0]	93h
	8994h	DH_Color_B148[7:0]	94h
	8995h	DH_Color_B149[7:0]	95h
	8996h	DH_Color_B150[7:0]	96h
	8997h	DH_Color_B151[7:0]	97h
	8998h	DH_Color_B152[7:0]	98h
	8999h	DH_Color_B153[7:0]	99h
	899Ah	DH_Color_B154[7:0]	9Ah
	899Bh	DH_Color_B155[7:0]	9Bh
	899Ch	DH_Color_B156[7:0]	9Ch
	899Dh	DH_Color_B157[7:0]	9Dh
	899Eh	DH_Color_B158[7:0]	9Eh
	899Fh	DH_Color_B159[7:0]	9Fh
	89A0h	DH_Color_B160[7:0]	A0h
	89A1h	DH_Color_B161[7:0]	A1h
	89A2h	DH_Color_B162[7:0]	A2h
	89A3h	DH_Color_B163[7:0]	A3h
	89A4h	DH_Color_B164[7:0]	A4h

	89A5h	DH_Color_B165[7:0]	A5h
	89A6h	DH_Color_B166[7:0]	A6h
	89A7h	DH_Color_B167[7:0]	A7h
	89A8h	DH_Color_B168[7:0]	A8h
	89A9h	DH_Color_B169[7:0]	A9h
	89AAh	DH_Color_B170[7:0]	AAh
	89ABh	DH_Color_B171[7:0]	ABh
	89ACh	DH_Color_B172[7:0]	ACh
	89ADh	DH_Color_B173[7:0]	ADh
	89AEh	DH_Color_B174[7:0]	AEh
	89AFh	DH_Color_B175[7:0]	AFh
	89B0h	DH_Color_B176[7:0]	B0h
	89B1h	DH_Color_B177[7:0]	B1h
	89B2h	DH_Color_B178[7:0]	B2h
	89B3h	DH_Color_B179[7:0]	B3h
	89B4h	DH_Color_B180[7:0]	B4h
	89B5h	DH_Color_B181[7:0]	B5h
	89B6h	DH_Color_B182[7:0]	B6h
	89B7h	DH_Color_B183[7:0]	B7h
	89B8h	DH_Color_B184[7:0]	B8h
	89B9h	DH_Color_B185[7:0]	B9h
	89BAh	DH_Color_B186[7:0]	BAh
	89BBh	DH_Color_B187[7:0]	BBh
	89BCh	DH_Color_B188[7:0]	BCh
	89BDh	DH_Color_B189[7:0]	BDh
	89BEh	DH_Color_B190[7:0]	BEh
	89BFh	DH_Color_B191[7:0]	BFh
	89C0h	DH_Color_B192[7:0]	C0h
	89C1h	DH_Color_B193[7:0]	C1h
	89C2h	DH_Color_B194[7:0]	C2h
	89C3h	DH_Color_B195[7:0]	C3h
	89C4h	DH_Color_B196[7:0]	C4h
	89C5h	DH_Color_B197[7:0]	C5h
	89C6h	DH_Color_B198[7:0]	C6h
	89C7h	DH_Color_B199[7:0]	C7h
	89C8h	DH_Color_B200[7:0]	C8h
	89C9h	DH_Color_B201[7:0]	C9h
	89CAh	DH_Color_B202[7:0]	CAh
	89CBh	DH_Color_B203[7:0]	CBh
	89CCh	DH_Color_B204[7:0]	CCh
	89CDh	DH_Color_B205[7:0]	CDh
	89CEh	DH_Color_B206[7:0]	CEh

	89CFh	DH_Color_B207[7:0]	CFh
	89D0h	DH_Color_B208[7:0]	D0h
	89D1h	DH_Color_B209[7:0]	D1h
	89D2h	DH_Color_B210[7:0]	D2h
	89D3h	DH_Color_B211[7:0]	D3h
	89D4h	DH_Color_B212[7:0]	D4h
	89D5h	DH_Color_B213[7:0]	D5h
	89D6h	DH_Color_B214[7:0]	D6h
	89D7h	DH_Color_B215[7:0]	D7h
	89D8h	DH_Color_B216[7:0]	D8h
	89D9h	DH_Color_B217[7:0]	D9h
	89DAh	DH_Color_B218[7:0]	DAh
	89DBh	DH_Color_B219[7:0]	DBh
	89DCh	DH_Color_B220[7:0]	DCh
	89DDh	DH_Color_B221[7:0]	DDh
	89DEh	DH_Color_B222[7:0]	DEh
	89DFh	DH_Color_B223[7:0]	DFh
	89E0h	DH_Color_B224[7:0]	E0h
	89E1h	DH_Color_B225[7:0]	E1h
	89E2h	DH_Color_B226[7:0]	E2h
	89E3h	DH_Color_B227[7:0]	E3h
	89E4h	DH_Color_B228[7:0]	E4h
	89E5h	DH_Color_B229[7:0]	E5h
	89E6h	DH_Color_B230[7:0]	E6h
	89E7h	DH_Color_B231[7:0]	E7h
	89E8h	DH_Color_B232[7:0]	E8h
	89E9h	DH_Color_B233[7:0]	E9h
	89EAh	DH_Color_B234[7:0]	EAh
	89EBh	DH_Color_B235[7:0]	EBh
	89ECh	DH_Color_B236[7:0]	ECh
	89EDh	DH_Color_B237[7:0]	EDh
	89EEh	DH_Color_B238[7:0]	EEh
	89EFh	DH_Color_B239[7:0]	EFh
	89F0h	DH_Color_B240[7:0]	F0h
	89F1h	DH_Color_B241[7:0]	F1h
	89F2h	DH_Color_B242[7:0]	F2h
	89F3h	DH_Color_B243[7:0]	F3h
	89F4h	DH_Color_B244[7:0]	F4h
	89F5h	DH_Color_B245[7:0]	F5h
	89F6h	DH_Color_B246[7:0]	F6h
	89F7h	DH_Color_B247[7:0]	F7h
	89F8h	DH_Color_B248[7:0]	F8h

	89F9h	DH_Color_B249[7:0]	F9h
	89FAh	DH_Color_B250[7:0]	FAh
	89FBh	DH_Color_B251[7:0]	FBh
	89FCh	DH_Color_B252[7:0]	FCh
	89FDh	DH_Color_B253[7:0]	FDh
	89FEh	DH_Color_B254[7:0]	FEh
	89FFh	DH_Color_B255[7:0]	FFh
Description		This command is used to set digital clock hour color.	
Restriction		-	

DHCOLORA: Digital clock Hour color setting (8A00h~8AFFh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
8Ah	8A00h	DH_Color_A0[7:0]								00h
	8A01h	DH_Color_A1[7:0]								01h
	8A02h	DH_Color_A2[7:0]								02h
	8A03h	DH_Color_A3[7:0]								03h
	8A04h	DH_Color_A4[7:0]								04h
	8A05h	DH_Color_A5[7:0]								05h
	8A06h	DH_Color_A6[7:0]								06h
	8A07h	DH_Color_A7[7:0]								07h
	8A08h	DH_Color_A8[7:0]								08h
	8A09h	DH_Color_A9[7:0]								09h
	8A0Ah	DH_Color_A10[7:0]								0Ah
	8A0Bh	DH_Color_A11[7:0]								0Bh
	8A0Ch	DH_Color_A12[7:0]								0Ch
	8A0Dh	DH_Color_A13[7:0]								0Dh
	8A0Eh	DH_Color_A14[7:0]								0Eh
	8A0Fh	DH_Color_A15[7:0]								0Fh
	8A10h	DH_Color_A16[7:0]								10h
	8A11h	DH_Color_A17[7:0]								11h
	8A12h	DH_Color_A18[7:0]								12h
	8A13h	DH_Color_A19[7:0]								13h
	8A14h	DH_Color_A20[7:0]								14h
	8A15h	DH_Color_A21[7:0]								15h
	8A16h	DH_Color_A22[7:0]								16h
	8A17h	DH_Color_A23[7:0]								17h
	8A18h	DH_Color_A24[7:0]								18h
	8A19h	DH_Color_A25[7:0]								19h
	8A1Ah	DH_Color_A26[7:0]								1Ah
	8A1Bh	DH_Color_A27[7:0]								1Bh
	8A1Ch	DH_Color_A28[7:0]								1Ch
	8A1Dh	DH_Color_A29[7:0]								1Dh
	8A1Eh	DH_Color_A30[7:0]								1Eh
	8A1Fh	DH_Color_A31[7:0]								1Fh
	8A20h	DH_Color_A32[7:0]								20h
	8A21h	DH_Color_A33[7:0]								21h
	8A22h	DH_Color_A34[7:0]								22h
	8A23h	DH_Color_A35[7:0]								23h
	8A24h	DH_Color_A36[7:0]								24h
	8A25h	DH_Color_A37[7:0]								25h
	8A26h	DH_Color_A38[7:0]								26h

	8A27h	DH_Color_A39[7:0]	27h
	8A28h	DH_Color_A40[7:0]	28h
	8A29h	DH_Color_A41[7:0]	29h
	8A2Ah	DH_Color_A42[7:0]	2Ah
	8A2Bh	DH_Color_A43[7:0]	2Bh
	8A2Ch	DH_Color_A44[7:0]	2Ch
	8A2Dh	DH_Color_A45[7:0]	2Dh
	8A2Eh	DH_Color_A46[7:0]	2Eh
	8A2Fh	DH_Color_A47[7:0]	2Fh
	8A30h	DH_Color_A48[7:0]	30h
	8A31h	DH_Color_A49[7:0]	31h
	8A32h	DH_Color_A50[7:0]	32h
	8A33h	DH_Color_A51[7:0]	33h
	8A34h	DH_Color_A52[7:0]	34h
	8A35h	DH_Color_A53[7:0]	35h
	8A36h	DH_Color_A54[7:0]	36h
	8A37h	DH_Color_A55[7:0]	37h
	8A38h	DH_Color_A56[7:0]	38h
	8A39h	DH_Color_A57[7:0]	39h
	8A3Ah	DH_Color_A58[7:0]	3Ah
	8A3Bh	DH_Color_A59[7:0]	3Bh
	8A3Ch	DH_Color_A60[7:0]	3Ch
	8A3Dh	DH_Color_A61[7:0]	3Dh
	8A3Eh	DH_Color_A62[7:0]	3Eh
	8A3Fh	DH_Color_A63[7:0]	3Fh
	8A40h	DH_Color_A64[7:0]	40h
	8A41h	DH_Color_A65[7:0]	41h
	8A42h	DH_Color_A66[7:0]	42h
	8A43h	DH_Color_A67[7:0]	43h
	8A44h	DH_Color_A68[7:0]	44h
	8A45h	DH_Color_A69[7:0]	45h
	8A46h	DH_Color_A70[7:0]	46h
	8A47h	DH_Color_A71[7:0]	47h
	8A48h	DH_Color_A72[7:0]	48h
	8A49h	DH_Color_A73[7:0]	49h
	8A4Ah	DH_Color_A74[7:0]	4Ah
	8A4Bh	DH_Color_A75[7:0]	4Bh
	8A4Ch	DH_Color_A76[7:0]	4Ch
	8A4Dh	DH_Color_A77[7:0]	4Dh
	8A4Eh	DH_Color_A78[7:0]	4Eh
	8A4Fh	DH_Color_A79[7:0]	4Fh
	8A50h	DH_Color_A80[7:0]	50h

	8A51h	DH_Color_A81[7:0]	51h
	8A52h	DH_Color_A82[7:0]	52h
	8A53h	DH_Color_A83[7:0]	53h
	8A54h	DH_Color_A84[7:0]	54h
	8A55h	DH_Color_A85[7:0]	55h
	8A56h	DH_Color_A86[7:0]	56h
	8A57h	DH_Color_A87[7:0]	57h
	8A58h	DH_Color_A88[7:0]	58h
	8A59h	DH_Color_A89[7:0]	59h
	8A5Ah	DH_Color_A90[7:0]	5Ah
	8A5Bh	DH_Color_A91[7:0]	5Bh
	8A5Ch	DH_Color_A92[7:0]	5Ch
	8A5Dh	DH_Color_A93[7:0]	5Dh
	8A5Eh	DH_Color_A94[7:0]	5Eh
	8A5Fh	DH_Color_A95[7:0]	5Fh
	8A60h	DH_Color_A96[7:0]	60h
	8A61h	DH_Color_A97[7:0]	61h
	8A62h	DH_Color_A98[7:0]	62h
	8A63h	DH_Color_A99[7:0]	63h
	8A64h	DH_Color_A100[7:0]	64h
	8A65h	DH_Color_A101[7:0]	65h
	8A66h	DH_Color_A102[7:0]	66h
	8A67h	DH_Color_A103[7:0]	67h
	8A68h	DH_Color_A104[7:0]	68h
	8A69h	DH_Color_A105[7:0]	69h
	8A6Ah	DH_Color_A106[7:0]	6Ah
	8A6Bh	DH_Color_A107[7:0]	6Bh
	8A6Ch	DH_Color_A108[7:0]	6Ch
	8A6Dh	DH_Color_A109[7:0]	6Dh
	8A6Eh	DH_Color_A110[7:0]	6Eh
	8A6Fh	DH_Color_A111[7:0]	6Fh
	8A70h	DH_Color_A112[7:0]	70h
	8A71h	DH_Color_A113[7:0]	71h
	8A72h	DH_Color_A114[7:0]	72h
	8A73h	DH_Color_A115[7:0]	73h
	8A74h	DH_Color_A116[7:0]	74h
	8A75h	DH_Color_A117[7:0]	75h
	8A76h	DH_Color_A118[7:0]	76h
	8A77h	DH_Color_A119[7:0]	77h
	8A78h	DH_Color_A120[7:0]	78h
	8A79h	DH_Color_A121[7:0]	79h
	8A7Ah	DH_Color_A122[7:0]	7Ah

	8A7Bh	DH_Color_A123[7:0]	7Bh
	8A7Ch	DH_Color_A124[7:0]	7Ch
	8A7Dh	DH_Color_A125[7:0]	7Dh
	8A7Eh	DH_Color_A126[7:0]	7Eh
	8A7Fh	DH_Color_A127[7:0]	7Fh
	8A80h	DH_Color_A128[7:0]	80h
	8A81h	DH_Color_A129[7:0]	81h
	8A82h	DH_Color_A130[7:0]	82h
	8A83h	DH_Color_A131[7:0]	83h
	8A84h	DH_Color_A132[7:0]	84h
	8A85h	DH_Color_A133[7:0]	85h
	8A86h	DH_Color_A134[7:0]	86h
	8A87h	DH_Color_A135[7:0]	87h
	8A88h	DH_Color_A136[7:0]	88h
	8A89h	DH_Color_A137[7:0]	89h
	8A8Ah	DH_Color_A138[7:0]	8Ah
	8A8Bh	DH_Color_A139[7:0]	8Bh
	8A8Ch	DH_Color_A140[7:0]	8Ch
	8A8Dh	DH_Color_A141[7:0]	8Dh
	8A8Eh	DH_Color_A142[7:0]	8Eh
	8A8Fh	DH_Color_A143[7:0]	8Fh
	8A90h	DH_Color_A144[7:0]	90h
	8A91h	DH_Color_A145[7:0]	91h
	8A92h	DH_Color_A146[7:0]	92h
	8A93h	DH_Color_A147[7:0]	93h
	8A94h	DH_Color_A148[7:0]	94h
	8A95h	DH_Color_A149[7:0]	95h
	8A96h	DH_Color_A150[7:0]	96h
	8A97h	DH_Color_A151[7:0]	97h
	8A98h	DH_Color_A152[7:0]	98h
	8A99h	DH_Color_A153[7:0]	99h
	8A9Ah	DH_Color_A154[7:0]	9Ah
	8A9Bh	DH_Color_A155[7:0]	9Bh
	8A9Ch	DH_Color_A156[7:0]	9Ch
	8A9Dh	DH_Color_A157[7:0]	9Dh
	8A9Eh	DH_Color_A158[7:0]	9Eh
	8A9Fh	DH_Color_A159[7:0]	9Fh
	8AA0h	DH_Color_A160[7:0]	A0h
	8AA1h	DH_Color_A161[7:0]	A1h
	8AA2h	DH_Color_A162[7:0]	A2h
	8AA3h	DH_Color_A163[7:0]	A3h
	8AA4h	DH_Color_A164[7:0]	A4h

	8AA5h	DH_Color_A165[7:0]	A5h
	8AA6h	DH_Color_A166[7:0]	A6h
	8AA7h	DH_Color_A167[7:0]	A7h
	8AA8h	DH_Color_A168[7:0]	A8h
	8AA9h	DH_Color_A169[7:0]	A9h
	8AAAh	DH_Color_A170[7:0]	AAh
	8AABh	DH_Color_A171[7:0]	ABh
	8AACh	DH_Color_A172[7:0]	ACh
	8AADh	DH_Color_A173[7:0]	ADh
	8AAEh	DH_Color_A174[7:0]	AEh
	8AAFh	DH_Color_A175[7:0]	AFh
	8AB0h	DH_Color_A176[7:0]	B0h
	8AB1h	DH_Color_A177[7:0]	B1h
	8AB2h	DH_Color_A178[7:0]	B2h
	8AB3h	DH_Color_A179[7:0]	B3h
	8AB4h	DH_Color_A180[7:0]	B4h
	8AB5h	DH_Color_A181[7:0]	B5h
	8AB6h	DH_Color_A182[7:0]	B6h
	8AB7h	DH_Color_A183[7:0]	B7h
	8AB8h	DH_Color_A184[7:0]	B8h
	8AB9h	DH_Color_A185[7:0]	B9h
	8ABAh	DH_Color_A186[7:0]	BAh
	8ABBh	DH_Color_A187[7:0]	BBh
	8ABCh	DH_Color_A188[7:0]	BCh
	8ABDh	DH_Color_A189[7:0]	BDh
	8ABEh	DH_Color_A190[7:0]	BEh
	8ABFh	DH_Color_A191[7:0]	BFh
	8AC0h	DH_Color_A192[7:0]	C0h
	8AC1h	DH_Color_A193[7:0]	C1h
	8AC2h	DH_Color_A194[7:0]	C2h
	8AC3h	DH_Color_A195[7:0]	C3h
	8AC4h	DH_Color_A196[7:0]	C4h
	8AC5h	DH_Color_A197[7:0]	C5h
	8AC6h	DH_Color_A198[7:0]	C6h
	8AC7h	DH_Color_A199[7:0]	C7h
	8AC8h	DH_Color_A200[7:0]	C8h
	8AC9h	DH_Color_A201[7:0]	C9h
	8ACAh	DH_Color_A202[7:0]	CAh
	8ACBh	DH_Color_A203[7:0]	CBh
	8ACCh	DH_Color_A204[7:0]	CCh
	8ACDh	DH_Color_A205[7:0]	CDh
	8ACEh	DH_Color_A206[7:0]	CEh

	8ACFh	DH_Color_A207[7:0]	CFh
	8AD0h	DH_Color_A208[7:0]	D0h
	8AD1h	DH_Color_A209[7:0]	D1h
	8AD2h	DH_Color_A210[7:0]	D2h
	8AD3h	DH_Color_A211[7:0]	D3h
	8AD4h	DH_Color_A212[7:0]	D4h
	8AD5h	DH_Color_A213[7:0]	D5h
	8AD6h	DH_Color_A214[7:0]	D6h
	8AD7h	DH_Color_A215[7:0]	D7h
	8AD8h	DH_Color_A216[7:0]	D8h
	8AD9h	DH_Color_A217[7:0]	D9h
	8ADAh	DH_Color_A218[7:0]	DAh
	8ADBh	DH_Color_A219[7:0]	DBh
	8ADCh	DH_Color_A220[7:0]	DCh
	8ADDh	DH_Color_A221[7:0]	DDh
	8ADEh	DH_Color_A222[7:0]	DEh
	8ADFh	DH_Color_A223[7:0]	DFh
	8AE0h	DH_Color_A224[7:0]	E0h
	8AE1h	DH_Color_A225[7:0]	E1h
	8AE2h	DH_Color_A226[7:0]	E2h
	8AE3h	DH_Color_A227[7:0]	E3h
	8AE4h	DH_Color_A228[7:0]	E4h
	8AE5h	DH_Color_A229[7:0]	E5h
	8AE6h	DH_Color_A230[7:0]	E6h
	8AE7h	DH_Color_A231[7:0]	E7h
	8AE8h	DH_Color_A232[7:0]	E8h
	8AE9h	DH_Color_A233[7:0]	E9h
	8AEAh	DH_Color_A234[7:0]	EAh
	8AEBh	DH_Color_A235[7:0]	EBh
	8AECh	DH_Color_A236[7:0]	ECh
	8AEDh	DH_Color_A237[7:0]	EDh
	8AEEh	DH_Color_A238[7:0]	EEh
	8AEFh	DH_Color_A239[7:0]	EFh
	8AF0h	DH_Color_A240[7:0]	F0h
	8AF1h	DH_Color_A241[7:0]	F1h
	8AF2h	DH_Color_A242[7:0]	F2h
	8AF3h	DH_Color_A243[7:0]	F3h
	8AF4h	DH_Color_A244[7:0]	F4h
	8AF5h	DH_Color_A245[7:0]	F5h
	8AF6h	DH_Color_A246[7:0]	F6h
	8AF7h	DH_Color_A247[7:0]	F7h
	8AF8h	DH_Color_A248[7:0]	F8h

	8AF9h	DH_Color_A249[7:0]	F9h
	8AFAh	DH_Color_A250[7:0]	FAh
	8AFBh	DH_Color_A251[7:0]	FBh
	8AFCh	DH_Color_A252[7:0]	FCh
	8AFDh	DH_Color_A253[7:0]	FDh
	8AFEh	DH_Color_A254[7:0]	FEh
	8AFFh	DH_Color_A255[7:0]	FFh
Description		This command is used to set digital clock hour color.	
Restriction		-	

DMCOLORR: Digital clock minute color setting (8B00h~8BFFh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
8Bh	8B00h	DM_Color_R0[7:0]								00h
	8B01h	DM_Color_R1[7:0]								01h
	8B02h	DM_Color_R2[7:0]								02h
	8B03h	DM_Color_R3[7:0]								03h
	8B04h	DM_Color_R4[7:0]								04h
	8B05h	DM_Color_R5[7:0]								05h
	8B06h	DM_Color_R6[7:0]								06h
	8B07h	DM_Color_R7[7:0]								07h
	8B08h	DM_Color_R8[7:0]								08h
	8B09h	DM_Color_R9[7:0]								09h
	8B0Ah	DM_Color_R10[7:0]								0Ah
	8B0Bh	DM_Color_R11[7:0]								0Bh
	8B0Ch	DM_Color_R12[7:0]								0Ch
	8B0Dh	DM_Color_R13[7:0]								0Dh
	8B0Eh	DM_Color_R14[7:0]								0Eh
	8B0Fh	DM_Color_R15[7:0]								0Fh
	8B10h	DM_Color_R16[7:0]								10h
	8B11h	DM_Color_R17[7:0]								11h
	8B12h	DM_Color_R18[7:0]								12h
	8B13h	DM_Color_R19[7:0]								13h
	8B14h	DM_Color_R20[7:0]								14h
	8B15h	DM_Color_R21[7:0]								15h
	8B16h	DM_Color_R22[7:0]								16h
	8B17h	DM_Color_R23[7:0]								17h
	8B18h	DM_Color_R24[7:0]								18h
	8B19h	DM_Color_R25[7:0]								19h
	8B1Ah	DM_Color_R26[7:0]								1Ah
	8B1Bh	DM_Color_R27[7:0]								1Bh
	8B1Ch	DM_Color_R28[7:0]								1Ch
	8B1Dh	DM_Color_R29[7:0]								1Dh
	8B1Eh	DM_Color_R30[7:0]								1Eh
	8B1Fh	DM_Color_R31[7:0]								1Fh
	8B20h	DM_Color_R32[7:0]								20h
	8B21h	DM_Color_R33[7:0]								21h
	8B22h	DM_Color_R34[7:0]								22h
	8B23h	DM_Color_R35[7:0]								23h
	8B24h	DM_Color_R36[7:0]								24h
	8B25h	DM_Color_R37[7:0]								25h
	8B26h	DM_Color_R38[7:0]								26h

	8B27h	DM_Color_R39[7:0]	27h
	8B28h	DM_Color_R40[7:0]	28h
	8B29h	DM_Color_R41[7:0]	29h
	8B2Ah	DM_Color_R42[7:0]	2Ah
	8B2Bh	DM_Color_R43[7:0]	2Bh
	8B2Ch	DM_Color_R44[7:0]	2Ch
	8B2Dh	DM_Color_R45[7:0]	2Dh
	8B2Eh	DM_Color_R46[7:0]	2Eh
	8B2Fh	DM_Color_R47[7:0]	2Fh
	8B30h	DM_Color_R48[7:0]	30h
	8B31h	DM_Color_R49[7:0]	31h
	8B32h	DM_Color_R50[7:0]	32h
	8B33h	DM_Color_R51[7:0]	33h
	8B34h	DM_Color_R52[7:0]	34h
	8B35h	DM_Color_R53[7:0]	35h
	8B36h	DM_Color_R54[7:0]	36h
	8B37h	DM_Color_R55[7:0]	37h
	8B38h	DM_Color_R56[7:0]	38h
	8B39h	DM_Color_R57[7:0]	39h
	8B3Ah	DM_Color_R58[7:0]	3Ah
	8B3Bh	DM_Color_R59[7:0]	3Bh
	8B3Ch	DM_Color_R60[7:0]	3Ch
	8B3Dh	DM_Color_R61[7:0]	3Dh
	8B3Eh	DM_Color_R62[7:0]	3Eh
	8B3Fh	DM_Color_R63[7:0]	3Fh
	8B40h	DM_Color_R64[7:0]	40h
	8B41h	DM_Color_R65[7:0]	41h
	8B42h	DM_Color_R66[7:0]	42h
	8B43h	DM_Color_R67[7:0]	43h
	8B44h	DM_Color_R68[7:0]	44h
	8B45h	DM_Color_R69[7:0]	45h
	8B46h	DM_Color_R70[7:0]	46h
	8B47h	DM_Color_R71[7:0]	47h
	8B48h	DM_Color_R72[7:0]	48h
	8B49h	DM_Color_R73[7:0]	49h
	8B4Ah	DM_Color_R74[7:0]	4Ah
	8B4Bh	DM_Color_R75[7:0]	4Bh
	8B4Ch	DM_Color_R76[7:0]	4Ch
	8B4Dh	DM_Color_R77[7:0]	4Dh
	8B4Eh	DM_Color_R78[7:0]	4Eh
	8B4Fh	DM_Color_R79[7:0]	4Fh
	8B50h	DM_Color_R80[7:0]	50h

	8B51h	DM_Color_R81[7:0]	51h
	8B52h	DM_Color_R82[7:0]	52h
	8B53h	DM_Color_R83[7:0]	53h
	8B54h	DM_Color_R84[7:0]	54h
	8B55h	DM_Color_R85[7:0]	55h
	8B56h	DM_Color_R86[7:0]	56h
	8B57h	DM_Color_R87[7:0]	57h
	8B58h	DM_Color_R88[7:0]	58h
	8B59h	DM_Color_R89[7:0]	59h
	8B5Ah	DM_Color_R90[7:0]	5Ah
	8B5Bh	DM_Color_R91[7:0]	5Bh
	8B5Ch	DM_Color_R92[7:0]	5Ch
	8B5Dh	DM_Color_R93[7:0]	5Dh
	8B5Eh	DM_Color_R94[7:0]	5Eh
	8B5Fh	DM_Color_R95[7:0]	5Fh
	8B60h	DM_Color_R96[7:0]	60h
	8B61h	DM_Color_R97[7:0]	61h
	8B62h	DM_Color_R98[7:0]	62h
	8B63h	DM_Color_R99[7:0]	63h
	8B64h	DM_Color_R100[7:0]	64h
	8B65h	DM_Color_R101[7:0]	65h
	8B66h	DM_Color_R102[7:0]	66h
	8B67h	DM_Color_R103[7:0]	67h
	8B68h	DM_Color_R104[7:0]	68h
	8B69h	DM_Color_R105[7:0]	69h
	8B6Ah	DM_Color_R106[7:0]	6Ah
	8B6Bh	DM_Color_R107[7:0]	6Bh
	8B6Ch	DM_Color_R108[7:0]	6Ch
	8B6Dh	DM_Color_R109[7:0]	6Dh
	8B6Eh	DM_Color_R110[7:0]	6Eh
	8B6Fh	DM_Color_R111[7:0]	6Fh
	8B70h	DM_Color_R112[7:0]	70h
	8B71h	DM_Color_R113[7:0]	71h
	8B72h	DM_Color_R114[7:0]	72h
	8B73h	DM_Color_R115[7:0]	73h
	8B74h	DM_Color_R116[7:0]	74h
	8B75h	DM_Color_R117[7:0]	75h
	8B76h	DM_Color_R118[7:0]	76h
	8B77h	DM_Color_R119[7:0]	77h
	8B78h	DM_Color_R120[7:0]	78h
	8B79h	DM_Color_R121[7:0]	79h
	8B7Ah	DM_Color_R122[7:0]	7Ah

	8B7Bh	DM_Color_R123[7:0]	7Bh
	8B7Ch	DM_Color_R124[7:0]	7Ch
	8B7Dh	DM_Color_R125[7:0]	7Dh
	8B7Eh	DM_Color_R126[7:0]	7Eh
	8B7Fh	DM_Color_R127[7:0]	7Fh
	8B80h	DM_Color_R128[7:0]	80h
	8B81h	DM_Color_R129[7:0]	81h
	8B82h	DM_Color_R130[7:0]	82h
	8B83h	DM_Color_R131[7:0]	83h
	8B84h	DM_Color_R132[7:0]	84h
	8B85h	DM_Color_R133[7:0]	85h
	8B86h	DM_Color_R134[7:0]	86h
	8B87h	DM_Color_R135[7:0]	87h
	8B88h	DM_Color_R136[7:0]	88h
	8B89h	DM_Color_R137[7:0]	89h
	8B8Ah	DM_Color_R138[7:0]	8Ah
	8B8Bh	DM_Color_R139[7:0]	8Bh
	8B8Ch	DM_Color_R140[7:0]	8Ch
	8B8Dh	DM_Color_R141[7:0]	8Dh
	8B8Eh	DM_Color_R142[7:0]	8Eh
	8B8Fh	DM_Color_R143[7:0]	8Fh
	8B90h	DM_Color_R144[7:0]	90h
	8B91h	DM_Color_R145[7:0]	91h
	8B92h	DM_Color_R146[7:0]	92h
	8B93h	DM_Color_R147[7:0]	93h
	8B94h	DM_Color_R148[7:0]	94h
	8B95h	DM_Color_R149[7:0]	95h
	8B96h	DM_Color_R150[7:0]	96h
	8B97h	DM_Color_R151[7:0]	97h
	8B98h	DM_Color_R152[7:0]	98h
	8B99h	DM_Color_R153[7:0]	99h
	8B9Ah	DM_Color_R154[7:0]	9Ah
	8B9Bh	DM_Color_R155[7:0]	9Bh
	8B9Ch	DM_Color_R156[7:0]	9Ch
	8B9Dh	DM_Color_R157[7:0]	9Dh
	8B9Eh	DM_Color_R158[7:0]	9Eh
	8B9Fh	DM_Color_R159[7:0]	9Fh
	8BA0h	DM_Color_R160[7:0]	A0h
	8BA1h	DM_Color_R161[7:0]	A1h
	8BA2h	DM_Color_R162[7:0]	A2h
	8BA3h	DM_Color_R163[7:0]	A3h
	8BA4h	DM_Color_R164[7:0]	A4h

	8BA5h	DM_Color_R165[7:0]	A5h
	8BA6h	DM_Color_R166[7:0]	A6h
	8BA7h	DM_Color_R167[7:0]	A7h
	8BA8h	DM_Color_R168[7:0]	A8h
	8BA9h	DM_Color_R169[7:0]	A9h
	8BAAh	DM_Color_R170[7:0]	AAh
	8BABh	DM_Color_R171[7:0]	ABh
	8BACh	DM_Color_R172[7:0]	ACh
	8BADh	DM_Color_R173[7:0]	ADh
	8BAEh	DM_Color_R174[7:0]	AEh
	8BAFh	DM_Color_R175[7:0]	AFh
	8BB0h	DM_Color_R176[7:0]	B0h
	8BB1h	DM_Color_R177[7:0]	B1h
	8BB2h	DM_Color_R178[7:0]	B2h
	8BB3h	DM_Color_R179[7:0]	B3h
	8BB4h	DM_Color_R180[7:0]	B4h
	8BB5h	DM_Color_R181[7:0]	B5h
	8BB6h	DM_Color_R182[7:0]	B6h
	8BB7h	DM_Color_R183[7:0]	B7h
	8BB8h	DM_Color_R184[7:0]	B8h
	8BB9h	DM_Color_R185[7:0]	B9h
	8BBAh	DM_Color_R186[7:0]	BAh
	8BBBh	DM_Color_R187[7:0]	BBh
	8BBCh	DM_Color_R188[7:0]	BCh
	8BBDh	DM_Color_R189[7:0]	BDh
	8BBEh	DM_Color_R190[7:0]	BEh
	8BBFh	DM_Color_R191[7:0]	BFh
	8BC0h	DM_Color_R192[7:0]	C0h
	8BC1h	DM_Color_R193[7:0]	C1h
	8BC2h	DM_Color_R194[7:0]	C2h
	8BC3h	DM_Color_R195[7:0]	C3h
	8BC4h	DM_Color_R196[7:0]	C4h
	8BC5h	DM_Color_R197[7:0]	C5h
	8BC6h	DM_Color_R198[7:0]	C6h
	8BC7h	DM_Color_R199[7:0]	C7h
	8BC8h	DM_Color_R200[7:0]	C8h
	8BC9h	DM_Color_R201[7:0]	C9h
	8BCAh	DM_Color_R202[7:0]	CAh
	8BCBh	DM_Color_R203[7:0]	CBh
	8BCCh	DM_Color_R204[7:0]	CCh
	8BCDh	DM_Color_R205[7:0]	CDh
	8BCEh	DM_Color_R206[7:0]	CEh

	8BCFh	DM_Color_R207[7:0]	CFh
	8BD0h	DM_Color_R208[7:0]	D0h
	8BD1h	DM_Color_R209[7:0]	D1h
	8BD2h	DM_Color_R210[7:0]	D2h
	8BD3h	DM_Color_R211[7:0]	D3h
	8BD4h	DM_Color_R212[7:0]	D4h
	8BD5h	DM_Color_R213[7:0]	D5h
	8BD6h	DM_Color_R214[7:0]	D6h
	8BD7h	DM_Color_R215[7:0]	D7h
	8BD8h	DM_Color_R216[7:0]	D8h
	8BD9h	DM_Color_R217[7:0]	D9h
	8BDAh	DM_Color_R218[7:0]	DAh
	8BDBh	DM_Color_R219[7:0]	DBh
	8BDCh	DM_Color_R220[7:0]	DCh
	8BDDh	DM_Color_R221[7:0]	DDh
	8BDEh	DM_Color_R222[7:0]	DEh
	8BDFh	DM_Color_R223[7:0]	DFh
	8BE0h	DM_Color_R224[7:0]	E0h
	8BE1h	DM_Color_R225[7:0]	E1h
	8BE2h	DM_Color_R226[7:0]	E2h
	8BE3h	DM_Color_R227[7:0]	E3h
	8BE4h	DM_Color_R228[7:0]	E4h
	8BE5h	DM_Color_R229[7:0]	E5h
	8BE6h	DM_Color_R230[7:0]	E6h
	8BE7h	DM_Color_R231[7:0]	E7h
	8BE8h	DM_Color_R232[7:0]	E8h
	8BE9h	DM_Color_R233[7:0]	E9h
	8BEAh	DM_Color_R234[7:0]	EAh
	8BEBh	DM_Color_R235[7:0]	EBh
	8BECh	DM_Color_R236[7:0]	ECh
	8BEDh	DM_Color_R237[7:0]	EDh
	8BEEh	DM_Color_R238[7:0]	EEh
	8BEFh	DM_Color_R239[7:0]	EFh
	8BF0h	DM_Color_R240[7:0]	F0h
	8BF1h	DM_Color_R241[7:0]	F1h
	8BF2h	DM_Color_R242[7:0]	F2h
	8BF3h	DM_Color_R243[7:0]	F3h
	8BF4h	DM_Color_R244[7:0]	F4h
	8BF5h	DM_Color_R245[7:0]	F5h
	8BF6h	DM_Color_R246[7:0]	F6h
	8BF7h	DM_Color_R247[7:0]	F7h
	8BF8h	DM_Color_R248[7:0]	F8h

	8BF9h	DM_Color_R249[7:0]	F9h
	8BFAh	DM_Color_R250[7:0]	FAh
	8BFBh	DM_Color_R251[7:0]	FBh
	8BFCh	DM_Color_R252[7:0]	FCh
	8BFDh	DM_Color_R253[7:0]	FDh
	8BFEh	DM_Color_R254[7:0]	FEh
	8BFFh	DM_Color_R255[7:0]	FFh
Description		This command is used to set digital clock minute color.	
Restriction		-	

DMCOLORG: Digital clock minute color setting (8C00h~8CFFh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
8Ch	8C00h	DM_Color_G0[7:0]								00h
	8C01h	DM_Color_G1[7:0]								01h
	8C02h	DM_Color_G2[7:0]								02h
	8C03h	DM_Color_G3[7:0]								03h
	8C04h	DM_Color_G4[7:0]								04h
	8C05h	DM_Color_G5[7:0]								05h
	8C06h	DM_Color_G6[7:0]								06h
	8C07h	DM_Color_G7[7:0]								07h
	8C08h	DM_Color_G8[7:0]								08h
	8C09h	DM_Color_G9[7:0]								09h
	8C0Ah	DM_Color_G10[7:0]								0Ah
	8C0Bh	DM_Color_G11[7:0]								0Bh
	8C0Ch	DM_Color_G12[7:0]								0Ch
	8C0Dh	DM_Color_G13[7:0]								0Dh
	8C0Eh	DM_Color_G14[7:0]								0Eh
	8C0Fh	DM_Color_G15[7:0]								0Fh
	8C10h	DM_Color_G16[7:0]								10h
	8C11h	DM_Color_G17[7:0]								11h
	8C12h	DM_Color_G18[7:0]								12h
	8C13h	DM_Color_G19[7:0]								13h
	8C14h	DM_Color_G20[7:0]								14h
	8C15h	DM_Color_G21[7:0]								15h
	8C16h	DM_Color_G22[7:0]								16h
	8C17h	DM_Color_G23[7:0]								17h
	8C18h	DM_Color_G24[7:0]								18h
	8C19h	DM_Color_G25[7:0]								19h
	8C1Ah	DM_Color_G26[7:0]								1Ah
	8C1Bh	DM_Color_G27[7:0]								1Bh
	8C1Ch	DM_Color_G28[7:0]								1Ch
	8C1Dh	DM_Color_G29[7:0]								1Dh
	8C1Eh	DM_Color_G30[7:0]								1Eh
	8C1Fh	DM_Color_G31[7:0]								1Fh
	8C20h	DM_Color_G32[7:0]								20h
	8C21h	DM_Color_G33[7:0]								21h
	8C22h	DM_Color_G34[7:0]								22h
	8C23h	DM_Color_G35[7:0]								23h
	8C24h	DM_Color_G36[7:0]								24h
	8C25h	DM_Color_G37[7:0]								25h
	8C26h	DM_Color_G38[7:0]								26h

	8C27h	DM_Color_G39[7:0]	27h
	8C28h	DM_Color_G40[7:0]	28h
	8C29h	DM_Color_G41[7:0]	29h
	8C2Ah	DM_Color_G42[7:0]	2Ah
	8C2Bh	DM_Color_G43[7:0]	2Bh
	8C2Ch	DM_Color_G44[7:0]	2Ch
	8C2Dh	DM_Color_G45[7:0]	2Dh
	8C2Eh	DM_Color_G46[7:0]	2Eh
	8C2Fh	DM_Color_G47[7:0]	2Fh
	8C30h	DM_Color_G48[7:0]	30h
	8C31h	DM_Color_G49[7:0]	31h
	8C32h	DM_Color_G50[7:0]	32h
	8C33h	DM_Color_G51[7:0]	33h
	8C34h	DM_Color_G52[7:0]	34h
	8C35h	DM_Color_G53[7:0]	35h
	8C36h	DM_Color_G54[7:0]	36h
	8C37h	DM_Color_G55[7:0]	37h
	8C38h	DM_Color_G56[7:0]	38h
	8C39h	DM_Color_G57[7:0]	39h
	8C3Ah	DM_Color_G58[7:0]	3Ah
	8C3Bh	DM_Color_G59[7:0]	3Bh
	8C3Ch	DM_Color_G60[7:0]	3Ch
	8C3Dh	DM_Color_G61[7:0]	3Dh
	8C3Eh	DM_Color_G62[7:0]	3Eh
	8C3Fh	DM_Color_G63[7:0]	3Fh
	8C40h	DM_Color_G64[7:0]	40h
	8C41h	DM_Color_G65[7:0]	41h
	8C42h	DM_Color_G66[7:0]	42h
	8C43h	DM_Color_G67[7:0]	43h
	8C44h	DM_Color_G68[7:0]	44h
	8C45h	DM_Color_G69[7:0]	45h
	8C46h	DM_Color_G70[7:0]	46h
	8C47h	DM_Color_G71[7:0]	47h
	8C48h	DM_Color_G72[7:0]	48h
	8C49h	DM_Color_G73[7:0]	49h
	8C4Ah	DM_Color_G74[7:0]	4Ah
	8C4Bh	DM_Color_G75[7:0]	4Bh
	8C4Ch	DM_Color_G76[7:0]	4Ch
	8C4Dh	DM_Color_G77[7:0]	4Dh
	8C4Eh	DM_Color_G78[7:0]	4Eh
	8C4Fh	DM_Color_G79[7:0]	4Fh
	8C50h	DM_Color_G80[7:0]	50h

	8C51h	DM_Color_G81[7:0]	51h
	8C52h	DM_Color_G82[7:0]	52h
	8C53h	DM_Color_G83[7:0]	53h
	8C54h	DM_Color_G84[7:0]	54h
	8C55h	DM_Color_G85[7:0]	55h
	8C56h	DM_Color_G86[7:0]	56h
	8C57h	DM_Color_G87[7:0]	57h
	8C58h	DM_Color_G88[7:0]	58h
	8C59h	DM_Color_G89[7:0]	59h
	8C5Ah	DM_Color_G90[7:0]	5Ah
	8C5Bh	DM_Color_G91[7:0]	5Bh
	8C5Ch	DM_Color_G92[7:0]	5Ch
	8C5Dh	DM_Color_G93[7:0]	5Dh
	8C5Eh	DM_Color_G94[7:0]	5Eh
	8C5Fh	DM_Color_G95[7:0]	5Fh
	8C60h	DM_Color_G96[7:0]	60h
	8C61h	DM_Color_G97[7:0]	61h
	8C62h	DM_Color_G98[7:0]	62h
	8C63h	DM_Color_G99[7:0]	63h
	8C64h	DM_Color_G100[7:0]	64h
	8C65h	DM_Color_G101[7:0]	65h
	8C66h	DM_Color_G102[7:0]	66h
	8C67h	DM_Color_G103[7:0]	67h
	8C68h	DM_Color_G104[7:0]	68h
	8C69h	DM_Color_G105[7:0]	69h
	8C6Ah	DM_Color_G106[7:0]	6Ah
	8C6Bh	DM_Color_G107[7:0]	6Bh
	8C6Ch	DM_Color_G108[7:0]	6Ch
	8C6Dh	DM_Color_G109[7:0]	6Dh
	8C6Eh	DM_Color_G110[7:0]	6Eh
	8C6Fh	DM_Color_G111[7:0]	6Fh
	8C70h	DM_Color_G112[7:0]	70h
	8C71h	DM_Color_G113[7:0]	71h
	8C72h	DM_Color_G114[7:0]	72h
	8C73h	DM_Color_G115[7:0]	73h
	8C74h	DM_Color_G116[7:0]	74h
	8C75h	DM_Color_G117[7:0]	75h
	8C76h	DM_Color_G118[7:0]	76h
	8C77h	DM_Color_G119[7:0]	77h
	8C78h	DM_Color_G120[7:0]	78h
	8C79h	DM_Color_G121[7:0]	79h
	8C7Ah	DM_Color_G122[7:0]	7Ah

	8C7Bh	DM_Color_G123[7:0]	7Bh
	8C7Ch	DM_Color_G124[7:0]	7Ch
	8C7Dh	DM_Color_G125[7:0]	7Dh
	8C7Eh	DM_Color_G126[7:0]	7Eh
	8C7Fh	DM_Color_G127[7:0]	7Fh
	8C80h	DM_Color_G128[7:0]	80h
	8C81h	DM_Color_G129[7:0]	81h
	8C82h	DM_Color_G130[7:0]	82h
	8C83h	DM_Color_G131[7:0]	83h
	8C84h	DM_Color_G132[7:0]	84h
	8C85h	DM_Color_G133[7:0]	85h
	8C86h	DM_Color_G134[7:0]	86h
	8C87h	DM_Color_G135[7:0]	87h
	8C88h	DM_Color_G136[7:0]	88h
	8C89h	DM_Color_G137[7:0]	89h
	8C8Ah	DM_Color_G138[7:0]	8Ah
	8C8Bh	DM_Color_G139[7:0]	8Bh
	8C8Ch	DM_Color_G140[7:0]	8Ch
	8C8Dh	DM_Color_G141[7:0]	8Dh
	8C8Eh	DM_Color_G142[7:0]	8Eh
	8C8Fh	DM_Color_G143[7:0]	8Fh
	8C90h	DM_Color_G144[7:0]	90h
	8C91h	DM_Color_G145[7:0]	91h
	8C92h	DM_Color_G146[7:0]	92h
	8C93h	DM_Color_G147[7:0]	93h
	8C94h	DM_Color_G148[7:0]	94h
	8C95h	DM_Color_G149[7:0]	95h
	8C96h	DM_Color_G150[7:0]	96h
	8C97h	DM_Color_G151[7:0]	97h
	8C98h	DM_Color_G152[7:0]	98h
	8C99h	DM_Color_G153[7:0]	99h
	8C9Ah	DM_Color_G154[7:0]	9Ah
	8C9Bh	DM_Color_G155[7:0]	9Bh
	8C9Ch	DM_Color_G156[7:0]	9Ch
	8C9Dh	DM_Color_G157[7:0]	9Dh
	8C9Eh	DM_Color_G158[7:0]	9Eh
	8C9Fh	DM_Color_G159[7:0]	9Fh
	8CA0h	DM_Color_G160[7:0]	A0h
	8CA1h	DM_Color_G161[7:0]	A1h
	8CA2h	DM_Color_G162[7:0]	A2h
	8CA3h	DM_Color_G163[7:0]	A3h
	8CA4h	DM_Color_G164[7:0]	A4h

	8CA5h	DM_Color_G165[7:0]	A5h
	8CA6h	DM_Color_G166[7:0]	A6h
	8CA7h	DM_Color_G167[7:0]	A7h
	8CA8h	DM_Color_G168[7:0]	A8h
	8CA9h	DM_Color_G169[7:0]	A9h
	8CAAh	DM_Color_G170[7:0]	AAh
	8CABh	DM_Color_G171[7:0]	ABh
	8CACh	DM_Color_G172[7:0]	ACh
	8CADh	DM_Color_G173[7:0]	ADh
	8CAEh	DM_Color_G174[7:0]	AEh
	8CAFh	DM_Color_G175[7:0]	AFh
	8CB0h	DM_Color_G176[7:0]	B0h
	8CB1h	DM_Color_G177[7:0]	B1h
	8CB2h	DM_Color_G178[7:0]	B2h
	8CB3h	DM_Color_G179[7:0]	B3h
	8CB4h	DM_Color_G180[7:0]	B4h
	8CB5h	DM_Color_G181[7:0]	B5h
	8CB6h	DM_Color_G182[7:0]	B6h
	8CB7h	DM_Color_G183[7:0]	B7h
	8CB8h	DM_Color_G184[7:0]	B8h
	8CB9h	DM_Color_G185[7:0]	B9h
	8CBAh	DM_Color_G186[7:0]	BAh
	8CBBh	DM_Color_G187[7:0]	BBh
	8CBCh	DM_Color_G188[7:0]	BCh
	8CBDh	DM_Color_G189[7:0]	BDh
	8CBEh	DM_Color_G190[7:0]	BEh
	8CBFh	DM_Color_G191[7:0]	BFh
	8CC0h	DM_Color_G192[7:0]	C0h
	8CC1h	DM_Color_G193[7:0]	C1h
	8CC2h	DM_Color_G194[7:0]	C2h
	8CC3h	DM_Color_G195[7:0]	C3h
	8CC4h	DM_Color_G196[7:0]	C4h
	8CC5h	DM_Color_G197[7:0]	C5h
	8CC6h	DM_Color_G198[7:0]	C6h
	8CC7h	DM_Color_G199[7:0]	C7h
	8CC8h	DM_Color_G200[7:0]	C8h
	8CC9h	DM_Color_G201[7:0]	C9h
	8CCAh	DM_Color_G202[7:0]	CAh
	8CCBh	DM_Color_G203[7:0]	CBh
	8CCCh	DM_Color_G204[7:0]	CCh
	8CCDh	DM_Color_G205[7:0]	CDh
	8CCEh	DM_Color_G206[7:0]	CEh

	8CCFh	DM_Color_G207[7:0]	CFh
	8CD0h	DM_Color_G208[7:0]	D0h
	8CD1h	DM_Color_G209[7:0]	D1h
	8CD2h	DM_Color_G210[7:0]	D2h
	8CD3h	DM_Color_G211[7:0]	D3h
	8CD4h	DM_Color_G212[7:0]	D4h
	8CD5h	DM_Color_G213[7:0]	D5h
	8CD6h	DM_Color_G214[7:0]	D6h
	8CD7h	DM_Color_G215[7:0]	D7h
	8CD8h	DM_Color_G216[7:0]	D8h
	8CD9h	DM_Color_G217[7:0]	D9h
	8CDAh	DM_Color_G218[7:0]	DAh
	8CDBh	DM_Color_G219[7:0]	DBh
	8CDCh	DM_Color_G220[7:0]	DCh
	8CDDh	DM_Color_G221[7:0]	DDh
	8CDEh	DM_Color_G222[7:0]	DEh
	8CDFh	DM_Color_G223[7:0]	DFh
	8CE0h	DM_Color_G224[7:0]	E0h
	8CE1h	DM_Color_G225[7:0]	E1h
	8CE2h	DM_Color_G226[7:0]	E2h
	8CE3h	DM_Color_G227[7:0]	E3h
	8CE4h	DM_Color_G228[7:0]	E4h
	8CE5h	DM_Color_G229[7:0]	E5h
	8CE6h	DM_Color_G230[7:0]	E6h
	8CE7h	DM_Color_G231[7:0]	E7h
	8CE8h	DM_Color_G232[7:0]	E8h
	8CE9h	DM_Color_G233[7:0]	E9h
	8CEAh	DM_Color_G234[7:0]	EAh
	8CEBh	DM_Color_G235[7:0]	EBh
	8CECh	DM_Color_G236[7:0]	ECh
	8CEDh	DM_Color_G237[7:0]	EDh
	8CEEh	DM_Color_G238[7:0]	EEh
	8CEFh	DM_Color_G239[7:0]	EFh
	8CF0h	DM_Color_G240[7:0]	F0h
	8CF1h	DM_Color_G241[7:0]	F1h
	8CF2h	DM_Color_G242[7:0]	F2h
	8CF3h	DM_Color_G243[7:0]	F3h
	8CF4h	DM_Color_G244[7:0]	F4h
	8CF5h	DM_Color_G245[7:0]	F5h
	8CF6h	DM_Color_G246[7:0]	F6h
	8CF7h	DM_Color_G247[7:0]	F7h
	8CF8h	DM_Color_G248[7:0]	F8h

	8CF9h	DM_Color_G249[7:0]	F9h
	8CFAh	DM_Color_G250[7:0]	FAh
	8CFBh	DM_Color_G251[7:0]	FBh
	8CFCh	DM_Color_G252[7:0]	FCh
	8CFDh	DM_Color_G253[7:0]	FDh
	8CFEh	DM_Color_G254[7:0]	FEh
	8CFFh	DM_Color_G255[7:0]	FFh
Description		This command is used to set digital clock minute color.	
Restriction		-	

DMCOLORB: Digital clock minute color setting (8D00h~8DFFh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
8Dh	8D00h	DM_Color_B0[7:0]								00h
	8D01h	DM_Color_B1[7:0]								01h
	8D02h	DM_Color_B2[7:0]								02h
	8D03h	DM_Color_B3[7:0]								03h
	8D04h	DM_Color_B4[7:0]								04h
	8D05h	DM_Color_B5[7:0]								05h
	8D06h	DM_Color_B6[7:0]								06h
	8D07h	DM_Color_B7[7:0]								07h
	8D08h	DM_Color_B8[7:0]								08h
	8D09h	DM_Color_B9[7:0]								09h
	8D0Ah	DM_Color_B10[7:0]								0Ah
	8D0Bh	DM_Color_B11[7:0]								0Bh
	8D0Ch	DM_Color_B12[7:0]								0Ch
	8D0Dh	DM_Color_B13[7:0]								0Dh
	8D0Eh	DM_Color_B14[7:0]								0Eh
	8D0Fh	DM_Color_B15[7:0]								0Fh
	8D10h	DM_Color_B16[7:0]								10h
	8D11h	DM_Color_B17[7:0]								11h
	8D12h	DM_Color_B18[7:0]								12h
	8D13h	DM_Color_B19[7:0]								13h
	8D14h	DM_Color_B20[7:0]								14h
	8D15h	DM_Color_B21[7:0]								15h
	8D16h	DM_Color_B22[7:0]								16h
	8D17h	DM_Color_B23[7:0]								17h
	8D18h	DM_Color_B24[7:0]								18h
	8D19h	DM_Color_B25[7:0]								19h
	8D1Ah	DM_Color_B26[7:0]								1Ah
	8D1Bh	DM_Color_B27[7:0]								1Bh
	8D1Ch	DM_Color_B28[7:0]								1Ch
	8D1Dh	DM_Color_B29[7:0]								1Dh
	8D1Eh	DM_Color_B30[7:0]								1Eh
	8D1Fh	DM_Color_B31[7:0]								1Fh
	8D20h	DM_Color_B32[7:0]								20h
	8D21h	DM_Color_B33[7:0]								21h
	8D22h	DM_Color_B34[7:0]								22h
	8D23h	DM_Color_B35[7:0]								23h
	8D24h	DM_Color_B36[7:0]								24h
	8D25h	DM_Color_B37[7:0]								25h
	8D26h	DM_Color_B38[7:0]								26h

	8D27h	DM_Color_B39[7:0]	27h
	8D28h	DM_Color_B40[7:0]	28h
	8D29h	DM_Color_B41[7:0]	29h
	8D2Ah	DM_Color_B42[7:0]	2Ah
	8D2Bh	DM_Color_B43[7:0]	2Bh
	8D2Ch	DM_Color_B44[7:0]	2Ch
	8D2Dh	DM_Color_B45[7:0]	2Dh
	8D2Eh	DM_Color_B46[7:0]	2Eh
	8D2Fh	DM_Color_B47[7:0]	2Fh
	8D30h	DM_Color_B48[7:0]	30h
	8D31h	DM_Color_B49[7:0]	31h
	8D32h	DM_Color_B50[7:0]	32h
	8D33h	DM_Color_B51[7:0]	33h
	8D34h	DM_Color_B52[7:0]	34h
	8D35h	DM_Color_B53[7:0]	35h
	8D36h	DM_Color_B54[7:0]	36h
	8D37h	DM_Color_B55[7:0]	37h
	8D38h	DM_Color_B56[7:0]	38h
	8D39h	DM_Color_B57[7:0]	39h
	8D3Ah	DM_Color_B58[7:0]	3Ah
	8D3Bh	DM_Color_B59[7:0]	3Bh
	8D3Ch	DM_Color_B60[7:0]	3Ch
	8D3Dh	DM_Color_B61[7:0]	3Dh
	8D3Eh	DM_Color_B62[7:0]	3Eh
	8D3Fh	DM_Color_B63[7:0]	3Fh
	8D40h	DM_Color_B64[7:0]	40h
	8D41h	DM_Color_B65[7:0]	41h
	8D42h	DM_Color_B66[7:0]	42h
	8D43h	DM_Color_B67[7:0]	43h
	8D44h	DM_Color_B68[7:0]	44h
	8D45h	DM_Color_B69[7:0]	45h
	8D46h	DM_Color_B70[7:0]	46h
	8D47h	DM_Color_B71[7:0]	47h
	8D48h	DM_Color_B72[7:0]	48h
	8D49h	DM_Color_B73[7:0]	49h
	8D4Ah	DM_Color_B74[7:0]	4Ah
	8D4Bh	DM_Color_B75[7:0]	4Bh
	8D4Ch	DM_Color_B76[7:0]	4Ch
	8D4Dh	DM_Color_B77[7:0]	4Dh
	8D4Eh	DM_Color_B78[7:0]	4Eh
	8D4Fh	DM_Color_B79[7:0]	4Fh
	8D50h	DM_Color_B80[7:0]	50h

	8D51h	DM_Color_B81[7:0]	51h
	8D52h	DM_Color_B82[7:0]	52h
	8D53h	DM_Color_B83[7:0]	53h
	8D54h	DM_Color_B84[7:0]	54h
	8D55h	DM_Color_B85[7:0]	55h
	8D56h	DM_Color_B86[7:0]	56h
	8D57h	DM_Color_B87[7:0]	57h
	8D58h	DM_Color_B88[7:0]	58h
	8D59h	DM_Color_B89[7:0]	59h
	8D5Ah	DM_Color_B90[7:0]	5Ah
	8D5Bh	DM_Color_B91[7:0]	5Bh
	8D5Ch	DM_Color_B92[7:0]	5Ch
	8D5Dh	DM_Color_B93[7:0]	5Dh
	8D5Eh	DM_Color_B94[7:0]	5Eh
	8D5Fh	DM_Color_B95[7:0]	5Fh
	8D60h	DM_Color_B96[7:0]	60h
	8D61h	DM_Color_B97[7:0]	61h
	8D62h	DM_Color_B98[7:0]	62h
	8D63h	DM_Color_B99[7:0]	63h
	8D64h	DM_Color_B100[7:0]	64h
	8D65h	DM_Color_B101[7:0]	65h
	8D66h	DM_Color_B102[7:0]	66h
	8D67h	DM_Color_B103[7:0]	67h
	8D68h	DM_Color_B104[7:0]	68h
	8D69h	DM_Color_B105[7:0]	69h
	8D6Ah	DM_Color_B106[7:0]	6Ah
	8D6Bh	DM_Color_B107[7:0]	6Bh
	8D6Ch	DM_Color_B108[7:0]	6Ch
	8D6Dh	DM_Color_B109[7:0]	6Dh
	8D6Eh	DM_Color_B110[7:0]	6Eh
	8D6Fh	DM_Color_B111[7:0]	6Fh
	8D70h	DM_Color_B112[7:0]	70h
	8D71h	DM_Color_B113[7:0]	71h
	8D72h	DM_Color_B114[7:0]	72h
	8D73h	DM_Color_B115[7:0]	73h
	8D74h	DM_Color_B116[7:0]	74h
	8D75h	DM_Color_B117[7:0]	75h
	8D76h	DM_Color_B118[7:0]	76h
	8D77h	DM_Color_B119[7:0]	77h
	8D78h	DM_Color_B120[7:0]	78h
	8D79h	DM_Color_B121[7:0]	79h
	8D7Ah	DM_Color_B122[7:0]	7Ah

	8D7Bh	DM_Color_B123[7:0]	7Bh
	8D7Ch	DM_Color_B124[7:0]	7Ch
	8D7Dh	DM_Color_B125[7:0]	7Dh
	8D7Eh	DM_Color_B126[7:0]	7Eh
	8D7Fh	DM_Color_B127[7:0]	7Fh
	8D80h	DM_Color_B128[7:0]	80h
	8D81h	DM_Color_B129[7:0]	81h
	8D82h	DM_Color_B130[7:0]	82h
	8D83h	DM_Color_B131[7:0]	83h
	8D84h	DM_Color_B132[7:0]	84h
	8D85h	DM_Color_B133[7:0]	85h
	8D86h	DM_Color_B134[7:0]	86h
	8D87h	DM_Color_B135[7:0]	87h
	8D88h	DM_Color_B136[7:0]	88h
	8D89h	DM_Color_B137[7:0]	89h
	8D8Ah	DM_Color_B138[7:0]	8Ah
	8D8Bh	DM_Color_B139[7:0]	8Bh
	8D8Ch	DM_Color_B140[7:0]	8Ch
	8D8Dh	DM_Color_B141[7:0]	8Dh
	8D8Eh	DM_Color_B142[7:0]	8Eh
	8D8Fh	DM_Color_B143[7:0]	8Fh
	8D90h	DM_Color_B144[7:0]	90h
	8D91h	DM_Color_B145[7:0]	91h
	8D92h	DM_Color_B146[7:0]	92h
	8D93h	DM_Color_B147[7:0]	93h
	8D94h	DM_Color_B148[7:0]	94h
	8D95h	DM_Color_B149[7:0]	95h
	8D96h	DM_Color_B150[7:0]	96h
	8D97h	DM_Color_B151[7:0]	97h
	8D98h	DM_Color_B152[7:0]	98h
	8D99h	DM_Color_B153[7:0]	99h
	8D9Ah	DM_Color_B154[7:0]	9Ah
	8D9Bh	DM_Color_B155[7:0]	9Bh
	8D9Ch	DM_Color_B156[7:0]	9Ch
	8D9Dh	DM_Color_B157[7:0]	9Dh
	8D9Eh	DM_Color_B158[7:0]	9Eh
	8D9Fh	DM_Color_B159[7:0]	9Fh
	8DA0h	DM_Color_B160[7:0]	A0h
	8DA1h	DM_Color_B161[7:0]	A1h
	8DA2h	DM_Color_B162[7:0]	A2h
	8DA3h	DM_Color_B163[7:0]	A3h
	8DA4h	DM_Color_B164[7:0]	A4h

	8DA5h	DM_Color_B165[7:0]	A5h
	8DA6h	DM_Color_B166[7:0]	A6h
	8DA7h	DM_Color_B167[7:0]	A7h
	8DA8h	DM_Color_B168[7:0]	A8h
	8DA9h	DM_Color_B169[7:0]	A9h
	8DAAh	DM_Color_B170[7:0]	AAh
	8DABh	DM_Color_B171[7:0]	ABh
	8DACh	DM_Color_B172[7:0]	ACh
	8DADh	DM_Color_B173[7:0]	ADh
	8DAEh	DM_Color_B174[7:0]	AEh
	8DAFh	DM_Color_B175[7:0]	AFh
	8DB0h	DM_Color_B176[7:0]	B0h
	8DB1h	DM_Color_B177[7:0]	B1h
	8DB2h	DM_Color_B178[7:0]	B2h
	8DB3h	DM_Color_B179[7:0]	B3h
	8DB4h	DM_Color_B180[7:0]	B4h
	8DB5h	DM_Color_B181[7:0]	B5h
	8DB6h	DM_Color_B182[7:0]	B6h
	8DB7h	DM_Color_B183[7:0]	B7h
	8DB8h	DM_Color_B184[7:0]	B8h
	8DB9h	DM_Color_B185[7:0]	B9h
	8DBAh	DM_Color_B186[7:0]	BAh
	8DBBh	DM_Color_B187[7:0]	BBh
	8DBCh	DM_Color_B188[7:0]	BCh
	8DBDh	DM_Color_B189[7:0]	BDh
	8DBEh	DM_Color_B190[7:0]	BEh
	8DBFh	DM_Color_B191[7:0]	BFh
	8DC0h	DM_Color_B192[7:0]	C0h
	8DC1h	DM_Color_B193[7:0]	C1h
	8DC2h	DM_Color_B194[7:0]	C2h
	8DC3h	DM_Color_B195[7:0]	C3h
	8DC4h	DM_Color_B196[7:0]	C4h
	8DC5h	DM_Color_B197[7:0]	C5h
	8DC6h	DM_Color_B198[7:0]	C6h
	8DC7h	DM_Color_B199[7:0]	C7h
	8DC8h	DM_Color_B200[7:0]	C8h
	8DC9h	DM_Color_B201[7:0]	C9h
	8DCAh	DM_Color_B202[7:0]	CAh
	8DCBh	DM_Color_B203[7:0]	CBh
	8DCCh	DM_Color_B204[7:0]	CCh
	8DCDh	DM_Color_B205[7:0]	CDh
	8DCEh	DM_Color_B206[7:0]	CEh

	8DCFh	DM_Color_B207[7:0]	CFh
	8DD0h	DM_Color_B208[7:0]	D0h
	8DD1h	DM_Color_B209[7:0]	D1h
	8DD2h	DM_Color_B210[7:0]	D2h
	8DD3h	DM_Color_B211[7:0]	D3h
	8DD4h	DM_Color_B212[7:0]	D4h
	8DD5h	DM_Color_B213[7:0]	D5h
	8DD6h	DM_Color_B214[7:0]	D6h
	8DD7h	DM_Color_B215[7:0]	D7h
	8DD8h	DM_Color_B216[7:0]	D8h
	8DD9h	DM_Color_B217[7:0]	D9h
	8DDAh	DM_Color_B218[7:0]	DAh
	8DDBh	DM_Color_B219[7:0]	DBh
	8DDCh	DM_Color_B220[7:0]	DCh
	8DDDh	DM_Color_B221[7:0]	DDh
	8DDEh	DM_Color_B222[7:0]	DEh
	8DDFh	DM_Color_B223[7:0]	DFh
	8DE0h	DM_Color_B224[7:0]	E0h
	8DE1h	DM_Color_B225[7:0]	E1h
	8DE2h	DM_Color_B226[7:0]	E2h
	8DE3h	DM_Color_B227[7:0]	E3h
	8DE4h	DM_Color_B228[7:0]	E4h
	8DE5h	DM_Color_B229[7:0]	E5h
	8DE6h	DM_Color_B230[7:0]	E6h
	8DE7h	DM_Color_B231[7:0]	E7h
	8DE8h	DM_Color_B232[7:0]	E8h
	8DE9h	DM_Color_B233[7:0]	E9h
	8DEAh	DM_Color_B234[7:0]	EAh
	8DEBh	DM_Color_B235[7:0]	EBh
	8DECh	DM_Color_B236[7:0]	ECh
	8DEDh	DM_Color_B237[7:0]	EDh
	8DEEh	DM_Color_B238[7:0]	EEh
	8DEFh	DM_Color_B239[7:0]	EFh
	8DF0h	DM_Color_B240[7:0]	F0h
	8DF1h	DM_Color_B241[7:0]	F1h
	8DF2h	DM_Color_B242[7:0]	F2h
	8DF3h	DM_Color_B243[7:0]	F3h
	8DF4h	DM_Color_B244[7:0]	F4h
	8DF5h	DM_Color_B245[7:0]	F5h
	8DF6h	DM_Color_B246[7:0]	F6h
	8DF7h	DM_Color_B247[7:0]	F7h
	8DF8h	DM_Color_B248[7:0]	F8h

	8DF9h	DM_Color_B249[7:0]	F9h
	8DFAh	DM_Color_B250[7:0]	FAh
	8DFBh	DM_Color_B251[7:0]	FBh
	8DFCh	DM_Color_B252[7:0]	FCh
	8DFDh	DM_Color_B253[7:0]	FDh
	8DFEh	DM_Color_B254[7:0]	FEh
	8DFFh	DM_Color_B255[7:0]	FFh
Description		This command is used to set digital clock minute color.	
Restriction		-	

DMCOLORA: Digital clock minute color setting (8E00h~8EFFh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
8Eh	8E00h	DM_Color_A0[7:0]								00h
	8E01h	DM_Color_A1[7:0]								01h
	8E02h	DM_Color_A2[7:0]								02h
	8E03h	DM_Color_A3[7:0]								03h
	8E04h	DM_Color_A4[7:0]								04h
	8E05h	DM_Color_A5[7:0]								05h
	8E06h	DM_Color_A6[7:0]								06h
	8E07h	DM_Color_A7[7:0]								07h
	8E08h	DM_Color_A8[7:0]								08h
	8E09h	DM_Color_A9[7:0]								09h
	8E0Ah	DM_Color_A10[7:0]								0Ah
	8E0Bh	DM_Color_A11[7:0]								0Bh
	8E0Ch	DM_Color_A12[7:0]								0Ch
	8E0Dh	DM_Color_A13[7:0]								0Dh
	8E0Eh	DM_Color_A14[7:0]								0Eh
	8E0Fh	DM_Color_A15[7:0]								0Fh
	8E10h	DM_Color_A16[7:0]								10h
	8E11h	DM_Color_A17[7:0]								11h
	8E12h	DM_Color_A18[7:0]								12h
	8E13h	DM_Color_A19[7:0]								13h
	8E14h	DM_Color_A20[7:0]								14h
	8E15h	DM_Color_A21[7:0]								15h
	8E16h	DM_Color_A22[7:0]								16h
	8E17h	DM_Color_A23[7:0]								17h
	8E18h	DM_Color_A24[7:0]								18h
	8E19h	DM_Color_A25[7:0]								19h
	8E1Ah	DM_Color_A26[7:0]								1Ah
	8E1Bh	DM_Color_A27[7:0]								1Bh
	8E1Ch	DM_Color_A28[7:0]								1Ch
	8E1Dh	DM_Color_A29[7:0]								1Dh
	8E1Eh	DM_Color_A30[7:0]								1Eh
	8E1Fh	DM_Color_A31[7:0]								1Fh
	8E20h	DM_Color_A32[7:0]								20h
	8E21h	DM_Color_A33[7:0]								21h
	8E22h	DM_Color_A34[7:0]								22h
	8E23h	DM_Color_A35[7:0]								23h
	8E24h	DM_Color_A36[7:0]								24h
	8E25h	DM_Color_A37[7:0]								25h
	8E26h	DM_Color_A38[7:0]								26h

	8E27h	DM_Color_A39[7:0]	27h
	8E28h	DM_Color_A40[7:0]	28h
	8E29h	DM_Color_A41[7:0]	29h
	8E2Ah	DM_Color_A42[7:0]	2Ah
	8E2Bh	DM_Color_A43[7:0]	2Bh
	8E2Ch	DM_Color_A44[7:0]	2Ch
	8E2Dh	DM_Color_A45[7:0]	2Dh
	8E2Eh	DM_Color_A46[7:0]	2Eh
	8E2Fh	DM_Color_A47[7:0]	2Fh
	8E30h	DM_Color_A48[7:0]	30h
	8E31h	DM_Color_A49[7:0]	31h
	8E32h	DM_Color_A50[7:0]	32h
	8E33h	DM_Color_A51[7:0]	33h
	8E34h	DM_Color_A52[7:0]	34h
	8E35h	DM_Color_A53[7:0]	35h
	8E36h	DM_Color_A54[7:0]	36h
	8E37h	DM_Color_A55[7:0]	37h
	8E38h	DM_Color_A56[7:0]	38h
	8E39h	DM_Color_A57[7:0]	39h
	8E3Ah	DM_Color_A58[7:0]	3Ah
	8E3Bh	DM_Color_A59[7:0]	3Bh
	8E3Ch	DM_Color_A60[7:0]	3Ch
	8E3Dh	DM_Color_A61[7:0]	3Dh
	8E3Eh	DM_Color_A62[7:0]	3Eh
	8E3Fh	DM_Color_A63[7:0]	3Fh
	8E40h	DM_Color_A64[7:0]	40h
	8E41h	DM_Color_A65[7:0]	41h
	8E42h	DM_Color_A66[7:0]	42h
	8E43h	DM_Color_A67[7:0]	43h
	8E44h	DM_Color_A68[7:0]	44h
	8E45h	DM_Color_A69[7:0]	45h
	8E46h	DM_Color_A70[7:0]	46h
	8E47h	DM_Color_A71[7:0]	47h
	8E48h	DM_Color_A72[7:0]	48h
	8E49h	DM_Color_A73[7:0]	49h
	8E4Ah	DM_Color_A74[7:0]	4Ah
	8E4Bh	DM_Color_A75[7:0]	4Bh
	8E4Ch	DM_Color_A76[7:0]	4Ch
	8E4Dh	DM_Color_A77[7:0]	4Dh
	8E4Eh	DM_Color_A78[7:0]	4Eh
	8E4Fh	DM_Color_A79[7:0]	4Fh
	8E50h	DM_Color_A80[7:0]	50h

	8E51h	DM_Color_A81[7:0]	51h
	8E52h	DM_Color_A82[7:0]	52h
	8E53h	DM_Color_A83[7:0]	53h
	8E54h	DM_Color_A84[7:0]	54h
	8E55h	DM_Color_A85[7:0]	55h
	8E56h	DM_Color_A86[7:0]	56h
	8E57h	DM_Color_A87[7:0]	57h
	8E58h	DM_Color_A88[7:0]	58h
	8E59h	DM_Color_A89[7:0]	59h
	8E5Ah	DM_Color_A90[7:0]	5Ah
	8E5Bh	DM_Color_A91[7:0]	5Bh
	8E5Ch	DM_Color_A92[7:0]	5Ch
	8E5Dh	DM_Color_A93[7:0]	5Dh
	8E5Eh	DM_Color_A94[7:0]	5Eh
	8E5Fh	DM_Color_A95[7:0]	5Fh
	8E60h	DM_Color_A96[7:0]	60h
	8E61h	DM_Color_A97[7:0]	61h
	8E62h	DM_Color_A98[7:0]	62h
	8E63h	DM_Color_A99[7:0]	63h
	8E64h	DM_Color_A100[7:0]	64h
	8E65h	DM_Color_A101[7:0]	65h
	8E66h	DM_Color_A102[7:0]	66h
	8E67h	DM_Color_A103[7:0]	67h
	8E68h	DM_Color_A104[7:0]	68h
	8E69h	DM_Color_A105[7:0]	69h
	8E6Ah	DM_Color_A106[7:0]	6Ah
	8E6Bh	DM_Color_A107[7:0]	6Bh
	8E6Ch	DM_Color_A108[7:0]	6Ch
	8E6Dh	DM_Color_A109[7:0]	6Dh
	8E6Eh	DM_Color_A110[7:0]	6Eh
	8E6Fh	DM_Color_A111[7:0]	6Fh
	8E70h	DM_Color_A112[7:0]	70h
	8E71h	DM_Color_A113[7:0]	71h
	8E72h	DM_Color_A114[7:0]	72h
	8E73h	DM_Color_A115[7:0]	73h
	8E74h	DM_Color_A116[7:0]	74h
	8E75h	DM_Color_A117[7:0]	75h
	8E76h	DM_Color_A118[7:0]	76h
	8E77h	DM_Color_A119[7:0]	77h
	8E78h	DM_Color_A120[7:0]	78h
	8E79h	DM_Color_A121[7:0]	79h
	8E7Ah	DM_Color_A122[7:0]	7Ah

	8E7Bh	DM_Color_A123[7:0]	7Bh
	8E7Ch	DM_Color_A124[7:0]	7Ch
	8E7Dh	DM_Color_A125[7:0]	7Dh
	8E7Eh	DM_Color_A126[7:0]	7Eh
	8E7Fh	DM_Color_A127[7:0]	7Fh
	8E80h	DM_Color_A128[7:0]	80h
	8E81h	DM_Color_A129[7:0]	81h
	8E82h	DM_Color_A130[7:0]	82h
	8E83h	DM_Color_A131[7:0]	83h
	8E84h	DM_Color_A132[7:0]	84h
	8E85h	DM_Color_A133[7:0]	85h
	8E86h	DM_Color_A134[7:0]	86h
	8E87h	DM_Color_A135[7:0]	87h
	8E88h	DM_Color_A136[7:0]	88h
	8E89h	DM_Color_A137[7:0]	89h
	8E8Ah	DM_Color_A138[7:0]	8Ah
	8E8Bh	DM_Color_A139[7:0]	8Bh
	8E8Ch	DM_Color_A140[7:0]	8Ch
	8E8Dh	DM_Color_A141[7:0]	8Dh
	8E8Eh	DM_Color_A142[7:0]	8Eh
	8E8Fh	DM_Color_A143[7:0]	8Fh
	8E90h	DM_Color_A144[7:0]	90h
	8E91h	DM_Color_A145[7:0]	91h
	8E92h	DM_Color_A146[7:0]	92h
	8E93h	DM_Color_A147[7:0]	93h
	8E94h	DM_Color_A148[7:0]	94h
	8E95h	DM_Color_A149[7:0]	95h
	8E96h	DM_Color_A150[7:0]	96h
	8E97h	DM_Color_A151[7:0]	97h
	8E98h	DM_Color_A152[7:0]	98h
	8E99h	DM_Color_A153[7:0]	99h
	8E9Ah	DM_Color_A154[7:0]	9Ah
	8E9Bh	DM_Color_A155[7:0]	9Bh
	8E9Ch	DM_Color_A156[7:0]	9Ch
	8E9Dh	DM_Color_A157[7:0]	9Dh
	8E9Eh	DM_Color_A158[7:0]	9Eh
	8E9Fh	DM_Color_A159[7:0]	9Fh
	8EA0h	DM_Color_A160[7:0]	A0h
	8EA1h	DM_Color_A161[7:0]	A1h
	8EA2h	DM_Color_A162[7:0]	A2h
	8EA3h	DM_Color_A163[7:0]	A3h
	8EA4h	DM_Color_A164[7:0]	A4h

	8EA5h	DM_Color_A165[7:0]	A5h
	8EA6h	DM_Color_A166[7:0]	A6h
	8EA7h	DM_Color_A167[7:0]	A7h
	8EA8h	DM_Color_A168[7:0]	A8h
	8EA9h	DM_Color_A169[7:0]	A9h
	8EAAh	DM_Color_A170[7:0]	AAh
	8EABh	DM_Color_A171[7:0]	ABh
	8EACh	DM_Color_A172[7:0]	ACh
	8EADh	DM_Color_A173[7:0]	ADh
	8EAEh	DM_Color_A174[7:0]	AEh
	8EAFh	DM_Color_A175[7:0]	AFh
	8EB0h	DM_Color_A176[7:0]	B0h
	8EB1h	DM_Color_A177[7:0]	B1h
	8EB2h	DM_Color_A178[7:0]	B2h
	8EB3h	DM_Color_A179[7:0]	B3h
	8EB4h	DM_Color_A180[7:0]	B4h
	8EB5h	DM_Color_A181[7:0]	B5h
	8EB6h	DM_Color_A182[7:0]	B6h
	8EB7h	DM_Color_A183[7:0]	B7h
	8EB8h	DM_Color_A184[7:0]	B8h
	8EB9h	DM_Color_A185[7:0]	B9h
	8EBAh	DM_Color_A186[7:0]	BAh
	8EBBh	DM_Color_A187[7:0]	BBh
	8EBCh	DM_Color_A188[7:0]	BCh
	8EBDh	DM_Color_A189[7:0]	BDh
	8EBEh	DM_Color_A190[7:0]	BEh
	8EBFh	DM_Color_A191[7:0]	BFh
	8EC0h	DM_Color_A192[7:0]	C0h
	8EC1h	DM_Color_A193[7:0]	C1h
	8EC2h	DM_Color_A194[7:0]	C2h
	8EC3h	DM_Color_A195[7:0]	C3h
	8EC4h	DM_Color_A196[7:0]	C4h
	8EC5h	DM_Color_A197[7:0]	C5h
	8EC6h	DM_Color_A198[7:0]	C6h
	8EC7h	DM_Color_A199[7:0]	C7h
	8EC8h	DM_Color_A200[7:0]	C8h
	8EC9h	DM_Color_A201[7:0]	C9h
	8ECAh	DM_Color_A202[7:0]	CAh
	8ECBh	DM_Color_A203[7:0]	CBh
	8ECCh	DM_Color_A204[7:0]	CCh
	8ECDh	DM_Color_A205[7:0]	CDh
	8ECEh	DM_Color_A206[7:0]	CEh

	8ECFh	DM_Color_A207[7:0]	CFh
	8ED0h	DM_Color_A208[7:0]	D0h
	8ED1h	DM_Color_A209[7:0]	D1h
	8ED2h	DM_Color_A210[7:0]	D2h
	8ED3h	DM_Color_A211[7:0]	D3h
	8ED4h	DM_Color_A212[7:0]	D4h
	8ED5h	DM_Color_A213[7:0]	D5h
	8ED6h	DM_Color_A214[7:0]	D6h
	8ED7h	DM_Color_A215[7:0]	D7h
	8ED8h	DM_Color_A216[7:0]	D8h
	8ED9h	DM_Color_A217[7:0]	D9h
	8EDAh	DM_Color_A218[7:0]	DAh
	8EDBh	DM_Color_A219[7:0]	DBh
	8EDCh	DM_Color_A220[7:0]	DCh
	8EDDh	DM_Color_A221[7:0]	DDh
	8EDEh	DM_Color_A222[7:0]	DEh
	8EDFh	DM_Color_A223[7:0]	DFh
	8EE0h	DM_Color_A224[7:0]	E0h
	8EE1h	DM_Color_A225[7:0]	E1h
	8EE2h	DM_Color_A226[7:0]	E2h
	8EE3h	DM_Color_A227[7:0]	E3h
	8EE4h	DM_Color_A228[7:0]	E4h
	8EE5h	DM_Color_A229[7:0]	E5h
	8EE6h	DM_Color_A230[7:0]	E6h
	8EE7h	DM_Color_A231[7:0]	E7h
	8EE8h	DM_Color_A232[7:0]	E8h
	8EE9h	DM_Color_A233[7:0]	E9h
	8EEAh	DM_Color_A234[7:0]	EAh
	8EEBh	DM_Color_A235[7:0]	EBh
	8EECh	DM_Color_A236[7:0]	ECh
	8EEDh	DM_Color_A237[7:0]	EDh
	8EEEh	DM_Color_A238[7:0]	EEh
	8EEFh	DM_Color_A239[7:0]	EFh
	8EF0h	DM_Color_A240[7:0]	F0h
	8EF1h	DM_Color_A241[7:0]	F1h
	8EF2h	DM_Color_A242[7:0]	F2h
	8EF3h	DM_Color_A243[7:0]	F3h
	8EF4h	DM_Color_A244[7:0]	F4h
	8EF5h	DM_Color_A245[7:0]	F5h
	8EF6h	DM_Color_A246[7:0]	F6h
	8EF7h	DM_Color_A247[7:0]	F7h
	8EF8h	DM_Color_A248[7:0]	F8h

	8EF9h	DM_Color_A249[7:0]	F9h
	8EFAh	DM_Color_A250[7:0]	FAh
	8EFBh	DM_Color_A251[7:0]	FBh
	8EFCh	DM_Color_A252[7:0]	FCh
	8EFDh	DM_Color_A253[7:0]	FDh
	8EFEh	DM_Color_A254[7:0]	FEh
	8EFFh	DM_Color_A255[7:0]	FFh
Description		This command is used to set digital clock minute color.	
Restriction		-	

DCCOLOR: Digital clock colon color setting (8F00h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>8Fh</td><td>8F00h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>DC_CHOOSE</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to set digital clock colon color.
DC_CHOOSE: Digital clock colon color setting.
<table>
<tr><th>DC_CHOOSE</th><th>Digital clock colon color setting</th></tr>
<tr><td>0</td><td>reference to digital clock Hour color setting (8700h~8AFFh)</td></tr>
<tr><td>1</td><td>reference to digital clock Minute color setting (8B00h~8EFFh)</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

DCLKHC: Digital clock location setting (9000h-9002h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="3">90h</td><td>9000h</td><td>-</td><td>-</td><td>-</td><td>DClockC[8]</td><td>-</td><td>-</td><td colspan="2">DClockR[9:8]</td><td>00h</td></tr>
<tr><td>9001h</td><td colspan="8">DClockR[7:0]</td><td>D7h</td></tr>
<tr><td>9002h</td><td colspan="8">DClockC[7:0]</td><td>A7h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to set digital clock location.
DClockR[9:0]: Digital Clock Location Row Settings.
DClockC[8:0]: Digital Clock Location column Settings.
<table>
<tr><th>DClockR[9:0]</th><th>Row</th><th>DClockC[8:0]</th><th>Column</th></tr>
<tr><td>000h~002h</td><td>reserve</td><td>000h~002h</td><td>reserve</td></tr>
<tr><td>003h</td><td>4nd line</td><td>003h</td><td>4nd column</td></tr>
<tr><td>004h</td><td>5rd line</td><td>004h</td><td>5rd column</td></tr>
<tr><td>……</td><td>……</td><td>……</td><td>……</td></tr>
<tr><td>0D7h</td><td>216th line</td><td>0A7h</td><td>168th column</td></tr>
<tr><td>……</td><td>……</td><td>……</td><td>……</td></tr>
<tr><td>2CEh</td><td>719th line</td><td>1DEh</td><td>479th column</td></tr>
<tr><td>2CFh~3FFh</td><td>720 line</td><td>1DFh~1FFh</td><td>480th column</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

DCLKOCS: Digital clock offset coordinate setting (9100h-910Ch)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
91h	9100h	DClockY4[9:8]		DClockY3[9:8]		DClockY2[9:8]		DClockY1[9:8]		00h
	9101h	-	-	-	-	-	-	DClockY5[9:8]		00h
	9102h	-	-	-	DClockX 5[8]	DClockX 4[8]	DClockX 3[8]	DClockX 2[8]	DClockX 1[8]	00h
	9103h	DClockY1[7:0]								00h
	9104h	DClockX1[7:0]								00h
	9105h	DClockY2[7:0]								00h
	9106h	DClockX2[7:0]								19h
	9107h	DClockY3[7:0]								00h
	9108h	DClockX3[7:0]								31h
	9109h	DClockY4[7:0]								00h
	910Ah	DClockX4[7:0]								3Dh
	910Bh	DClockY5[7:0]								00h
	910Ch	DClockX5[7:0]								55h

Description

This command is used to set digital clock coordinate.
DClockYn[9:0]: Digital Clock coordinate Row offset Settings.
DClockXn[8:0]: Digital Clock coordinate columnoffset Settings.

DClockYn[9:0]	Row offset	DClockXn[8:0]	Column offset
00h	R+0 line	00h	C+0 column
01h	R+1 line	01h	C+1 column
02h	R+2 line	02h	C+2 column
……	……	……	……
30h	R+48 line	19h	C+25 column
……	……	……	……
2CFh	R+719 line	1DFh	C+479 column
2D0h~3FFh	R+720 line	1E0h~1FFh	C+480 column

Restriction: -

ACLKSET: Analog clock setting (9200h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>92h</td><td>9200h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>ACLKSQ_EN</td><td>ACLKSEC_EN</td><td>ACLKMIN_EN</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to set analog clock mode.
ACLKMIN_EN: Analog clock minute hand enable.
<table>
<tr><th>ACLKMIN_EN</th><th>Analog clock minute hand enable</th></tr>
<tr><td>0</td><td>Minute hand Disable</td></tr>
<tr><td>1</td><td>Minute hand Enable</td></tr>
</table>
ACLKSEC_EN: Analog clock second hand enable.
<table>
<tr><th>ACLKSEC_EN</th><th>Analog clock second hand enable</th></tr>
<tr><td>0</td><td>Second hand Disable</td></tr>
<tr><td>1</td><td>Second hand Enable</td></tr>
</table>
ACLKSQ_EN: Analog clock center square enable.
<table>
<tr><th>ACLKSQ_EN</th><th>Analog clock center square enable</th></tr>
<tr><td>0</td><td>Center square Disable</td></tr>
<tr><td>1</td><td>Center square Enable</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

ACLKRCC: Analog clock rotate center coordinate setting (9300h~9303h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="4">93h</td><td>9300h</td><td colspan="8">MINUTE_ROTATE_R[7:0]</td><td>EFh</td></tr>
<tr><td>9301h</td><td>-</td><td>-</td><td colspan="6">MINUTE_ROTATE_C[5:0]</td><td>13h</td></tr>
<tr><td>9302h</td><td colspan="8">SECOND_ROTATE_R[7:0]</td><td>EFh</td></tr>
<tr><td>9303h</td><td>-</td><td>-</td><td>-</td><td colspan="5">SECOND_ROTATE_C[4:0]</td><td>09h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">
This command is used to set analog clock rotate center coordinate.
MINUTE_ROTATE_R[7:0]: Minute hand rotate center coordinate row Settings.
MINUTE_ROTATE_C[5:0]: Minute hand rotate center coordinate column Settings.
<table>
<tr><th>MINUTE_ROTATE_R[7:0]</th><th>Row</th><th>MINUTE_ROTATE_C[5:0]</th><th>Column</th></tr>
<tr><td>00h</td><td>1st line</td><td>00h</td><td>1st column</td></tr>
<tr><td>01h</td><td>2nd line</td><td>01h</td><td>2nd column</td></tr>
<tr><td>02h</td><td>3rd line</td><td>02h</td><td>3rd column</td></tr>
<tr><td>……</td><td>……</td><td>……</td><td>……</td></tr>
<tr><td>D7h</td><td>216th line</td><td>13h</td><td>20th column</td></tr>
<tr><td>……</td><td>……</td><td>……</td><td>……</td></tr>
<tr><td>EEh</td><td>239th line</td><td>26h</td><td>39th column</td></tr>
<tr><td>EFh~FFh</td><td>240th line</td><td>27h~3Fh</td><td>40th column</td></tr>
</table>
SECOND_ROTATE_R[7:0]: Second hand rotate center coordinate row Settings.
SECOND_ROTATE_C[4:0]: Second hand rotate center coordinate column Settings.
<table>
<tr><th>SECOND_ROTATE_R[7:0]</th><th>Row</th><th>SECOND_ROTATE_C[4:0]</th><th>Column</th></tr>
<tr><td>00h</td><td>1st line</td><td>00h</td><td>1st column</td></tr>
<tr><td>01h</td><td>2nd line</td><td>01h</td><td>2nd column</td></tr>
<tr><td>02h</td><td>3rd line</td><td>02h</td><td>3rd column</td></tr>
<tr><td>……</td><td>……</td><td>……</td><td>……</td></tr>
<tr><td>D7h</td><td>216th line</td><td>09h</td><td>10th column</td></tr>
<tr><td>……</td><td>……</td><td>……</td><td>……</td></tr>
<tr><td>EEh</td><td>239th line</td><td>12h</td><td>19th column</td></tr>
<tr><td>EFh~FFh</td><td>240th line</td><td>13h~1Fh</td><td>20th column</td></tr>
</table>
</td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

ACLKCLS: Analog clock Center location setting (9400h~9402h)

<table>
<tr><th colspan="2">Address</th><th colspan="8">Parameter</th><th rowspan="2">Default Value</th></tr>
<tr><th>MIPI</th><th>Others</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="3">94h</td><td>9400h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>AClockR[8]</td><td>00h</td></tr>
<tr><td>9401h</td><td colspan="8">AClockR[7:0]</td><td>E2h</td></tr>
<tr><td>9402h</td><td colspan="8">AClockC[7:0]</td><td>E2h</td></tr>
<tr><td colspan="2">Description</td><td colspan="9">This command is used to set analog clock center location for center square.
AClockR[8:0]: Analog Clock center location Row Settings.
AClockC[7:0]: Analog Clock center location column Settings.
<table>
<tr><th>AClockR[8:0]</th><th>Row</th><th>AClockC[7:0]</th><th>Column</th></tr>
<tr><td>000h</td><td>1st line</td><td>000h</td><td>1st column</td></tr>
<tr><td>001h</td><td>2nd line</td><td>001h</td><td>2nd column</td></tr>
<tr><td>002h</td><td>3rd line</td><td>002h</td><td>3rd column</td></tr>
<tr><td>……</td><td>……</td><td>……</td><td>……</td></tr>
<tr><td>0E2h</td><td>227th line</td><td>E2h</td><td>227th column</td></tr>
<tr><td>……</td><td>……</td><td>……</td><td>……</td></tr>
<tr><td>166h</td><td>359th line</td><td>EEh</td><td>239th column</td></tr>
<tr><td>167h~1FFh</td><td>360th line</td><td>EFh~FFh</td><td>240th column</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="9">-</td></tr>
</table>

DEBURNSET: AOD De-burn-in setting (9500h~9503h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
95h	9500h	-	-	-	DE_BURN_EN	-	-	SP_AOD		10h
	9501h	-	DE_BURNSMS			-	DE_BURNSMP			10h
	9502h	-	SP_X							44h
	9503h	-	SP_Y							46h

Description

This command is used to set AOD de-burn-in function.
DE_BURN_EN: De-burn-in enable.

DE_BURN_EN	De-burn-in enable when AOD_EN send
0	De-burn-in Disable
1	De-burn-in Enable

SP_AOD: De-burn-in start point setting when normal display mode into AOD mode.

SP_AOD[1:0]	De-burn-in start point setting
00	Start from center then to pre-AOD next step
01	Start from pre-AOD next step
10	Start from pre-AOD next 2-step
11	Start from pre-AOD next 3-step

DE_BURNSMP: De-burn-in self-move period.

DE_BURNSMP[2:0]	De-burn-in self-move period
000	1 min
001	2 min
010	3 min
011	4 min
100	Reserved
101	Reserved
110~111	1 min

DE_BURNSMS: De-burn-in self-move step.

DE_BURNSMS[2:0]	De-burn-in self-move step
000	1 pixel
001	2 pixel
010	3 pixel
…	…l
110	7 pixel
111	8 pixel

SP_X: De-burn-in X-axis start point setting when DDIC has been reset and into AOD mode.

SP_X [6:0]	De-burn-in Start Point
000-0000	+0 pixel
000-0001	+1 pixel
000-0010	+2 pixel
...	...

	011-1111 | +63 pixel 100-0000 | -0 pixel 100-0001 | -1 pixel 100-0010 | -2 pixel ... | ... 111-1111 | -63 pixel Note: +X < HBP ; -X < HFP SP_Y: De-burn-in Y-axis start point setting when DDIC has been reset and into AOD mode. SP_Y [6:0] | De-burn-in Start Point 000-0000 | +0 line 000-0001 | +1 line 000-0010 | +2 line ... | ... 011-1111 | +63 line 100-0000 | -0 line 100-0001 | -1 line 100-0010 | -2 line ... | ... 111-1111 | -63 line Note:+Y < VBP ; -Y < VFP
Restriction	-

DEBURNDIR_LSB: AOD De-burn-in direction of each step setting (9600h~960Fh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
96h	9600h	X2Dir[1:0]		Y2Dir[1:0]		X1Dir[1:0]		Y1Dir[1:0]		44h
	9601h	X4Dir[1:0]		Y4Dir[1:0]		X3Dir[1:0]		Y3Dir[1:0]		44h
	9602h	X6Dir[1:0]		Y6Dir[1:0]		X5Dir[1:0]		Y5Dir[1:0]		85h
	9603h	X8Dir[1:0]		Y8Dir[1:0]		X7Dir[1:0]		Y7Dir[1:0]		88h
	9604h	X10Dir[1:0]		Y10Dir[1:0]		X9Dir[1:0]		Y9Dir[1:0]		88h
	9605h	X12Dir[1:0]		Y12Dir[1:0]		X11Dir[1:0]		Y11Dir[1:0]		18h
	9606h	X14Dir[1:0]		Y14Dir[1:0]		X13Dir[1:0]		Y13Dir[1:0]		44h
	9607h	X16Dir[1:0]		Y16Dir[1:0]		X15Dir[1:0]		Y15Dir[1:0]		44h
	9608h	X18Dir[1:0]		Y18Dir[1:0]		X17Dir[1:0]		Y17Dir[1:0]		44h
	9609h	X20Dir[1:0]		Y20Dir[1:0]		X19Dir[1:0]		Y19Dir[1:0]		81h
	960Ah	X22Dir[1:0]		Y22Dir[1:0]		X21Dir[1:0]		Y21Dir[1:0]		88h
	960Bh	X24Dir[1:0]		Y24Dir[1:0]		X23Dir[1:0]		Y23Dir[1:0]		88h
	960Ch	X26Dir[1:0]		Y26Dir[1:0]		X25Dir[1:0]		Y25Dir[1:0]		18h
	960Dh	X28Dir[1:0]		Y28Dir[1:0]		X27Dir[1:0]		Y27Dir[1:0]		44h
	960Eh	X30Dir[1:0]		Y30Dir[1:0]		X29Dir[1:0]		Y29Dir[1:0]		44h
	960Fh	X32Dir[1:0]		Y32Dir[1:0]		X31Dir[1:0]		Y31Dir[1:0]		44h

Description

This command is used to set AOD de-burn-in ditection of each step setting.
XnDir: X-axis direction of each step.

XnDir[1:0]	the direction of each step setting
00	Without moving (--)
01	Right moving (→)
10	Left moving (←)
11	When YnDir[1:0] = 11 Back to start point When YnDir[1:0] ≠ 11 without moving

YnDir: Y-axis direction of each step.

YnDir[1:0]	the direction of each step setting
00	without moving (--)
01	Up moving (↑)
10	Down moving (↓)
11	When XnDir[1:0] = 11 Back to start point When XnDir[1:0] ≠ 11 without moving

Restriction

-

DEBURNDIR_MSB: AOD De-burn-in direction of each step setting (9700h~970Fh)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
97h	9700h	X34Dir[1:0]		Y34Dir[1:0]		X33Dir[1:0]		Y33Dir[1:0]		81h
	9701h	X36Dir[1:0]		Y36Dir[1:0]		X35Dir[1:0]		Y35Dir[1:0]		88h
	9702h	X38Dir[1:0]		Y38Dir[1:0]		X37Dir[1:0]		Y37Dir[1:0]		88h
	9703h	X40Dir[1:0]		Y40Dir[1:0]		X39Dir[1:0]		Y39Dir[1:0]		58h
	9704h	X42Dir[1:0]		Y42Dir[1:0]		X41Dir[1:0]		Y41Dir[1:0]		44h
	9705h	X44Dir[1:0]		Y44Dir[1:0]		X43Dir[1:0]		Y43Dir[1:0]		44h
	9706h	X46Dir[1:0]		Y46Dir[1:0]		X45Dir[1:0]		Y45Dir[1:0]		0Fh
	9707h	X48Dir[1:0]		Y48Dir[1:0]		X47Dir[1:0]		Y47Dir[1:0]		00h
	9708h	X50Dir[1:0]		Y50Dir[1:0]		X49Dir[1:0]		Y49Dir[1:0]		00h
	9709h	X52Dir[1:0]		Y52Dir[1:0]		X51Dir[1:0]		Y51Dir[1:0]		00h
	970Ah	X54Dir[1:0]		Y54Dir[1:0]		X53Dir[1:0]		Y53Dir[1:0]		00h
	970Bh	X56Dir[1:0]		Y56Dir[1:0]		X55Dir[1:0]		Y55Dir[1:0]		00h
	970Ch	X58Dir[1:0]		Y58Dir[1:0]		X57Dir[1:0]		Y57Dir[1:0]		00h
	970Dh	X60Dir[1:0]		Y60Dir[1:0]		X59Dir[1:0]		Y59Dir[1:0]		00h
	970Eh	X62Dir[1:0]		Y62Dir[1:0]		X61Dir[1:0]		Y61Dir[1:0]		00h
	970Fh	X64Dir[1:0]		Y64Dir[1:0]		X63Dir[1:0]		Y63Dir[1:0]		00h

Description

This command is used to set AOD de-burn-in ditection of each step setting.
XnDir: X-axis direction of each step.

XnDir[1:0]	the direction of each step setting
00	Without moving (--)
01	Right moving (→)
10	Left moving (←)
11	When YnDir[1:0] = 11 Back to start point When YnDir[1:0] ≠ 11 without moving

YnDir: Y-axis direction of each step.

YnDir[1:0]	the direction of each step setting
00	without moving (--)
01	Up moving (↑)
10	Down moving (↓)
11	When XnDir[1:0] = 11 Back to start point When XnDir[1:0] ≠ 11 without moving

Restriction

-

RDID1: Read ID1 Value (DA00h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
DAh	DA00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00h
Description		This read byte identifies the AMOLED module's manufacture ID.								
Restriction		-								

RDID2: Read ID2 Value (DB00h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
DBh	DB00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80h
Description		This read byte is used to track the AMOLED module/driver version. It is defined by module maker and changes each time a revision is made to the display, material or construction specifications.								
Restriction		-								

RDID3: Read ID3 Value (DC00h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
DCh	DC00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00h
Description		This read byte identifies the AMOLED module's manufacture ID.								
Restriction		-								

6 Interface

The CH13613 supports MIPI Interface and serial peripheral interfaces (SPI).
The interface type can be selected by setting IM1, IM0 pins as shown below:

Table Interface Type Selection

IM[1:0]	Display Data	Command
00	MIPI DSI / 9 bit SPI	MIPI DSI / 9 bit SPI
01	MIPI DSI / 8 bit SPI	MIPI DSI / 8 bit SPI
10	MIPI DSI / Quad-SPI	MIPI DSI / Quad-SPI
11	MIPI DSI	MIPI DSI / 16 bit rising SPI

6.1 Serial Interface connect with Host

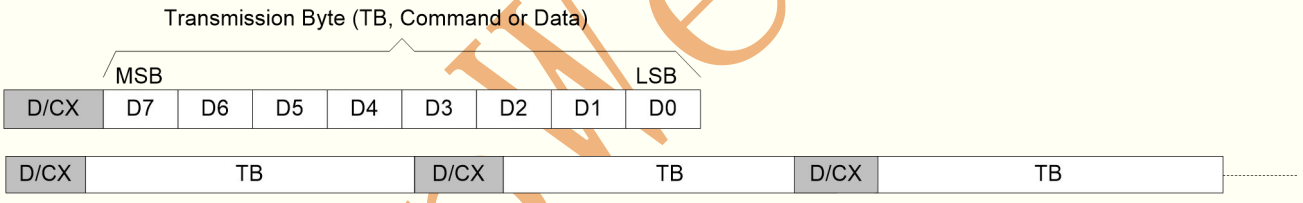
6.1.1 8/9 bit Serial Interface

The 8-bit SPI (4-pin) use CSB (chip select), DCX (data/command select), SCL (serial clock) and SDI/SDO (serial data input/output).
The 9-bit SPI (3-pin) use CSB, SCL and SDI/SDO. SCL is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

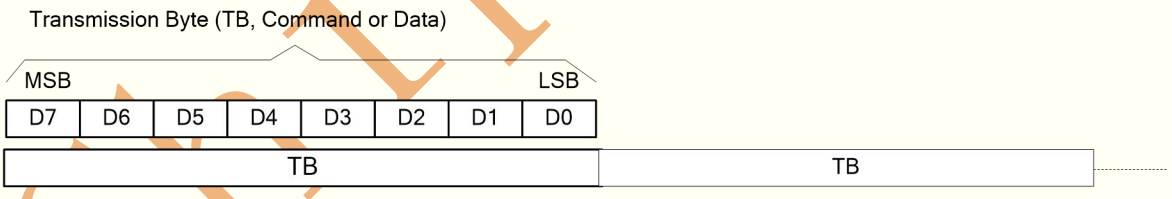
Write Mode

The write mode of the interface means the micro controller writes commands and data to the CH13613. 9-bit serial data packet contains a control bit D/CX and a transmission byte, in 8-bit serial case, data packet contains just transmission byte and control bit D/CX is transferred by D/CX pin. If D/CX is low, the transmission byte is interpreted as command byte. If D/CX is high, the transmission byte is stored in command register as parameter.
The MSB is transmitted first. The serial interface is initialized when CSB is high. In this state, SCL clock pulse or SDI/SDO data have no effect. A falling edge on CSB enables the serial interface and indicates the start of data transmission.

3 wire Serial Data Stream Format

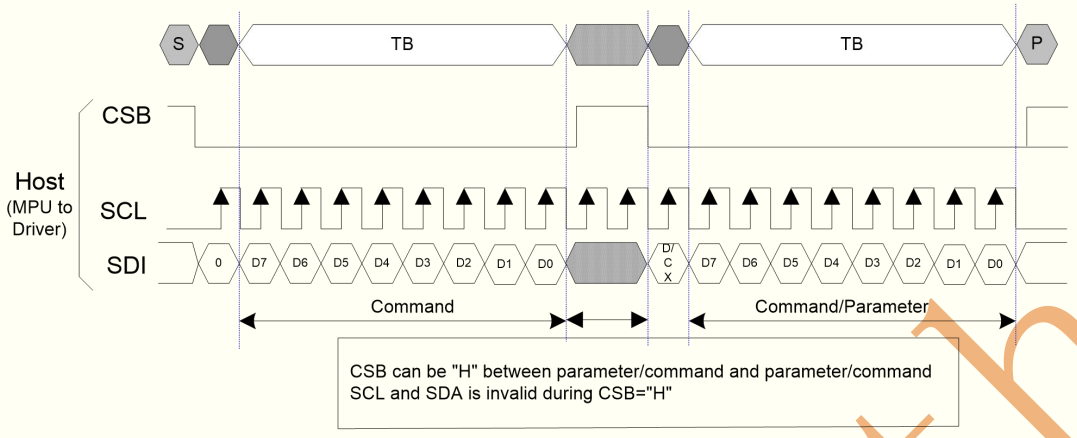


4 wire Serial Data Stream Format

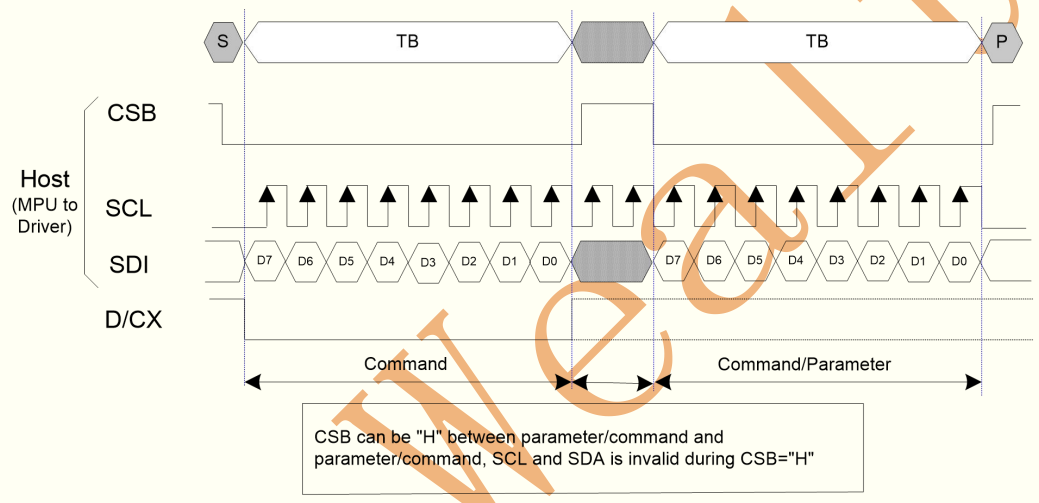


When CSB is high, SCL clock is ignored. During the high time of CSB the serial interface is initialized. At the falling CSB edge, SCL can be high or low (see below figure). SDI/SDO is sampled at the rising edge of SCL. D/CX indicates whether the byte is command code (D/CX=0) or parameter (D/CX=1). It is sampled when first rising SCL edge (3-line serial interface) or 8th rising SCLK edge (4-line serial interface). If CSB stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL.

1) 3-Pin Serial Interface Protocol for Register Write



2) 4-Pin Serial Interface Protocol for Register Write

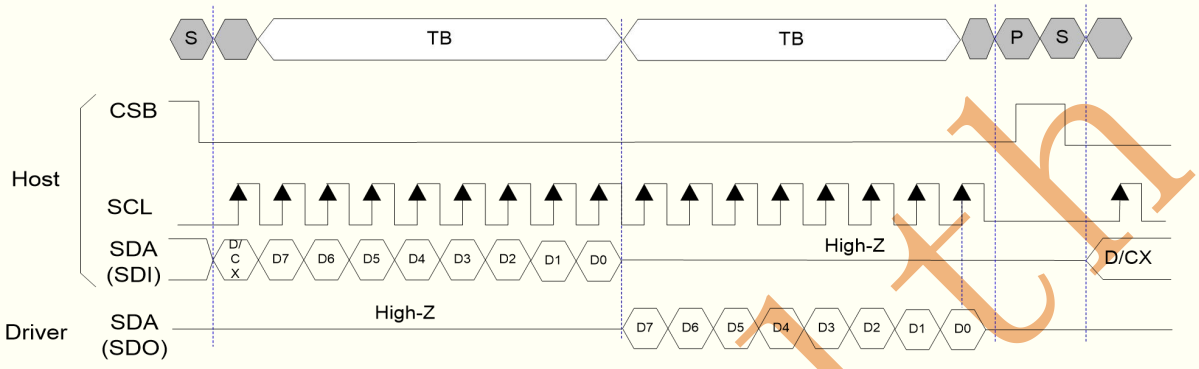


Serial bus protocol for register write mode

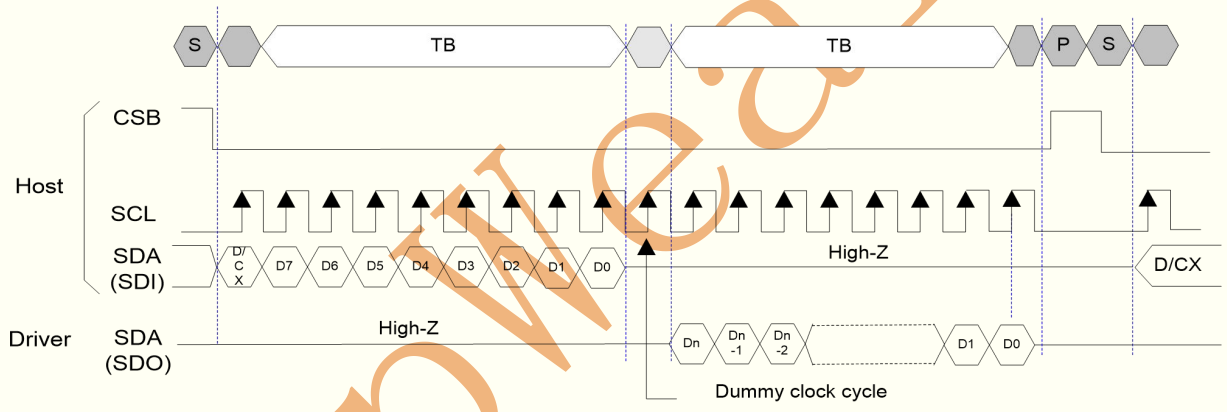
Read Mode

The read mode of the interface means that the micro controller reads register value from the CH13613. To do so the micro controller first has to send a command (Read ID or Read Register command) and then the following byte is transmitted in the opposite direction. After that CSB is required to go high before a new command is send. The CH13613 samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit.

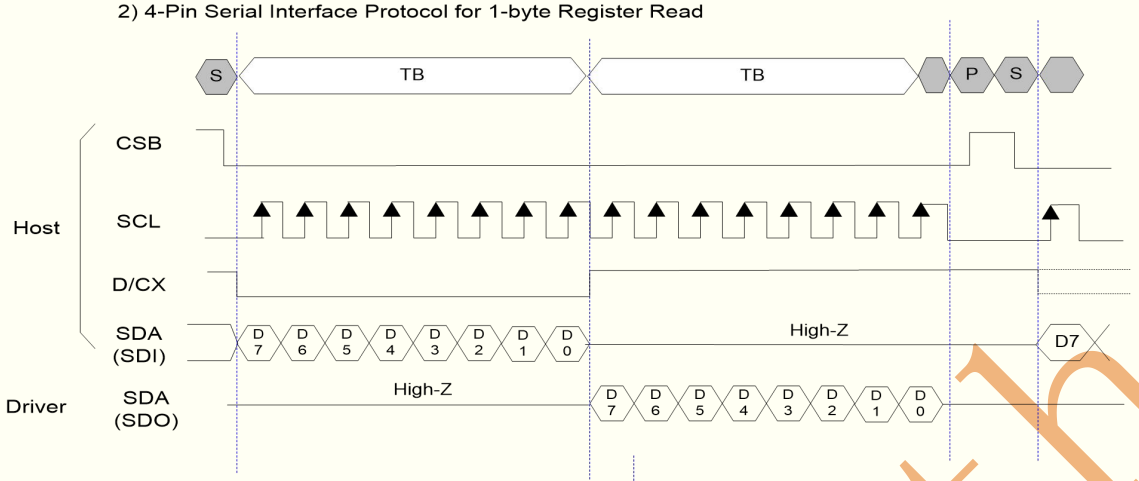
1) 3-Pin Serial Interface Protocol for 1-byte Register Read



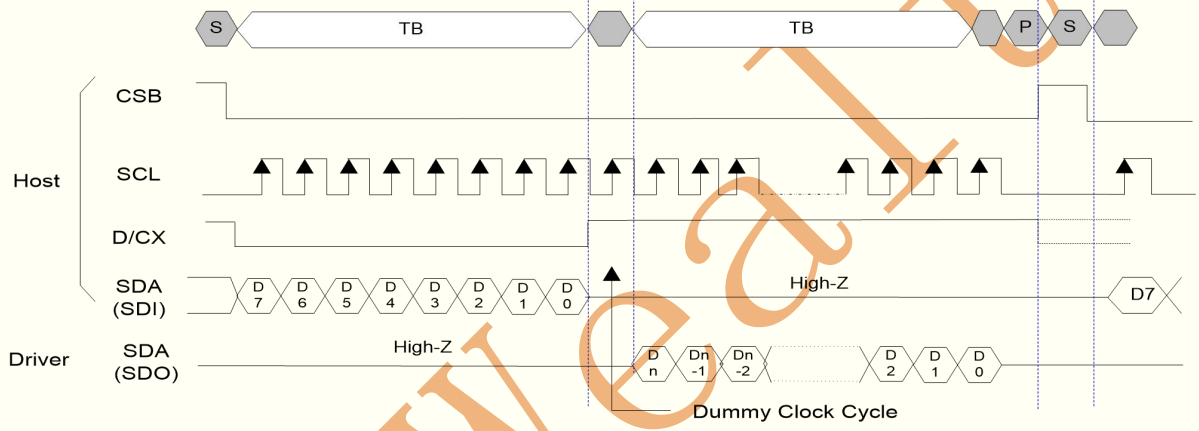
3-Pin Serial Interface Protocol for Multi-byte Register Read



2) 4-Pin Serial Interface Protocol for 1-byte Register Read



4-Pin Serial Interface Protocol for Multi-byte Register Read



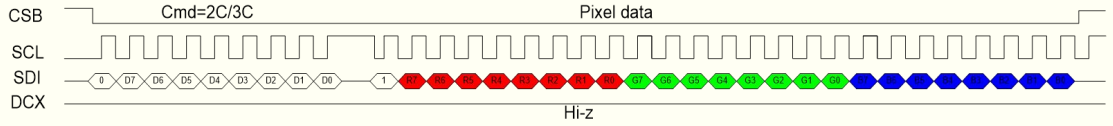
Serial bus protocol for register read mod

Dual-SPI Write RAM mode

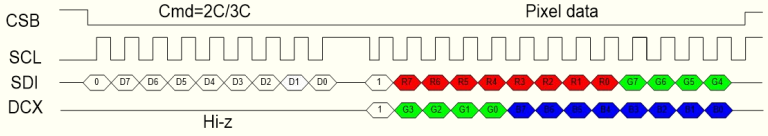
SPI_WRAM=1, Enable SPI Write RAM. DSPI_EN=1, Enable Dual-SPI interface. All 3-kinds of pixel format can be available during Dual-SPI interface (selected by the IPF command (3Ah): IFPF[2:0]).

SPI_WRAM	DSPI_EN	DSPI_CFG [1:0]	IM[1:0]	Pixel format
1	1	00:1P1T 1wire	00:9bit SPI	RGB888
				RGB666
				RGB565
			01:8bit SPI	RGB888
				RGB666
				RGB565
		01:1P1T 2wire	00:9bit SPI	RGB888
				RGB666
				RGB565
			01:8bit SPI	RGB888
				RGB666
				RGB565
		10:2P3T 2wire	00:9bit SPI	RGB888
				RGB666
			01:8bit SPI	RGB888
				RGB666
0	0	/	/	Not support write RAM

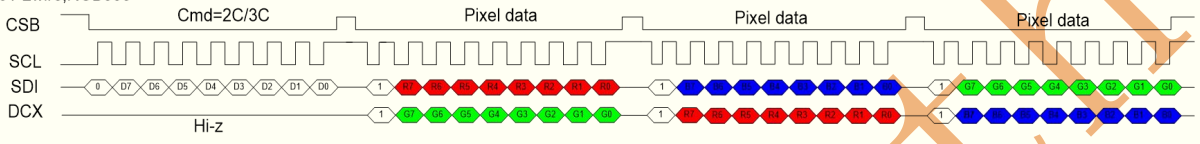
9bit-1P1T 1wire,RGB888



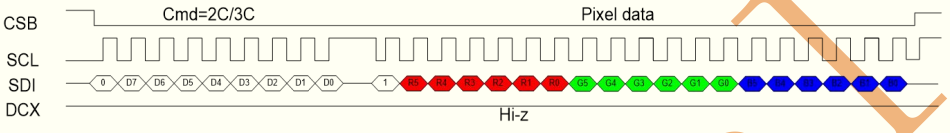
9bit-1P1T 2wire,RGB888



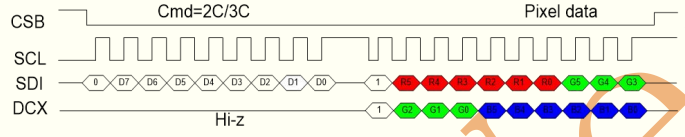
9bit-2P3T 2wire,RGB888



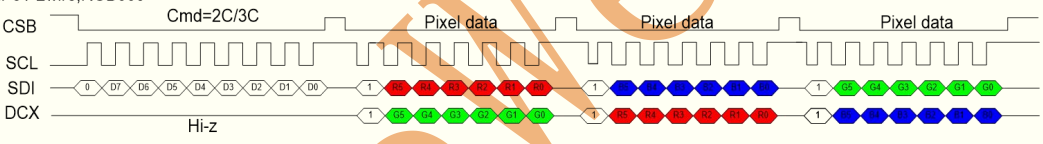
9bit-1P1T 1wire,RGB666



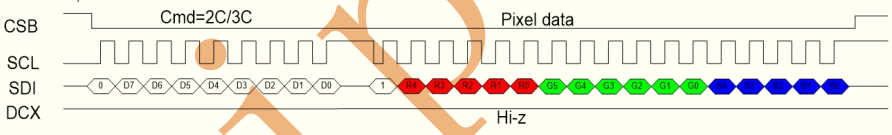
9bit-1P1T 2wire,RGB666



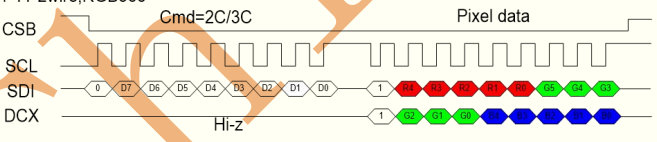
9bit-2P3T 2wire,RGB666



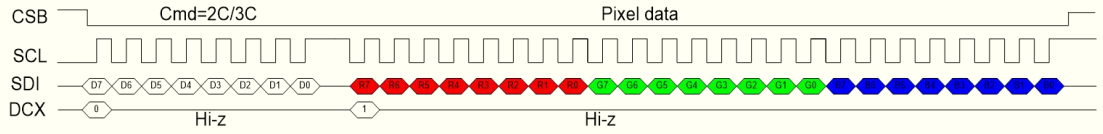
9bit-1P1T 1wire,RGB565



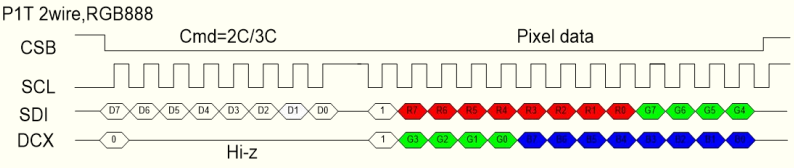
9bit-1P1T 2wire,RGB565



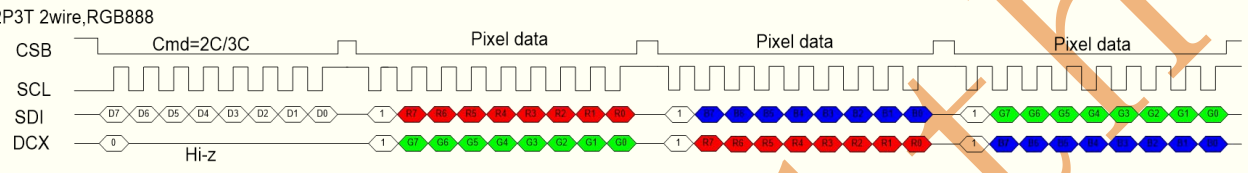
8bit-1P1T 1wire,RGB888



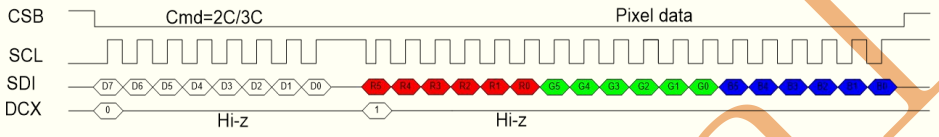
8bit-1P1T 2wire,RGB888



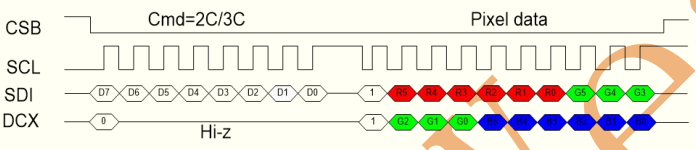
8bit-2P3T 2wire,RGB888



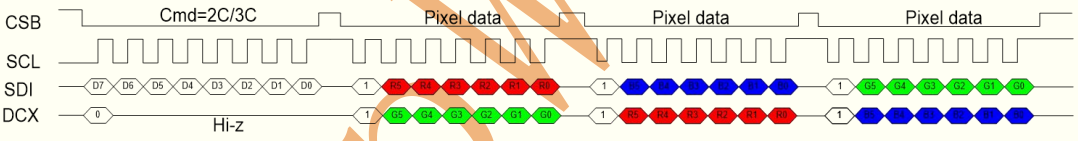
8bit-1P1T 1wire,RGB666



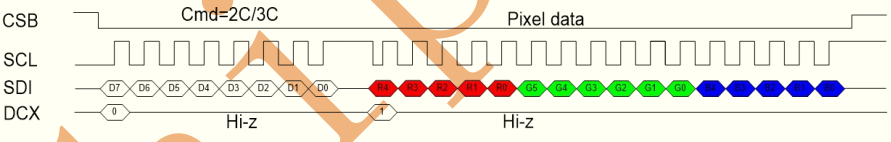
8bit-1P1T 2wire,RGB666



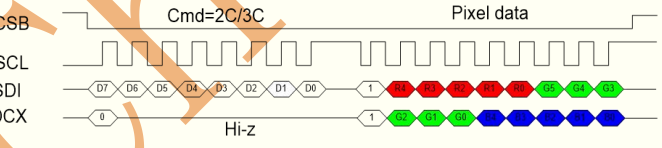
8bit-2P3T 2wire,RGB666



8bit-1P1T 1wire,RGB565



8bit-1P1T 2wire,RGB565



6.1.2 Quad-SPI Interface

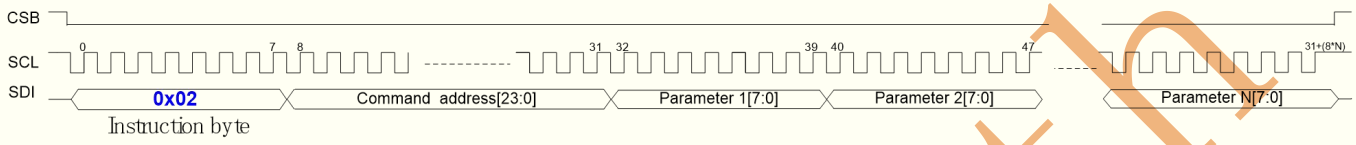
The Quad-SPI interface consists of CSB (chip select), SCL (serial clock), SDI / DCX / D0 / D1 (serial data input) and SDO (serial data output).

Quad-SPI Write mode

The write mode of the interface means the micro controller writes commands and data to the CH13613. Quad-SPI data packet contains an instruction byte. This byte specifies which type of data to be transferred.

Write Command Mode

QSPI Write Command – Instruction byte = 0x02 (Command – 1 wire / Parameter – 1 wire))

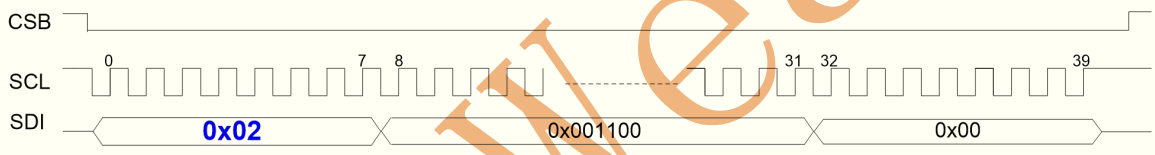


For example:

SLPOUT: Sleep Out (1100h)

Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
11h	1100h	No argument								Sleep in mode

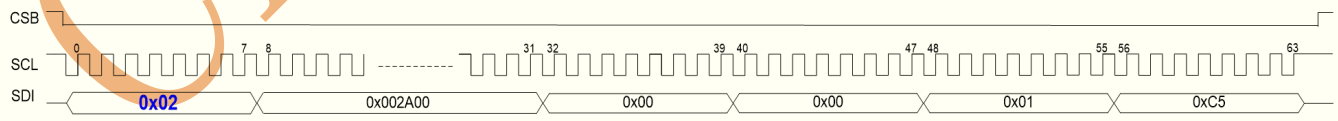
QSPI Write Command



CASET: Set Column Start Address (2A00h~2A03h)

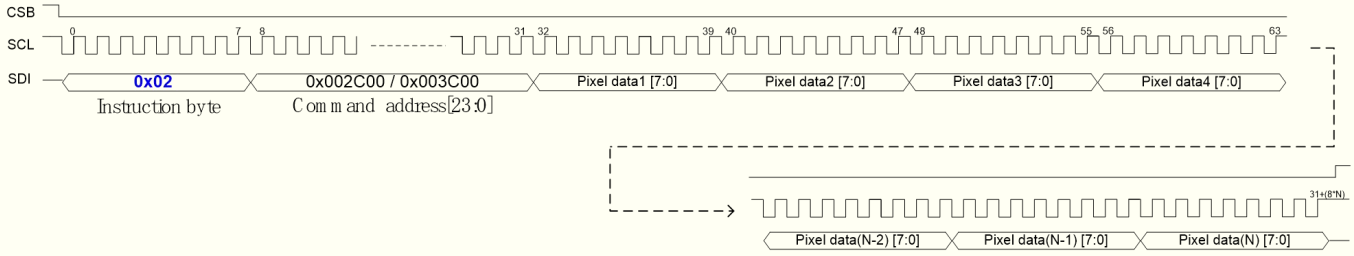
Address		Parameter								Default Value
MIPI	Others	D7	D6	D5	D4	D3	D2	D1	D0	
2Ah	2A00h	-	-	-	-	-	-	-	SC8	00h
	2A01h	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00h
	2A02h	-	-	-	-	-	-	-	EC8	01h
	2A03h	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	C5h

QSPI Write Command

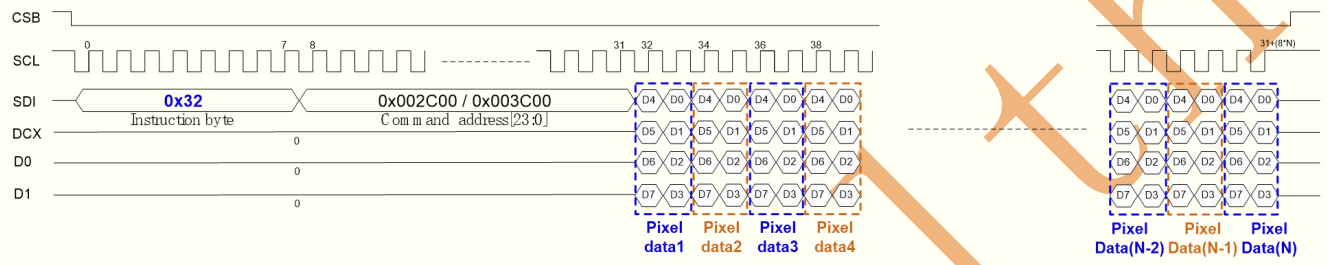


Write RAM mode

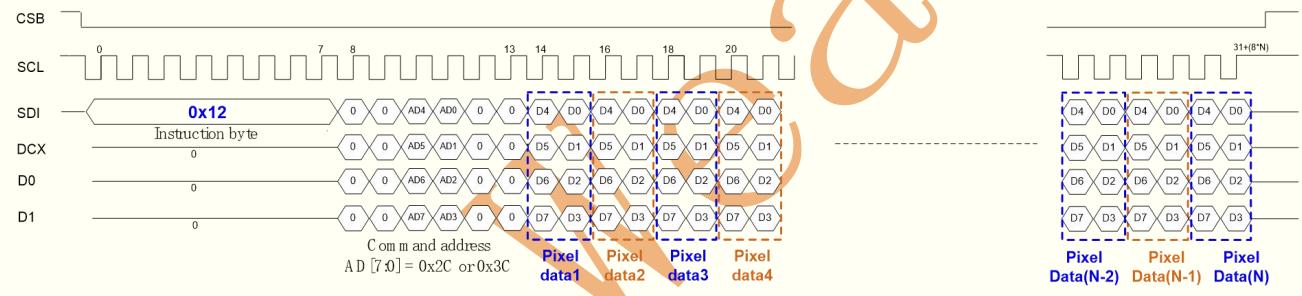
QSPI Write Ram – Instruction byte = 0x02 (Command – 1 wire / Data – 1 wire)



QSPI Write Ram – Instruction byte = 0x32 (Command – 1 wire / Data – 4 wire)



QSPI Write Ram – Instruction byte = 0x12 (Command – 4 wire / Data – 4 wire)

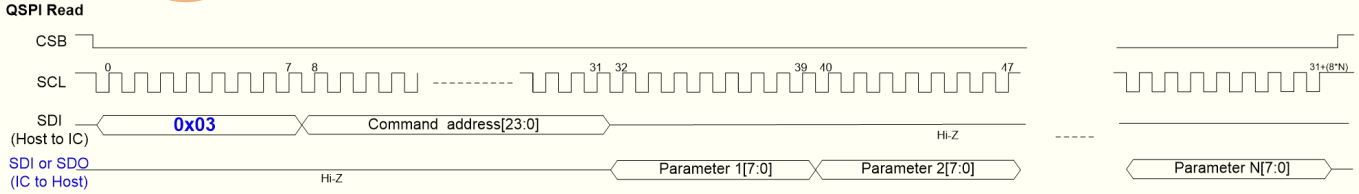


SPI_WRAM=1, Enable SPI Write RAM. IM[1:0]=10, Enable Quad-SPI interface. All 3-kinds of pixel format can be available during Quad-SPI interface (selected by the IPF command (3Ah): IFPF[2:0]).

SPI_WRAM	IM[1:0]	Pixel format
1	10: Quad-SPI	RGB888
		RGB666
		RGB565
		RGB332
		RGB111
		Gray256
0	/	Not support write RAM

Note. To avoid tearing effect, it is recommended to synchronize the TE signal when writing ram.

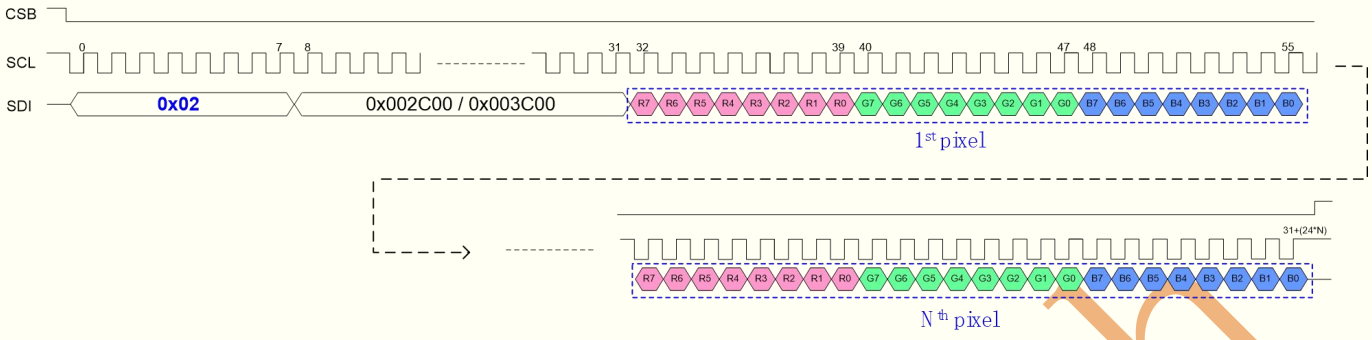
Quad-SPI Read Command/Ram – Instruction byte = 0x03



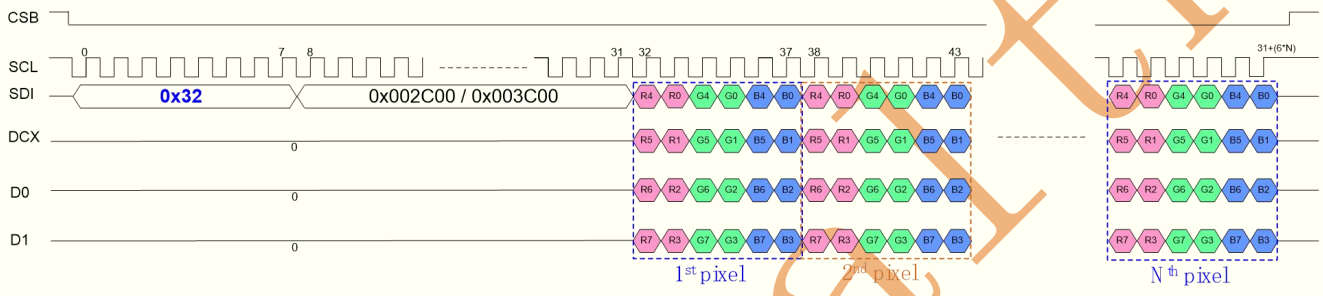
Note. The 1st read parameter is dummy packet in read ram.

Quad SPI – RGB888

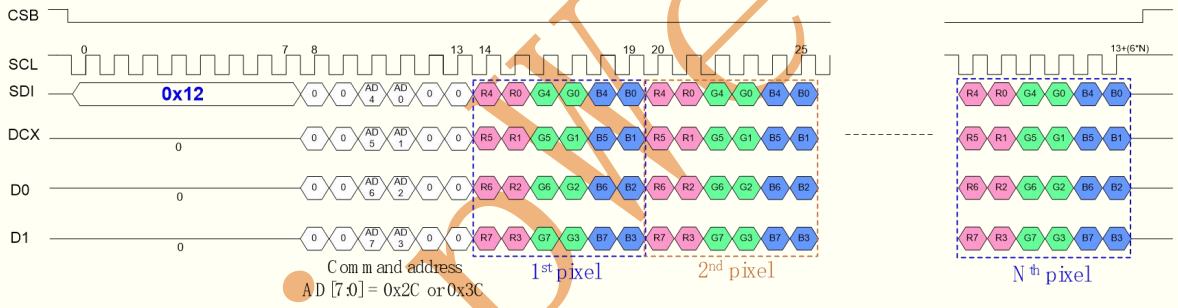
QSPI RGB888 – Instruction byte = 0x02



QSPI RGB888 – Instruction byte = 0x32

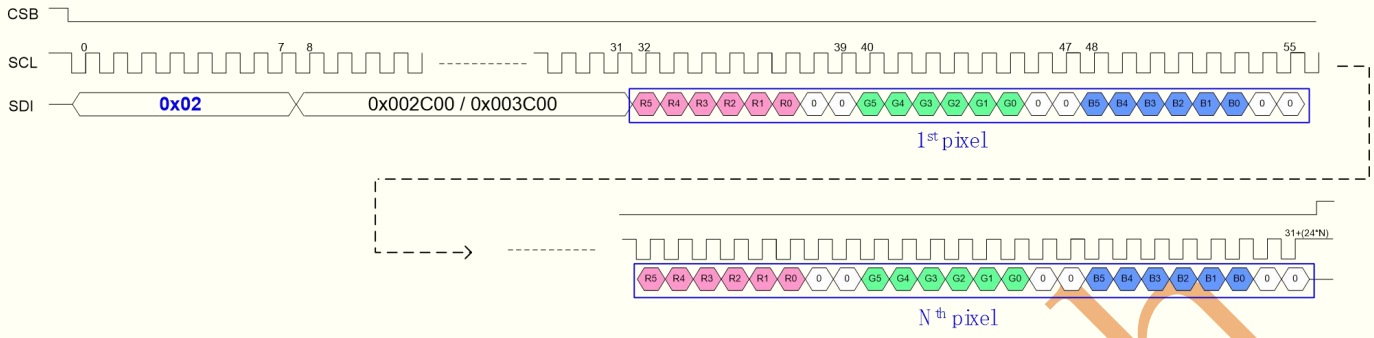


QSPI RGB888 – Instruction byte = 0x12

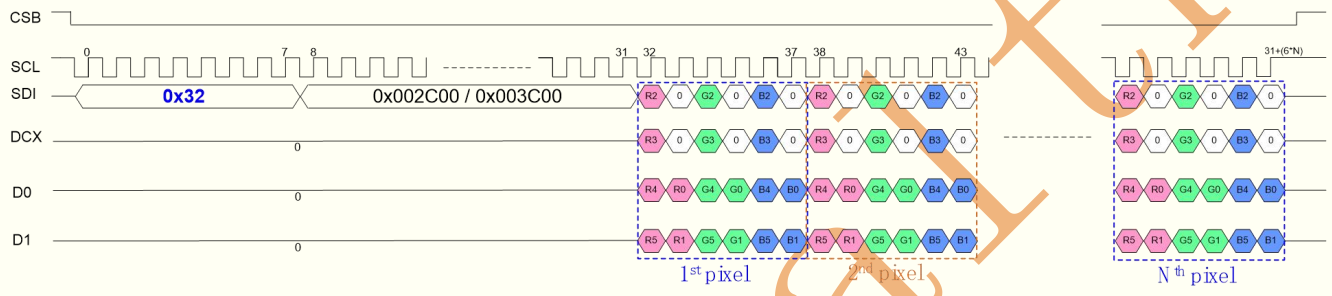


Quad SPI – RGB666

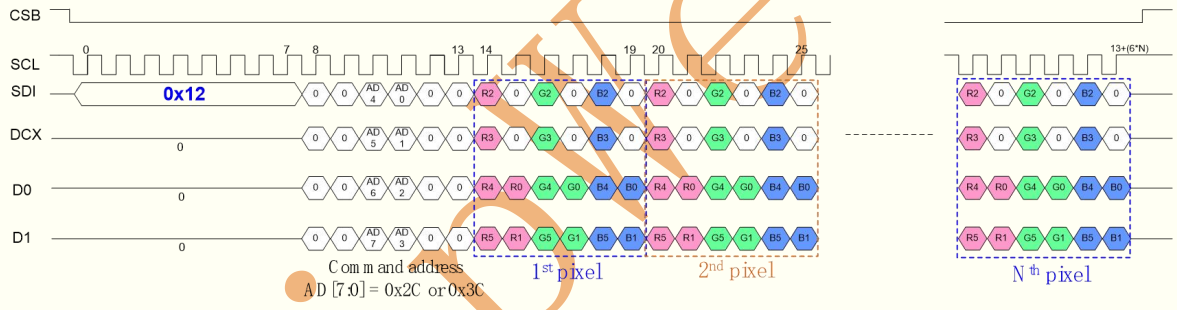
QSPI RGB666 – Instruction byte = 0x02



QSPI RGB666 – Instruction byte = 0x32

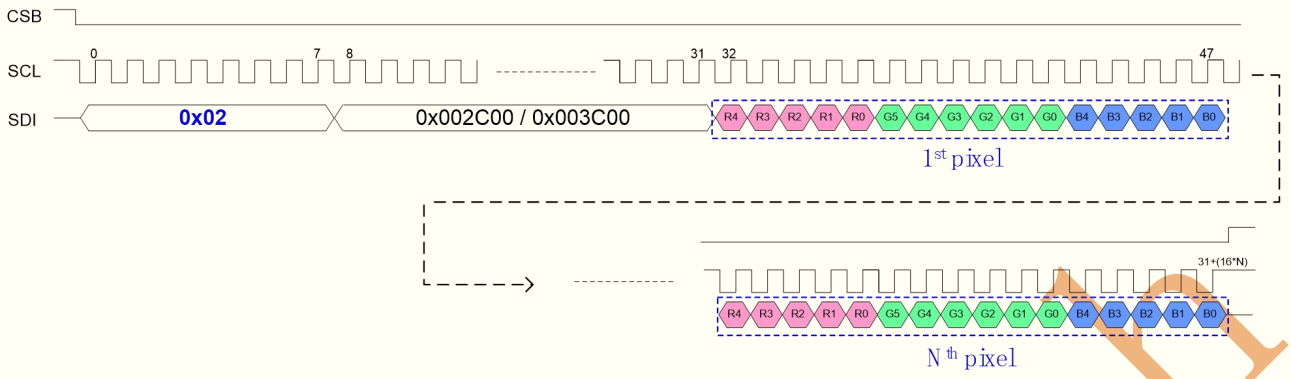


QSPI RGB666 – Instruction byte = 0x12

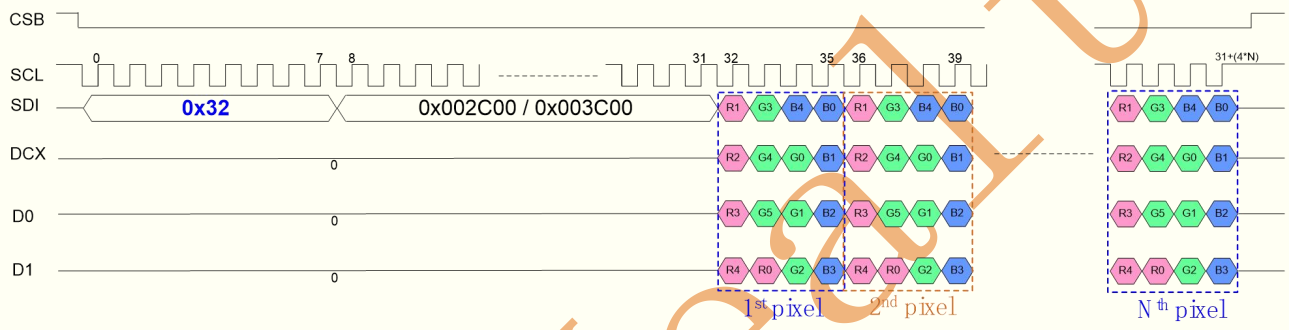


Quad SPI – RGB565

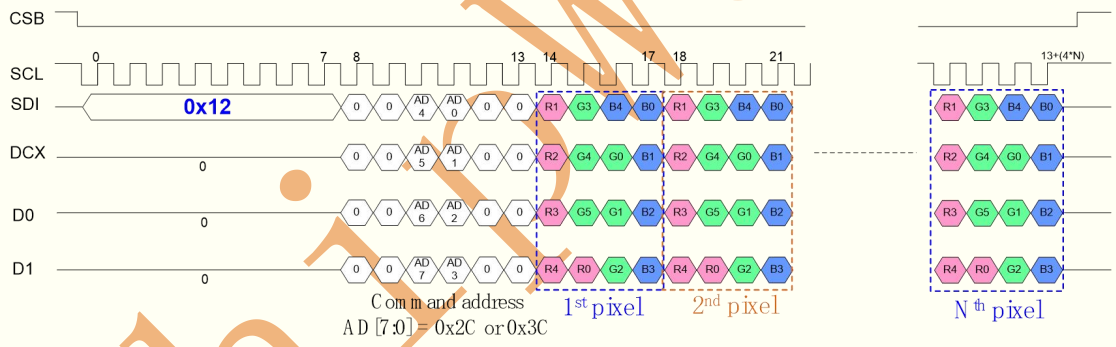
QSPI RGB565 – Instruction byte = 0x02



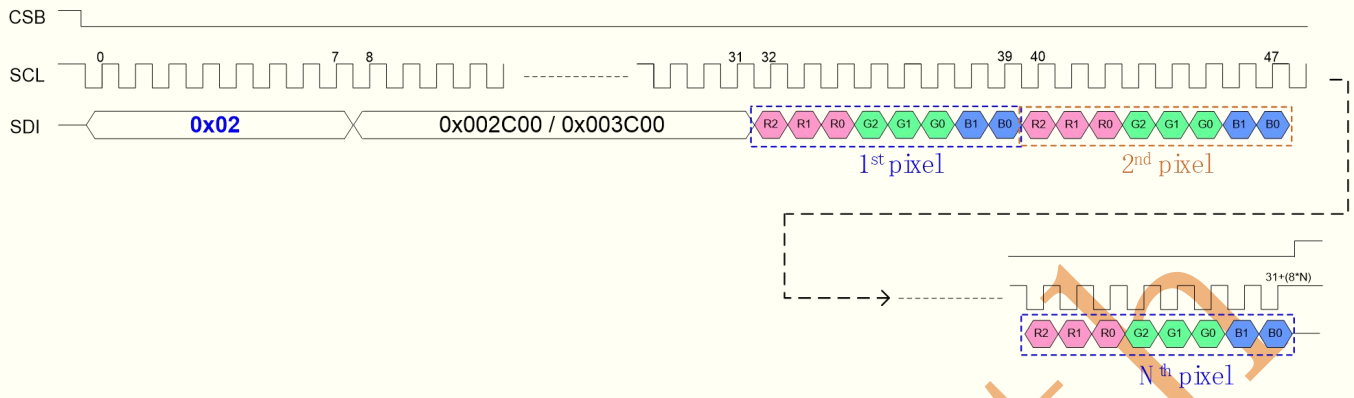
QSPI RGB565 – Instruction byte = 0x32



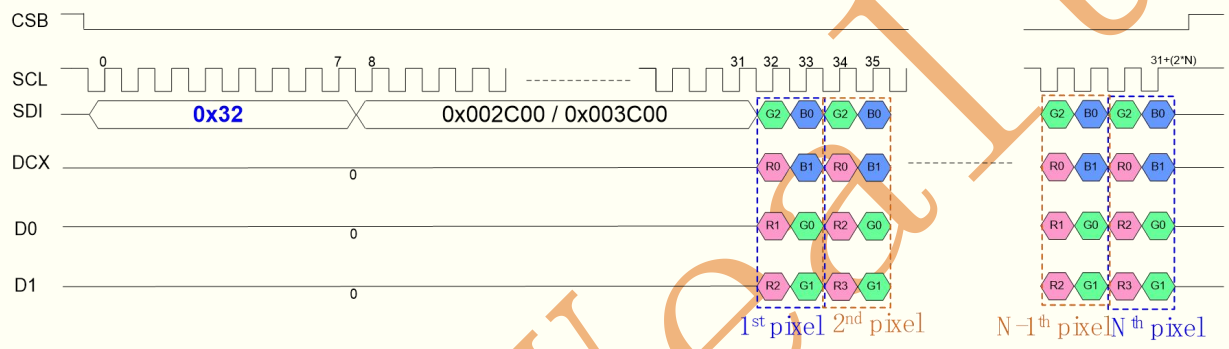
QSPI RGB565 – Instruction byte = 0x12



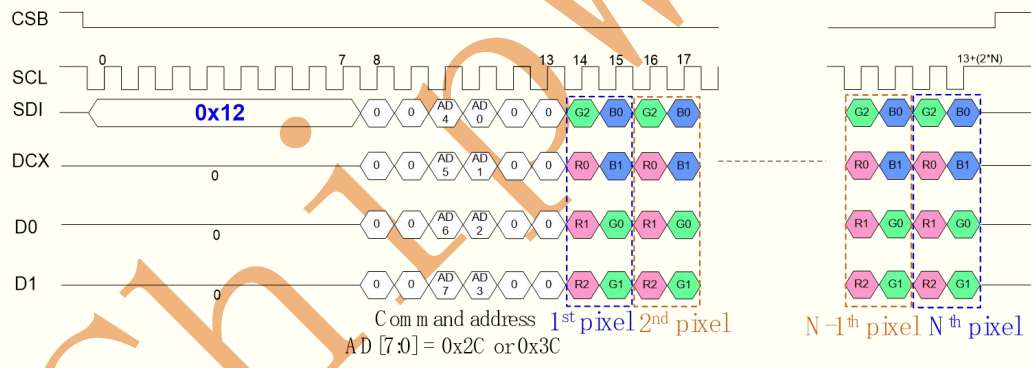
QSPI RGB332 – Instruction byte = 0x02



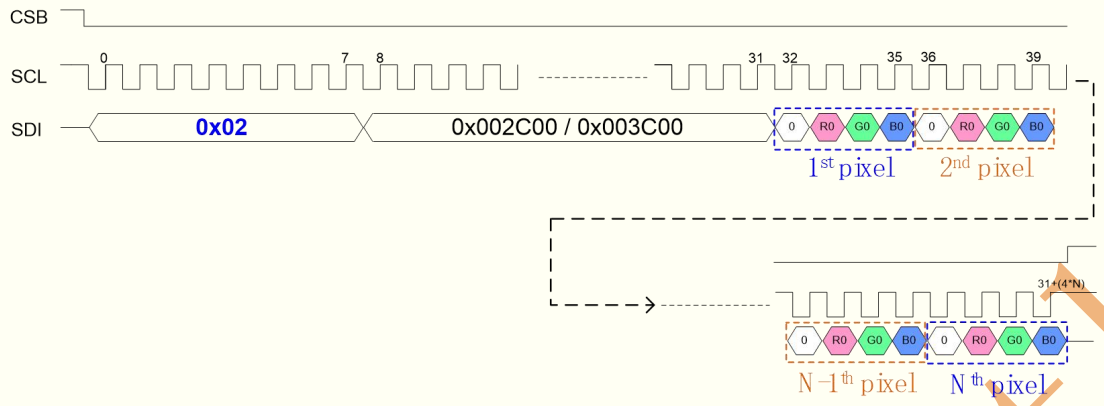
QSPI RGB332 – Instruction byte = 0x32



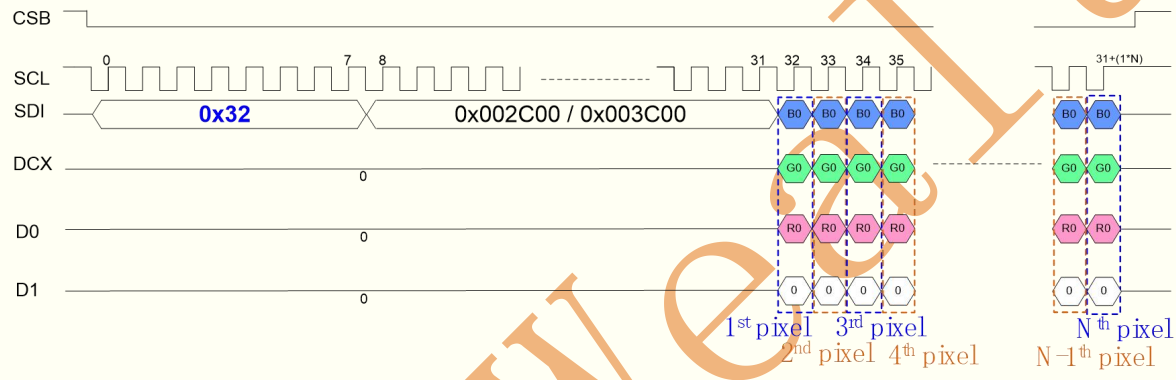
QSPI RGB332 – Instruction byte = 0x12



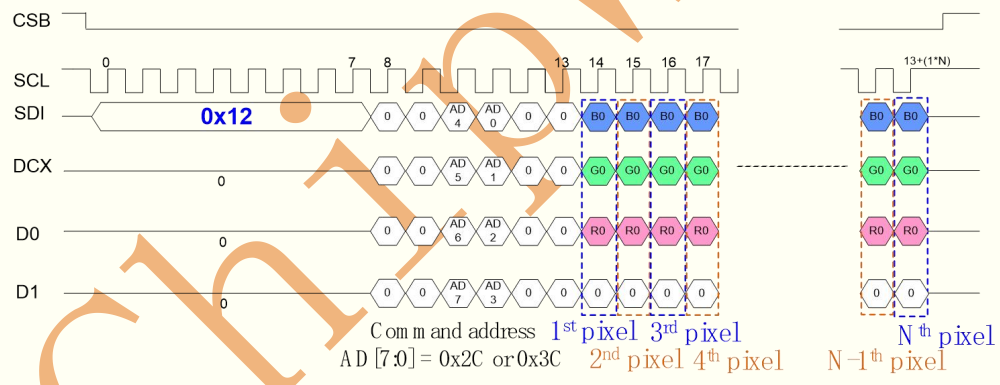
QSPI RGB111 – Instruction byte = 0x02



QSPI RGB111 – Instruction byte = 0x32

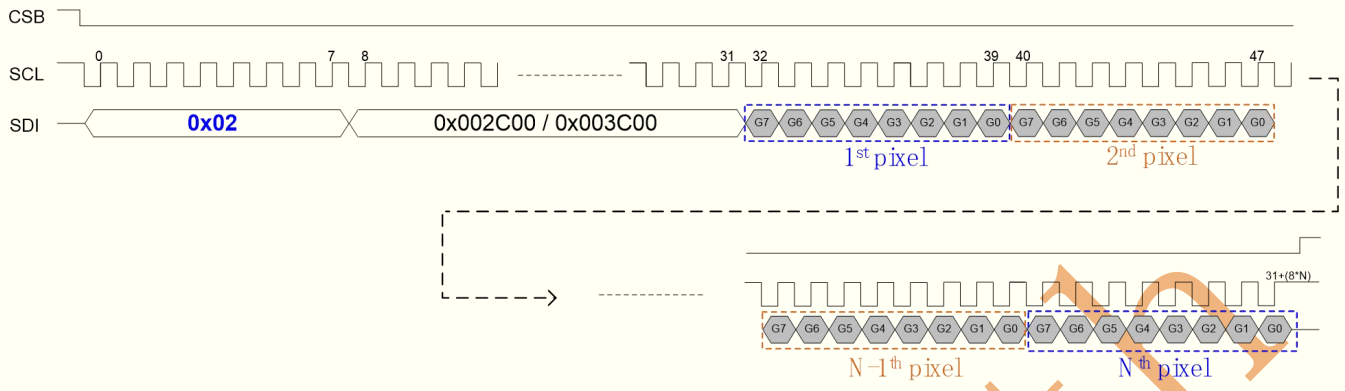


QSPI RGB111 – Instruction byte = 0x12

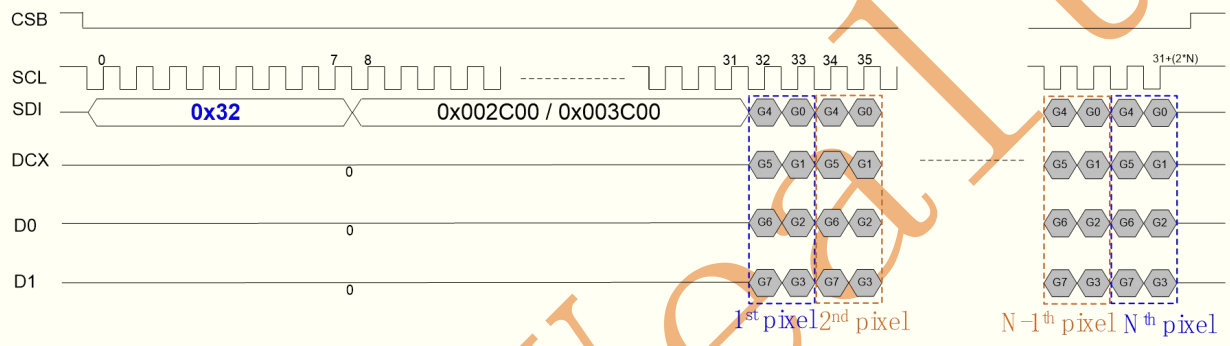


Quad SPI – Gray256

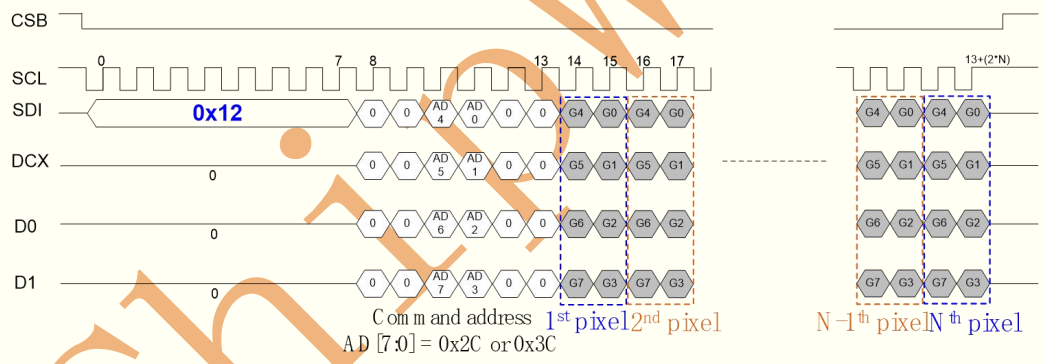
QSPI Gray256 – Instruction byte = 0x02



QSPI Gray256 – Instruction byte = 0x32

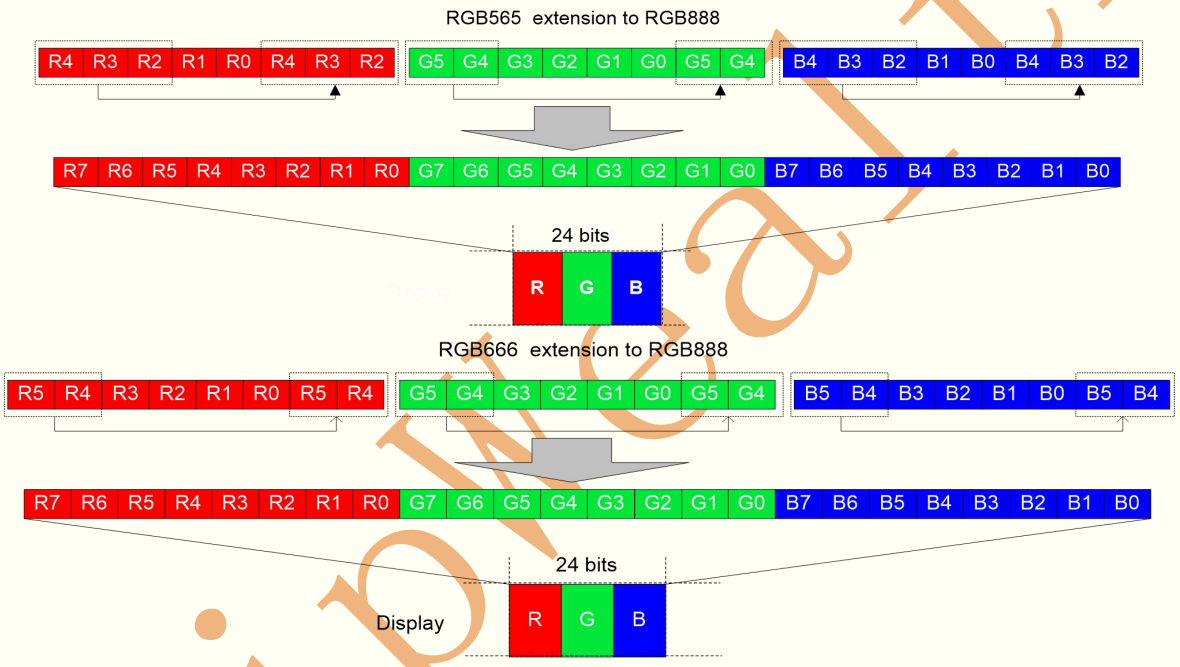


QSPI Gray256 – Instruction byte = 0x12



Quad-SPI support maximum frequency:

Quad SPI write/read		1-wire	4-wire
Write command		50 MHz	Not support
Write pixel data	RGB 888	50 MHz	50 MHz
	RGB 666	50 MHz	50 MHz
	RGB 565	50 MHz	50 MHz
	RGB 332	50 MHz	40 MHz
	RGB 111	50 MHz	20 MHz
	Gray 256	50 MHz	40 MHz
Read		10 MHz	Not support

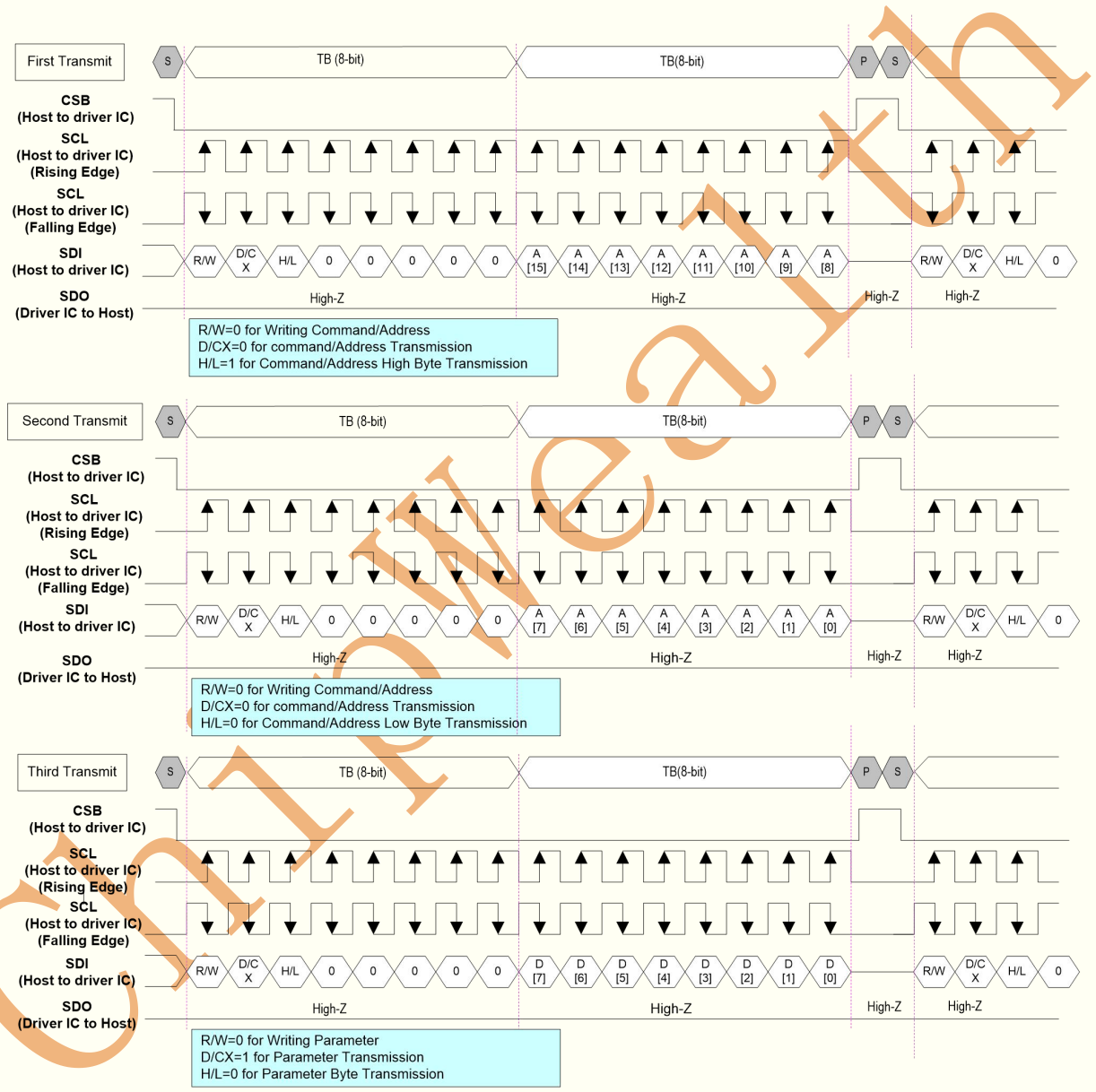


6.1.3 16 bit Serial Interface

The serial interface can select IM[1:0] to decide the trigger edge is rising edge. The serial interface is used to communication between the micro controller and the driver chip. It contains CSB (chip select), SCL (serial clock), SDI (serial data input) and SDO (serial data output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

Write Mode

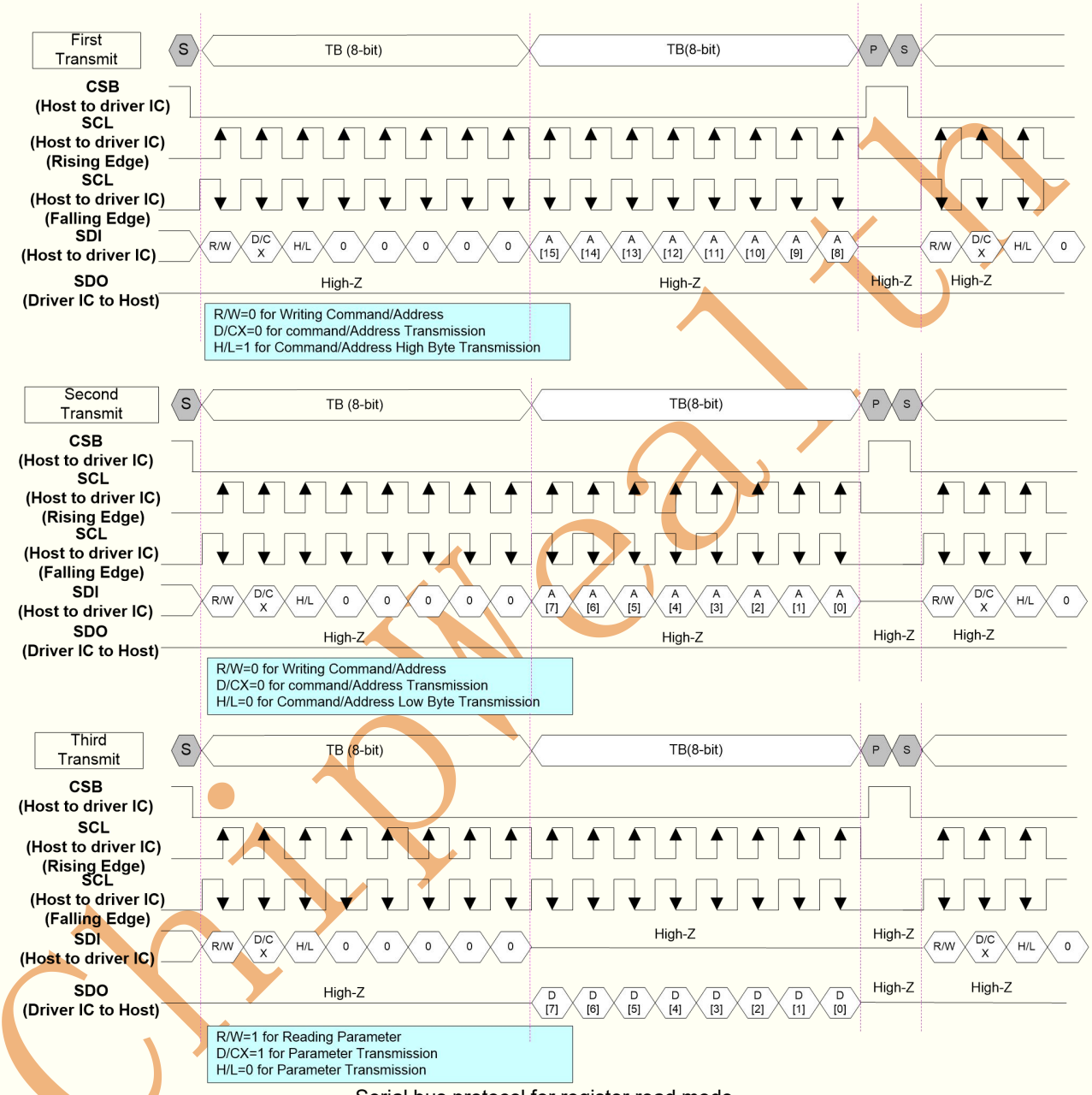
The write mode of the interface means the micro controller writes commands and data to the IC. When CSB is high, SCL clock is ignored. During the high time of CSB the serial interface is initialized. At the falling CSB edge, SCL can be high or low. SDI/SDO is sampled at the rising(falling) edge of SCL. R/W indicates, whether the byte is read command (R/W = '1') or write command (R/W = '0'). It is sampled when first rising(falling) SCL edge. If CSB stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising(falling) edge of SCL.



Serial bus protocol for register write mode

Read Mode

The read mode of the interface means that the micro controller reads register value from the IC. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSB is required to go high before a new command is send. The IC samples the SDI (input data) at the rising(falling) edges, but shifts SDO (output data) at the falling(rising) SCL edges. Thus the micro controller is supported to read data at the rising(falling) SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. It doesn't need any dummy clock when execute the command data read.



Serial bus protocol for register read mode

6.2 MIPI Interface

The Display Serial Interface (DSI) standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to Restriction DSI from operating in other applications. Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode refers to operation in which transactions primarily take the form of sending commands to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters to the display controller. The host processor can also read display module status information. Command Mode operation requires a bi-directional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. Some Video Mode architectures may include a simple timing controller, used to maintain lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Lane Pair	MCU (Master) Display Module (Slave)
Clock Lane	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane 0	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane 1	Unidirectional Lane ■ Forward High-Speed ■ Escape Mode (ULPM only) ■ No LPDT

Display Serial Interface (DSI)

The communication can be separated 2 different levels between the MCU and the display module:
• Low level communication what is done on the interface level
• High level communication what is done on the packet level

Interface Level Communication

The display module uses data and clock lane differential pairs for DSI. Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.
Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocol in each mode when there is wanted to transfer information from the MCU to the display module and vice versa.
The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

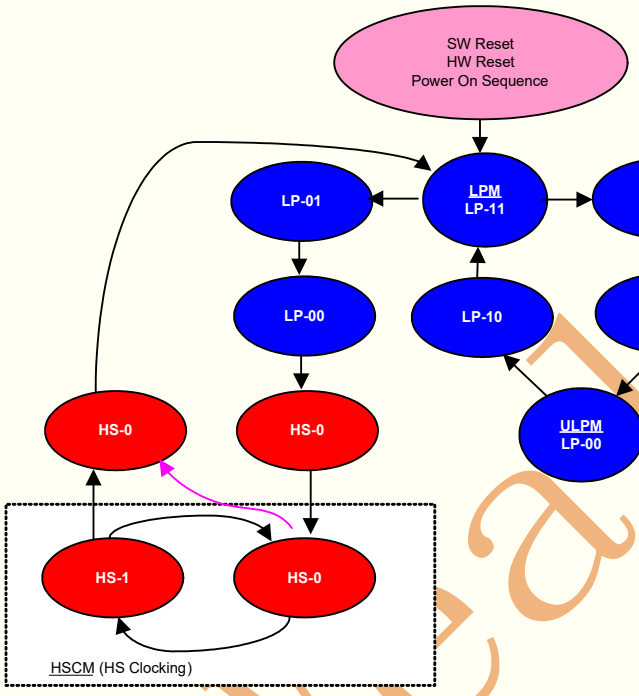
Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power(LP)	
	Dn+ -line	Dn- -line	Burst Mode	Control Mode	Escape Mode
HS -0	Low (HS)	High (HS)	Differential -0	Note 1	Note 1
HS -1	High (HS)	Low (HS)	Differential -1	Note 1	Note 1
LP - 00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP - 01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP - 10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP - 11	High (LP)	High (LP)	Not Defined	Stop	Note-2

Note 1: Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.
Note 2: If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM). These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principle flow chart of the different clock lanes power modes is illustrated below.



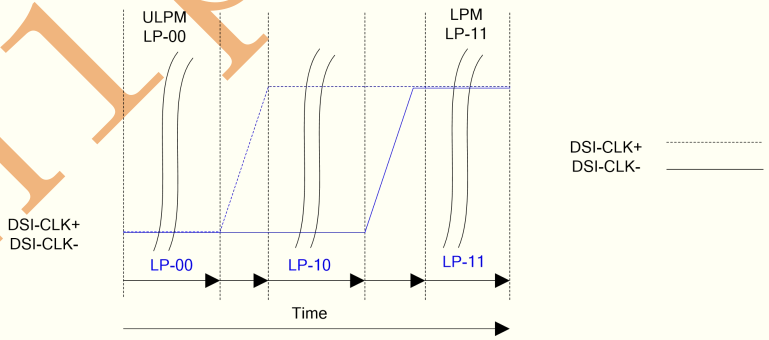
Clock Lanes Power Mode

Low Power Mode

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

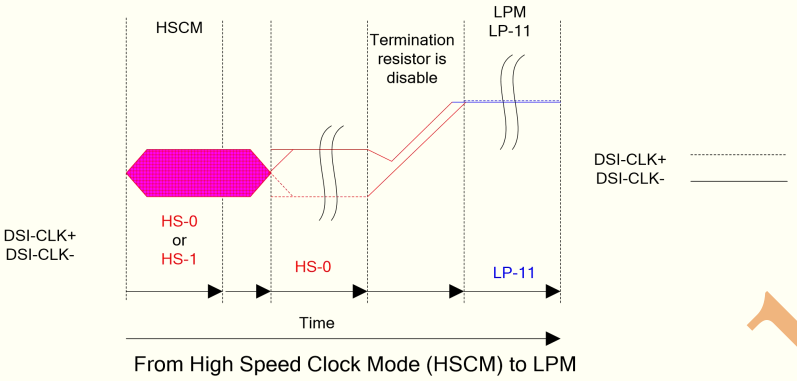
1) After SW Reset, HW Reset or Power On Sequence ⇒ LP-11

2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) ⇒LP-10 ⇒LP-11 (LPM). This sequence is illustrated below.



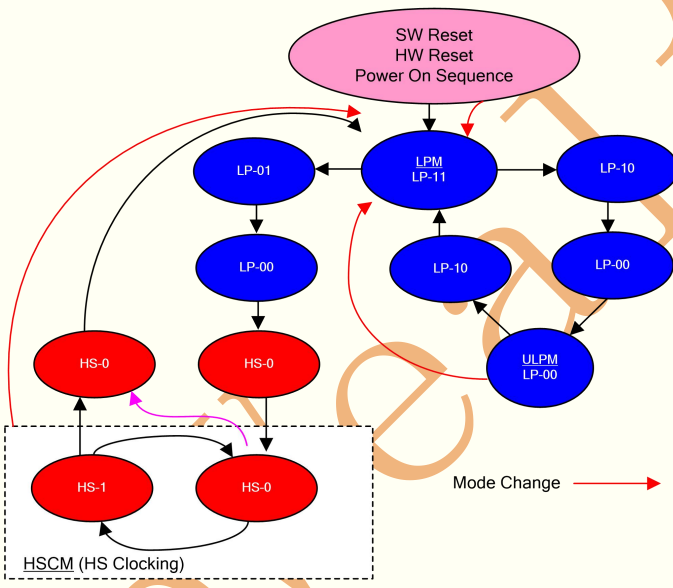
From ULPM to LPM

3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) ⇒HS-0⇒LP-11 (LPM). This sequence and all three mode changes are illustrated below.



From High Speed Clock Mode (HSCM) to LPM

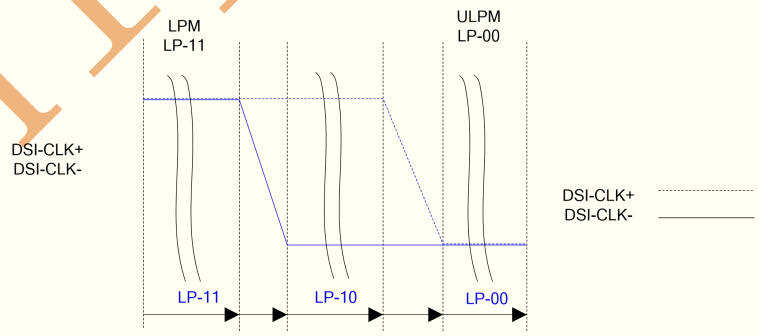
All three mode changes are illustrated a flow chart below.



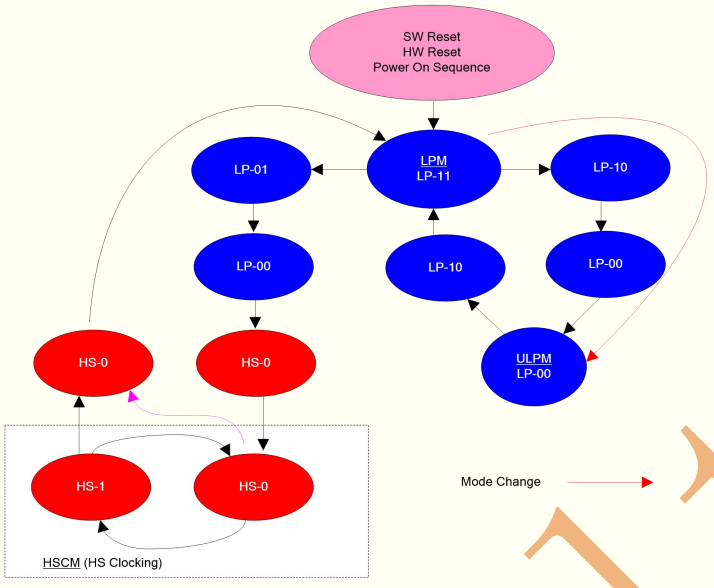
All Three Mode Change to LPM on the Flow Chart

Ultra low power mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) ⇒LP-10 ⇒LP-00 (ULPM). This sequence is illustrated below.

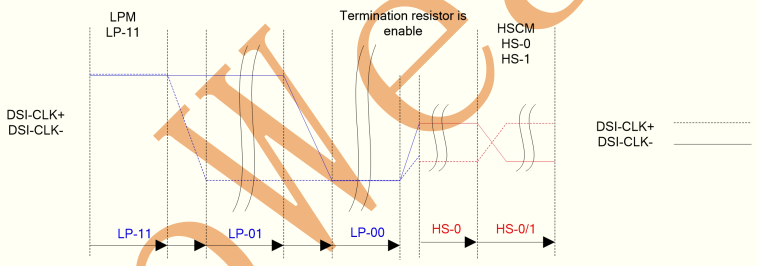


From LPM to ULPM
The mode change is also illustrated below:

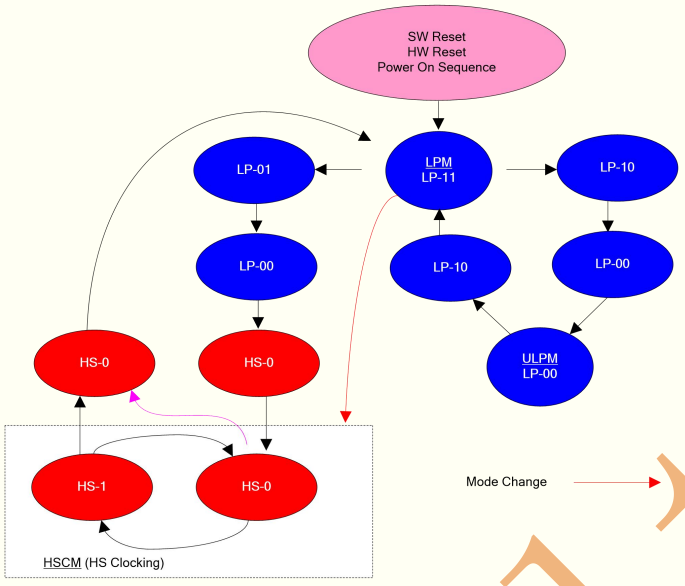


Mode Change from LPM to ULPM on the Flow Chart

High speed clock mode (HSCM)
DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) ⇒LP-01 ⇒LP-00 ⇒HS-0 ⇒HS-0/1 (HSCM). This sequence is illustrated below.

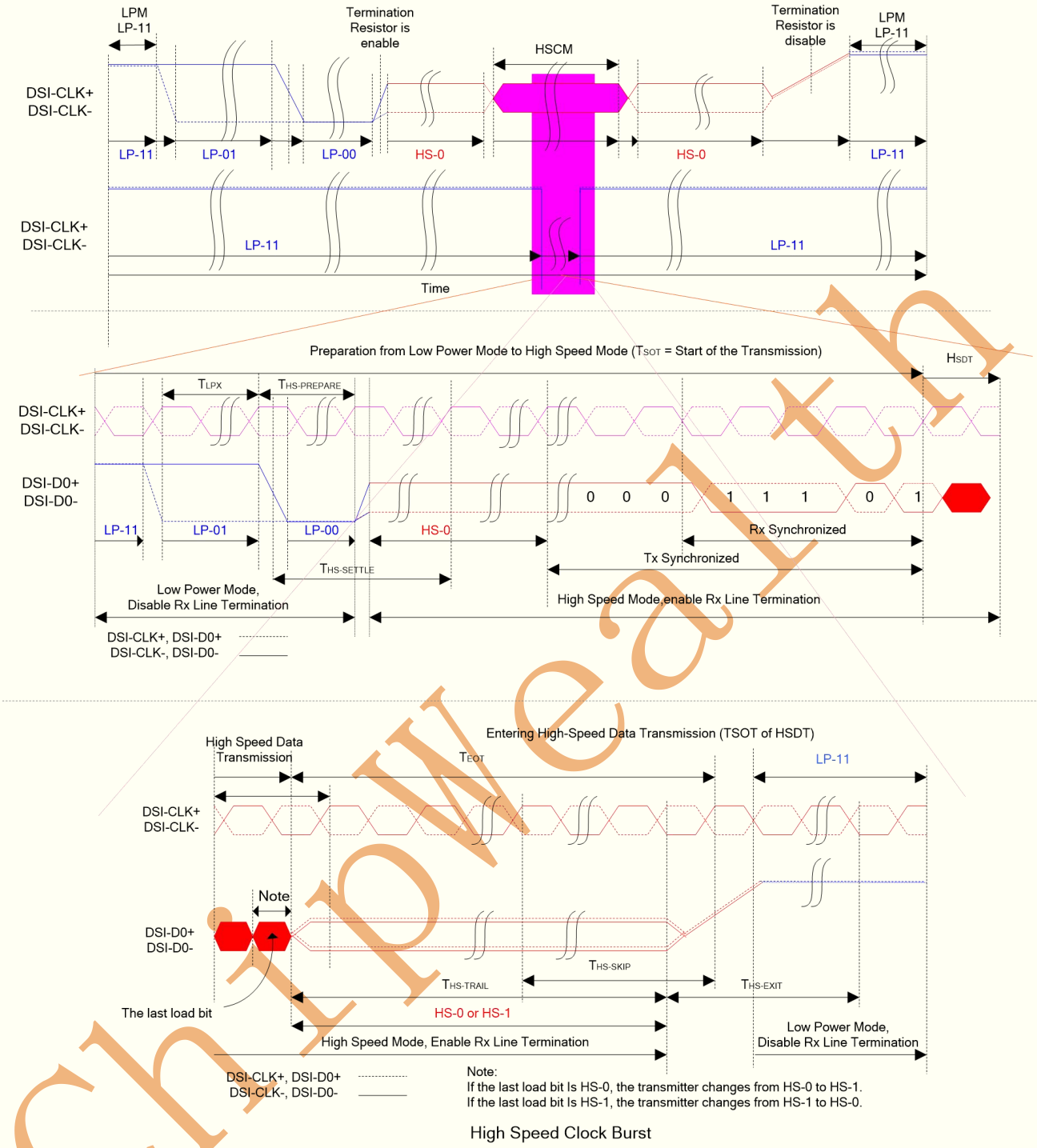


The mode change is also illustrated below:



Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.



High Speed Clock Burst

Note: The burst of the high speed clock consists of :

1. Even number of transitions
2. Start state is HS-0
3. End state is HS-0

DSI-DATA LANES

GENERAL

DSI-D0+/- Data Lanes can be driven in different modes which are:

• Escape Mode
• High-Speed Data Transmission
• Bus Turnaround Request

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 ⇒ LP-10 ⇒ LP-00 ⇒ LP-01 ⇒ LP-00	LP-00 ⇒ LP-10 ⇒ LP-11(Mark-1)
High-Speed Data Transmission	LP-11 ⇒ LP-01 ⇒ LP-00 ⇒ HS-0	(HS-0 or HS-1) ⇒ LP-11
Bus Turnaround Request	LP-11 ⇒ LP-10 ⇒ LP-00 ⇒ LP-10 ⇒ LP-00	High-Z

Notes:

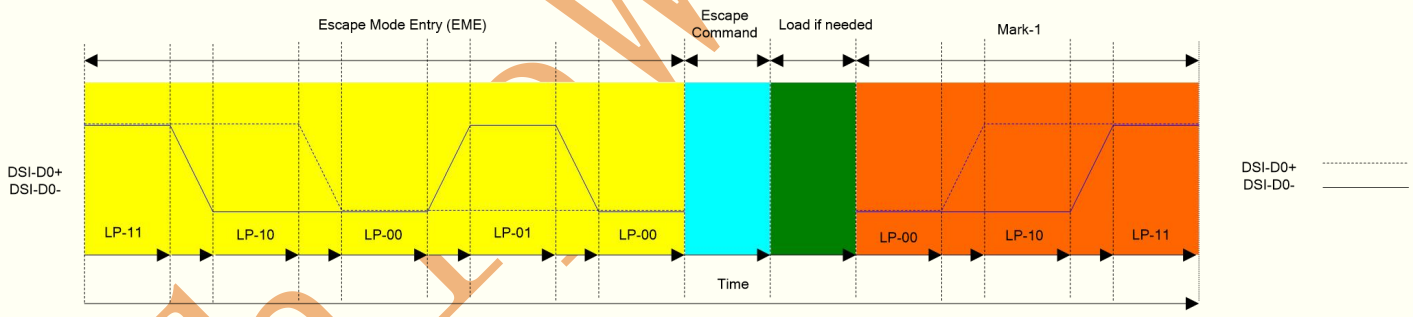
1. DSI-D0+/- data lane is used.
2. More information on section “Bus Turnaround (BTA)”

ESCAPE MODES

Data lanes (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

• Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module
• Drive data lanes to “Ultra-Low Power State” (ULPS)
• Indicate “Remote Application Reset” (RAR), which is reset the display module
• Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU. The basic sequence of the Escape Mode is as follow
• Start: LP-11
• Escape Mode Entry (EME): LP-11 ⇒ LP-10 ⇒ LP-00 ⇒ LP-01 ⇒ LP-00
• Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
• A load if it is needed
• Exit Escape (Mark-1) LP-00 ⇒ LP-10 ⇒ LP-11
• End: LP-11

This basic construction is illustrated below:



General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger.

Escape commands are defined on the next table.

This basic construction is illustrated below:

Escape command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001bin	-	×
Ultra-Low Power Mode	Mode	0001 1110bin	×	×
Underfined-1, Note1	Mode	1001 1111bin	-	-
Underfined-2, Note1	Mode	1101 1110bin	-	-
Remote Application Reset	Trigger	0110 0010bin	-	×
Tearing Effect	Trigger	0101 1101bin	-	-
Acknowledge	Trigger	0010 0001bin	-	×
Unknow-5, Note 1	Trigger	1010 0000bin	-	-

Notes:
1. This Escape command support has not been implemented on the display module.
2. “X”=Supported.
3. “-“=Not Supported.

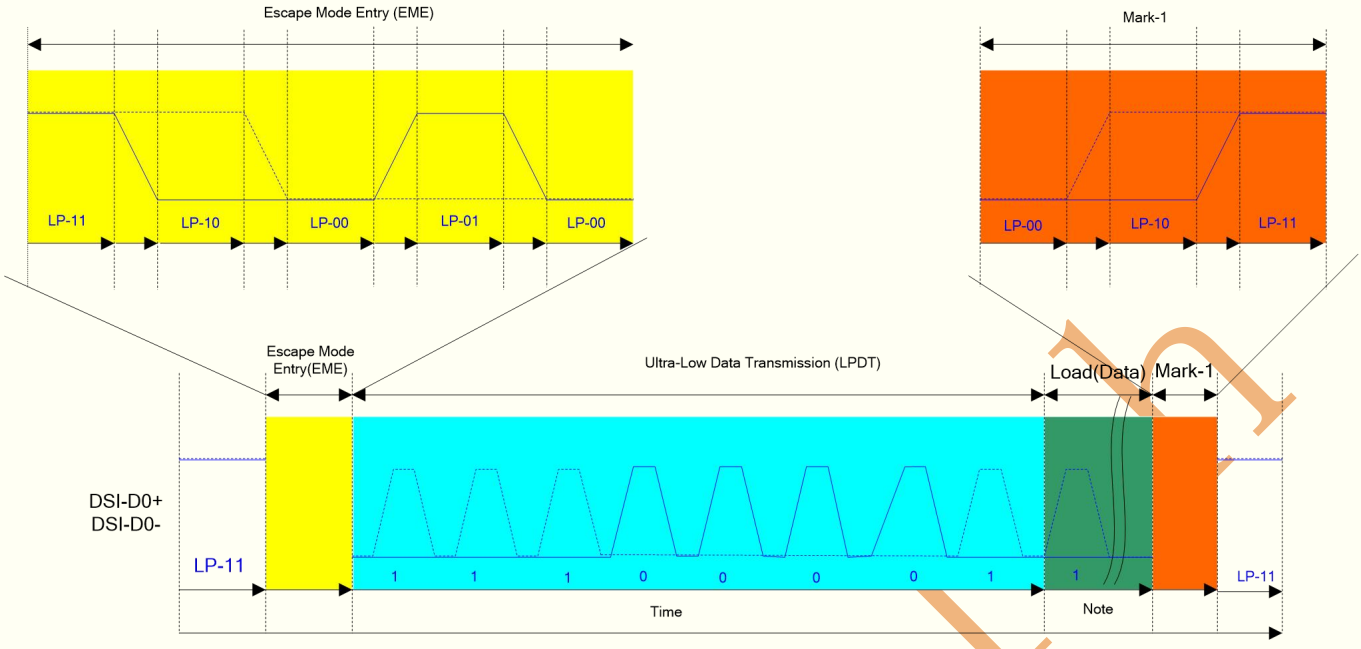
Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

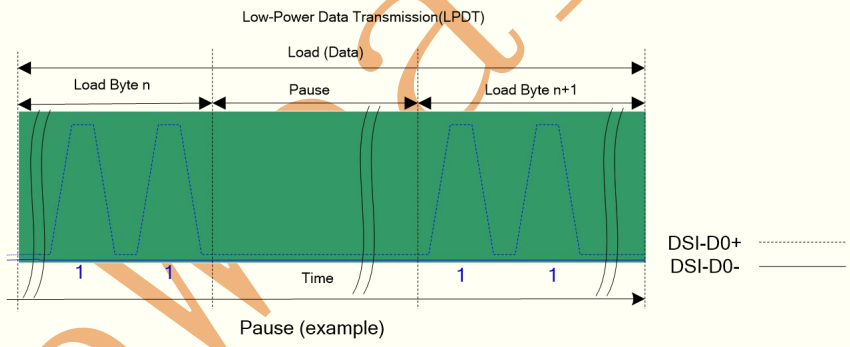
The Low Power Data Transmission (LPDT) is using a following sequence:

• Start: LP-11
• Escape Mode Entry (EME): LP-11 ⇒LP-10 ⇒LP-00⇒LP-01 ⇒LP-00
• Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
• Load (Data):
• One or more bytes (8 bit)
• Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
• Mark-1: LP-00 ⇒LP-10 ⇒LP-11
• End: LP-11

This sequence is illustrated for reference purposes below:



Note: Load (Data) is presenting that the first bit is logica"1" in this example



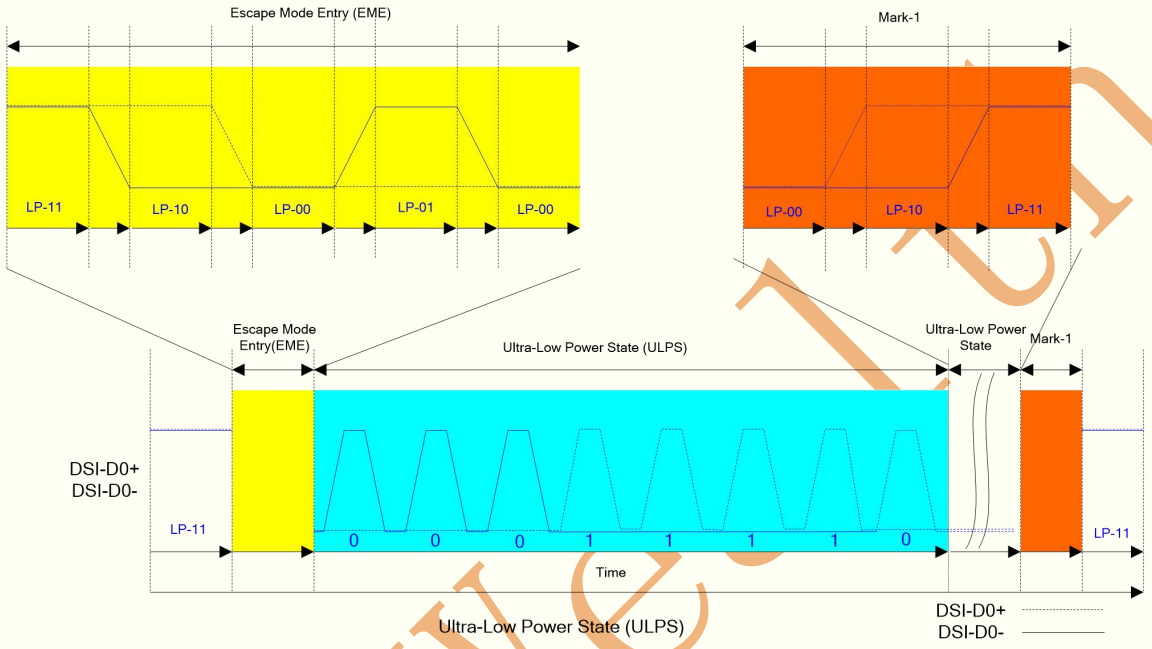
Pause (example)

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.
The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 ⇒ LP-10 ⇒ LP-00 ⇒ LP-01 ⇒ LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 ⇒ LP-10 ⇒ LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

• Start: LP-11

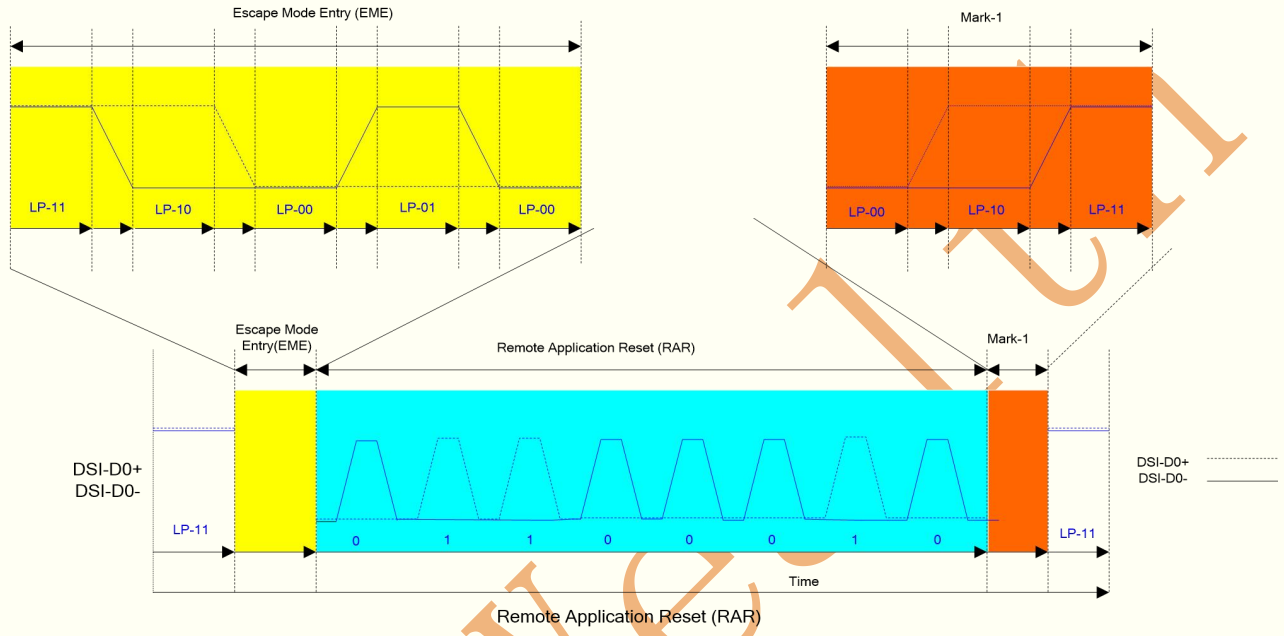
• Escape Mode Entry (EME): LP-11 ⇒ LP-10 ⇒ LP-00 ⇒ LP-01 ⇒ LP-00

• Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)

• Mark-1: LP-00 ⇒ LP-10 ⇒ LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

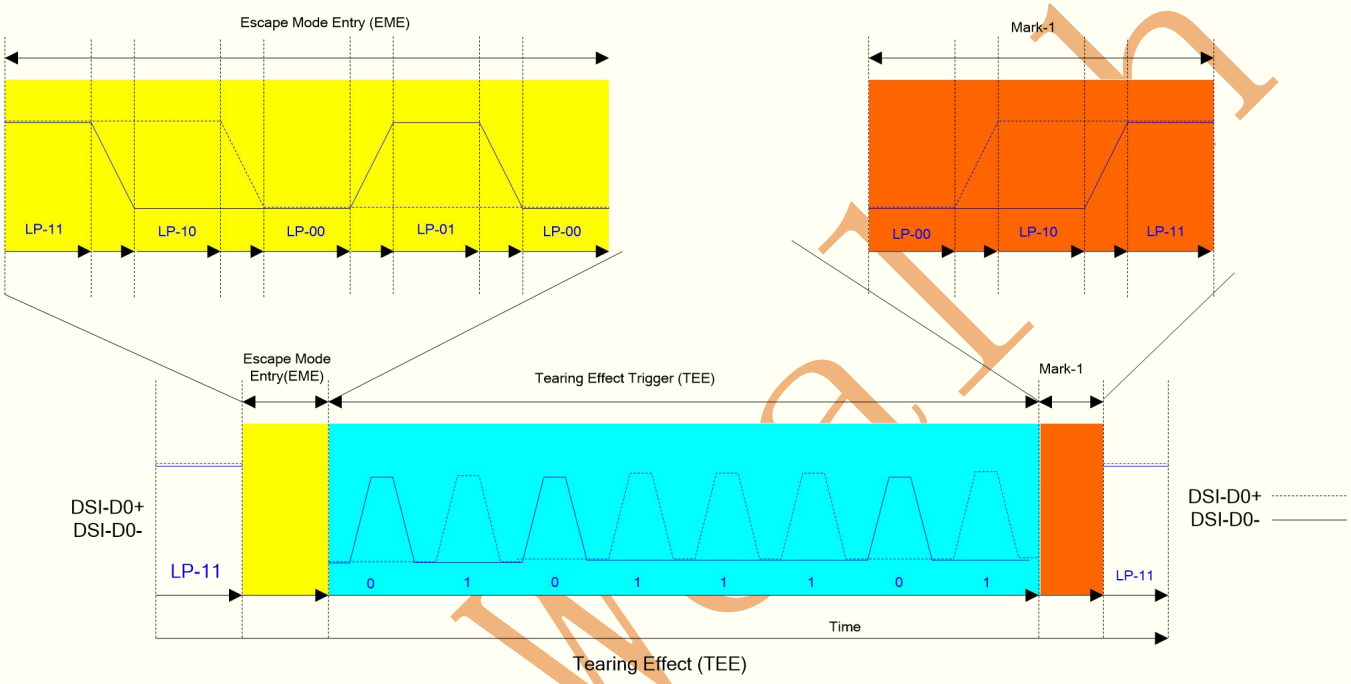


Tearing Effect (TEE)
The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

• Start: LP-11
• Escape Mode Entry (EME): LP-11 ⇒ LP-10 ⇒ LP-00 ⇒ LP-01 ⇒ LP-00
• Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
• Mark-1: LP-00 ⇒ LP-10 ⇒ LP-11
• End: LP-11

This sequence is illustrated for reference purposes below:

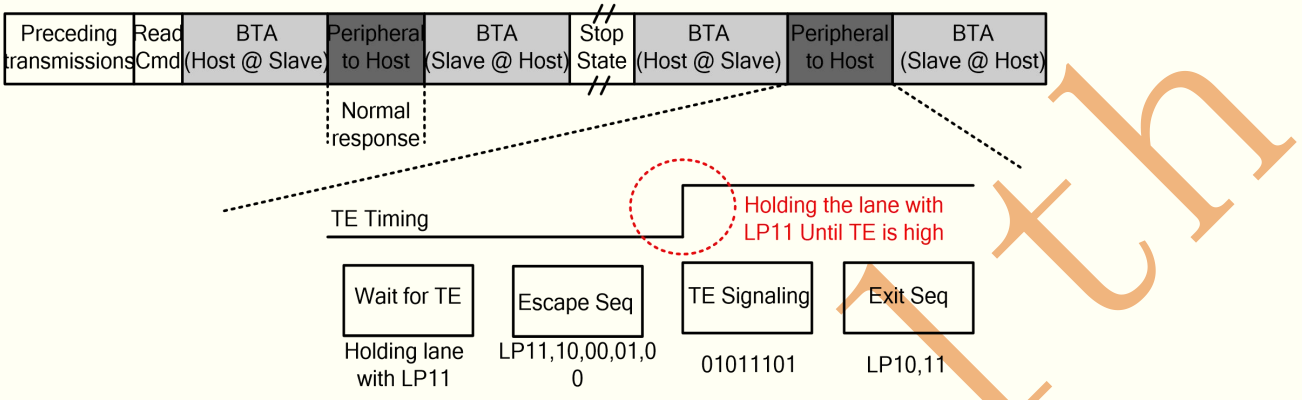


Note: Tearing Effect (TEE) can not be used in MIPI Video Mode

The TE Signaling function is enabled and disabled by three DCS commands to the display module's controller: set_tear_on, set_tear_off. After sending set_tear_on to enable this function, the host processor ends the transmission with BTA asserted, giving bus possession to the display module. Since the display module's DSI protocol layer does not interpret DCS commands, but only passes them through to the display controller, it responds with normal Acknowledge and returns bus possession to the host processor. In this state, the display module cannot report TE events to the host processor since it does not have bus possession. To enable TE Reporting, the host processor shall give bus possession to the display module without an accompanying DSI command transmission after TE Signaling has been enabled. This is accomplished by the host processor's protocol logic asserting (internal) BTA signal to its

PHY functional block. The PHY layer will then initiate a BTA sequence in LP mode, which gives bus possession to the display module.

The TE signaling Response procedure shows below:

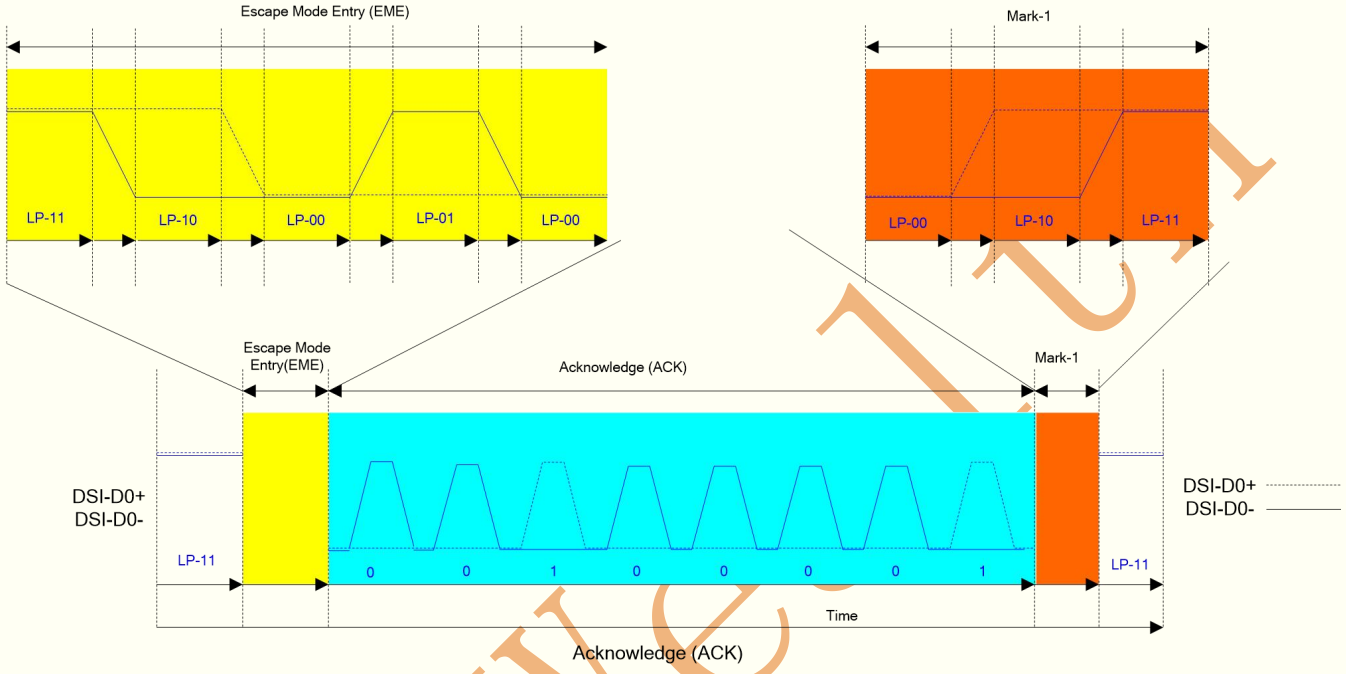


Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).
The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 ⇒ LP-10 ⇒ LP-00 ⇒ LP-01 ⇒ LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 ⇒ LP-10 ⇒ LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



HIGH SPEED DATA TRANSMISSION (HSDT)

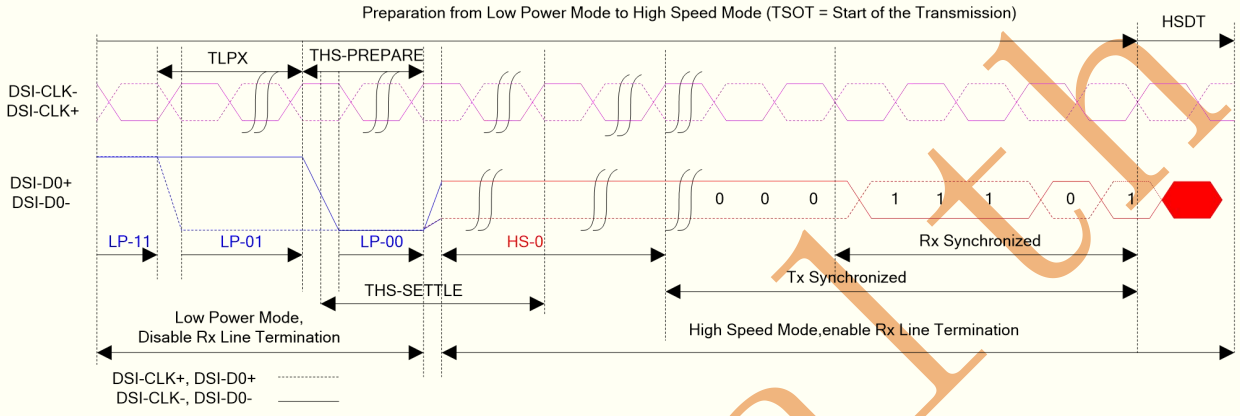
Entering High-Speed Data Transmission (TSOT of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 ⟹ HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below



Entering High-Speed Data Transmission (T_{SOT} of HSDT)

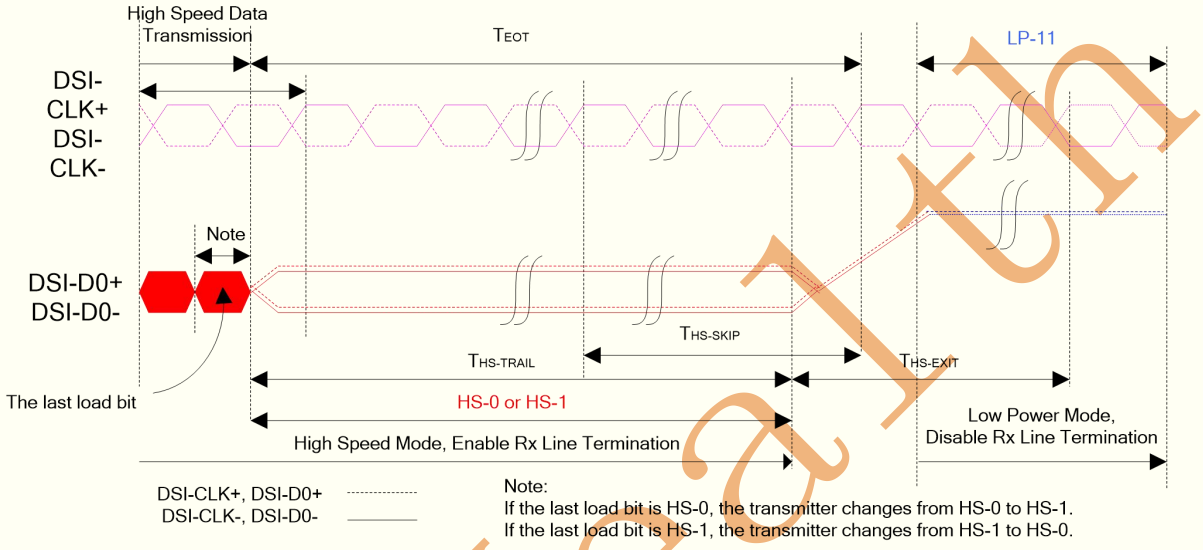
Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode. See more information on chapter "High-Speed Clock Mode (HSCM)".

Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
- MCU changes to HS-1, if the last load bit is HS-0
- MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below

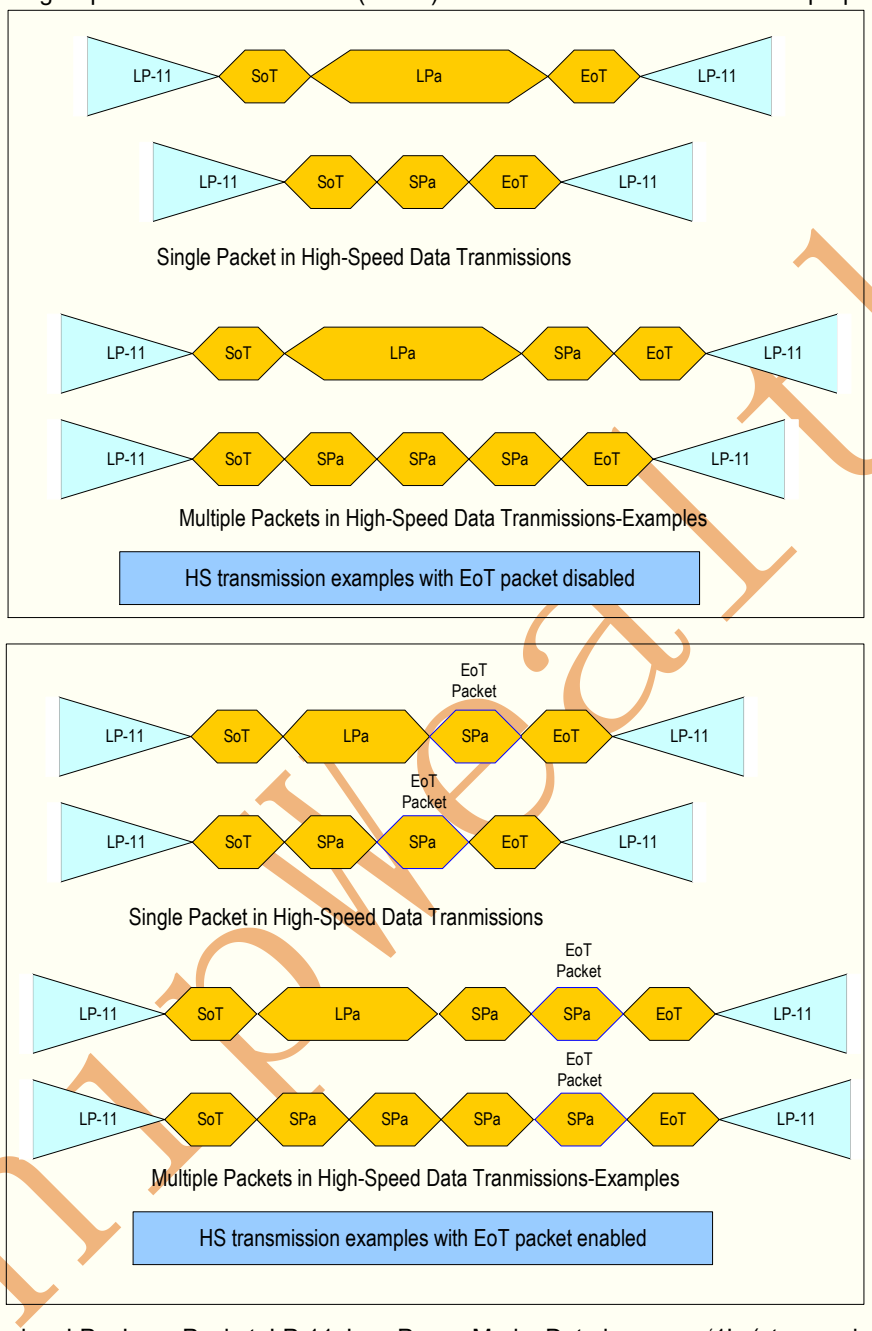


Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “Short Packet (SPa) and Long Packet (LPa) Structures“.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.



Note: EoT: end of transmission; LPa: Long Packet; LP-11: Low Power Mode, Data lanes are ‘1’s (stop mode)
Spa: Short Packet; SoT: Start of transmission.

Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module uses the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

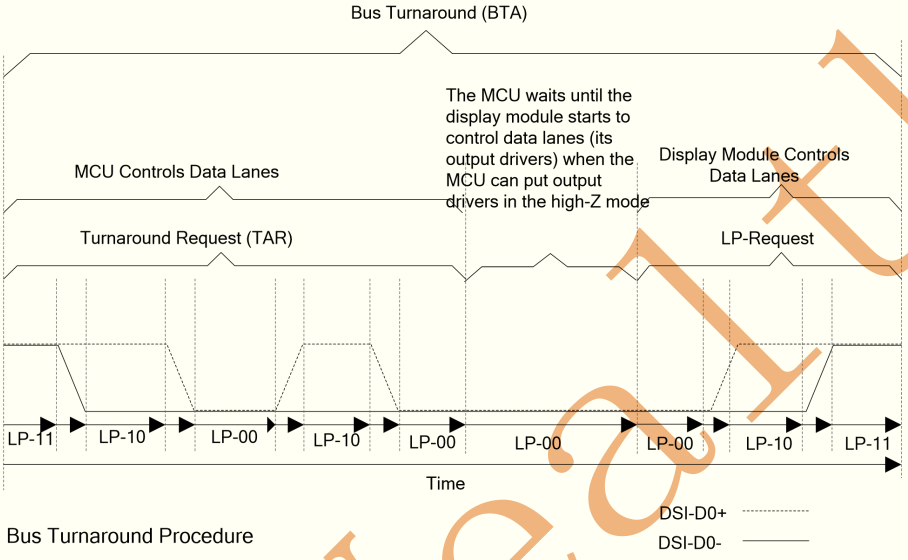
• Start (MCU): LP-11

• Turnaround Request (MCU): LP-11 →LP-10 →LP-00 → LP-10 →LP-00

• The MCU wait until the display module is starting to control DSI-D0+/- data lanes and the MCU stop to control DSI-D0+/- data lanes (=High-Z)

• The display module changes to the stop mode: LP-00 →LP-10 →LP-11

The same bus turnaround procedure (From the MCU to the display module) is illustrated below.



Bus Turnaround Procedure

MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU

Packet Level Communication

SHORT PACKET (SPA) AND LONE PACKET (LPA) STRUCTURE

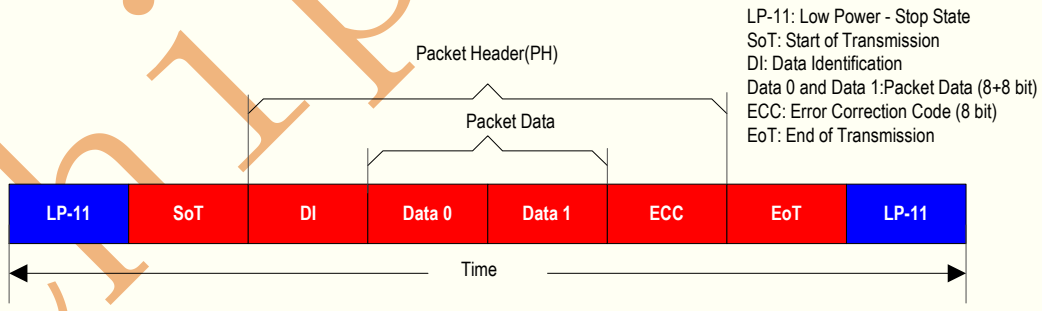
Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

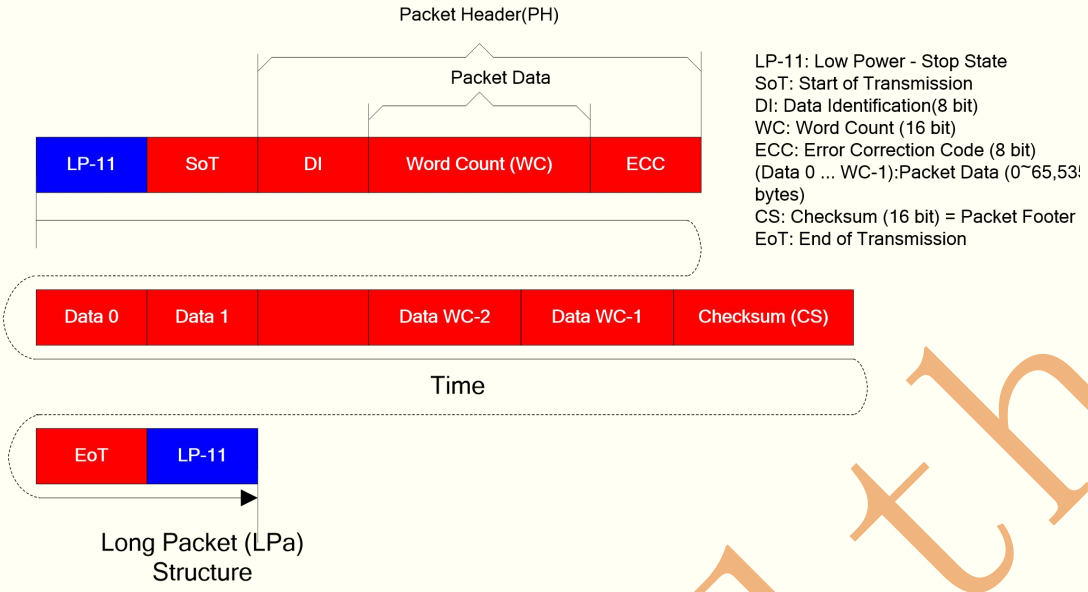
• Short Packet (SPa): 4 bytes

• Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).



Short Packet (SPa) Structure



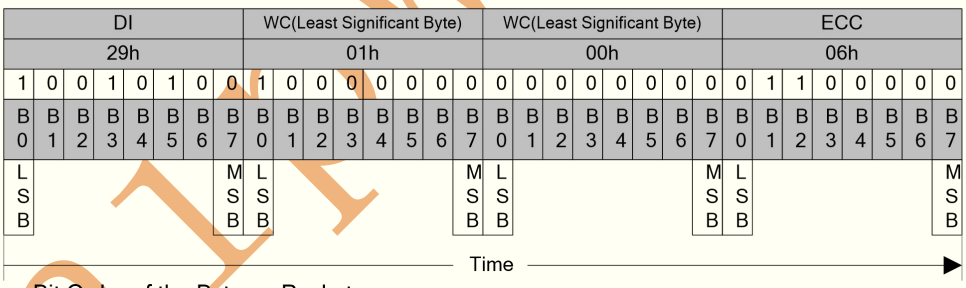
Long Packet (LPa) Structure

Note:
Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).
The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

* LP-11 ⇒ SoT ⇒ SPa ⇒ LPa ⇒ SPa ⇒ SPa ⇒ EoT ⇒ LP-11
* LP-11 ⇒ SoT ⇒ SPa ⇒ SPa ⇒ SPa ⇒ EoT ⇒ LP-11
* LP-11 ⇒ SoT ⇒ LPa ⇒ LPa ⇒ LPa ⇒ EoT ⇒ LP-11

BIT ORDER OF THE BYTE ON PACKETS

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.
This same order is illustrated for reference purposes below.

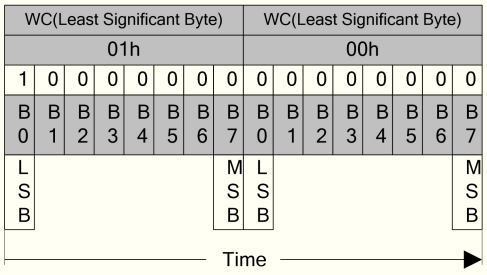


Bit Order of the Byte on Packets

BIT ORDER OF THE MULTIPLE BYTE INFORMATION ON PACKETS

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

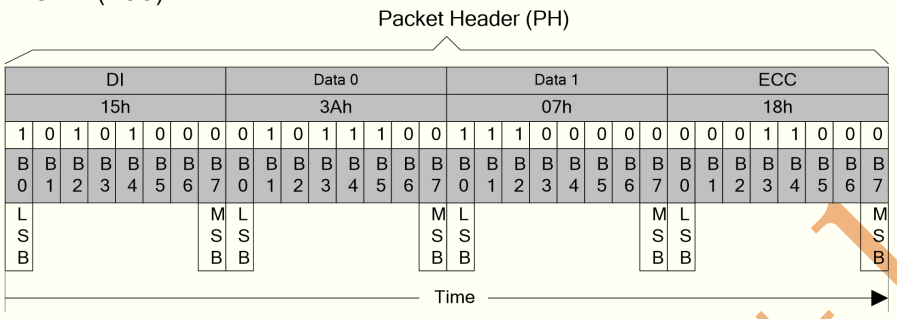


Bit Order of the Multiple Byte on Packets

PACKET HEADER (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).
Short Packet (SPa):

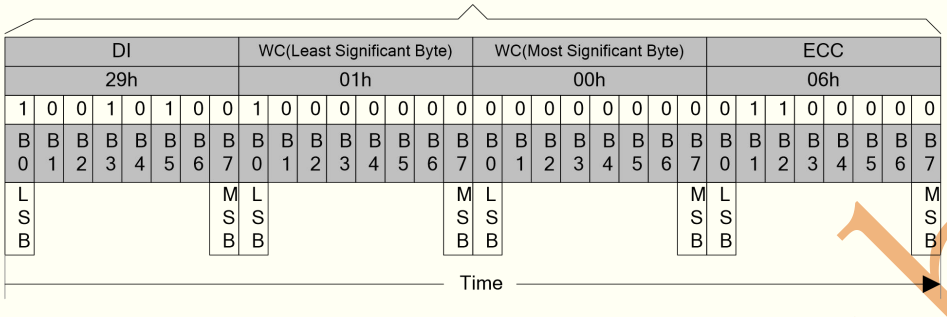
- 1st byte: Data Identification (DI) ⟹ Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)



Packet Header (PH) on Short Packet (SPa)

Long Packet (LPa):
• 1st byte: Data Identification (DI) ⟹ Identification that this is Long Packet (LPa)
• 2nd and 3rd bytes: Word Count (WC)
• 4th byte: Error Correction Code (ECC)

Packet Header(PH)



Packet Header (PH) on Long Packet (LPa)

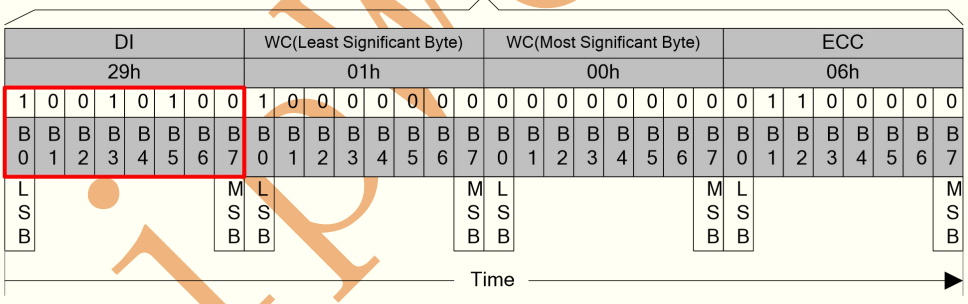
Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:
• Virtual Channel (VC), 2 bits, DI[7...6]
• Data Type (DT), 6 bits, DI[5…0]
The Data Identification (DI) structure is illustrated on the table below.
Data Identification (DI) Structure

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

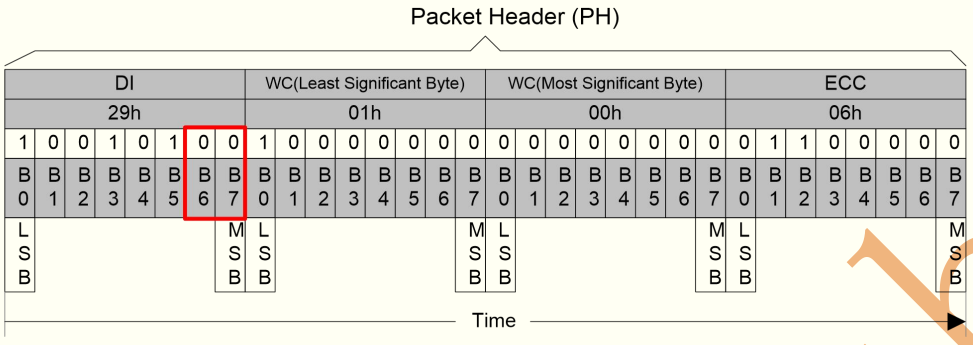
Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

Packet Header (PH)



Data Identification (DI) on the Packet Header (PH)

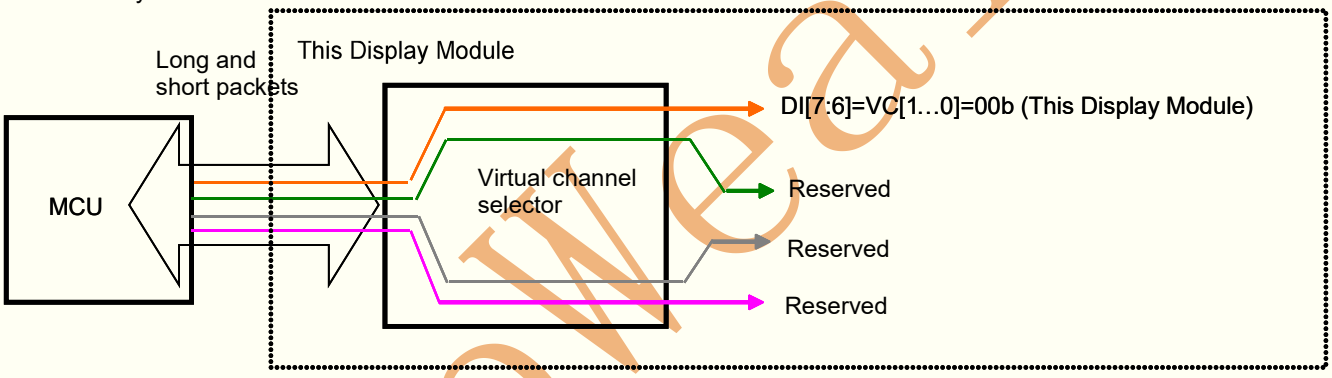
Virtual Channel (VC)
Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to Command where a packet is wanted to send from the MCU.
Bits of the Virtual Channel (VC) are illustrated for reference purposes below.



Virtual Channel (VC) on the Packet Header (PH)

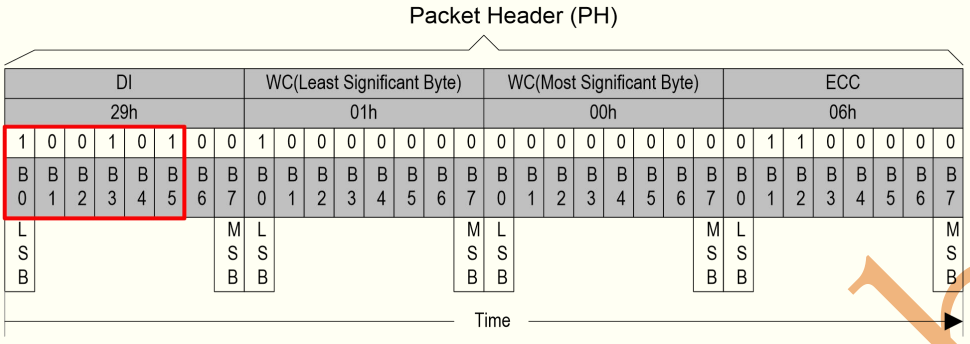
Virtual Channel (VC) can Command 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.
• The MCU is using the virtual channel 0 when it sends packets to this display module
• This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.



Virtual Channel (VC) Configuration
Virtual Channel (VC) always 0 (D[7...6]=VC[1…0]000b) when the MCU is sending “End of Transmission Packet” to the display module. See section “End of Transmission Packet (EoTP)
This display module is not supporting the virtual channel selector for other device (1 to 3) when only possible virtual channel (VC[1…0]) is 00b for this display module.

Data Type (DT)
Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.



Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.
These Data Type (DT) are defined on tables below.

Data Type (DT) from MCU to the Display Module (or Other Devices)

Data Type Hex	Data Type Binary	Description	Packet Size	Note
08h	00 1000	End of Transmission packet	Short	1
05h	00 0101	DCS WRITE, no parameters	Short	-
15h	01 0101	DCS WRITE, 1 parameter	Short	-
06h	00 0110	DCS READ, no parameters	Short	-
37h	11 0111	Set Maximum Return Packet Size	Short	-
09h	00 1001	Null Packet, no data	Long	2
19h	01 1001	Blanking Packet, no data	Long	2
39h	11 1001	DCS Long Write/Write_LUT Command Packet	Long	-
01h	00 0001	Sync Event, V Sync Start	Short	7
11h	01 0001	Sync Event, V Sync End	Short	7
21h	10 0001	Sync Event, H Sync Start	Short	7
31h	11 0001	Sync Event, H Sync End	Short	7
13h	01 0011	Generic Short Write, 1 parameter	Short	3,4
23h	10 0011	Generic Short Write, 2 parameter	Short	3,5
29h	10 1001	Generic Long Write	Long	3
14h	01 0100	Generic Read, 1 parameter	Short	3,4
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long	7
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long	7
2Eh	10 1110	Loosely Pixel Stream, 18-bit RGB, 6-6-6 Format	Long	7
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long	7

Notes:
1. This can be used when the MCU wants to secure that there is the end of transmission in High Speed Data Transmission (HSDT) mode.
2. This can be used when the data lanes are wanted to keep in High Speed Data Transmission (HSDT) mode.
3. The receiver process packets with data type (Generic Write/Read) the same way as data type (DCS Write / Read).
4. Generic Write/Read with 1 parameter: Payload Bytes = Command + 00h.
5. Generic Write/Read with 2 parameter: Payload Bytes = Command + Parameter.
6. The receiver will ignore packets with data type that neither listed in table above nor in MIPI DSI spec.
7. The data type for Video Mode Communication: 01h, 11h, 21h, 31h, 0Eh, 1Eh, 2Eh, 3Eh will be disable (ignored packet) if bit DSIM of command B200h is set to “0”.

Data Type (DT) from the Display Module (or Other Devices) to the MCU

Data Type Hex	Data Type Binary	Description	Packet Size	Abbreviation	Note
02h	000010	Acknowledge with Error Report	Short	AwER	
1Ch	011100	DCS Read Long response	Long	DCSRR-L	
21h	100001	DCS Read Short response, 1 byte returned	Short	DCSRR1-S	
22h	100010	DCS Read Short response, 2 byte returned	Short	DCSRR2-S	
1Ah	011010	Generic Read Long response	Long	GENRR-L	Note
11h	010001	Generic Read Short response, 1 byte returned	Short	GENRR1-S	Note
12h	010010	Generic Read Short response, 2 byte returned	Short	GENRR2-S	Note

Note:
The receiver will ignore other Data Type (DT) if they are not defined on tables: “Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “ Data Type (DT) from the Display Module (or Other Devices) to the “MCU”.

Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet of Packet Data (PD) send after the Packet Header.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

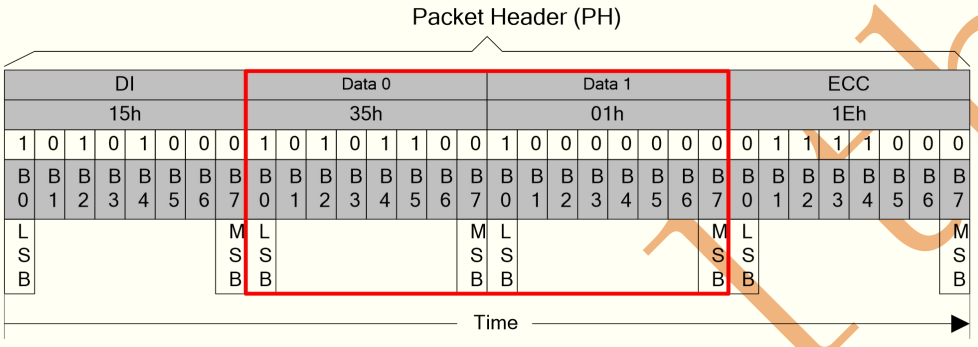
Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

• Data 0: 35hex (Display Command Set (DCS) with 1 Parameter ⇒ DI (Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS's parameter)

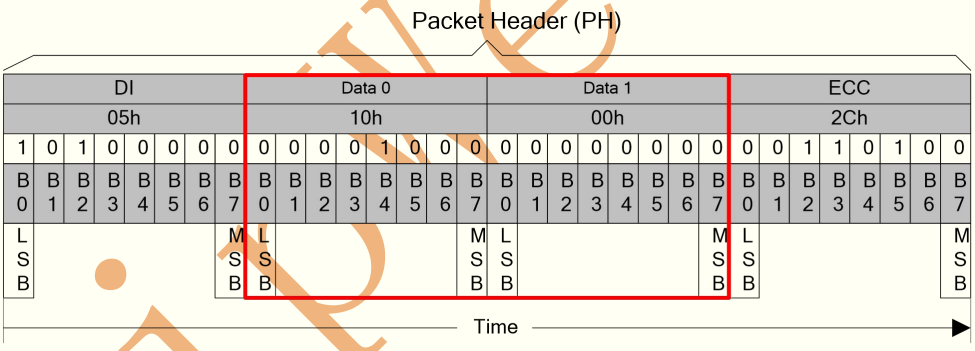


Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter ⇒ DI (Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)



Packet Data (PD) for Short Packet (SPa), 1 Byte Information

Word Count (WC) on the Long Packet (LPa)

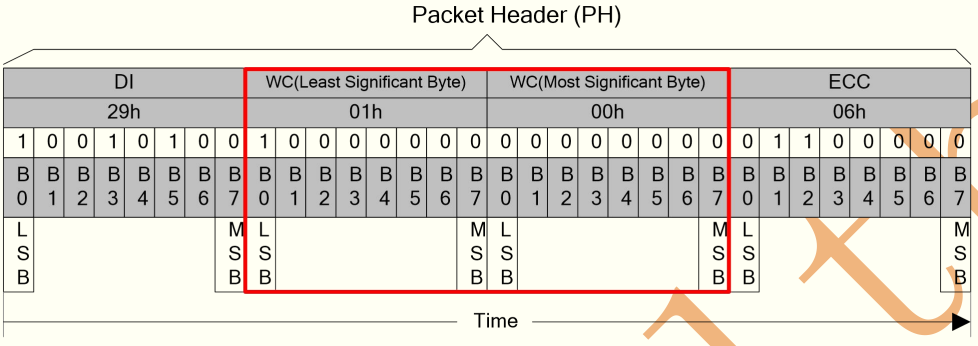
Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

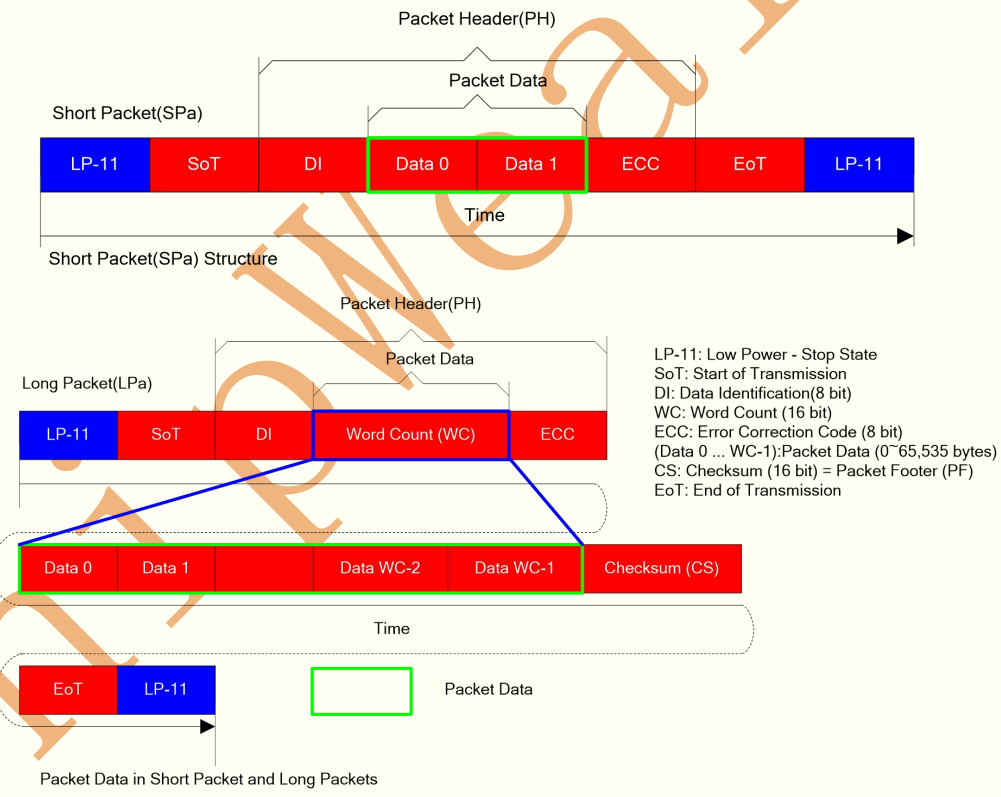
Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.



Word Count (WC) on the Long Packet (LPa)



Error Correction Code (ECC)

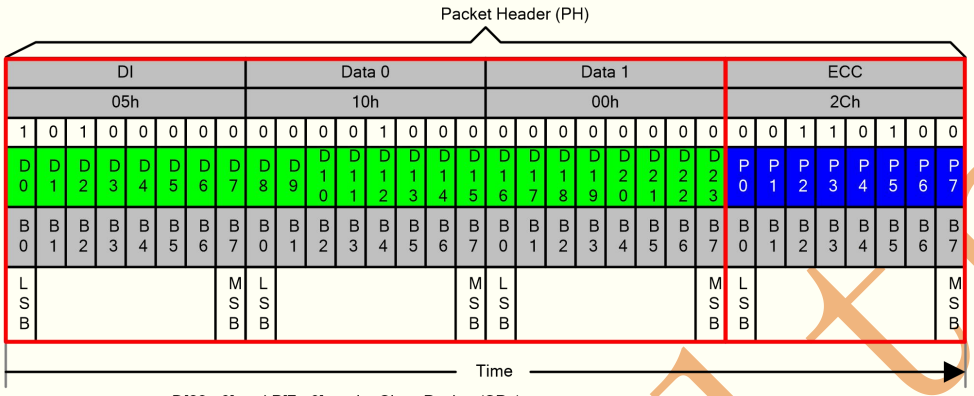
Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH):

The ECC protects the following field"

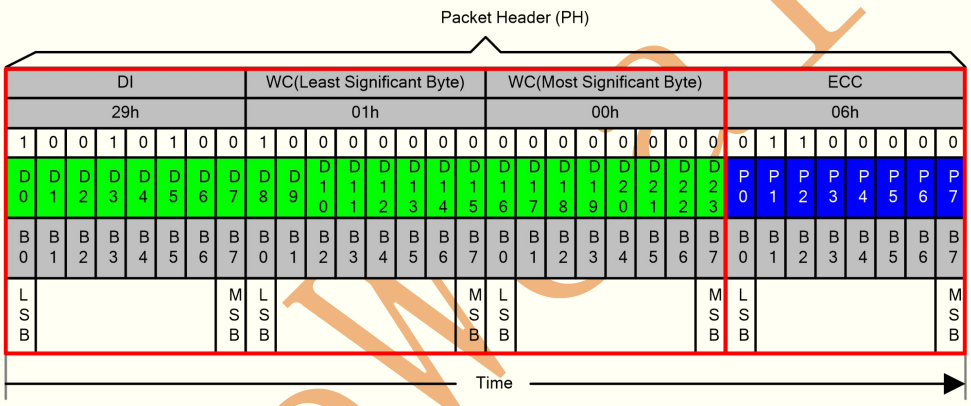
Short Packet (SPa): Data Identification (DI) byte (8 bits, D[0...7]), Packet Data (PD) bytes (16 bits, D[8...23]) and ECC(8 bits: P[0…7])

Long Packet (LPa): Data Identification (DI) byte (8 bits, D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits, P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.



D[23...0] and P[7...0] on the Short Packet (SPa)



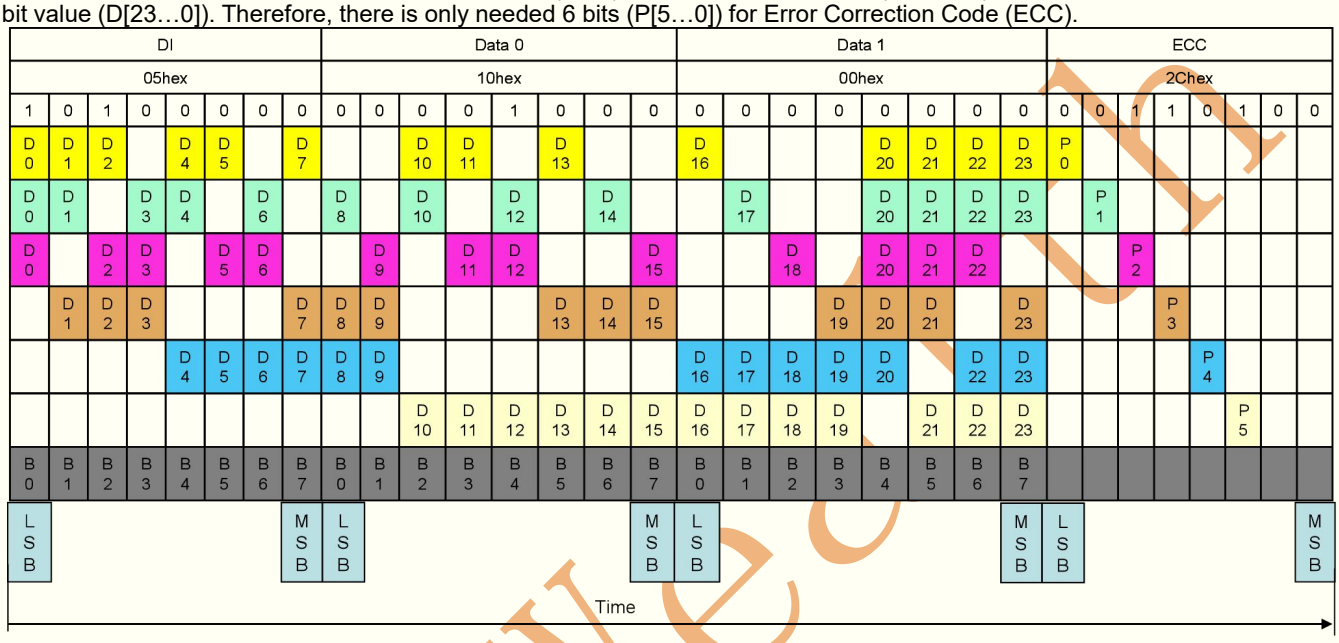
D[23...0] and P[7...0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

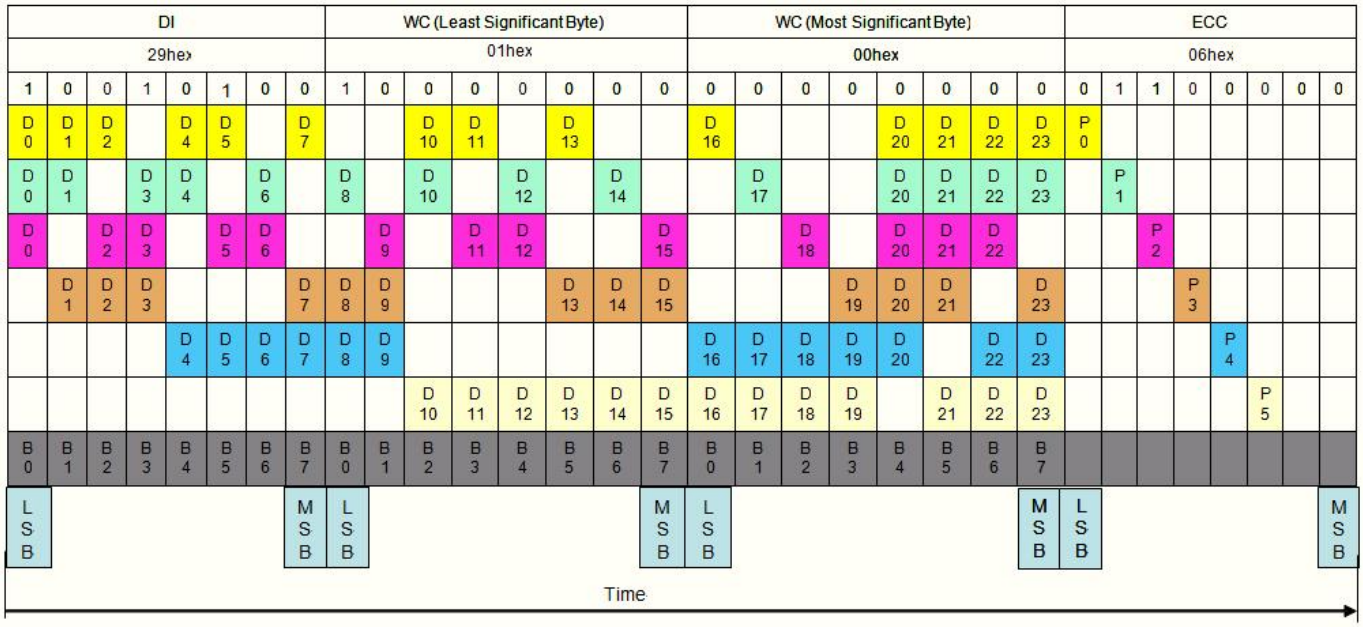
Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).



XOR Functionality on the Short Packet (SPa)



XOR Functionality on the Long Packet (LPa)

The transmitter (The MCU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MCU) calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].
The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.
The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

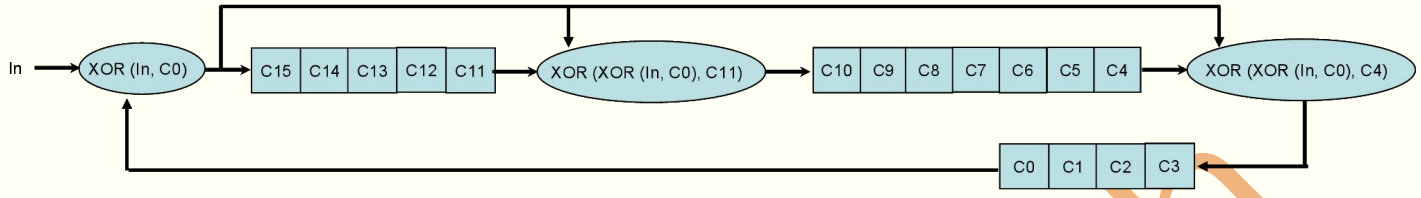
PACKET DATA (PD) ON THE LONG PACKET (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

PACKET FOOTER (PF) ON THE LONG PACKET (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it illustrates below.



16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

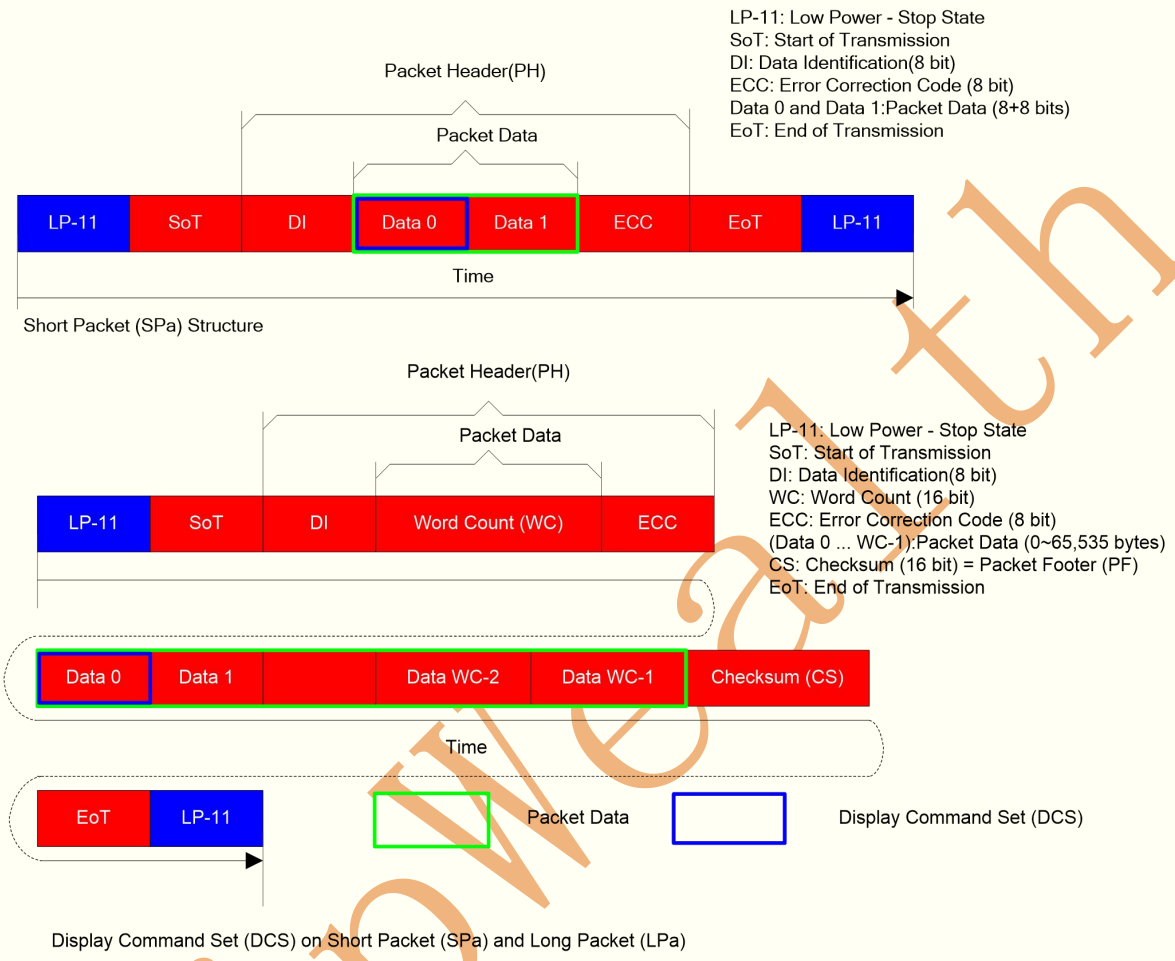
The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

PACKET TRANSMISSIONS

PACKET FROM THE MCU TO THE DISPLAY MODULE

Display Command Set (DCS), which is defined on chapter “Instruction Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.



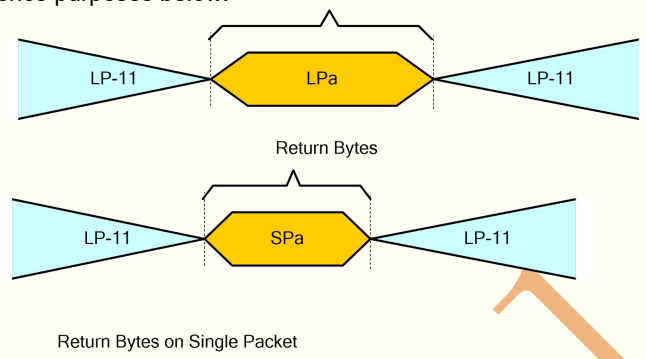
PACKET FROM THE DISPLAY MODULE TO THE MCU

Used Packet Types

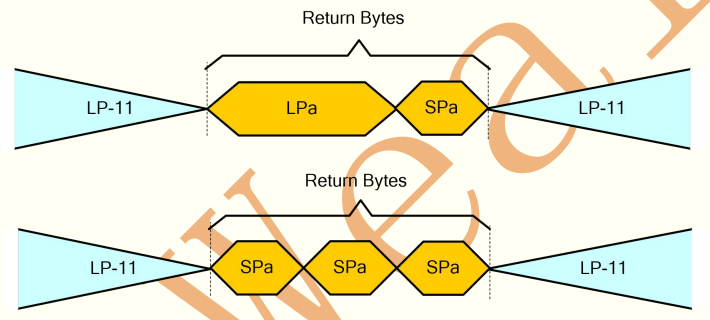
The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See chapter “Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See chapter: “Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined on Data Type (DT). See chapter “Data Type (DT)”. A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU. It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

Both cases are illustrated for reference purposes below.

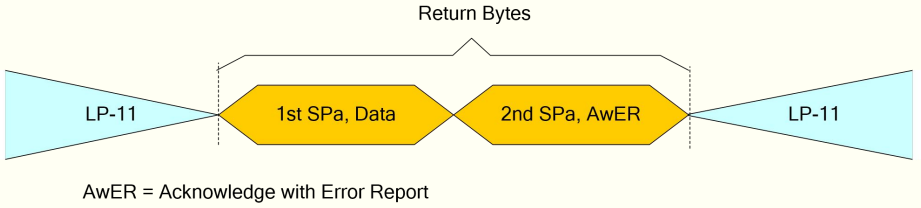


Return Bytes on Single Packet



Return Bytes on Several Packets-Not Possible

The display module is return 2 packets (1st packet: Data, 2nd packet Acknowledge with Error Report) to the MCU when the display module has received a read command. See section “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” where has been detected and corrected a single bit error by the EEC (See bit 8 on Table” Acknowledge with Error Report (AwER) for Short Packet (SPa) response”). These return packets are illustrated for reference purpose below.



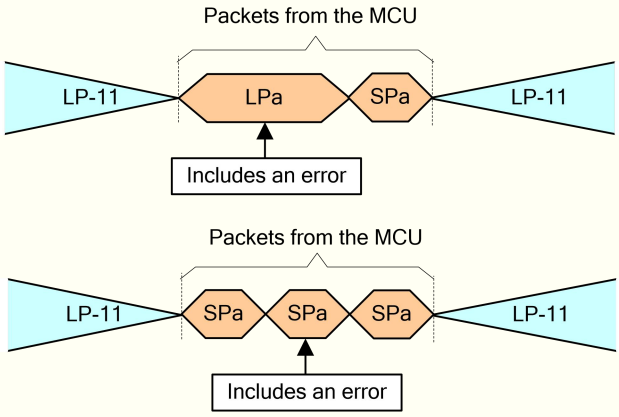
Exception when Return Bytes on Several Packet

Acknowledge with Error Report (AwER), Data Type = 02h
“Acknowledge with Error Report” (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 000010b), from the display module to the MCU.
The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to ‘1’, as they are defined on the following table.

Acknowledge with Error Report (AwER)

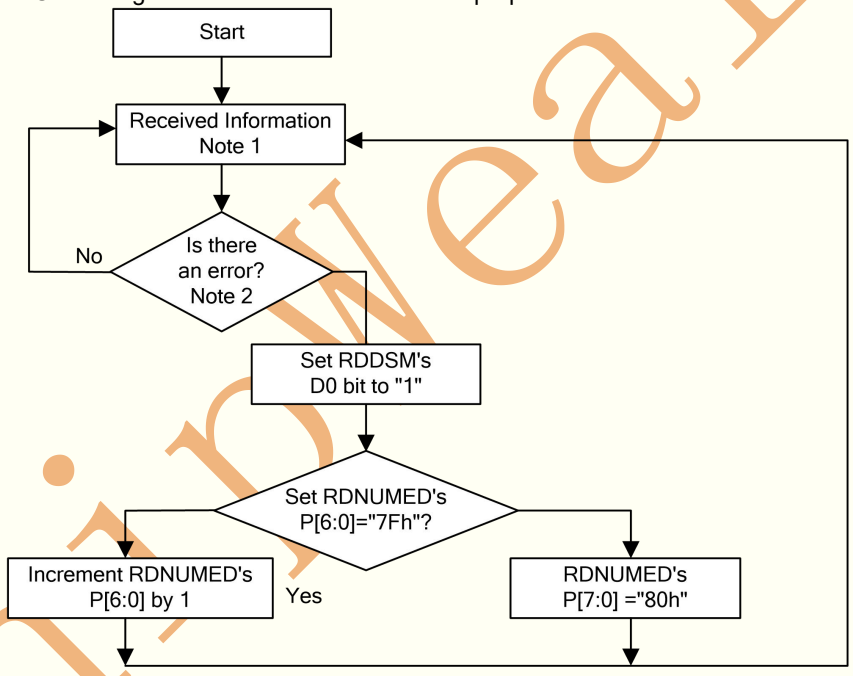
Bit	The Description of Acknowledge Error Report (AwER)	
	Long Packet (LPa)	Short Packet (SPa)
0	SoT Error	SoT Error
1	SoT Sync Error	SoT Sync Error
2	EoT Sync Error	EoT Sync Error
3	Escape Mode Entry Command Error	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out	Any Protocol Timer Time-Out
6	False Control Error	False Control Error
7	Contention is Detected on the Display Module	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)	Set to “0” internally (Only for Long Packet (LP))
11	DSI Data Type (DT) Not Recognized	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length	Invalid Transmission Length
14	Reserved, Set to ‘0’ internally	Reserved, Set to ‘0’ internally
15	DSI Protocol Violation	DSI Protocol Violation

These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).
The display module ignores the received packet which includes error or errors.
It is possible that the display module has received several packets, which have included errors, from the MCU before the MCU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.



Errors Packets

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.
The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from the display module.
The functionality of the RDNUMED register is illustrated for reference purposes below.



Notes:
1. This information can Interface or Packet Level Communication but it is always from the MCU to the display module in this case.
2. CRC or ECC error.

Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

TRANSMISSION PACKET SEQUENCES

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, *Burst Mode* refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so single Sync Event is substituted.

Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

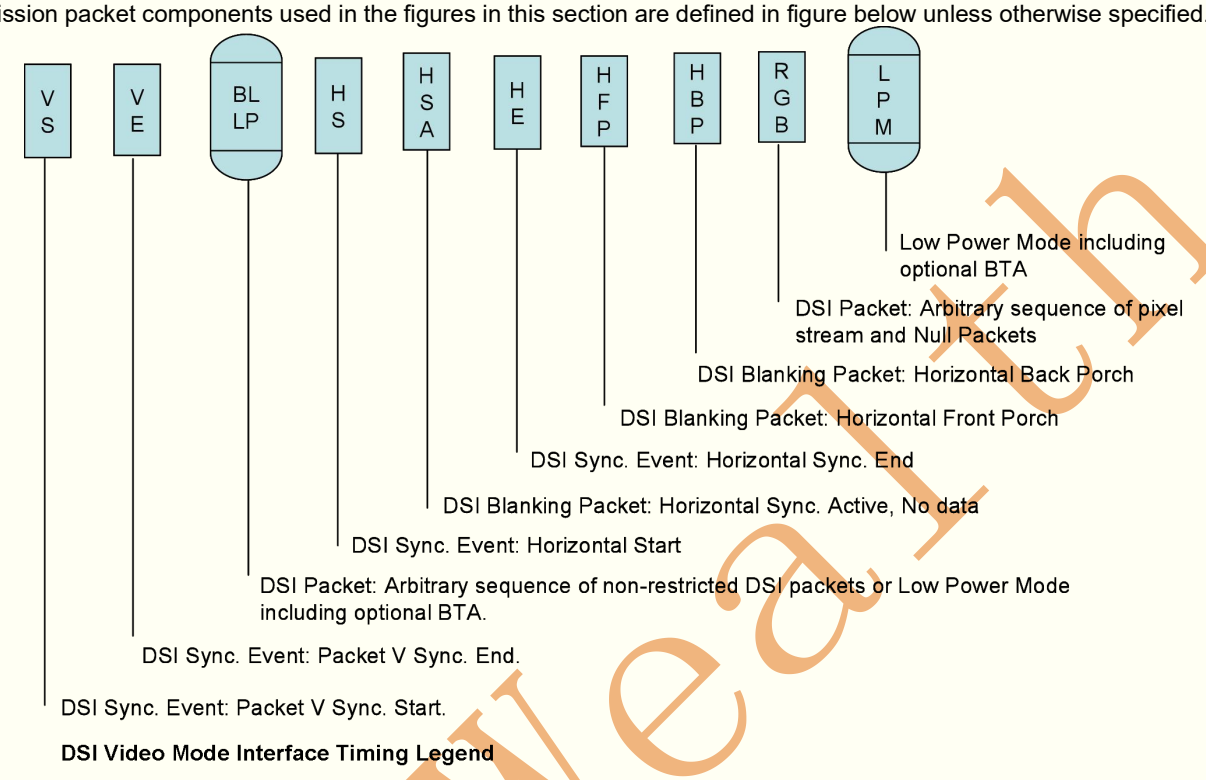
In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

During the BLLP the DSI Link may do any of the following:
Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode
Transmit one or more non-video packets from the host processor to the peripheral using HS Mode
If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode

Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel. Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in figure below unless otherwise specified.

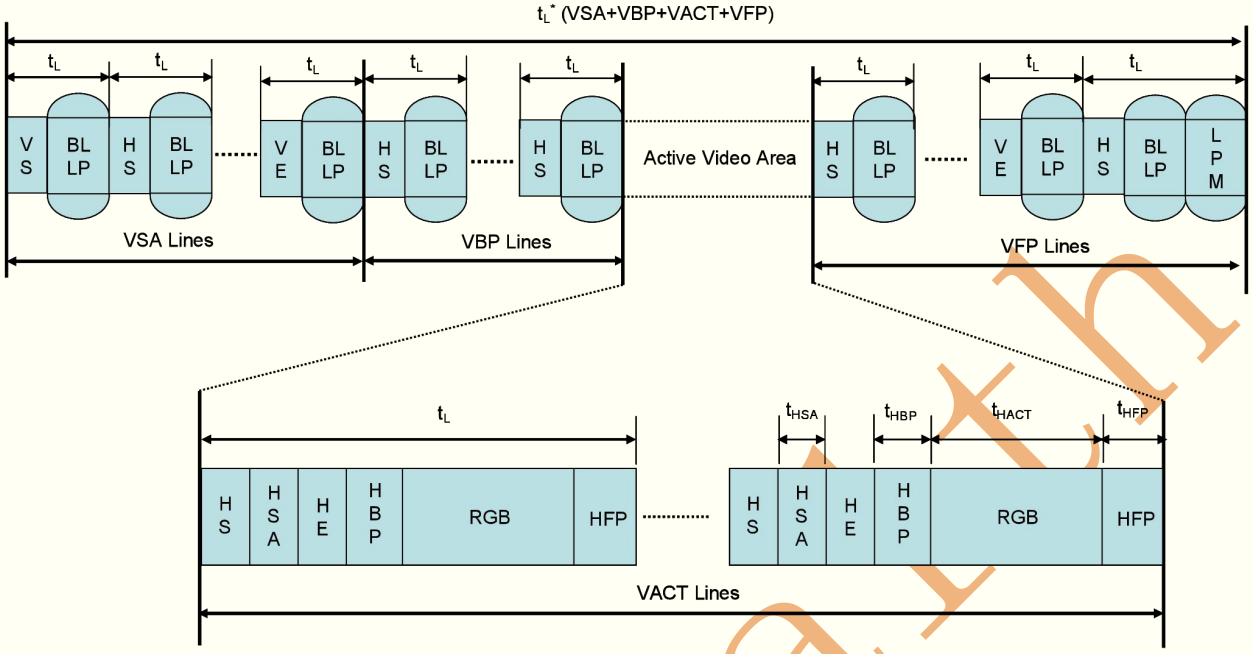


DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

NON-BURST MODE WITH SYNC PULSES

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.

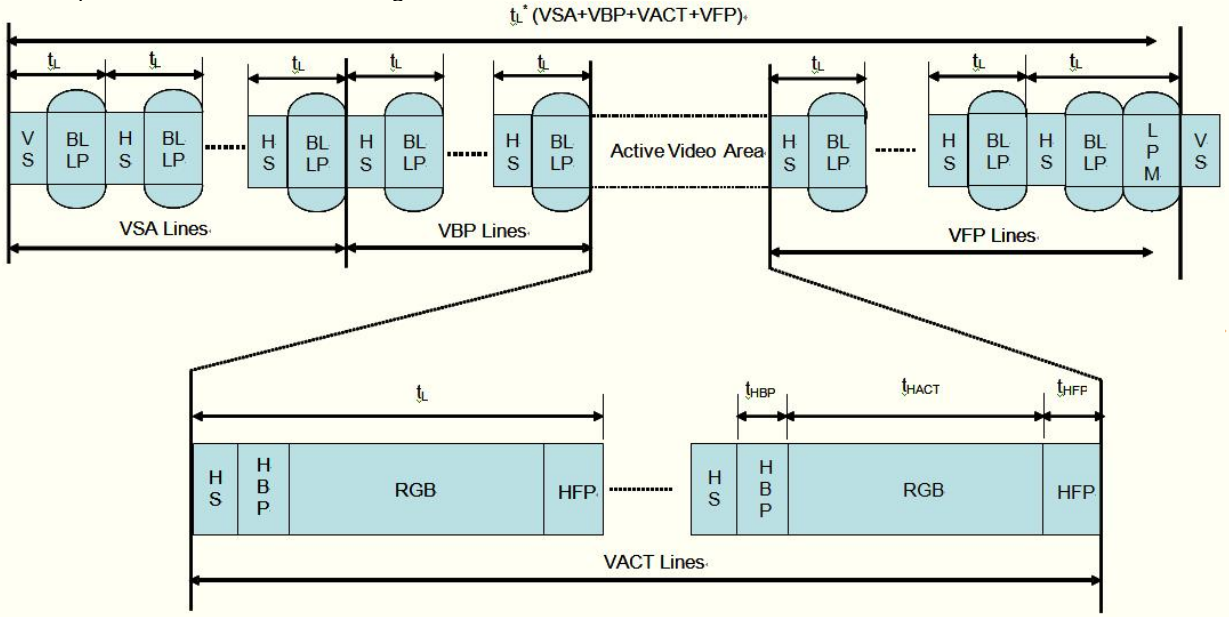


DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

NON-BURST MODE WITH SYNC EVENTS

Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in figure below.

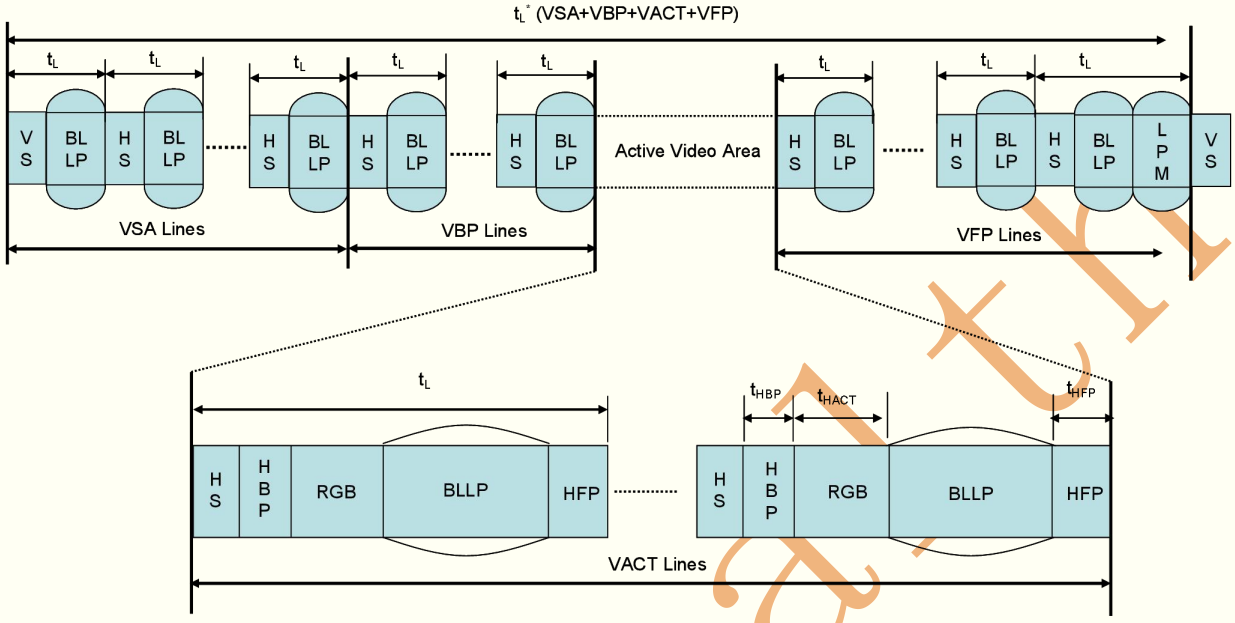


DSI Video Mode Interface Timing: Non- Burst Transmission with SYNC events

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

BURST MODE

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in figure below.



DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

PARAMETERS

Below table documents the parameters used in the preceding figures. Peripheral supplier companies are responsible for specifying suitable values for all blank fields in the table. The host processor shall meet these requirements to ensure interoperability.

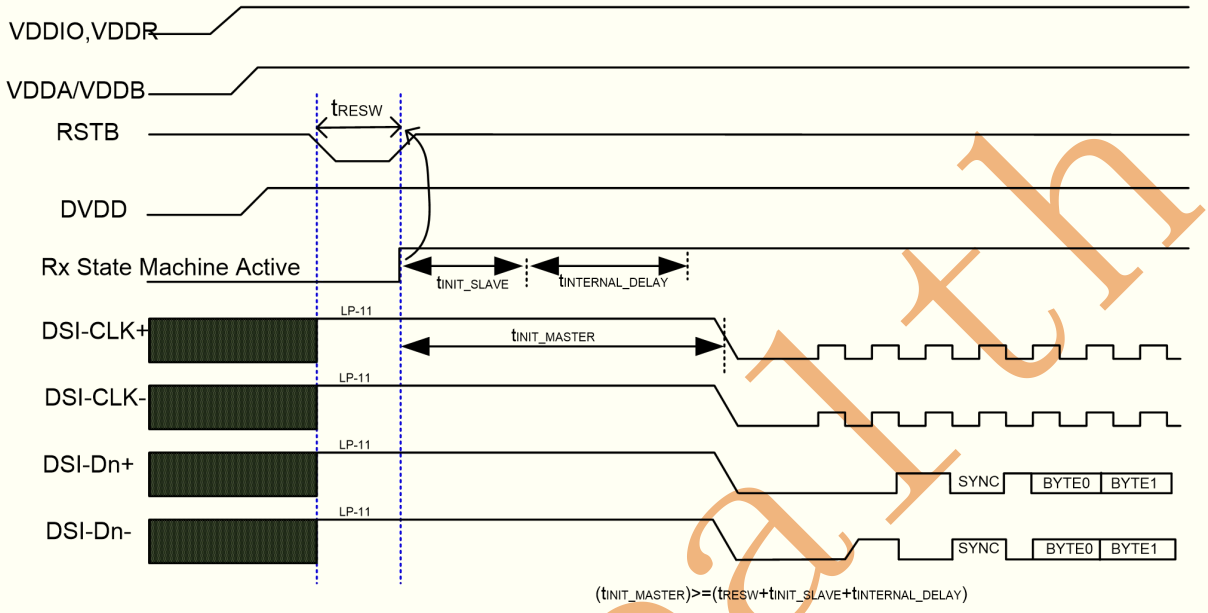
Required Peripheral Timing Parameters

symbol	Parameter	Condition	Min.	Typ.	Max.	Units
BRPHY	Bit rate total on all Lanes		80	-	500	Mbps
t_L	Line time		-	35 Note1	-	μs
t_{HBP}	Horizontal back porch		0.5	-	-	μs
t_{HACT}	Time for image data	2 data lane	25 Note3	-	-	μs
HACT	Active pixels per line		-	454	-	pixels
t_{HFP}	Horizontal front porch	-	0.5	-	-	μs
VSA	Vertical sync active	-	1	-	-	H
VBP	Vertical back porch	-	Note2	-	-	H
VACT	Active lines per frame		-	454	-	H
VFP	Vertical front porch	-	4	-	-	H

Note1: Frame rate (Typ)=60Hz
Note2: VBP (min) values are dependent on GOA timing.
Note3: tHACT + tHFP + tHBP ⩾ tLINE

System Power-Up and Initialization

After power-on, the host processor shall observe an initialization period, t_{INIT}, during which it shall drive a sustained Tx-Stop state (LP-11) on all Lanes of the Link.
Figure below illustrates an example power-up sequence for a DSI display module. In the figure, a hardware Reset (RSTB) mechanism is assumed for initialization. Internally within the display module, de-assertion of RSTB could happen after both IO and core voltages were ramped up. In this example, the host's t_{INIT_MASTER} parameter is programmed for driving LP-11 for a period longer than the sum of t_{RESW}, t_{INIT_SLAVE} and $t_{INTERNAL\_DELAY}$. The display module may ignore all Lane activities during this time.



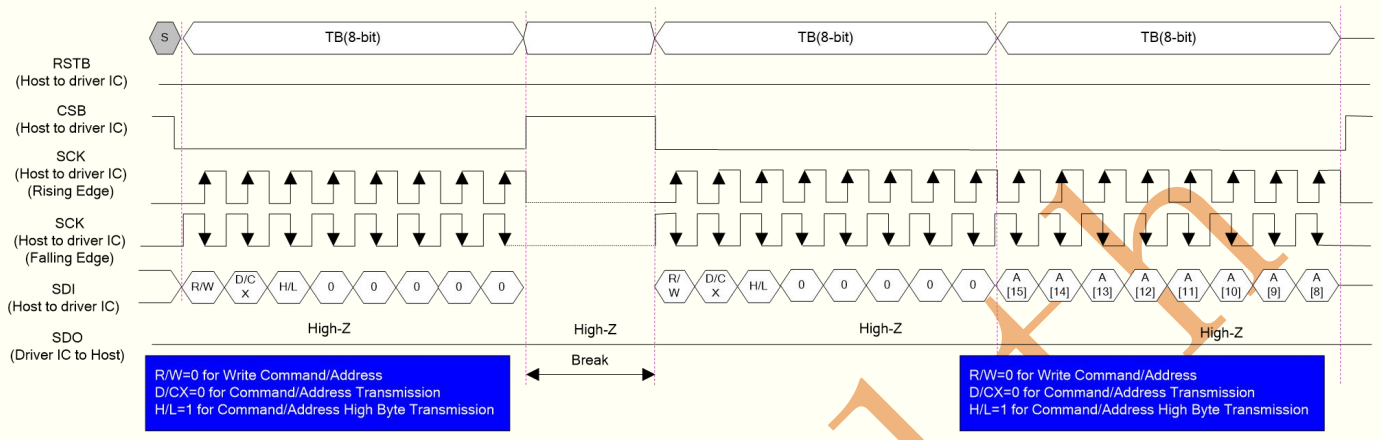
Symbol	Parameter	Min.	Typ.	Max.	Units
t_{INIT_MASTER}	MIPI Tx initialize time	10	-	-	ms
t_{RESW}	Reset "L" pulse width	Note	-	-	μs
t_{INIT_SLAVE}	MIPI Rx initialize time	4	-	-	ms
$t_{INTERNAL\_DELAY}$	Internal delay time.	500	-	-	μs

Note: See section "Reset Input Timing"

6.3 Data transfer break and recovery

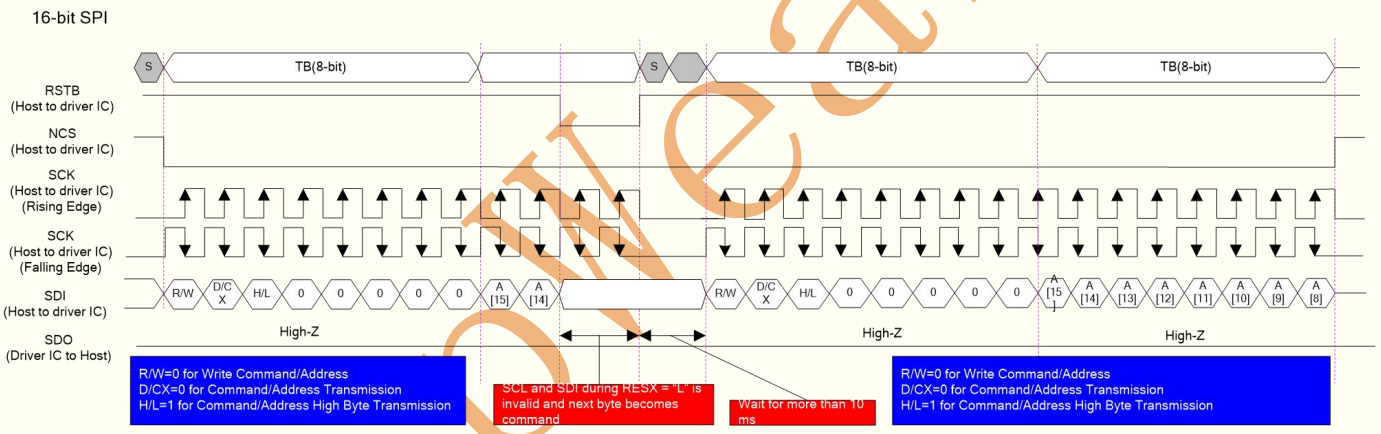
If there is a break in data transmission by CSB pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have Reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSB) is next activated after.

16-bit SPI



If there is a break in data transmission by RSTB pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have Reset the interface such that it will be ready to receive command data again when the chip select pin (CSB) is activated after RSTB have been in high state.

16-bit SPI



Serial bus protocol, write mode-interrupted by RSTB

The MCU can create a break condition when it is forcing DSI data lanes in the LP-11 mode The CH13613 stops to control DSI data lanes (change from a transmitter mode to a received mode) if it was controlling DSI data lanes as a transmitter when the MCU is forcing DSI data lanes in the LP-11.
The break condition can be done any time when the MCU or the driver IC is controlling DSI data lanes e.g. the driver IC is sending data to the MCU.

6.4 Interface Pause

16-bit SPI Interface Pause
16-bit SPI interface does not support “Pause Mode”.

MIPI Interface Pause
Pause can be done on DSI between Packets when they are sent to same or different receiver (Virtual Channel (VC)) e.g.
1) Same receiver: Packet 1 (VC=00) ⇒ Packet 2 (VC=00) ⇒ Packet 3 (VC=00) ⇒ …
2) Different receiver: Packet 1 (VC=00) ⇒ Packet 2 (VC=01) ⇒ Packet 3 (VC=10) ⇒ …
The means that “⇒ ” symbol means a pause on DSI.

7 Function Description

7.1 Power On/Off Sequence

During power off, if AMOLED is in the Sleep Out mode, VDDA/VDDB/VDDIO/VDDR must be powered down minimum 5 frames after RSTB has been released.
During power off, if AMOLED is in the Sleep In mode, VDDA/VDDB/VDDIO/VDDR can be powered down minimum 0msec after RSTB has been released.
Notes:
1. There will be no damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RSTB line is not held stable by host during Power On Sequence as defined in section “power Level Mode”, then it will be necessary to apply a Hardware Reset (RSTB) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. There is not a limit for Rise/Fall time on VDDA/VDDB/VDDIO/VDDR.
6. The display module can also initialize and calibrate DSI-CLK+/- and DSI-D0+/- lanes within 10ms after LP-11 (Clock and Data Channels), VDDA/VDDB/VDDIO/VDDR are applied and H/W Reset is not active (5ms is as same as the Reset Cancel Time).

Power on sequence

The Power on sequence has been applied following Fig1, otherwise correct functionality is not guaranteed.

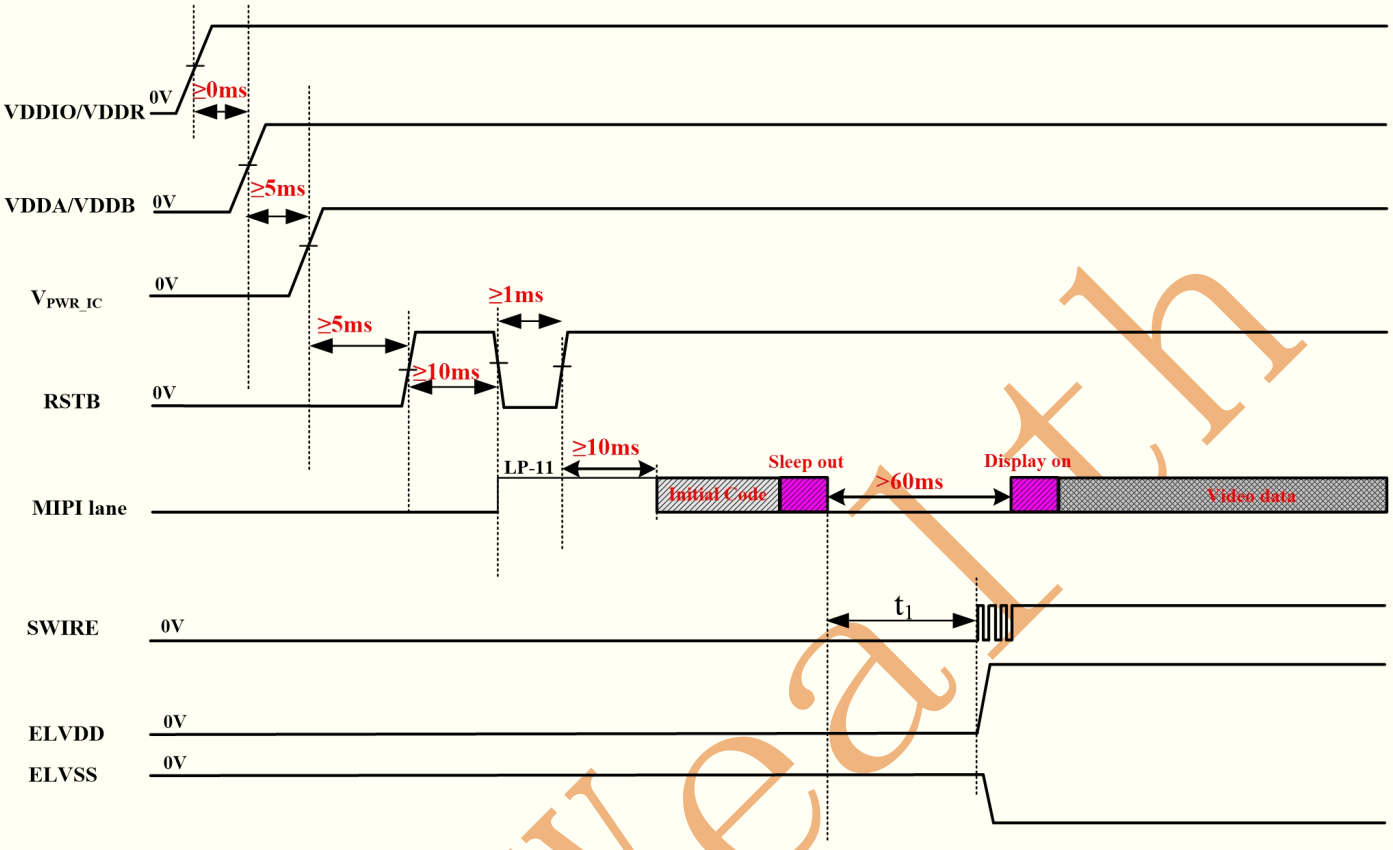


Fig 1 Power on sequence

Note1: t1 is ELVDD/ELVSS set up time, is controlled by SWIRE_ONF[5:0];
Note3: V_{PWR_IC} is the power of Power IC for ELVDD/ELVSS;

Power off sequence

The Power off sequence have been applied following Fig2, otherwise correct functionality is not guaranteed.

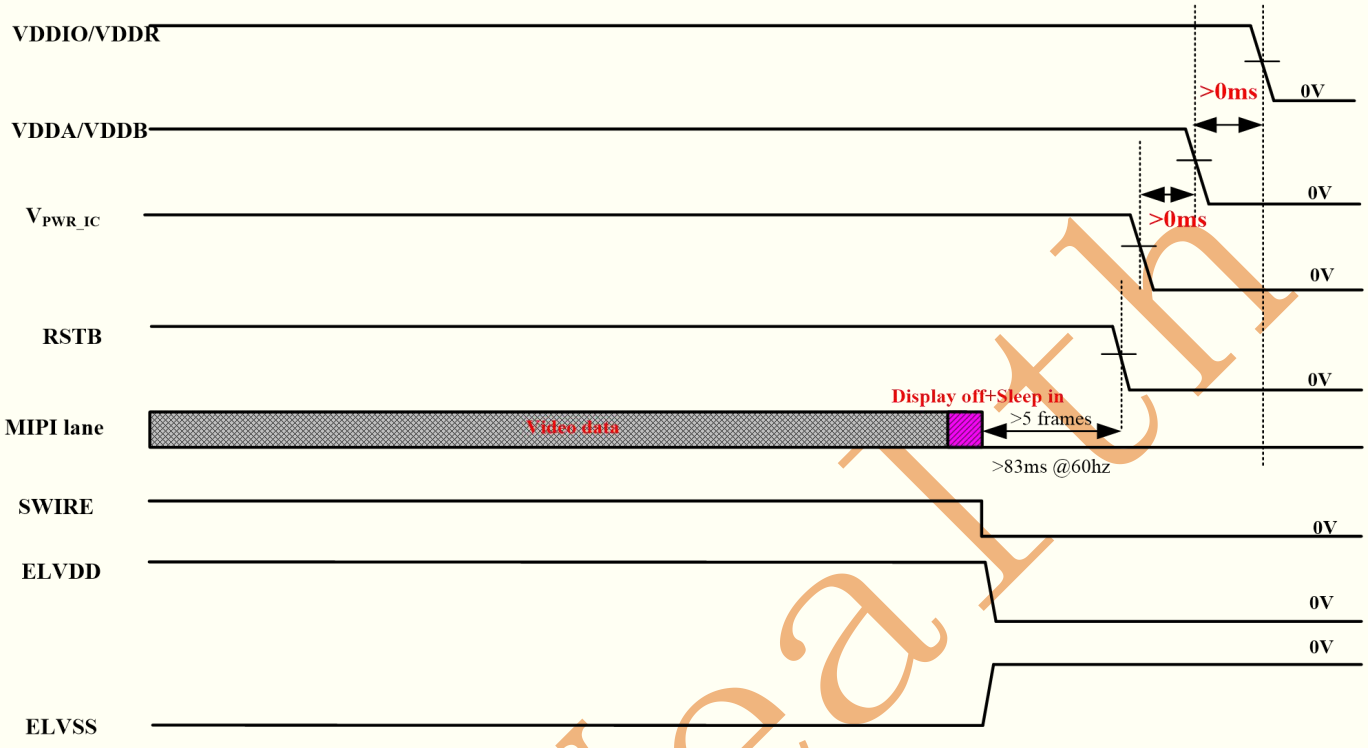


Fig 2 Power off sequence

Note1: V_{PWR_IC} is the power of Power IC for ELVDD/ELVSS;

Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

7.2 Power Level Modes

Definition

Four level modes are defined they are in order of maximum power consumption to minimum power consumption:

Normal Mode On (full display), Sleep Out.
In this mode, the display is able to show maximum 16.7M colors.

Normal Mode On, Idle Mode On, Sleep Out
In this mode, the display is able to show maximum 16.7M colors (include 8 colors).

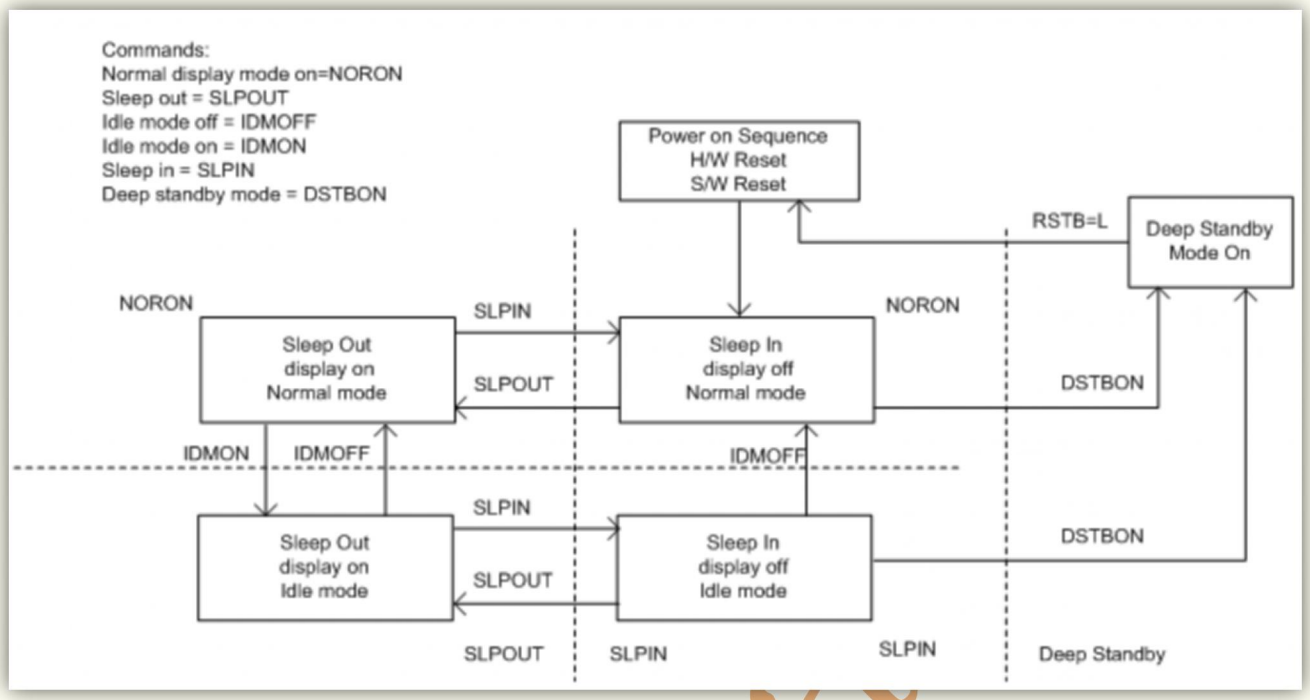
Sleep In Mode.
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDIO power supply.

Deep Standby Mode.
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working.

Power Off Mode
In this mode, VDDIO/VDDR and VDDA/VDDB are removed.

NOTE: Mode 4 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RSTB=L). Mode 4 is entered only when both power supplies for I/O and analog circuits are removed.

Power Level Mode Flow Chart



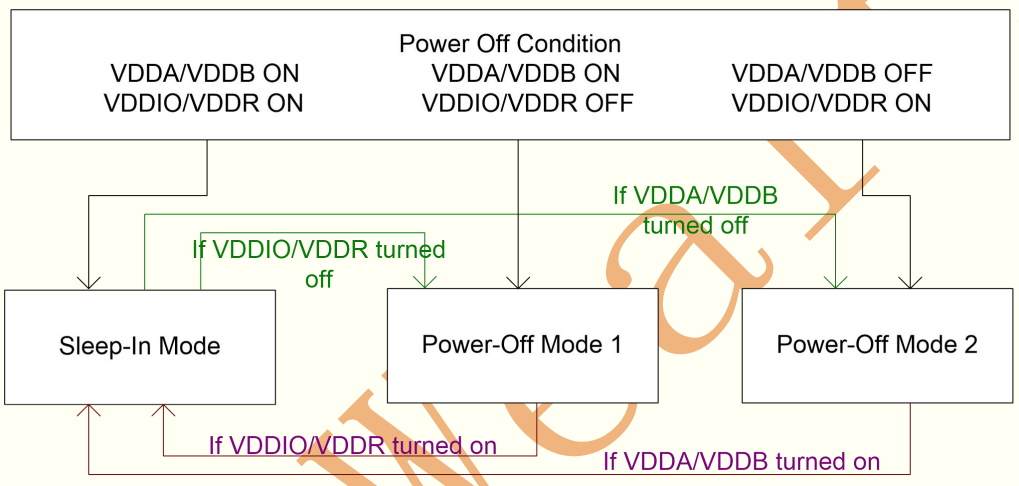
NOTES:
1) There is not any abnormal visual effect when there is changing from one power mode to another power mode.
2) There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode

The following table represents the registers its mode state.

Mode	Register	Control	
		Enter	Exit
Sleep in mode	Keep	Command	
Deep-standby mode	Loss	Command	RSTB pin
RSTB=L	Default Value	Reset(H/W)	

The condition for irregular power off mode is shown below:

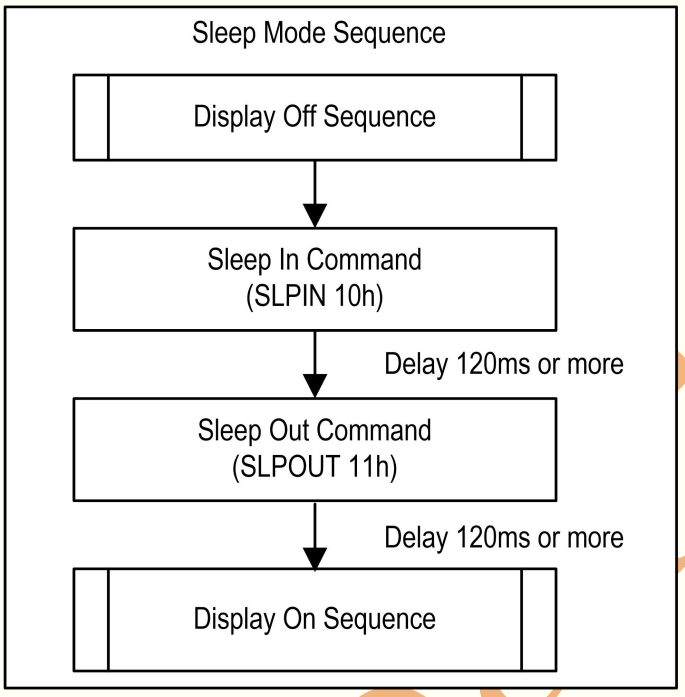
Power Off Mode	VDDA/VDDB	VDDIO/VDDR	RSTB	I/O
Mode 1	ON	OFF	H or L	L
Mode 2	OFF	ON	H or L	L



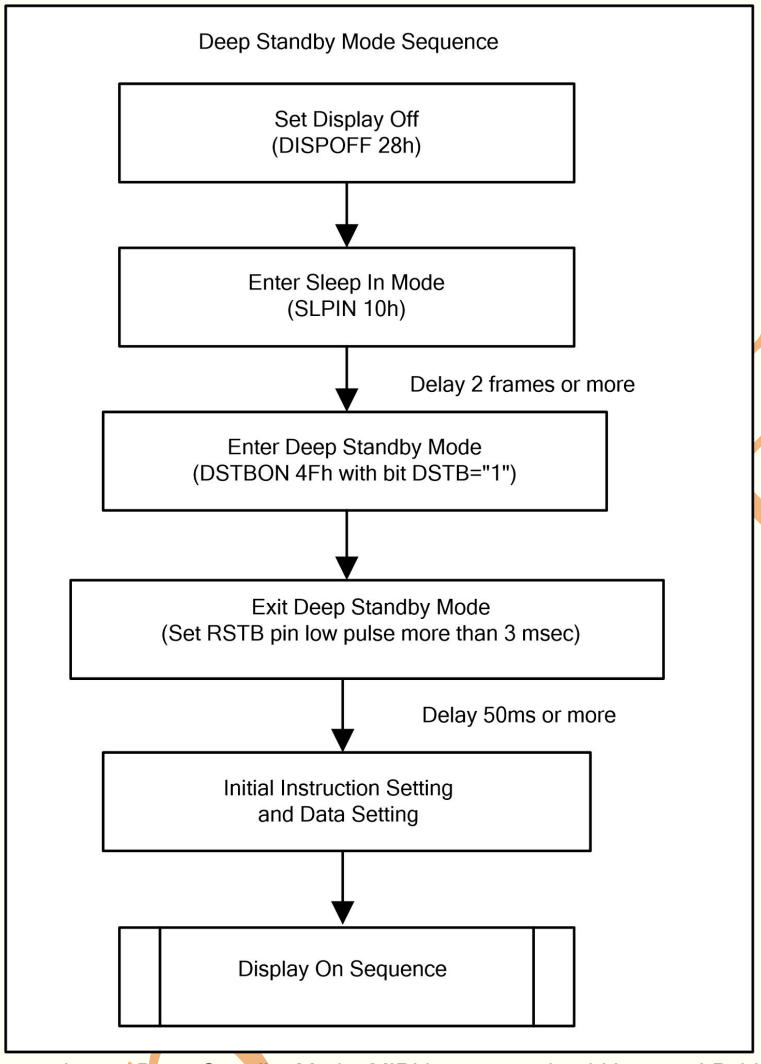
7.3 Instruction Setting Sequence

When setting instruction to the CH13613, the sequences shown in below figure must be followed to complete the instruction setting.

Sleep In/Out Sequence



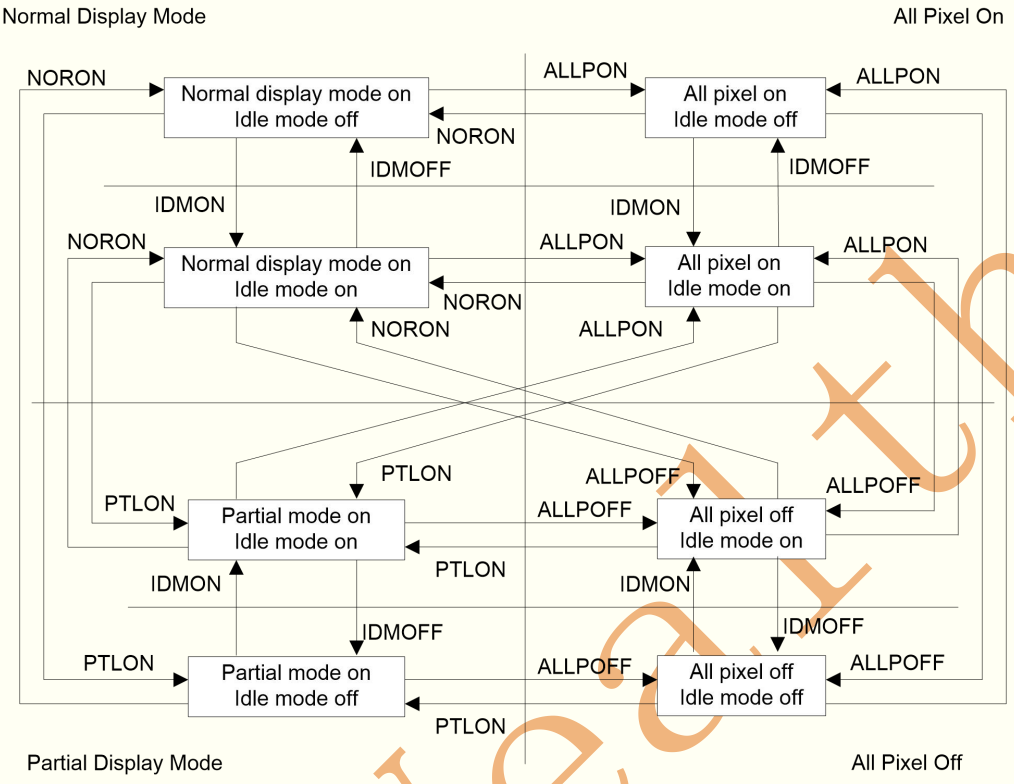
Deep Standby Mode Enter/Exit Sequence



Note: When using MIPI interface and enter Deep Standby Mode, MIPI lane state should keep to LP-00 or enter ULPM.

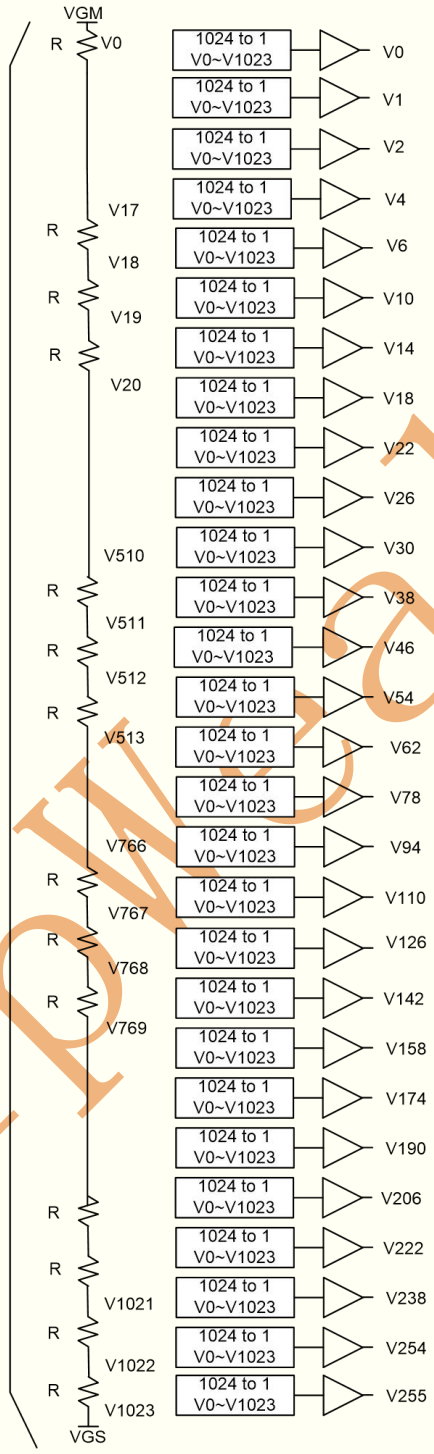
7.4 Basic Display Mode

The CH13613 has some basic operation modes which are Normal Display Mode, Idle Mode, All Pixel On and All Pixel Off for panel display. User can change these display modes for each other is illustrated below.



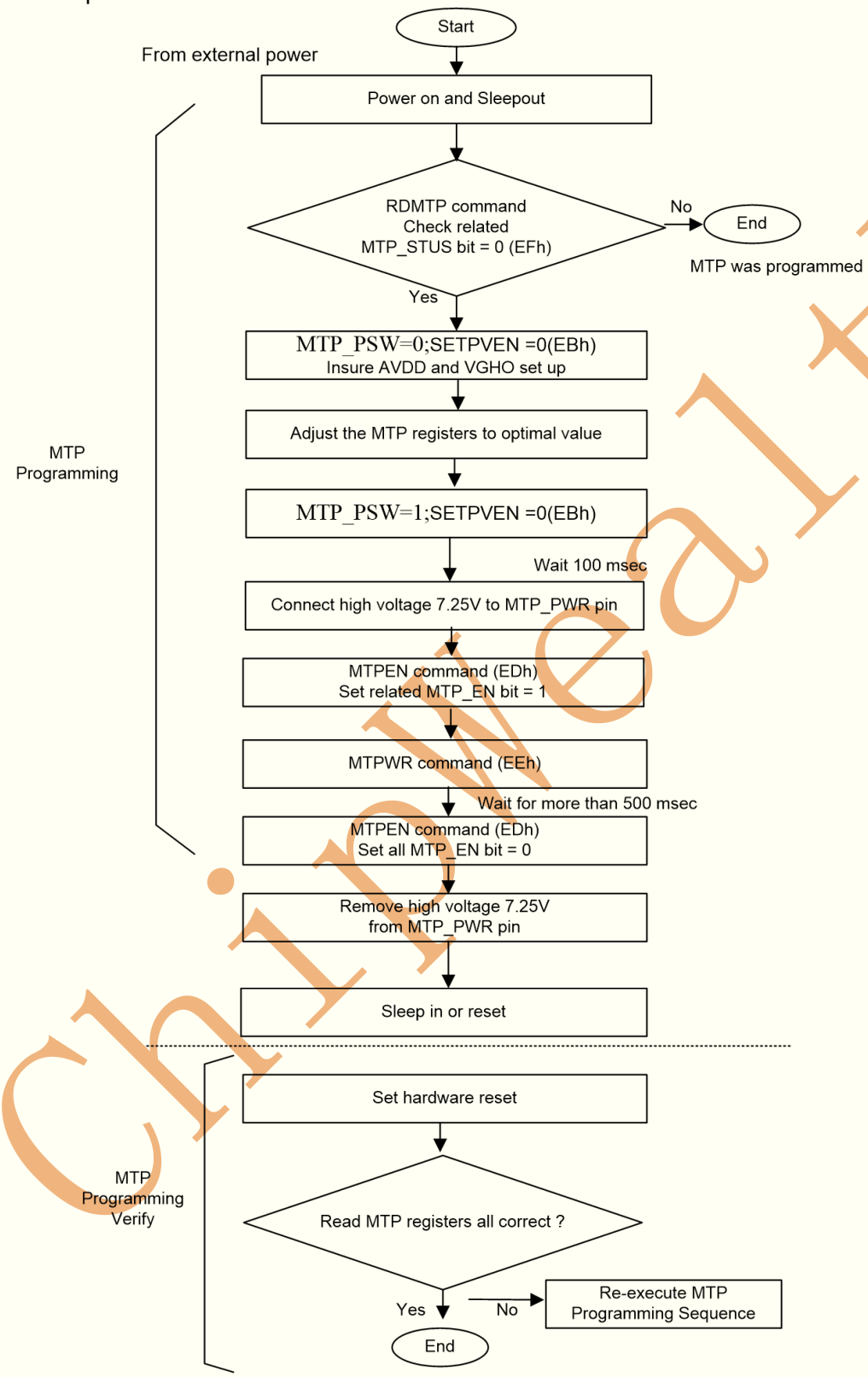
7.5 Gamma characteristic correction function

The structure of grayscale amplifier is shown as below. The 1024 voltage levels between VGM and VGS are determined by the reference adjustment register, the amplitude adjustment register and the micro-adjustment register.
There are 28 key point for Gamma correction.

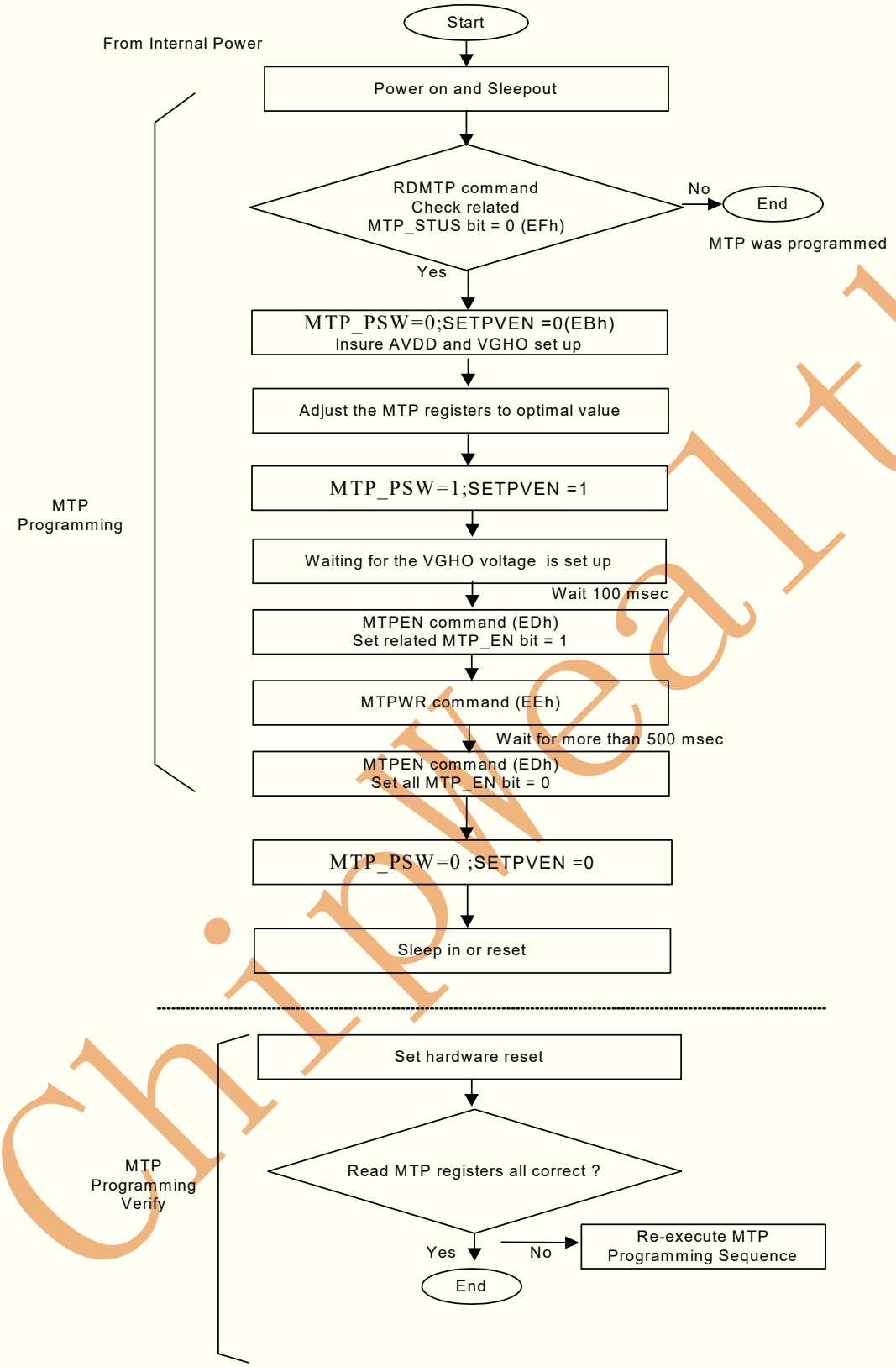


7.6 MTP Write Sequence

1) External power

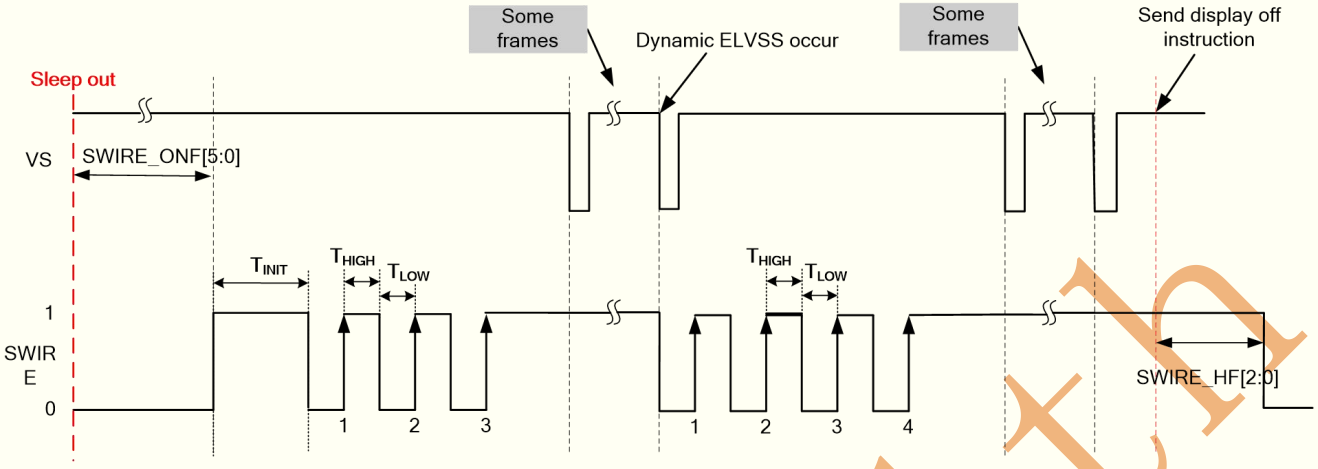


2) Internal Power


From Internal Power
Start
Power on and Sleepout
RDMTP command
Check related
MTP_STUS bit = 0 (EFh)
No
End
MTP was programmed
Yes
MTP_PSW=0;SETPVEN =0(EBh)
Insure AVDD and VGHO set up
Adjust the MTP registers to optimal value
MTP_PSW=1;SETPVEN =1
MTP
Programming
Waiting for the VGHO voltage is set up
Wait 100 msec
MTPEN command (EDh)
Set related MTP_EN bit = 1
MTPWR command (EEh)
Wait for more than 500 msec
MTPEN command (EDh)
Set all MTP_EN bit = 0
MTP_PSW=0 ;SETPVEN =0
Sleep in or reset
Set hardware reset
MTP
Programming
Verify
Read MTP registers all correct ?
Yes
No
Re-execute MTP
Programming Sequence
End

7.7 S-Wire Timing Control

S-wire interface is used to digitally communicate over a single cable with single-wire components. The CH13613 has a s-wire interface which allows programming the positive and negative output voltage of AMOLED panel power IC.



Parameter	Symbol	min.	typ.	max.	Unit
Power IC setup time	T_{INIT}	1	5	16	ms
SWIRE high time	T_{HIGH}	4	10	18	us
SWIRE low time	T_{LOW}	4	10	18	us

Note: The parameters of SWIRE pulse can be adjusted by SWIRECTR register.

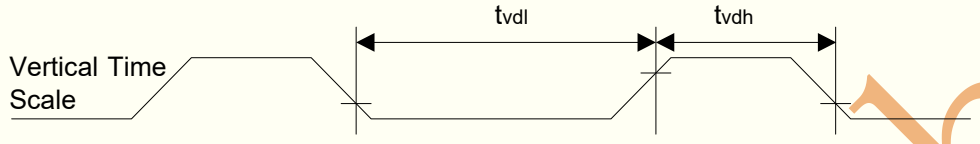
7.8 Tearing Effect information

7.8.1 Tear Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

7.8.2 Tearing Effect Line Modes

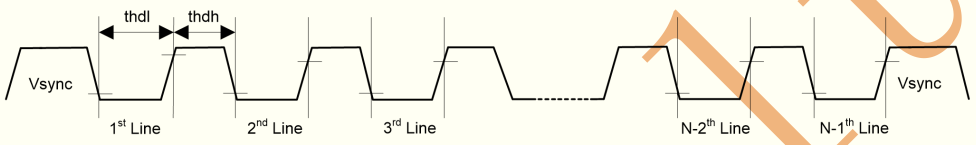
VS output1: The Tearing Effect Output signal consists of V-Blanking Information only:



Tvdh = The LCD display is not updated from the Frame Memory

Tvdl = The LCD display is updated from the Frame Memory(except Invisible Line –see below)

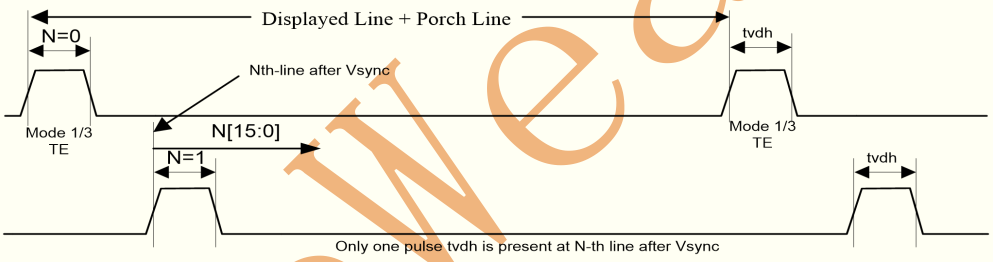
HS output: The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one Vsync and H-sync pulses per field.



Thdh = The LCD display is not updated from the Frame Memory

Thdl = The LCD display is updated from the Frame Memory(except Invisible Line-see above)

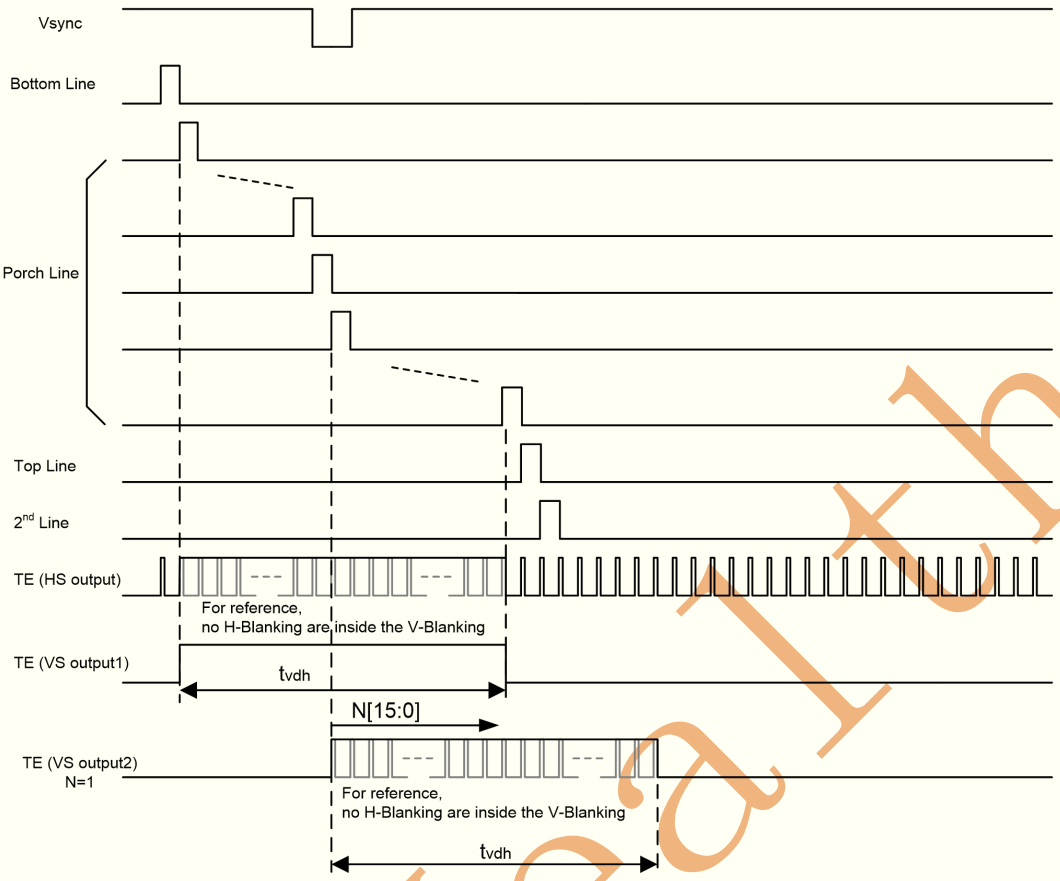
VS output2: This mode turn on the Tearing Effect output signal at line N after Vsync.



N = The N-th line, which set by register N[15:0] of command STESE(44h) after Vsyn.

The TE mode selection is described as below table

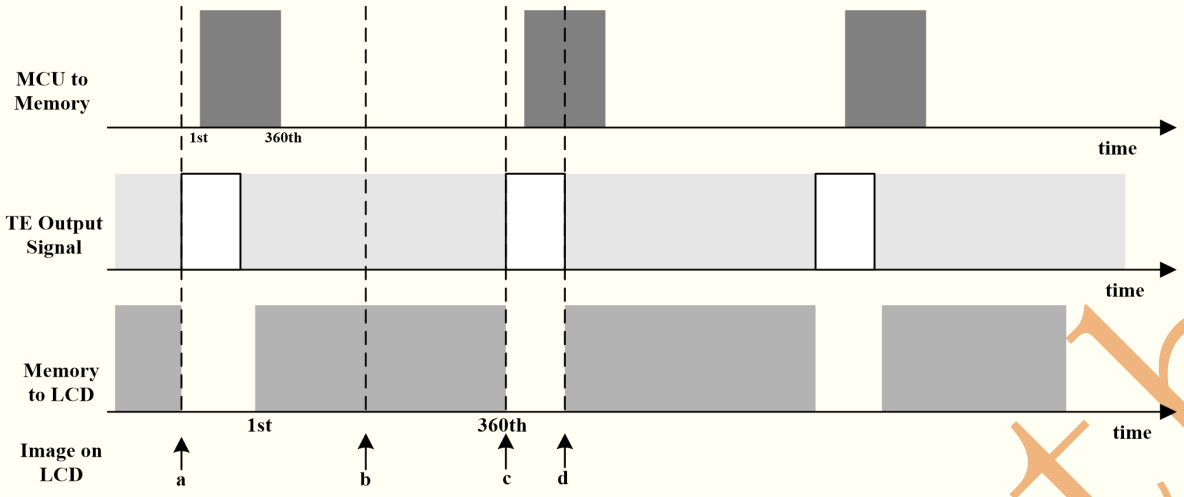
TEOFF(34h) TEON(35h) TELOM	STESL(44h) N[15:0]	TE Output
34h	X	TE off(output low)
35h with TELOM=0	N[15:0]=0	TE high in V-porch region（VS output1）
35h with TELOM=0	N[15:0]≠0	TE high at N-th line after Vsync（VS output2）
35h with TELOM =1	X	TE high in all V-porch and H-porch region（HS output）



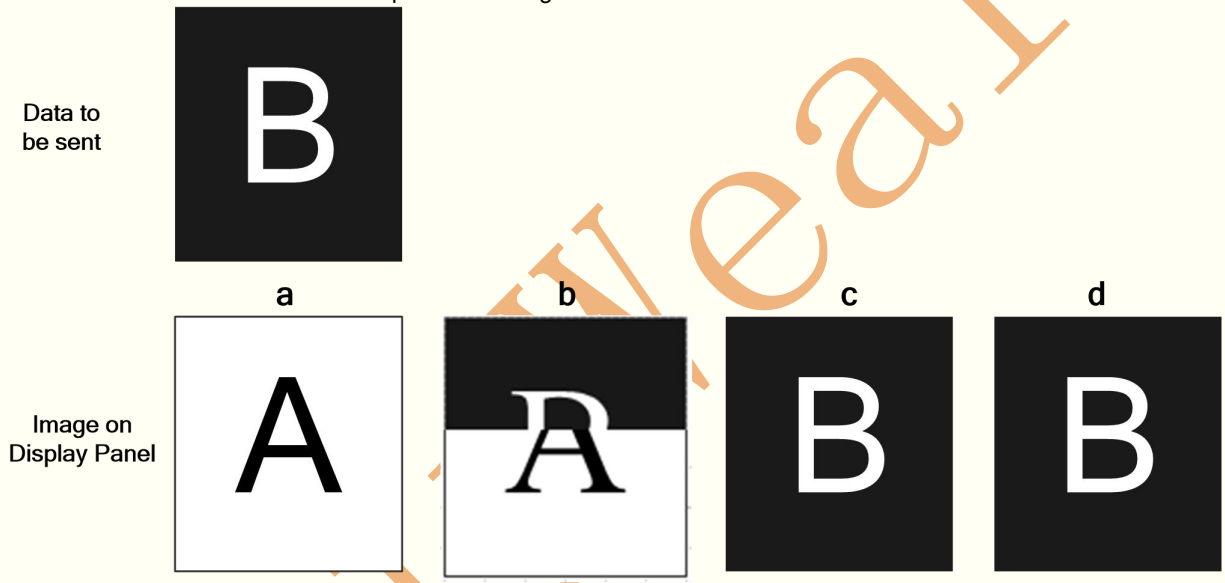
Notes:

1. During Sleep In Mode, the Tearing Output Pin is active Low.
2. N≦Displayed line + Porch line.
   Tvdh = width of porch line when N≦Displayed line
   tvdh = width of (Displayed line + Porch line-N) when N>Displayed line (falling edge of TE fixed at next Vsync)
3. Porch line = VBP+VFP.

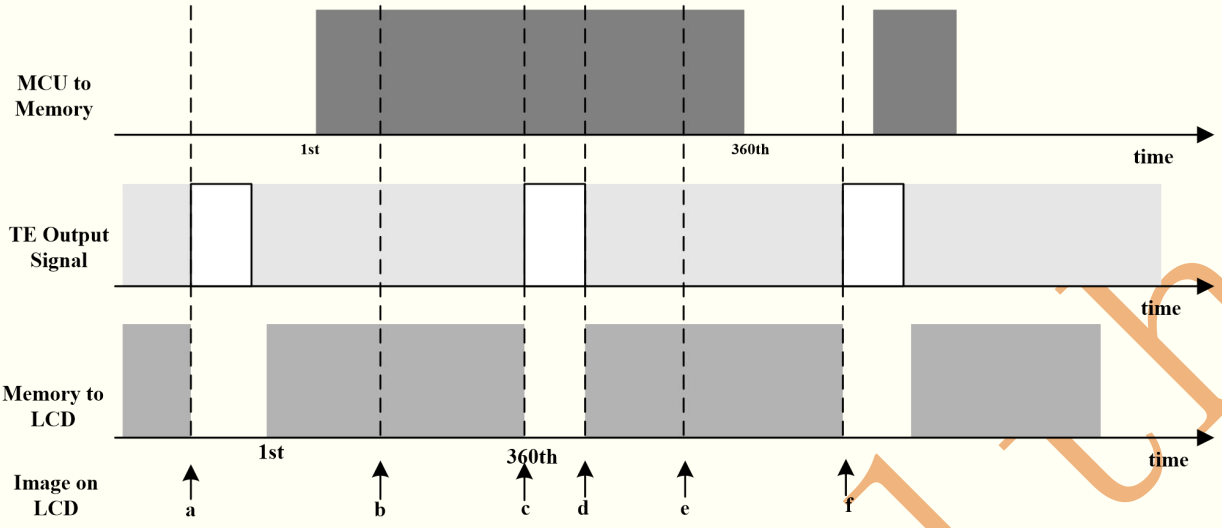
7.8.3 MPU Write is Faster Than Panel Read.



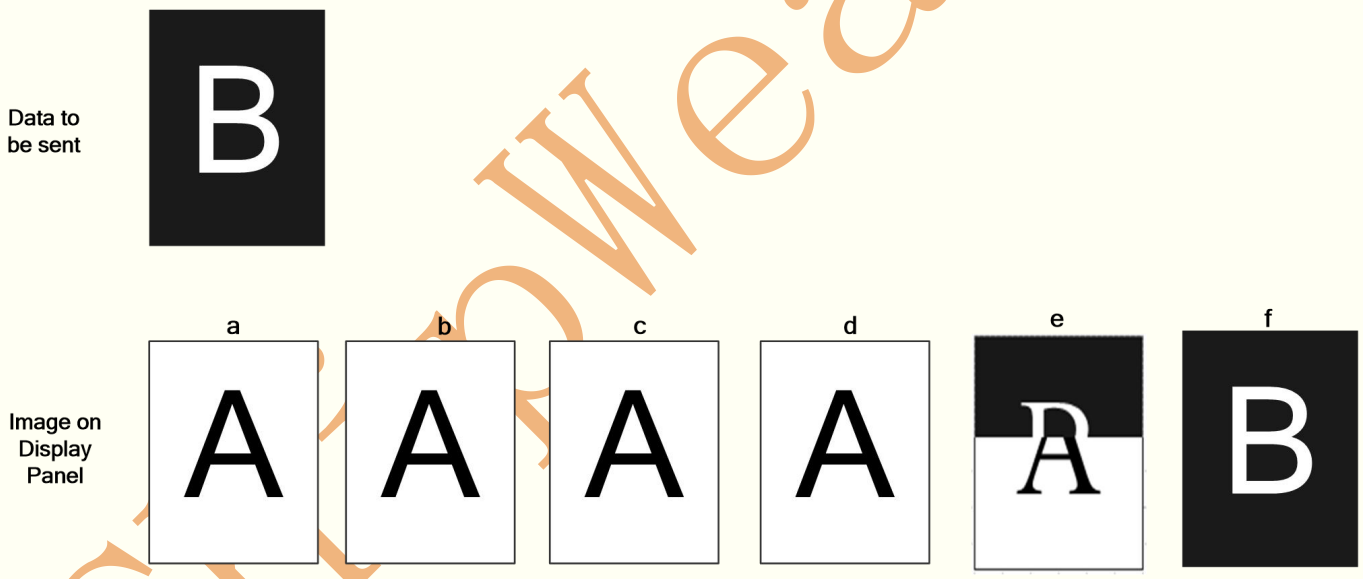
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



7.8.4 MPU Write is Slower Than Panel Read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



8 Electrical Specification

8.1 Absolute maximum ratings

Item	Symbol	Rating	unit
Supply voltage	VDDA,VDDB	-0.3 ~ +5.5	V
Supply voltage	VDDIO,VDDR	-0.3 ~ +5.5	V
Supply voltage (MV)	AVDD-VSS	-0.3 ~ +6.6	V
	AVEE-VSS	+0.3 ~ -5.5	V
Supply voltage (HV)	VGH-VSS	-0.3 ~ +15	V
	VGL-VSS	+0.3 ~ -15	V
	VGH-VGL (VGHO-VGLO)	-0.3 ~+32	V
Logic Input voltage range	VIN	-0.3 ~ VDDIO+0.3	V
Logic Output voltage range	VO	-0.3 ~ VDDIO+0.3	V
Differential Input Voltage	CLKP/N, D0P/N, D1P/N	-0.3 ~ +1.45	V
Operating temperature range	TOPR	-40 ~ +85	℃
Storage Temperature range	TSTG	-55 ~ +125	℃

NOTE:
1. VSS means VSSR, VSSG, VSSAM, VSSIO, AVSS and VSSB.
2. If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

8.2 DC characteristics

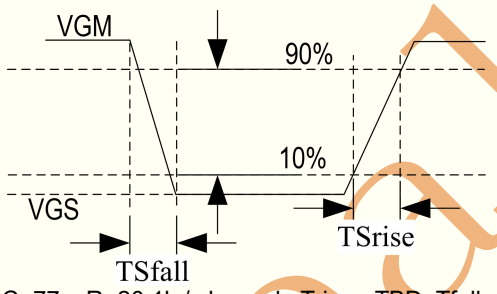
Basic characteristics

parameter	symbol	conditions	specification			Unit	Related Pins
			Min.	Typ.	Max.		
Power & Operation voltage							
Analog operating voltage	VDDA	Operating voltage	2.7	2.8	3.6	V	Note 1,2
Analog operating voltage	VDDB	Operating voltage	2.7	2.8	3.6	V	Note 1,2
Interface operating voltage	VDDIO	I/O supply voltage	1.65	1.8	3.6	V	Note 1,2
Logic operating voltage	VDDR	Logic supply voltage	1.65	1.8	3.6	V	Note 1,2
OTP programming voltage	MTP_PWR	OTP programming power supply	7.0	7.25	7.5	V	-
Input / Output							
Logic High Level Input Voltage	VIH	VDDIO=1.65~3.6	0.7VDDIO	-	VDDIO	V	Note 1,2,3
Logic Low Level Input Voltage	VIL	VDDIO=1.65~3.6	VSS	-	0.3VDDIO	V	Note 1,2,3
Logic High Level Output Voltage	VOH	VDDIO=1.65~3.6 IOH= -1.0 mA	0.8VDDIO	-	VDDIO	V	Note 1,2,5
Logic Low Level Output Voltage	VOL	VDDIO=1.65~3.6 IOL= +1.0 mA	VSS	-	0.2VDDIO	V	Note 1,2,5
Logic High level leakage (Except MIPI)	ILIH	Vin=0~VDDIO	-	-	1	μA	Note 1,2,3
Logic Low level leakage (Except MIPI)	ILIL	Vin=0~VDDIO	-1	-	-	μA	Note 1,2,3
Logic High level leakage (MIPI)	ILIH	Vin=0~DVDD	-	-	1	μA	Note 2,8
Logic Low level leakage (MIPI)	ILIL	Vin=0~DVDD	-1	-	-	μA	Note 2,8
DC/DC Converter Operation							
AVDD booster voltage	AVDD	-	4.5	5.6	6.5	V	Note 2,7
AVEE booster voltage	AVEE	-	-5.5	-5.5	-1*VDDB	V	Note 2,7
VREFP reference voltage	VREFP	-	0.5	1.5	5.0	V	Note 2,7
VREFN reference voltage	VREFN	-	-5.0	-3	-0.2	V	Note 2,7
VGHO reference voltage	VGHO	-	3.0	6.5	10.0	V	Note 2,7
VGLO reference voltage	VGLO	-	-10.0	-8	-3.0	V	Note 2,7
ELVDD reference voltage	VEP	-	0.5	4.6	5.0	V	Note 2,7
ELVDD output current capability	IVEP	VEP=4.6V/drop 50mV (AVDD=2*VDDB)	-	-	4.5	mA	Note 2,7
		VEP=4.6V/drop 50mV (AVDD=3*VDDB)	-	-	3.7	mA	Note 2,7
ELVSS reference voltage	VEN	-	-5.0	-2.4	-0.2,0	V	Note 2,7
ELVSS output current capability	IVEN	VEN=-4.5V/drop 50mV (AVEE=-2*VDDB)	-	-	4	mA	Note 2,7
		VEN=-2.5V/drop 50mV (AVEE=-VDDB)	-	-	3.5	mA	Note 2,7
VGH booster voltage	VGH	-	AVDD	8.4	2*AVDD	V	Note 2,6
VGL booster voltage	VGL	-	AVEE	-11.1	AVEE-AVDD	V	Note 2,6

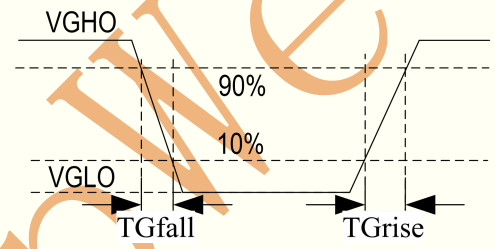
parameter	symbol	conditions	specification			Unit	Related Pins
			Min.	Typ.	Max.		
Voltage difference between VGH and VGL	VGHL	$\lvert VGH - VGL \rvert$	-	-	30	V	Note 2
Oscillator tolerance	Δ OSC	-40 ℃~ +85℃	-8	-	8	%	
Source Driver							
Gamma reference voltage	VGM	-	2.0	5.4	6.3	V	-
	VGS	-	0,0.2	2.15	4.5	V	

Output offset voltage	V_{OFFSET}	-	-	-	15	mV	Note 4
Output deviation voltage	Vdev	2.0V<Sout<5.0V	-	5	-	mV	Note 4
Output rising/falling Time	T_{SR}/T_{SF}	-	-	TBD	-	μs	Note 9
GOA Driver							
GOA rising/falling time	T_{GR}/T_{GF}	-	-	TBD	-	μs	Note10

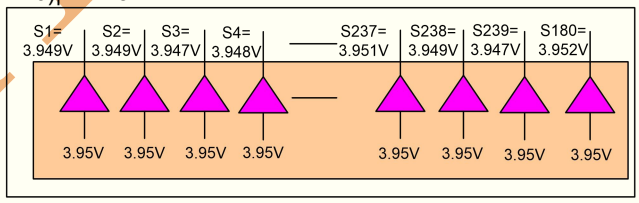
Note 1) VDDIO/ VDDR =1.65 to 3.6V, VDDA/VDDB=2.7 to 3.6V, VSS means VSSIO=DVSS=VSSG=VSSAM=VSSR=VSSB=0V, Ta=-40 ℃~ +85℃.
Note 2) when the measurements are performed with module. Measurement Points for all characteristics.
Note 3) RSTB, CSB, SCL, SDI, DSWAP, PSWAP, IM[1:0].
Note 4) Channel loading=18.5p, R=1.1k / channel, Ta=25 ºC after chop function.
Note 5) SDO, TE.
Note 6) VDDA/VDDB =2.8V, Ta=25 ºC, no load on panel and Iload=TBD mA, |Output Voltage – Target Voltage| < 100mV.
Note 7) VDDA/VDDB =2.8V, Ta=25 ºC, no load on panel and Iload=TBD mA, power pad serial resistor is smaller than maximum value.
Note 8) Vin = 0 to 1.2V, VDDA/VDDB =2.7 to 3.6V, VDDIO /VDDR=1.65 to 3.6V, VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 ℃~ +85℃.
Note 9) VGM=6.2V, VGS=1.2V, Ta=25 ºC, Channel loading=18.5p, R=1.1k / channel, Trise <TBD, Tfall <TBD;



Note 10) VGHO=7V,VGLO=-7V, Ta=25 ºC,C=77p, R=20.1k / channel , Trise <TBD, Tfall <TBD;



Measurement Points for all characteristics.
- When 2.0V <=Sout <= 5.0V
|(S1, S2, S3 …. , S240) – Average (S1, S2, S3, …. , S240)| <= 5mV
- Sout=V0~V255
$|S_{Target}$ – Average (S1, S2, S3, …. , S240)| <= 15mV

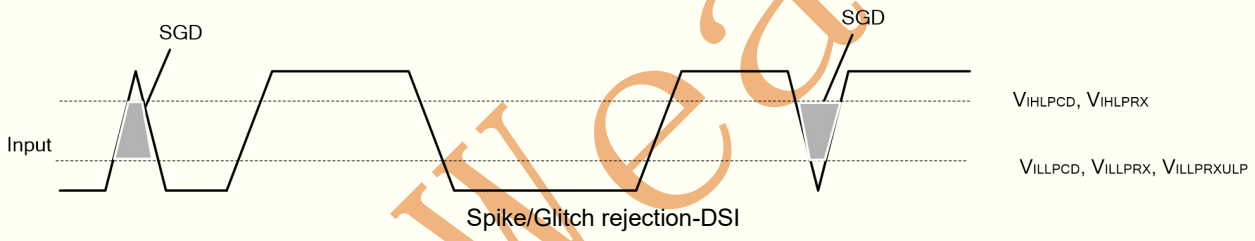


Source output deviation

DC characteristics for DSI LP Mode

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1, D2, D3)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1, D2, D3)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

Note 1: VDDIO/ VDDR =1.65~3.6V, VDDA/VDDB=2.7 to 3.6V, VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 to +85 ºC.
Note 2: DSI high speed is off.
Note 3: Peak interference amplitude max.200mV and interference frequency min.450MHz.

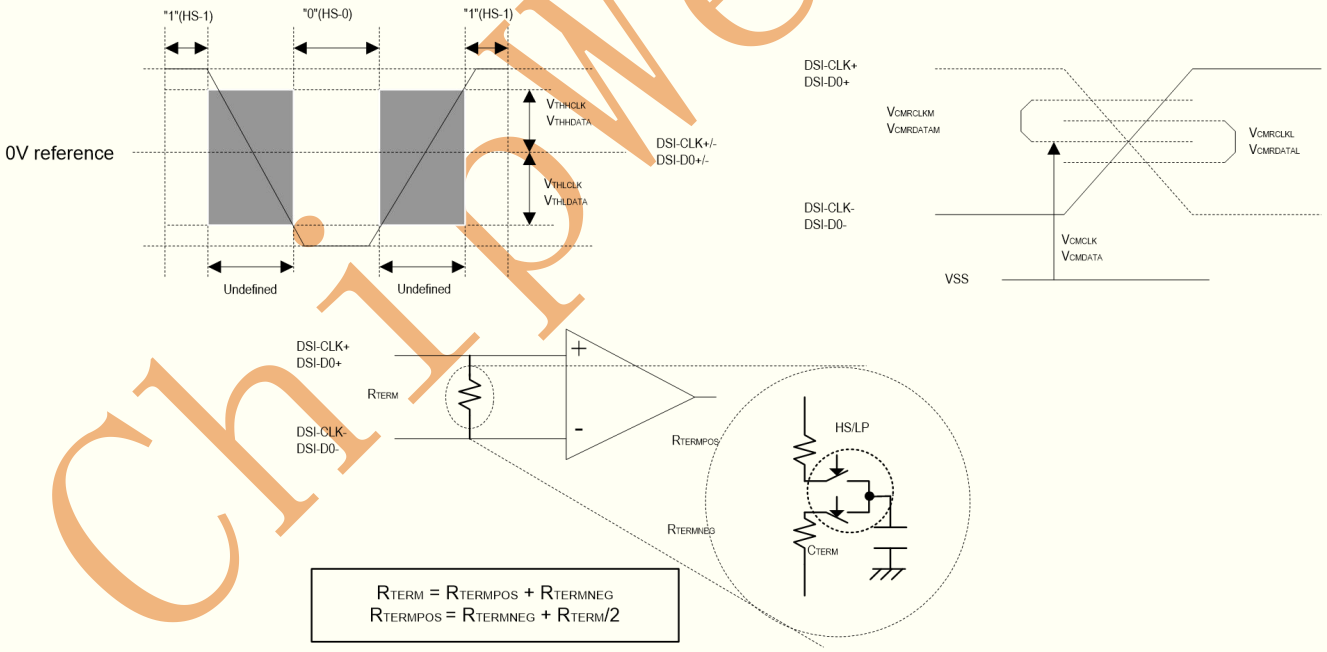


Spike/Glitch rejection-DSI

DC characteristics for DSI HS Mode

Parameter	Symbol	Condition	Specification			Unit
			Min.	Tpy.	Max.	
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≦450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≧450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

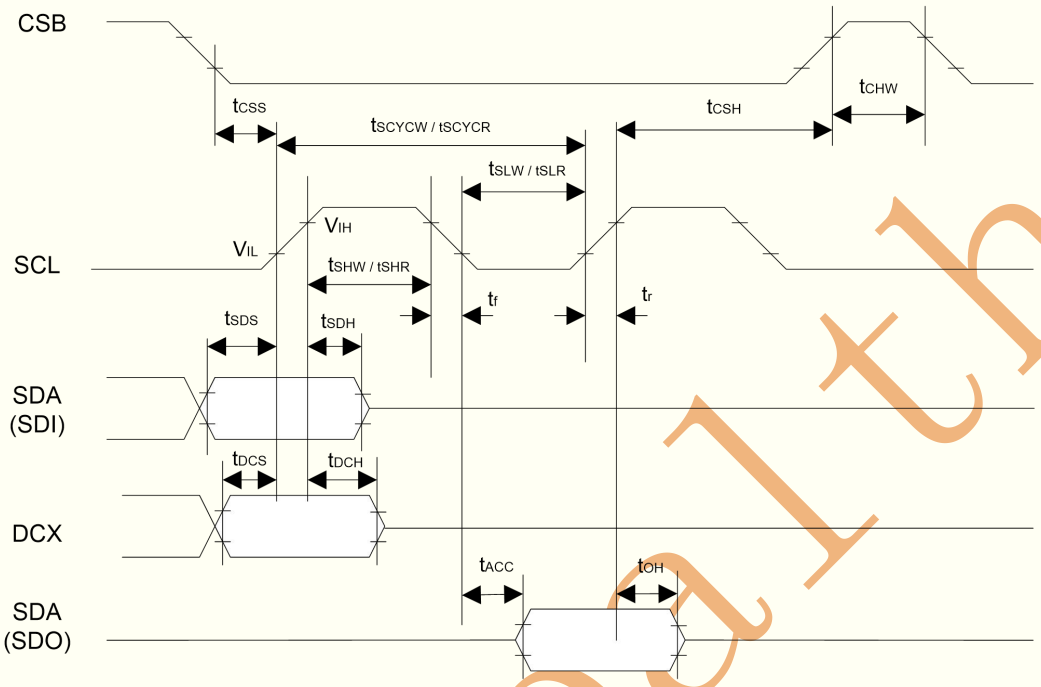
Note 1: VDDIO/ VDDR =1.65~3.6V, VDDA/VDDB=2.7 to 3.6V,VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 to +85 ºC.
Note 2: Includes 50mV (-50mV to 50mV) ground difference.
Note 3: Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$
Note 4: Without 50mV (-50mV to 50mV) ground difference.
Note 5: Dn=D0 and D1



Differential voltage range, termination resistor and common mode voltage

8.3 AC Characteristics

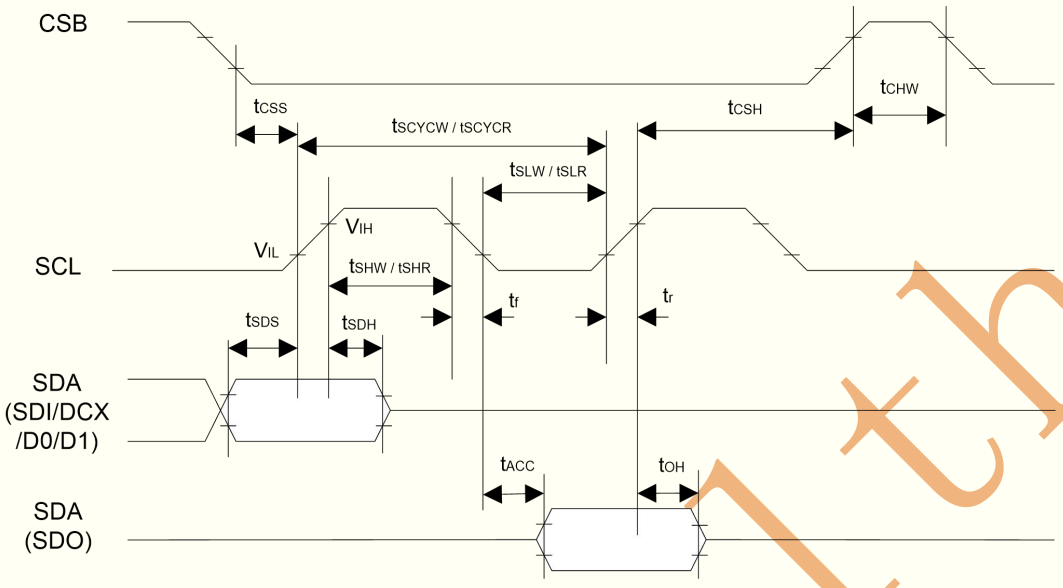
8bit/9bit SPI Connect with Host Characteristics



Signal	Symbol	Parameter	Min.	Max.	Unit	Description
SCL	t_{SCYCW}	Serial clock cycle (Write)	20	-	ns	
	t_{SHW}	SCL “H” pulse width (Write)	9	-	ns	
	t_{SLW}	SCL “L” pulse width (Write)	9	-	ns	
	t_{SCYCR}	Serial clock cycle (Read register)	300	-	ns	
	t_{SHR}	SCL “H” pulse width (Read register)	140	-	ns	
	t_{SLR}	SCL “L” pulse width (Read register)	140	-	ns	
SDI (SDO) DCX	t_{SDS}/t_{DCS}	Data setup time	5	-	ns	
	t_{SDH}/t_{DCH}	Data hold time	5	-	ns	
	t_{ACC}	Access time	-	120	ns	
	t_{OH}	Output disable time	5	-	ns	
CSB	t_{CHW}	Chip select “H” pulse width	45	-	ns	
	t_{CSS}	Chip select setup time	10	-	ns	
	t_{CSH}	Chip select hold time	10	-	ns	

Note 1: VDDIO/VDDR =1.65 to 3.6V, VDDA/VDDB =2.7 to 3.6V, VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 to +85 ºC.

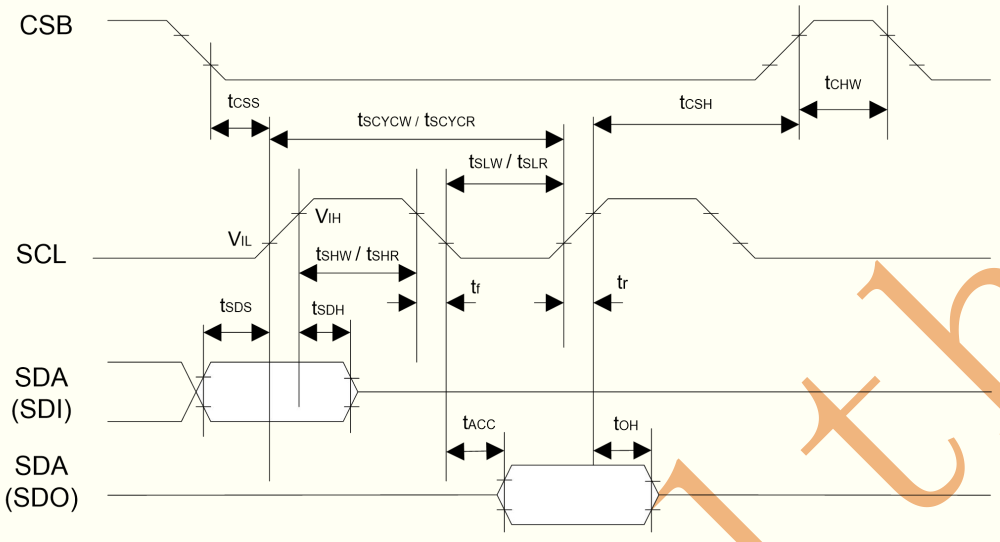
Quad SPI Connect with Host Characteristics



Signal	Symbol	Parameter	Min.	Max.	Unit	Description
SCL	t_{SCYCW}	Serial clock cycle (Write)	20	-	ns	
	t_{SHW}	SCL “H” pulse width (Write)	9	-	ns	
	t_{SLW}	SCL “L” pulse width (Write)	9	-	ns	
	t_{SCYCR}	Serial clock cycle (Read register)	100	-	ns	
	t_{SHR}	SCL “H” pulse width (Read register)	46	-	ns	
	t_{SLR}	SCL “L” pulse width (Read register)	46	-	ns	
SDI (SDO) DCX	t_{SDS}/t_{DCS}	Data setup time	5	-	ns	
	t_{SDH}/t_{DCH}	Data hold time	5	-	ns	
	t_{ACC}	Access time	-	40	ns	
	t_{OH}	Output disable time	5	-	ns	
CSB	t_{CHW}	Chip select “H” pulse width	45	-	ns	
	t_{CSS}	Chip select setup time	10	-	ns	
	t_{CSH}	Chip select hold time	10	-	ns	

Note 1: VDDIO/VDDR =1.65 to 3.6V, VDDA/VDDB =2.7 to 3.6V, VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 to +85 ºC.

16-bit SPI characteristics



Signal	Symbol	Parameter	Min.	Max.	Unit	Description
SCL	t_{SCYCW}	Serial clock cycle (Write)	100	-	ns	
	t_{SHW}	SCL “H” pulse width (Write)	40	-	ns	
	t_{SLW}	SCL “L” pulse width (Write)	40	-	ns	
	t_{SCYCR}	Serial clock cycle (Read register)	300	-	ns	
	t_{SHR}	SCL “H” pulse width (Read register)	140	-	ns	
	t_{SLR}	SCL “L” pulse width (Read register)	140	-	ns	
SDI (SDO)	t_{SDS}	Data setup time	20	-	ns	
	t_{SDH}	Data hold time	20	-	ns	
	t_{ACC}	Access time	-	120	ns	
	t_{OH}	Output disable time	5	-	ns	
CSB	t_{CHW}	Chip select “H” pulse width	45	-	ns	
	t_{CSS}	Chip select setup time	20	-	ns	
	t_{CSH}	Chip select hold time	50	-	ns	

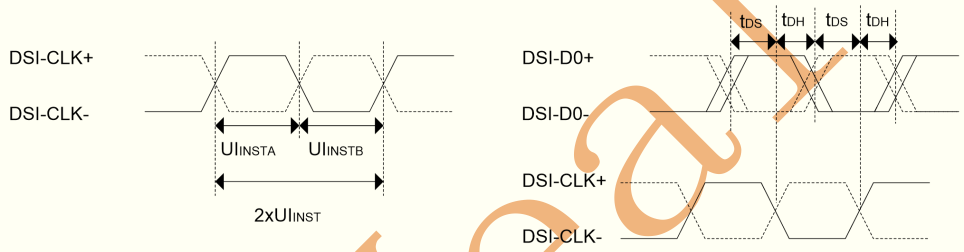
Note 1: VDDIO/ VDDR =1.65 to 3.6V, VDDA/VDDB =2.7 to 3.6V, VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 to +85 ºC

MIPI DSI Timing Characteristics

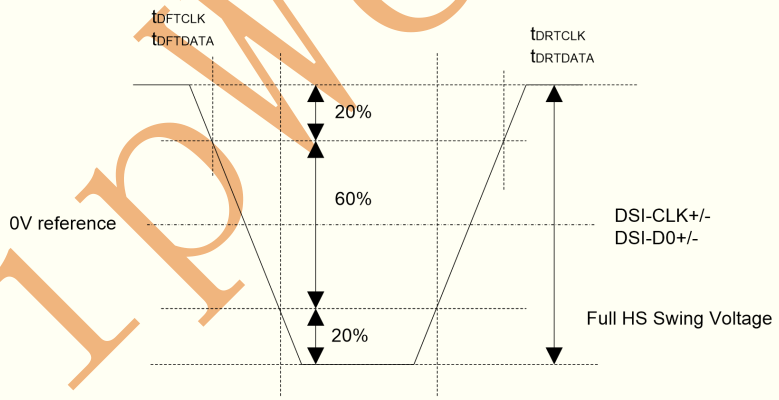
High Speed Mode

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
DSI-CLK+/-	$2\times UI_{INST}$	Double UI instantaneous	4	-	TBD	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halves ($UI = UI_{INSTA} = UI_{INSTB}$)	2	-	TBD	ns	
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15×UI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15×UI	-	-	ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3×UI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3×UI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3×UI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3×UI	ps	

Note 1: VDDIO/ VDDR =1.65~3.6V, VDDA/VDDB=2.7 to 3.6V, VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 to +85 ºC.
Note 2) Dn=D0 and D1.



DSI clock channel timing

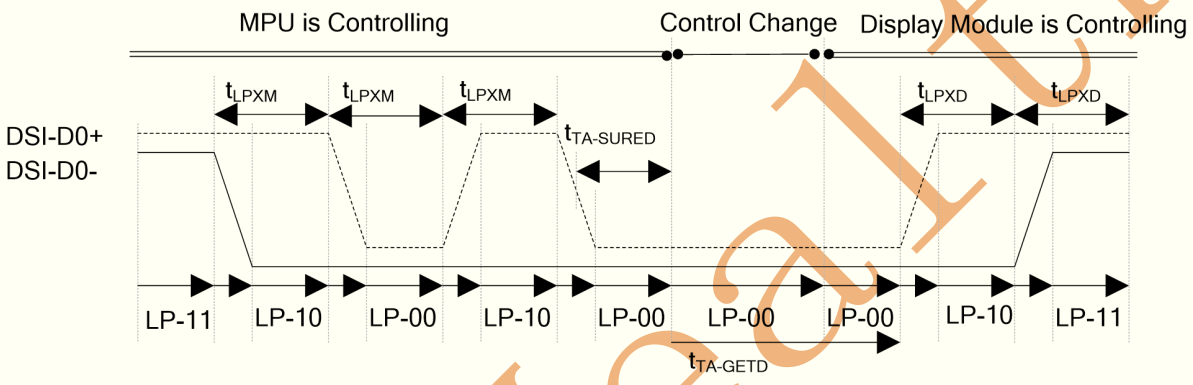


Rising and falling time on clock and data channel

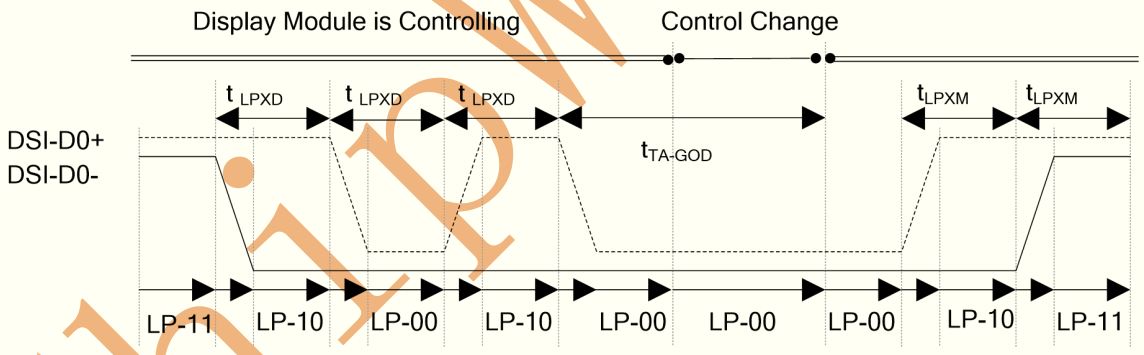
Low Power Mode

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
DSI-D0+/-	t_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	t_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$t_{TA-SURED}$	Time-out before the MPU start driving	t_{LPXD}	-	$2\times t_{LPXD}$	ns	Output
DSI-D0+/-	$t_{TA-GETD}$	Time to drive LP-00 by display module	$5\times t_{LPXD}$	-	-	ns	Input
DSI-D0+/-	t_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4\times t_{LPXD}$	-	-	ns	Output

Note 1: VDDIO/ VDDR =1.65~3.6V, VDDA/VDDB=2.7 to 3.6V, VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 to +85 ºC.



Bus Turnaround (BAT) from MPU to display module Timing

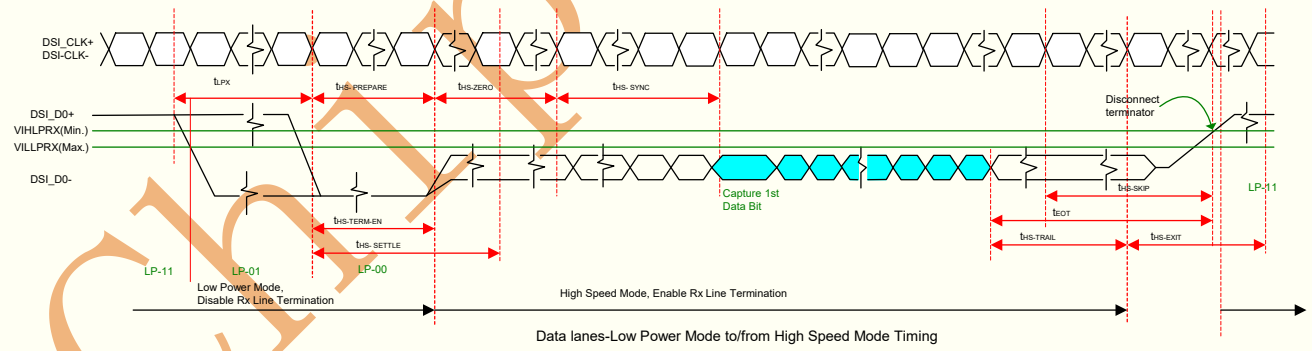


Bus Turnaround (BAT) from display module to MPU Timing

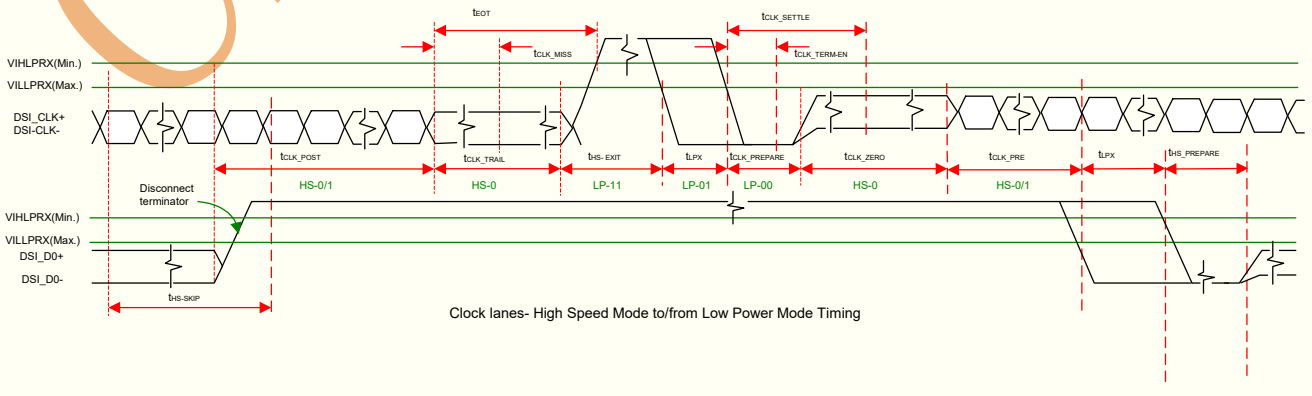
DSI Bursts

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	t_{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	$t_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40+4×UI	-	85+6×UI	ns	Input
DSI-Dn+/-	$t_{HS-TERM-EN}$	Time to enable data receiver line termination measured from when Dn crosses V_{ILMAX}	-	-	35+4×UI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	$t_{HS-SKIP}$	Time-out at display module to ignore transition period of EoT	40	-	55+4×UI	ns	Input
DSI-Dn+/-	$t_{HS-EXIT}$	Time to drive LP-11 after HS burst	**100**	-	-	ns	Input
DSI-Dn+/-	$t_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4×UI	-	-	ns	Input
High Speed Mode to/from Low Power Mode timing							
DSI-CLK+/-	$t_{CLK-POS}$	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	**60+52×UI**	-	-	ns	Input
DSI-CLK+/-	$t_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	$t_{HS-EXIT}$	Time to drive LP-11 after HS burst	**100**	-	-	ns	Input
DSI-CLK+/-	$t_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	$t_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	$t_{CLK-PREPARE}$ +$t_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	$t_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8×UI	-	-	ns	Input

Note 1: VDDIO/ VDDR =1.65~3.6V, VDDA/VDDB=2.7 to 3.6V,VSSIO=DVSS=VSSG=VSSAM=VSSR =VSSB=0V, Ta=-40 to +85 ºC.
Note 2: Dn=D0 and D1.

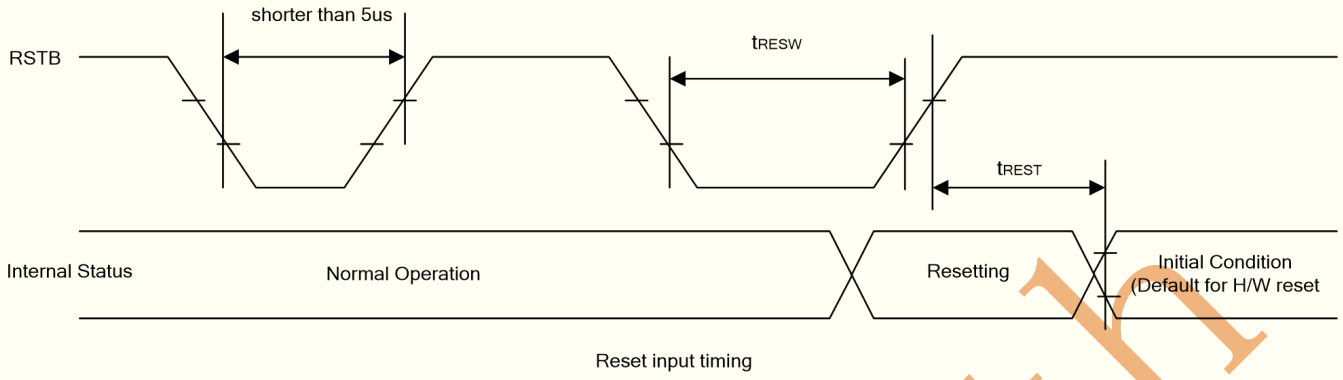


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

Reset Input Timing



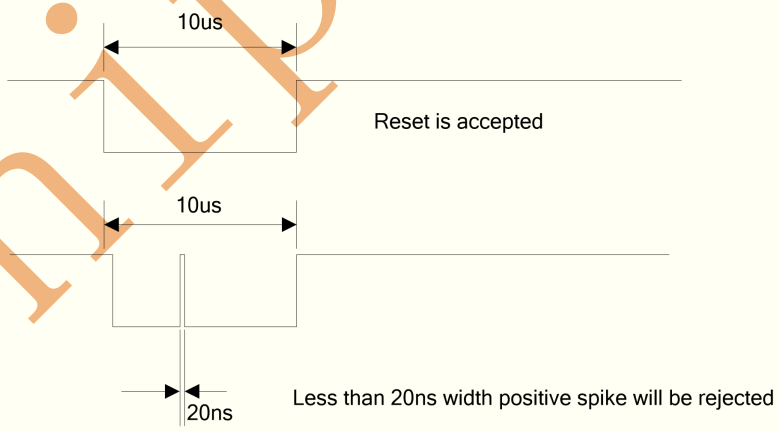
Reset input timing

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
RSTB	tRESW	Reset "L" pulse width (Note 1)	10	-	-	µs	-
	tREST	Reset complete time (Note 2)	-	-	10	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode

Note 1: Spike due to an electrostatic discharge on RSTB line does not cause irregular system Reset according to the table below.

RSTB Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

Note 2: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W Reset.
Note 3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W Reset complete time (t_{REST}) within 5ms after a rising edge of RSTB.
Note 4: Spike Rejection also applies during a valid Reset pulse as shown below:



Note 5: It is necessary to wait 5msec after releasing RSTB before sending commands. Also Sleep Out command cannot be sent for 120msec.

8.4 ESD Protection level

Model	Test Condition	Protection Level	Unit
Human Body Model	C = 100 pF, R = 1.5 kΩ	> 3000	V
Machine Model	C = 200 pF, R = 0.0 Ω	> 300	V

8.5 Latch-up protection level

The device will not latch up at trigger current levels less than ±200 mA.

8.6 Current consumption

Parameter	Symbol	Conditions	Specification			Unit
			Min.	Typ.	Max.	
Sleep out & display on mode	I total (I_{VDDA}+ I_{VDDB} + I_{VDDIO} + I_{VDDR})	VDDIO=VDDR=1.8V,VDDA/VDDB=2.8V, ta = 25ºC,white picture	-	TBD	-	mW
Sleep in mode (Note 1)	I total (I_{VDDA}+ I_{VDDB} + I_{VDDIO} + I_{VDDR})	VDDIO=VDDR=1.8V,VDDA/VDDB=2.8V, ta = 25ºC,white picture	-	TBD	-	μW
Deep standby mode (Note 2)	I total (I_{VDDA}+ I_{VDDB} + I_{VDDIO} + I_{VDDR})	VDDIO=VDDR=1.8V,VDDA/VDDB=2.8V, ta = 25ºC,white picture	-	TBD	-	μW

Note 1: For sleep in mode, MIPI in stop state (LP11). SPI Interface also included in it.
Note 2: All Interfaces included.

9 Data Sheet History

Version	Contents	Date
V1.0	Original	2021-11-01