NV3002A Datasheet

A-Si TFT LCD Single Chip Driver

240RGBx240 Resolution and 262K color

Version 1.2

Jun., 2020

1. Introduction

NV3002 is a single-chip SOC driver for 262,144-color, a-TFT liquid crystal display with maximum resolution of 240RGBx240 dots. It contains 360-channel source driver, a 32-channel GIP driver which used for dual-gate control, 129600-byte GRAM for graphic display data, internal precise power supply circuit which supports full color, 8-color display mode and sleep mode.

NV3002 provides parallel 8 bits data bus MCU interface, 3-/4-line serial peripheral interface (SPI). The display area can be specified in internal GRAM by window address function.

NV3002 is suitable for medium or small size protable products which low power characteristics is major concern. And it can make a display system with fewest componets.

an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution option:
  - 240(RGB)(H) x 240(V)
  - 160(RGB)(H) x 320(V)
  - 160(RGB)(H) x 160(V)
  - 144(RGB)(H) x 328(V)
  - 128(RGB)(H) x 128(V)
  - 128(RGB)(H)x 268(V)
  - 120(RGB)(H) x 240(V)
  - 120(RGB)(H) x 120(V)
  - 80(RGB)(H) x160(V)
- LCD Driver Output:
  - Source outputs: 360 channel
  - GIP outputs: 32 channel for dual-gate control
- Interface:
  - 8-bits interface with 8080-I/8080-II series MCU
  - 8-bits/9-bits Serial Peripheral Interface (SPI) and 2 data lane SPI
- On chip Build-In Circuits:
  - Timing generator
  - Oscillator
  - Graphic RAM: 129600-byte
  - DC/DC converter
  - OTP to store initial Register setting and factory default value
- Low-power consumption architecture used
- Power supplies Range:
  - I/O and digital voltage (IOVCC)：1.65V ~ 3.6V
  - Analog voltage range (VCIB): 2.5V ~ 3.6V
- Output Voltage Range:
  - Source/Gamma power supply voltage

- GVDD - GVCL = 6.4V ~-4.6V
- Gate driver output voltage
- VGH - AGNDB = 10.8V ~ 13.8V
- VGL - AGNDB = -12.2V ~ -8.9V
- VGH - VGL ≦26V
- VCOM connect to DGND

◆ Display color:

- Normal mode: Full color, 262K-color (color depth selectable)
- Idle mode: 8-color

◆ Driving Algorithm：Dot/column inversion

◆ Power saving mode: Sleep mode

◆ Operate temperature range: -30℃to 85℃

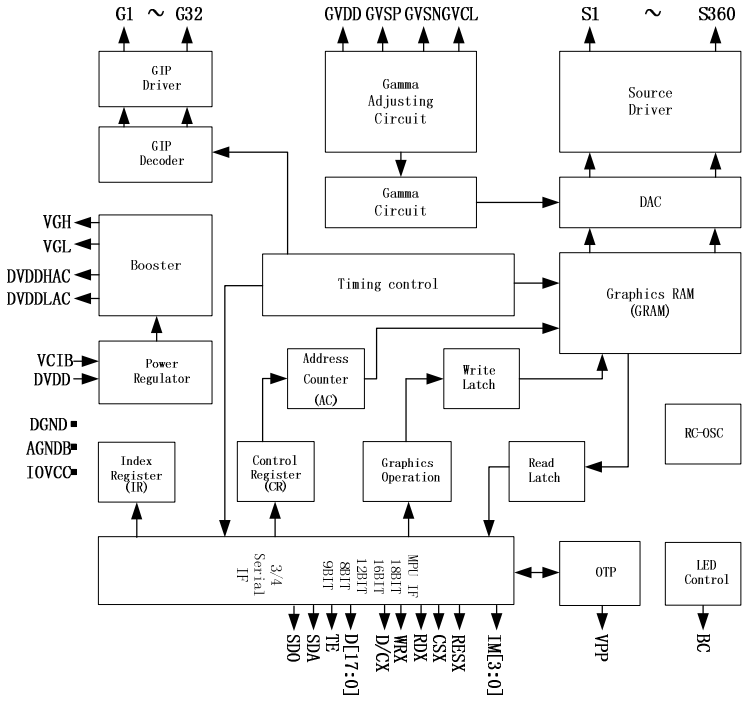
◆ No need for external electronic component

◆ a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram

3.1 Block diagram

Figure1



3.2 Pin Description

Table 1.

Power Supply Pins			
Pin Name	**I/O**	**Type**	**Descriptions**
IOVCC	I	Digital Power	Low voltage power supply for interface logic circuits(1.65~3.3V)
VCIB	I	Analog Power	High voltage power supply for analog circuit blocks(2.5~3.3V)
DVDD	O	Digital Power	Regulated Low voltage level for interface circuits Don't apply any external power to this pad
AGNDB	I	Analog Ground	System ground level for dynamic state. Connect to AGNDB on the FPC to prevent noise.
DGND	I	Digital Ground	System ground level for static state. Connect to DGND on the FPC to prevent noise.

Table 2.

<table>
<tr><th colspan="3">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>(IOVCC/DGND)</td><td>- Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface</th><th colspan="2">Pins in use</th></tr>
<tr><th>Register</th><th>GRAM</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>8080 MCU 8-bit bus interface I</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 8-bit bus interface II</td><td colspan="2">D[17:10]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface I</td><td>SDA: In/OUT</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td>SDA: In/SDO:OUT</td><td></td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface II</td><td>SDA: In/SDO:OUT</td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>2 data line serial interface I</td><td>SDA: In/OUT, DCX:In</td><td></td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td>1-wire quad Serial Peripheral Interface</td><td>SIO0</td><td></td></tr>
<tr><td>4-wire quad Serial Peripheral Interface</td><td>SIO0&SIO1 &SIO2&SIO3</td><td></td></tr>
</table>
MPU Parallel interface bus and serial interface Select .
Fix this pin at IOVCC or DGND.D8:E8</td></tr>
<tr><td>RESX</td><td>I</td><td>MCU (IOVCC//AGNDB)</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU (IOVCC//AGNDB)</td><td>Chip select input pin("Low" enable).
This pin can be permanently fixed "Low" in MPU interface mode only.</td></tr>
<tr><td>D/CX(SCL)</td><td>I</td><td>MCU(IOVCC / DGND)</td><td>This pin is used to select "Data or Command" in the parallel interface
When DCX='1', data is selected.
When DCX='0', command is selected.
This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface.
If not used, this pin should be connected to IOVCC or DGND.</td></tr>
<tr><td>RDX</td><td>I</td><td>MCU(IOVCC / DGND)</td><td>8080-I/8080-II system (RDX): Serves as a read signal and MCU read data at the rising edge.
Fix to IOVCC level when not in use</td></tr>
<tr><td>WRX (D/CX)</td><td>I</td><td>MCU (IOVCC/ DGND)</td><td>8080-I/8080-II system (WRX): Serves as a write signal and writes data at the rising edge.
4-line system (D/CX): Serves as command or parameter select.
Fix to IOVCC level when not in use.</td></tr>
<tr><td>D[17:0]</td><td>I/O</td><td>MCU(IOVCC / DGND)</td><td>18-bit parallel bi-directional data bus for MCU system .
Fix to DGND level when not in use</td></tr>
<tr><td>SDA</td><td>I/O</td><td>MCU (IOVCC/ DGND)</td><td>When IM[3]:Low, Serial in/out signal in 3-wire 9-bit/4-wire 8-bit serial data interface.
When IM[3]:High, Serial input signal in 3-wire 9-bit/4-wire 8-bit serial data interface.
The data is applied on the rising edge of the SCL signal.
If not used, fix this pin at IOVCC or DGND.</td></tr>
<tr><td>SDO</td><td>O</td><td>MCU (IOVCC/GND)</td><td>Serial output signal.
The data is outputted on the falling edge of the SCL signal.
If not used, open this pin</td></tr>
<tr><td>TE</td><td>O</td><td>MCU (IOVCC/DG</td><td>Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.</td></tr>
</table>

		ND)	
RAMBPS	I	MCU (IOVCC/DGND)	This pin is enable or disable memory bist; Enable :memory bist disable and P2D_BPS_IN enable; memory bist enable and P2D_BPS_IN disable. Disable:memory bist disable and P2D_BPS_IN disable ; memory bist enable and P2D_BPS_IN is enable. Ps:0:disable,1:enable.
ENABLE	I	MCU(IOVCC/DGND)	internal and external clock selection pin,with pull down function,0:selected internal clock,1:selected external

Note1: If CSX is connected to DGND in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

NOTE2: When CSX='1', there is no influence to the parallel and serial interface.

Table 3

LCD Driver Input/Output Pins			
Pin Name	I/O	Type	Descriptions
S360~S1	O	Source	Source output signals. Leave the pin to open when not in use.
G36~G1	O	Gate	Gate output signals. Leave the pin to open when not in use.
VCOM	O	DGND	Connect to DGND.
DDVDHAC	O	Power	Output voltage of 1st step up circuit(3*VCIB).Input voltage to 2nd step up circuit. Generated power output pad for source driver block.
DDVDLAC	O	Power	Output voltage of 1st step up circuit(-2*VCIB).Input voltage to 2nd step up circuit. Generated power output pad for source driver block.
VGH	O	Power	Power supply for the gate driver(Positive).
VGL	O	Power	Power supply for the gate driver(Negative).
VCL	O	Power	Power supply for VGH and VGL.VCL=0~-VCIB
GVDD	O	Ref	internal generated stable power for source driver unit GVDD is the highest positive grayscale reference voltage of source driver
GVSP	O	Ref	internal generated stable power for source driver unit GVSP is the lowest positive grayscale reference voltage of source driver
GVSN	O	Ref	internal generated stable power for source driver unit GVSN is the highest negative grayscale reference voltage of source driver
GVCL	O	Ref	internal generated stable power for source driver unit GVCL is the lowest negative grayscale reference voltage of source driver
BC	O	Dig IO	Output pin for PWM (Pulse width Modulation) signal of LED driving. If not used, open this pad.

Table 4

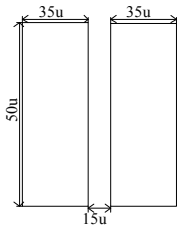
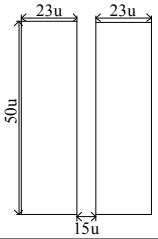
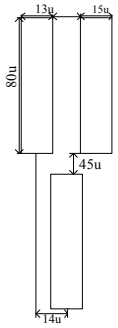
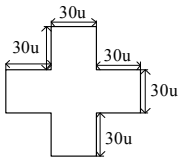
Test Pins			
Pin Name	I/O	Type	Descriptions
OSC_IN	I/O	Open	Input with pull down function
OSC_TEST	I/O	Open	Output with output enable function
VPP	I/O	Open	Internal test pins.
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.

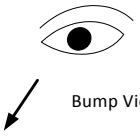
Liquid crystal power supply specifications Table

Table 5

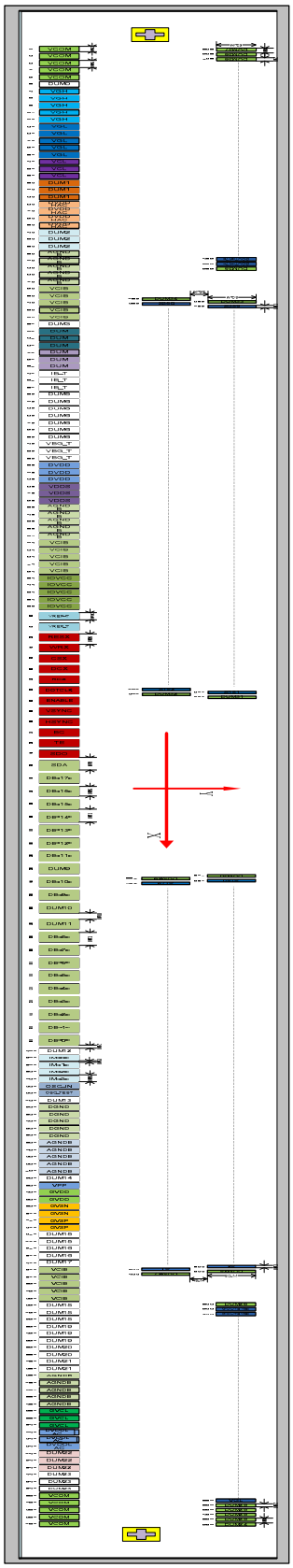
No.	Item		Description
1	Source Driver		240 pins (240*RGB)
2	GIP Diver for gate control		32 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Drive Output	S1~S360	V0~V63 grayscales
		G1~G36	VGH-VGL
5	Input Voltage	IOVCC	1.65~3.30V
		VCIB	2.50~3.30V
6	Liquid Crystal Drive Voltages	DDVDHAC	6.0~6.6V
		DDVDLAC	-5.0V~-4.5V
		VGH	12.0~13.0V
		VGL	-11.0~-8.0V
		VCL	-3.0~-1.5V
		VGH-VGL	Max.27.0V
7	Internal Boost circuits	DDVDHAC	VCIB*3
		DDVDLAC	VCIB*-2
		VGH	VCIB*5
		VGL	VCIB*-5
		VCL	VCIB*-1

3.3 Bump Arrangement

Chip Size(include scribe line):717umx10800um	
Chip thickness: 300um	
Bump height: 9um	
Input Pads 1~80 width: 35um 81~94 width: 38um 95~116 width: 50um 117~184 width: 35um	
Gout Related Pads 185~226,595~636	
Source Related Pads 227~594	
Mark The left is the Same with the right	

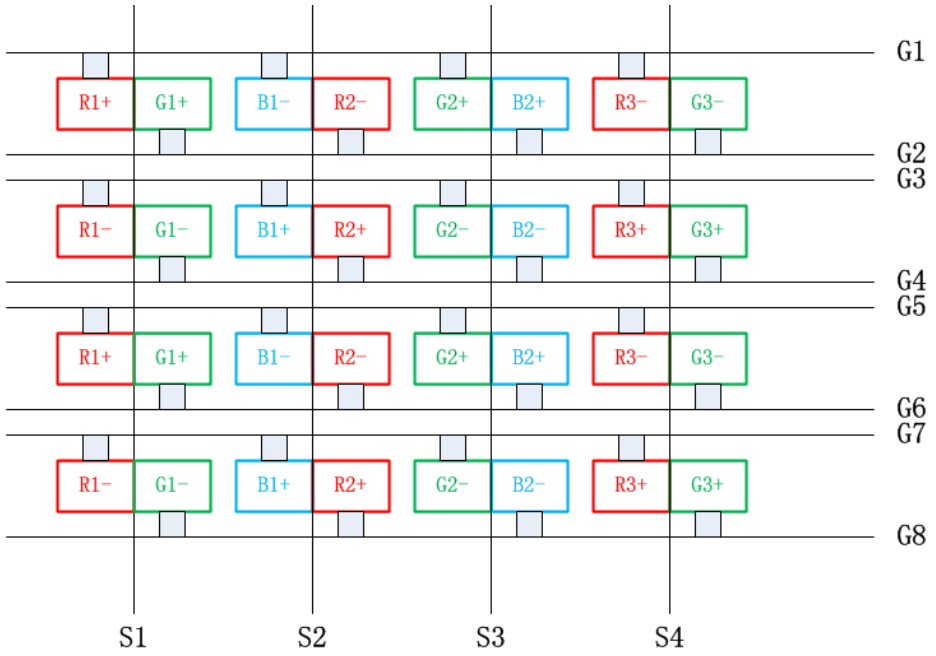


Bump View

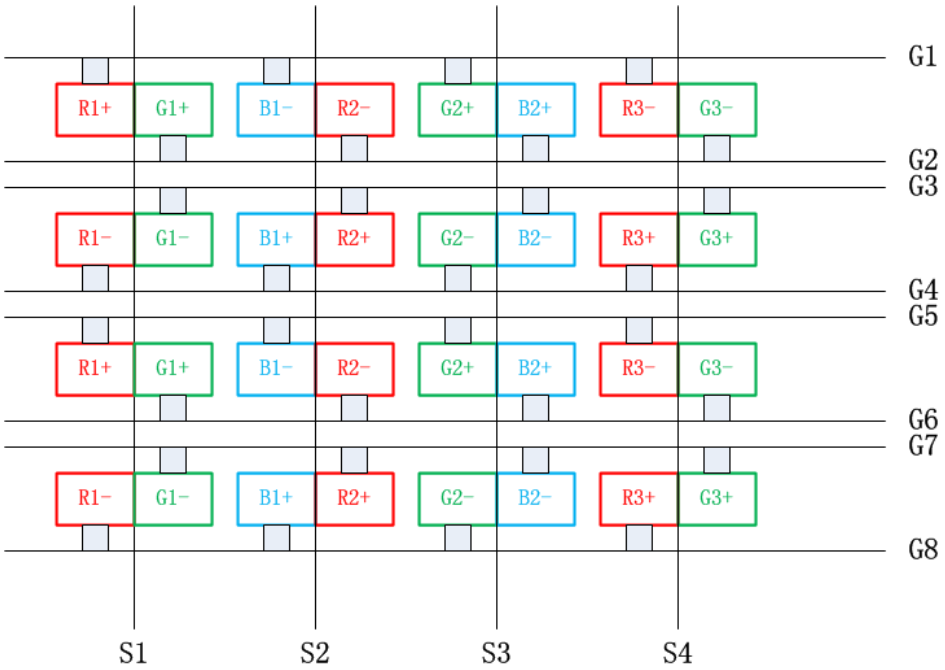


3.4 Supported pixel structure

3.4.1 Z type pixel structure



3.4.2 Bow-shaped type pixel structure



3.5 PAD coordinates

NO.	PAD_NAME	X-axis	Y-axis
1	VCOM	-4904.5	-285
2	VCOM	-4854.5	-285
3	VCOM	-4804.5	-285
4	VCOM	-4754.5	-285
5	VCOM	-4704.5	-285
6	DUM0	-4654.5	-285
7	VGH	-4604.5	-285
8	VGH	-4554.5	-285
9	VGH	-4504.5	-285
10	VGH	-4454.5	-285
11	VGH	-4404.5	-285
12	VGL	-4354.5	-285
13	VGL	-4304.5	-285
14	VGL	-4254.5	-285
15	VGL	-4204.5	-285
16	VGL	-4154.5	-285
17	VCL	-4104.5	-285
18	VCL	-4054.5	-285
19	VCL	-4004.5	-285
20	DUM1	-3954.5	-285
21	DUM1	-3904.5	-285
22	DUM1	-3854.5	-285
23	DDVDHAC	-3804.5	-285
24	DDVDHAC	-3754.5	-285
25	DDVDHAC	-3704.5	-285
26	DDVDHAC	-3654.5	-285
27	DUM2	-3604.5	-285
28	DUM2	-3554.5	-285
29	DUM2	-3504.5	-285
30	AGNDB	-3454.5	-285
31	AGNDB	-3404.5	-285
32	AGNDB	-3354.5	-285
33	AGNDB	-3304.5	-285
34	AGNDB	-3254.5	-285
35	VCIB	-3204.5	-285
36	VCIB	-3154.5	-285
37	VCIB	-3104.5	-285
38	VCIB	-3054.5	-285
39	VCIB	-3004.5	-285
40	DUM3	-2954.5	-285
41	DUM	-2904.5	-285
42	DUM	-2854.5	-285
43	DUM	-2804.5	-285
44	DUM	-2754.5	-285
45	DUM	-2704.5	-285
46	DUM	-2654.5	-285
47	IB_T	-2604.5	-285
48	IB_T	-2554.5	-285
49	IB_T	-2504.5	-285
50	DUM5	-2454.5	-285
51	DUM6	-2404.5	-285
52	DUM6	-2354.5	-285
53	DUM6	-2304.5	-285
54	DUM6	-2254.5	-285
55	DUM6	-2204.5	-285
56	DUM6	-2154.5	-285
57	VBG_T	-2104.5	-285
58	VBG_T	-2054.5	-285
59	VBG_T	-2004.5	-285
60	DVDD	-1954.5	-285
61	DVDD	-1904.5	-285
62	DVDD	-1854.5	-285
63	VDDS	-1804.5	-285
64	VDDS	-1754.5	-285
65	VDDS	-1704.5	-285
66	AGNDB	-1654.5	-285
67	AGNDB	-1604.5	-285
68	AGNDB	-1554.5	-285
69	AGNDB	-1504.5	-285
70	AGNDB	-1454.5	-285
71	VCIB	-1404.5	-285
72	VCIB	-1354.5	-285
73	VCIB	-1304.5	-285
74	VCIB	-1254.5	-285
75	VCIB	-1204.5	-285
76	IOVCC	-1154.5	-285
77	IOVCC	-1104.5	-285
78	IOVCC	-1054.5	-285
79	IOVCC	-1004.5	-285
80	IOVCC	-954.5	-285
81	VREF_T	-896	-285
82	VREF_T	-836	-285
83	RESX	-776	-285
84	WRX	-716	-285
85	CSX	-656	-285
86	DCX	-596	-285
87	RDX	-536	-285
88	DUM	-476	-285
89	ENABLE	-416	-285
90	DUM	-356	-285
91	DUM	-296	-285
92	BC	-236	-285
93	TE	-176	-285
94	SDO	-116	-285
95	SDA	-50	-285
96	DB<17>	22	-285
97	DB<16>	94	-285
98	DB<15>	166	-285
99	DB<14>	238	-285
100	DB<13>	310	-285
101	DB<12>	382	-285
102	DB<11>	454	-285
103	DUM9	526	-285
104	DB<10>	598	-285
105	DB<9>	670	-285
106	DUM10	742	-285
107	DUM11	843	-285
108	DB<8>	915	-285

NO.	PAD_NAME	X-axis	Y-axis
109	DB<7>	987	-285
110	DB<6>	1059	-285
111	DB<5>	1131	-285
112	DB<4>	1203	-285
113	DB<3>	1275	-285
114	DB<2>	1347	-285
115	DB<1>	1419	-285
116	DB<0>	1491	-285
117	DUM12	1554.5	-285
118	IM<0>	1604.5	-285
119	IM<1>	1654.5	-285
120	IM<2>	1704.5	-285
121	IM<3>	1754.5	-285
122	OSC_IN	1804.5	-285
123	OSC_TEST	1854.5	-285
124	RAMBPS	1904.5	-285
125	DGND	1954.5	-285
126	DGND	2004.5	-285
127	DGND	2054.5	-285
128	DGND	2104.5	-285
129	DGND	2154.5	-285
130	AGNDB	2204.5	-285
131	AGNDB	2254.5	-285
132	AGNDB	2304.5	-285
133	AGNDB	2354.5	-285
134	AGNDB	2404.5	-285
135	DUM14	2454.5	-285
136	VPP	2504.5	-285
137	GVDD	2554.5	-285
138	GVDD	2604.5	-285
139	GVSN	2654.5	-285
140	GVSN	2704.5	-285
141	GVSP	2754.5	-285
142	GVSP	2804.5	-285
143	DUM15	2854.5	-285
144	DUM15	2904.5	-285
145	DUM16	2954.5	-285
146	DUM16	3004.5	-285
147	DUM17	3054.5	-285
148	VCIB	3104.5	-285
149	VCIB	3154.5	-285
150	VCIB	3204.5	-285
151	VCIB	3254.5	-285
152	VCIB	3304.5	-285
153	DUM18	3354.5	-285
154	DUM18	3404.5	-285
155	DUM18	3454.5	-285
156	DUM19	3504.5	-285
157	DUM19	3554.5	-285
158	DUM19	3604.5	-285
159	DUM20	3654.5	-285
160	DUM20	3704.5	-285
161	DUM21	3754.5	-285
162	DUM21	3804.5	-285
163	AGNDB	3854.5	-285
164	AGNDB	3904.5	-285
165	AGNDB	3954.5	-285
166	AGNDB	4004.5	-285
167	AGNDB	4054.5	-285
168	GVCL	4104.5	-285
169	GVCL	4154.5	-285
170	GVCL	4204.5	-285
171	DDVDLAC	4254.5	-285
172	DDVDLAC	4304.5	-285
173	DDVDLAC	4354.5	-285
174	DUM22	4404.5	-285
175	DUM22	4454.5	-285
176	DUM22	4504.5	-285
177	DUM23	4554.5	-285
178	DUM23	4604.5	-285
179	DUM23	4654.5	-285
180	VCOM	4704.5	-285
181	VCOM	4754.5	-285
182	VCOM	4804.5	-285
183	VCOM	4854.5	-285
184	VCOM	4904.5	-285
185	DUM24	4908	285
186	DUM25	4870	285
187	DUM25	4832	285
188	DUM25	4794	285
189	DUM25	4756	285
190	VGL	4718	285
191	VGL	4680	285
192	VGL	4642	285
193	VGL	4604	285
194	STV4	4566	285
195	STV4	4528	285
196	STV2	4490	285
197	STV2	4452	285
198	GCH	4414	285
199	GCH	4376	285
200	VGL	4338	285
201	VGL	4300	285
202	CLK8	4262	285
203	CLK8	4224	285
204	CLK6	4186	285
205	CLK6	4148	285
206	CLK4	4110	285
207	CLK4	4072	285
208	CLK2	4034	285
209	CLK2	3996	285
210	STV0_R	3958	285
211	STV0_R	3920	285
212	GCL	3882	285
213	GCL	3844	285
214	VDS	3806	285
215	VDS	3768	285
216	VSD	3730	285
217	VSD	3692	285
218	GOUT<13>	3654	285
219	GOUT<13>	3616	285
220	GOUT<14>	3578	285
221	GOUT<14>	3540	285
222	GOUT<15>	3502	285

NO.	PAD_NAME	X-axis	Y-axis
223	GOUT<15>	3464	285
224	GOUT<16>	3426	285
225	GOUT<16>	3388	285
226	DUM26	3350	285
227	DUM27	3134	145
228	DUM28	3120	270
229	S<1>	3106	145
230	S<2>	3092	270
231	S<3>	3078	145
232	S<4>	3064	270
233	S<5>	3050	145
234	S<6>	3036	270
235	S<7>	3022	145
236	S<8>	3008	270
237	S<9>	2994	145
238	S<10>	2980	270
239	S<11>	2966	145
240	S<12>	2952	270
241	S<13>	2938	145
242	S<14>	2924	270
243	S<15>	2910	145
244	S<16>	2896	270
245	S<17>	2882	145
246	S<18>	2868	270
247	S<19>	2854	145
248	S<20>	2840	270
249	S<21>	2826	145
250	S<22>	2812	270
251	S<23>	2798	145
252	S<24>	2784	270
253	S<25>	2770	145
254	S<26>	2756	270
255	S<27>	2742	145
256	S<28>	2728	270
257	S<29>	2714	145
258	S<30>	2700	270
259	S<31>	2686	145
260	S<32>	2672	270

NO.	PAD_NAME	X-axis	Y-axis
261	S<33>	2658	145
262	S<34>	2644	270
263	S<35>	2630	145
264	S<36>	2616	270
265	S<37>	2602	145
266	S<38>	2588	270
267	S<39>	2574	145
268	S<40>	2560	270
269	S<41>	2546	145
270	S<42>	2532	270
271	S<43>	2518	145
272	S<44>	2504	270
273	S<45>	2490	145
274	S<46>	2476	270
275	S<47>	2462	145
276	S<48>	2448	270
277	S<49>	2434	145
278	S<50>	2420	270
279	S<51>	2406	145
280	S<52>	2392	270
281	S<53>	2378	145
282	S<54>	2364	270
283	S<55>	2350	145
284	S<56>	2336	270
285	S<57>	2322	145
286	S<58>	2308	270
287	S<59>	2294	145
288	S<60>	2280	270
289	S<61>	2266	145
290	S<62>	2252	270
291	S<63>	2238	145
292	S<64>	2224	270
293	S<65>	2210	145
294	S<66>	2196	270
295	S<67>	2182	145
296	S<68>	2168	270
297	S<69>	2154	145
298	S<70>	2140	270

NO.	PAD_NAME	X-axis	Y-axis
299	S<71>	2126	145
300	S<72>	2112	270
301	S<73>	2098	145
302	S<74>	2084	270
303	S<75>	2070	145
304	S<76>	2056	270
305	S<77>	2042	145
306	S<78>	2028	270
307	S<79>	2014	145
308	S<80>	2000	270
309	S<81>	1986	145
310	S<82>	1972	270
311	S<83>	1958	145
312	S<84>	1944	270
313	S<85>	1930	145
314	S<86>	1916	270
315	S<87>	1902	145
316	S<88>	1888	270
317	S<89>	1874	145
318	S<90>	1860	270
319	S<91>	1846	145
320	S<92>	1832	270
321	S<93>	1818	145
322	S<94>	1804	270
323	S<95>	1790	145
324	S<96>	1776	270
325	S<97>	1762	145
326	S<98>	1748	270
327	S<99>	1734	145
328	S<100>	1720	270
329	S<101>	1706	145
330	S<102>	1692	270
331	S<103>	1678	145
332	S<104>	1664	270
333	S<105>	1650	145
334	S<106>	1636	270
335	S<107>	1622	145
336	S<108>	1608	270

NO.	PAD_NAME	X-axis	Y-axis
337	S<109>	1594	145
338	S<110>	1580	270
339	S<111>	1566	145
340	S<112>	1552	270
341	S<113>	1538	145
342	S<114>	1524	270
343	S<115>	1510	145
344	S<116>	1496	270
345	S<117>	1482	145
346	S<118>	1468	270
347	S<119>	1454	145
348	S<120>	1440	270
349	S<121>	1426	145
350	S<122>	1412	270
351	S<123>	1398	145
352	S<124>	1384	270
353	S<125>	1370	145
354	S<126>	1356	270
355	S<127>	1342	145
356	S<128>	1328	270
357	S<129>	1314	145
358	S<130>	1300	270
359	S<131>	1286	145
360	S<132>	1272	270
361	S<133>	1258	145
362	S<134>	1244	270
363	S<135>	1230	145
364	S<136>	1216	270
365	S<137>	1202	145
366	S<138>	1188	270
367	S<139>	1174	145
368	S<140>	1160	270
369	S<141>	1146	145
370	S<142>	1132	270
371	S<143>	1118	145
372	S<144>	1104	270
373	S<145>	1090	145
374	S<146>	1076	270
375	S<147>	1062	145
376	S<148>	1048	270
377	S<149>	1034	145
378	S<150>	1020	270
379	S<151>	1006	145
380	S<152>	992	270
381	S<153>	978	145
382	S<154>	964	270
383	S<155>	950	145
384	S<156>	936	270
385	S<157>	922	145
386	S<158>	908	270
387	S<159>	894	145
388	S<160>	880	270
389	S<161>	866	145
390	S<162>	852	270
391	S<163>	838	145
392	S<164>	824	270
393	S<165>	810	145
394	S<166>	796	270
395	S<167>	782	145
396	S<168>	768	270
397	S<169>	754	145
398	S<170>	740	270
399	S<171>	726	145
400	S<172>	712	270
401	S<173>	698	145
402	S<174>	684	270
403	S<175>	670	145
404	S<176>	656	270
405	S<177>	642	145
406	S<178>	628	270
407	S<179>	614	145
408	S<180>	600	270
409	DUM29	586	145
410	DUM30	572	270
411	DUM31	-572	270
412	DUM32	-586	145
413	S<181>	-600	270
414	S<182>	-614	145
415	S<183>	-628	270
416	S<184>	-642	145
417	S<185>	-656	270
418	S<186>	-670	145
419	S<187>	-684	270
420	S<188>	-698	145
421	S<189>	-712	270
422	S<190>	-726	145
423	S<191>	-740	270
424	S<192>	-754	145
425	S<193>	-768	270
426	S<194>	-782	145
427	S<195>	-796	270
428	S<196>	-810	145
429	S<197>	-824	270
430	S<198>	-838	145
431	S<199>	-852	270
432	S<200>	-866	145
433	S<201>	-880	270
434	S<202>	-894	145
435	S<203>	-908	270
436	S<204>	-922	145
437	S<205>	-936	270
438	S<206>	-950	145
439	S<207>	-964	270
440	S<208>	-978	145
441	S<209>	-992	270
442	S<210>	-1006	145
443	S<211>	-1020	270
444	S<212>	-1034	145
445	S<213>	-1048	270
446	S<214>	-1062	145
447	S<215>	-1076	270
448	S<216>	-1090	145
449	S<217>	-1104	270
450	S<218>	-1118	145

NO.	PAD_NAME	X-axis	Y-axis
451	S<219>	-1132	270
452	S<220>	-1146	145
453	S<221>	-1160	270
454	S<222>	-1174	145
455	S<223>	-1188	270
456	S<224>	-1202	145
457	S<225>	-1216	270
458	S<226>	-1230	145
459	S<227>	-1244	270
460	S<228>	-1258	145
461	S<229>	-1272	270
462	S<230>	-1286	145
463	S<231>	-1300	270
464	S<232>	-1314	145
465	S<233>	-1328	270
466	S<234>	-1342	145
467	S<235>	-1356	270
468	S<236>	-1370	145
469	S<237>	-1384	270
470	S<238>	-1398	145
471	S<239>	-1412	270
472	S<240>	-1426	145
473	S<241>	-1440	270
474	S<242>	-1454	145
475	S<243>	-1468	270
476	S<244>	-1482	145
477	S<245>	-1496	270
478	S<246>	-1510	145
479	S<247>	-1524	270
480	S<248>	-1538	145
481	S<249>	-1552	270
482	S<250>	-1566	145
483	S<251>	-1580	270
484	S<252>	-1594	145
485	S<253>	-1608	270
486	S<254>	-1622	145
487	S<255>	-1636	270
488	S<256>	-1650	145

NO.	PAD_NAME	X-axis	Y-axis
489	S<257>	-1664	270
490	S<258>	-1678	145
491	S<259>	-1692	270
492	S<260>	-1706	145
493	S<261>	-1720	270
494	S<262>	-1734	145
495	S<263>	-1748	270
496	S<264>	-1762	145
497	S<265>	-1776	270
498	S<266>	-1790	145
499	S<267>	-1804	270
500	S<268>	-1818	145
501	S<269>	-1832	270
502	S<270>	-1846	145
503	S<271>	-1860	270
504	S<272>	-1874	145
505	S<273>	-1888	270
506	S<274>	-1902	145
507	S<275>	-1916	270
508	S<276>	-1930	145
509	S<277>	-1944	270
510	S<278>	-1958	145
511	S<279>	-1972	270
512	S<280>	-1986	145
513	S<281>	-2000	270
514	S<282>	-2014	145
515	S<283>	-2028	270
516	S<284>	-2042	145
517	S<285>	-2056	270
518	S<286>	-2070	145
519	S<287>	-2084	270
520	S<288>	-2098	145
521	S<289>	-2112	270
522	S<290>	-2126	145
523	S<291>	-2140	270
524	S<292>	-2154	145
525	S<293>	-2168	270
526	S<294>	-2182	145

NO.	PAD_NAME	X-axis	Y-axis
527	S<295>	-2196	270
528	S<296>	-2210	145
529	S<297>	-2224	270
530	S<298>	-2238	145
531	S<299>	-2252	270
532	S<300>	-2266	145
533	S<301>	-2280	270
534	S<302>	-2294	145
535	S<303>	-2308	270
536	S<304>	-2322	145
537	S<305>	-2336	270
538	S<306>	-2350	145
539	S<307>	-2364	270
540	S<308>	-2378	145
541	S<309>	-2392	270
542	S<310>	-2406	145
543	S<311>	-2420	270
544	S<312>	-2434	145
545	S<313>	-2448	270
546	S<314>	-2462	145
547	S<315>	-2476	270
548	S<316>	-2490	145
549	S<317>	-2504	270
550	S<318>	-2518	145
551	S<319>	-2532	270
552	S<320>	-2546	145
553	S<321>	-2560	270
554	S<322>	-2574	145
555	S<323>	-2588	270
556	S<324>	-2602	145
557	S<325>	-2616	270
558	S<326>	-2630	145
559	S<327>	-2644	270
560	S<328>	-2658	145
561	S<329>	-2672	270
562	S<330>	-2686	145
563	S<331>	-2700	270
564	S<332>	-2714	145

NO.	PAD_NAME	X-axis	Y-axis
565	S<333>	-2728	270
566	S<334>	-2742	145
567	S<335>	-2756	270
568	S<336>	-2770	145
569	S<337>	-2784	270
570	S<338>	-2798	145
571	S<339>	-2812	270
572	S<340>	-2826	145
573	S<341>	-2840	270
574	S<342>	-2854	145
575	S<343>	-2868	270
576	S<344>	-2882	145
577	S<345>	-2896	270
578	S<346>	-2910	145
579	S<347>	-2924	270
580	S<348>	-2938	145
581	S<349>	-2952	270
582	S<350>	-2966	145
583	S<351>	-2980	270
584	S<352>	-2994	145
585	S<353>	-3008	270
586	S<354>	-3022	145
587	S<355>	-3036	270
588	S<356>	-3050	145
589	S<357>	-3064	270
590	S<358>	-3078	145
591	S<359>	-3092	270
592	S<360>	-3106	145
593	DUM33	-3120	270
594	DUM34	-3134	145
595	DUM35	-3350	285
596	GOUT<17>	-3388	285
597	GOUT<17>	-3426	285
598	GOUT<18>	-3464	285
599	GOUT<18>	-3502	285
600	GOUT<19>	-3540	285
601	GOUT<19>	-3578	285
602	GOUT<20>	-3616	285

NO.	PAD_NAME	X-axis	Y-axis
603	GOUT<20>	-3654	285
604	VSD	-3692	285
605	VSD	-3730	285
606	VDS	-3768	285
607	VDS	-3806	285
608	GCL	-3844	285
609	GCL	-3882	285
610	STV0_L	-3920	285
611	STV0_L	-3958	285
612	CLK1	-3996	285
613	CLK1	-4034	285
614	CLK3	-4072	285
615	CLK3	-4110	285
616	CLK5	-4148	285
617	CLK5	-4186	285
618	CLK7	-4224	285
619	CLK7	-4262	285
620	VGL	-4300	285
621	VGL	-4338	285
622	GCH	-4376	285
623	GCH	-4414	285
624	STV1	-4452	285
625	STV1	-4490	285
626	STV3	-4528	285
627	STV3	-4566	285
628	VGL	-4604	285
629	VGL	-4642	285
630	VGL	-4680	285
631	VGL	-4718	285
632	DUM36	-4756	285
633	DUM36	-4794	285
634	DUM36	-4832	285
635	DUM36	-4870	285
636	DUM37	-4908	285

Name	X-axis	Y-axis
left mark	-5000	205
right mark	5000	205

4. Interface setting

4.1 MCU interfaces

NV3002 provides the 8bit parallel system interface for 8080-I /8080- II series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] 3-bits of 3Ah register.

4.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

Table 6

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	1	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	0	0	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX

4.1.2. 8080-I Series Parallel Interface

NV3002 can be accessed via 8bit MCU 8080-I series parallel interface. The chip select CSX (active low) is used to enable or disable NV3002 chip. The RESX (active low) is an external reset signal.WRX is the parallel data write strobe, RDX is the parallel data read strobe and D [7:0] is parallel data bus.

NV3002 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX=’1’, D [7:0] bits are display RAM data or command’s parameters. When D/CX=’0’, D [7:0] bits are commands.

The 8080-I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-I Interface selection is done when IM3 pin is low state (DGND level). Interface bus width can be selected by IM [2:0] bits.The selection of 8080-I series parallel interface is shown as the table in the following.Table 7

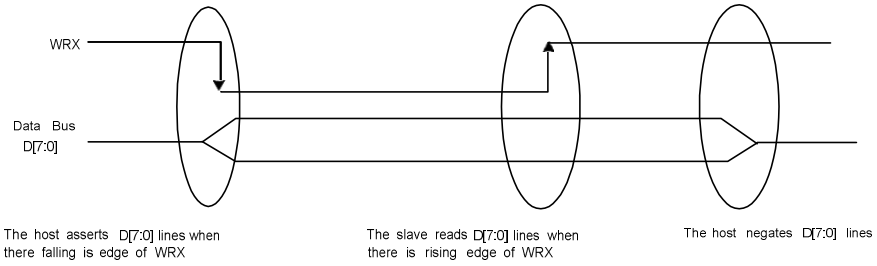
IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
0	1	0	0	8080 MCU8-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

4.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is SRAM data or command's parameter.

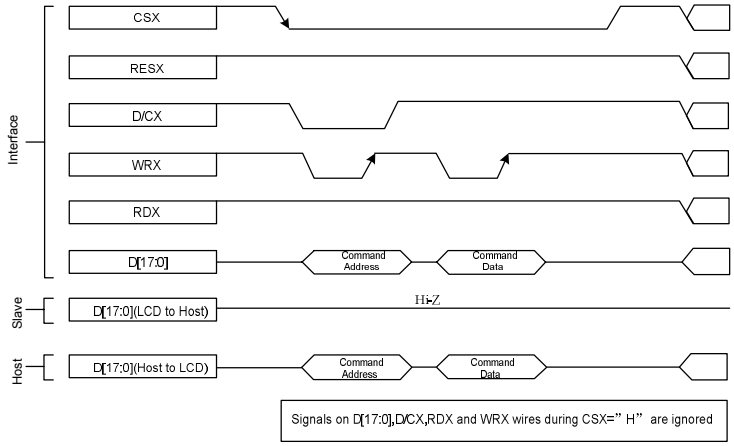
The following figure shows a write cycle for the 8080-I MCU interface.

Figure 2.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure 3.

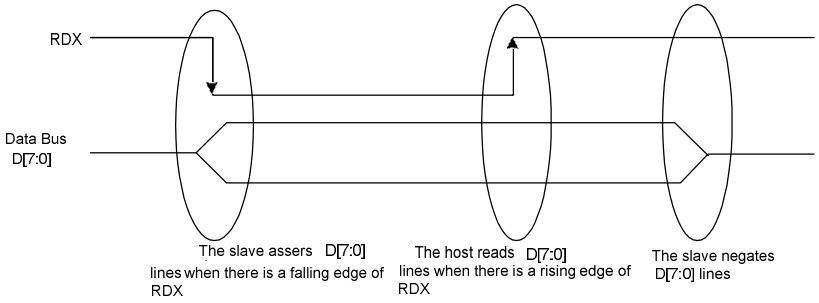


4.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle, while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

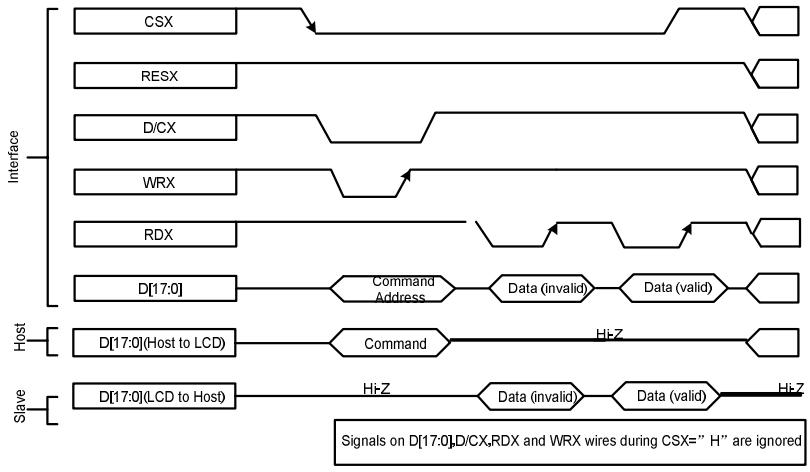
The following figure shows the read cycle for the 8080-I MCU interface.

Figure 4.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure 5.



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.5. 8080-Ⅱ Series Parallel Interface

NV3002 can be accessed via 8bit MCU 8080-Ⅱ series parallel interface. The chip select CSX (active low) is used to enable or disable NV3002 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:10] is parallel data bus.

NV3002 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:10] bits are display RAM data or command's parameters. When D/CX='0', D[17:10] bits are commands.

The 8080-II series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-II Interface selection is done when IM3 pin is high state (IOVCC level). Interface bus width can be selected by IM [2:0] bits.

The selection of 8080-II series parallel interface is shown as the table in the following.

Table 8

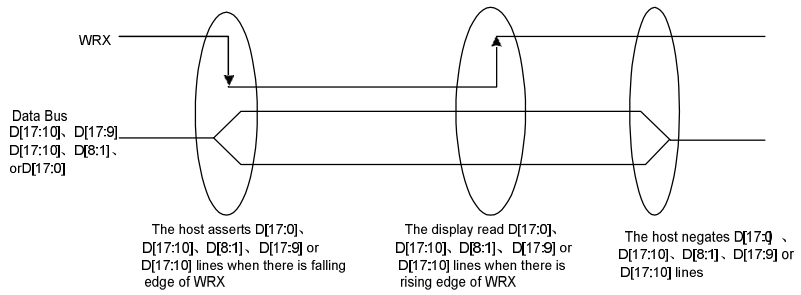
IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
0	0	0	0	8080 MCU 8-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

4.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

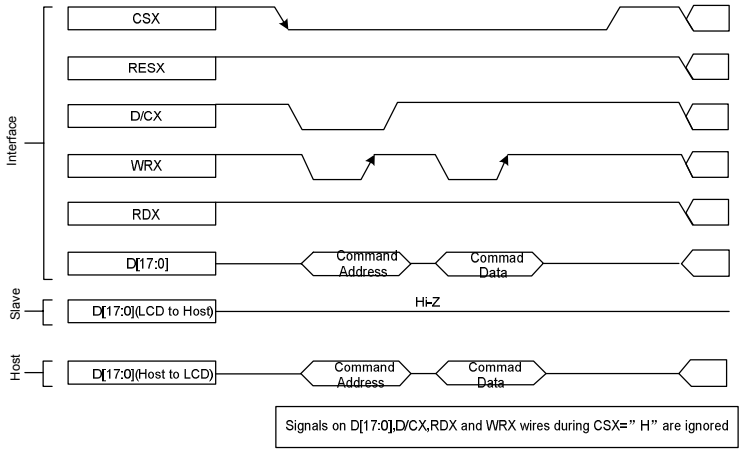
The following figure shows a write cycle for the 8080-II MCU interface.

Figure 6.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure 7.

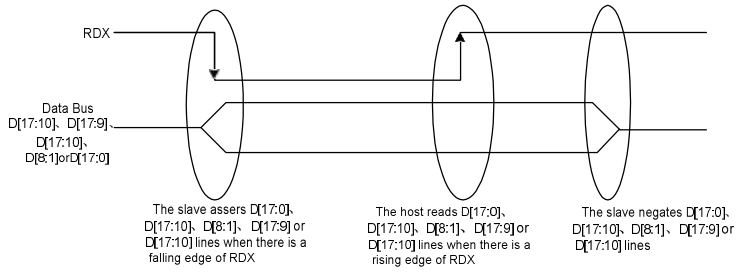


4.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

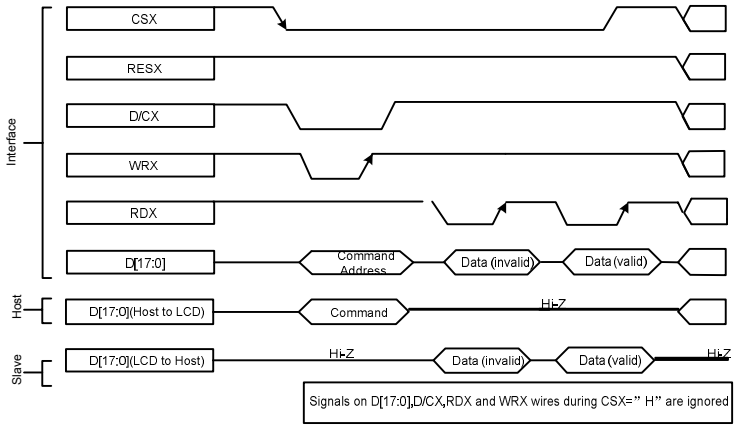
The following figure shows the read cycle for the 8080-II MCU interface.

Figure 8.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure 9.



4.2. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

Table 9.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
1	1	0	1	3-line serial interface	"L"	-	↑	Read/Write command, parameter or display data.
1	1	1	1	4-line serial interface	"L"	"H/L"	↑	Read/Write command, parameter or display data.
1	0	0	1	3-line serial interface	"L"	-	—	Read/Write command, parameter or display data.
1	0	1	1	4-line serial interface	"L"	"H/L"	—	Read/Write command, parameter or display data.

NV3002 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and NV3002. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/ Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to DGND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

4.2.1. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to NV3002. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM(Memory write command),or command register as parameter.

Any instruction can be sent in any order to NV3002 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

Figure 10.

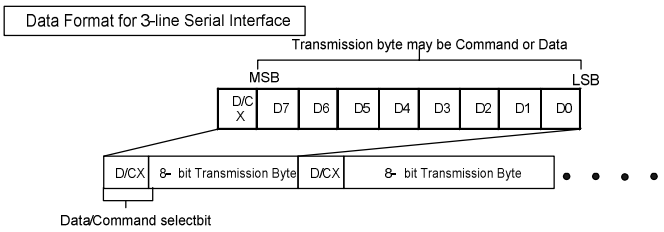
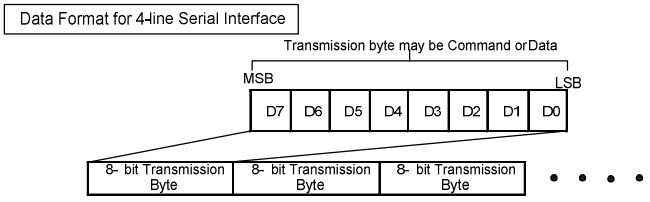


Figure 11.



Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by NV3002 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

Figure 12.

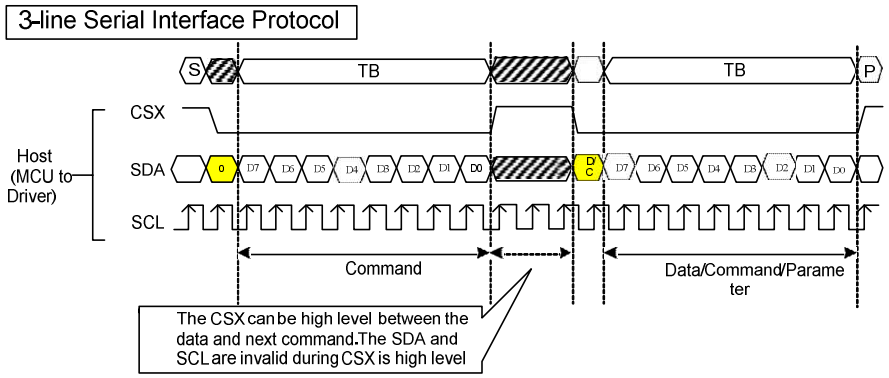
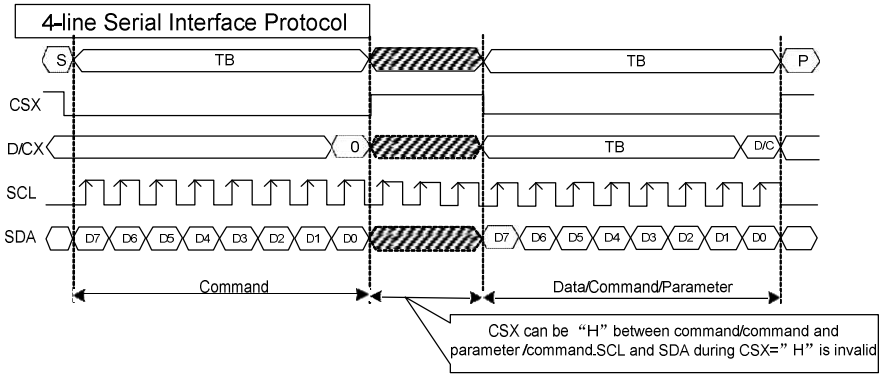


Figure 13.



4.2.2. Read Cycle Sequence

The read mode of interface means that the host reads register’s parameter from NV3002. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. NV3002 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

Figure 14

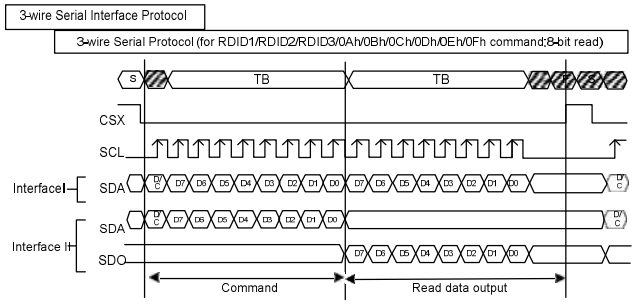


Figure 15

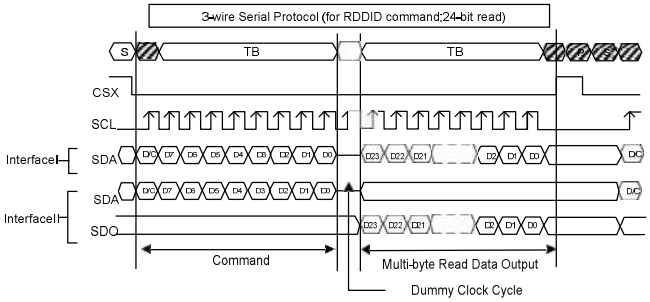


Figure 16

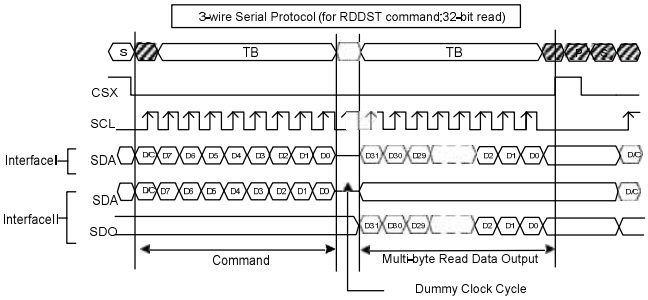


Figure 17.

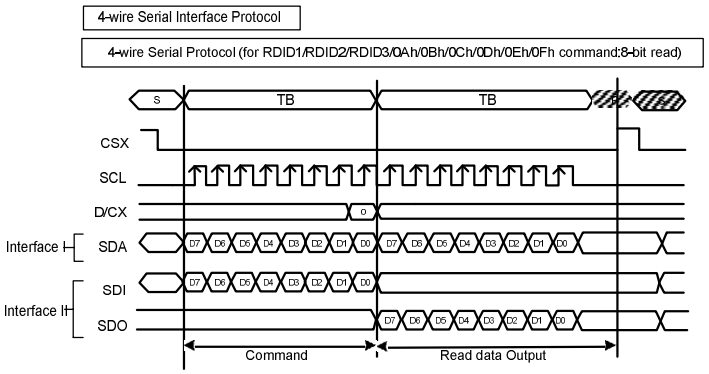


Figure 18.

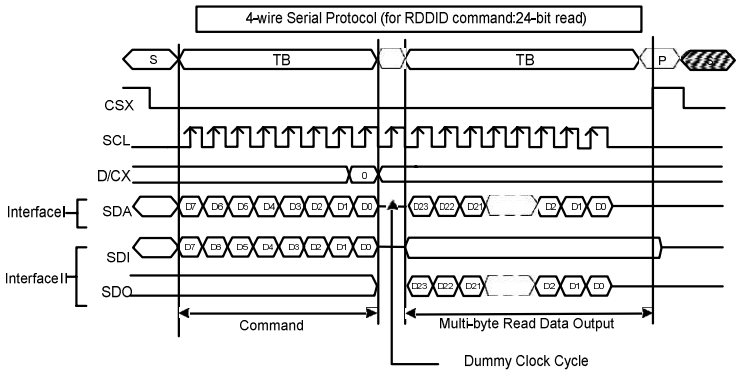
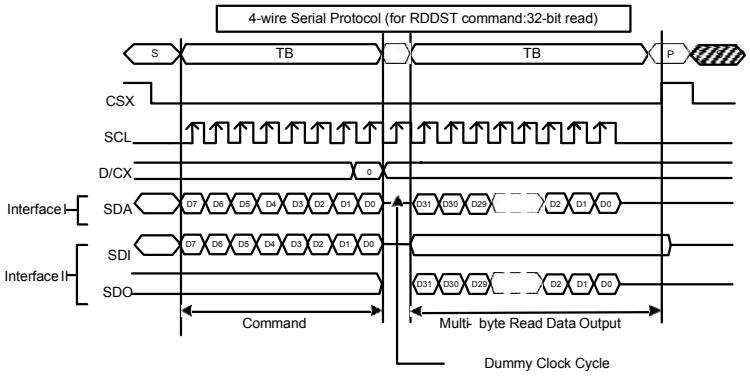


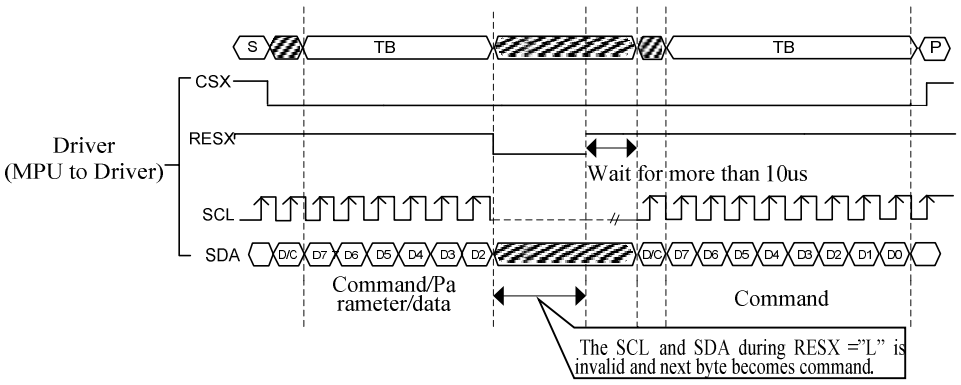
Figure 19.



4.2.3. Data Transfer Break and Recovery

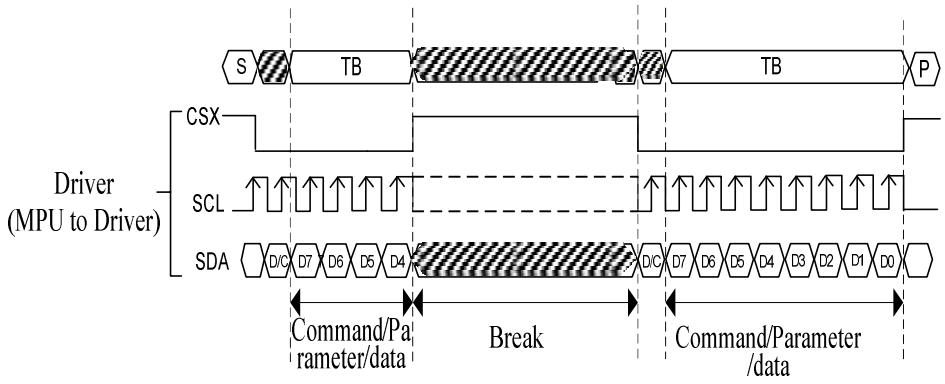
If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

Figure 20.



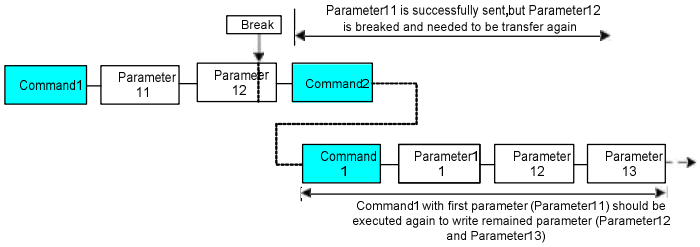
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

Figure 21.



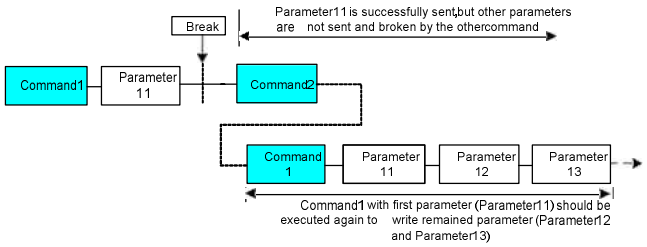
If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

Figure 22.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

Figure 23.



4.2.4. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then NV3002 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.

This applies to the following 4 conditions:

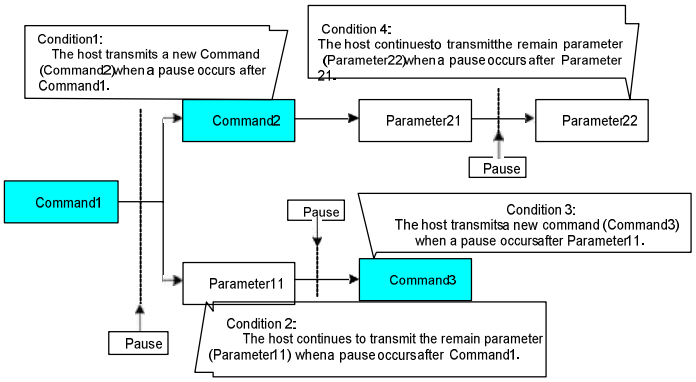
(1).Command-Pause-Command

(2).Command-Pause-Parameter

(3).Parameter-Pause-Command

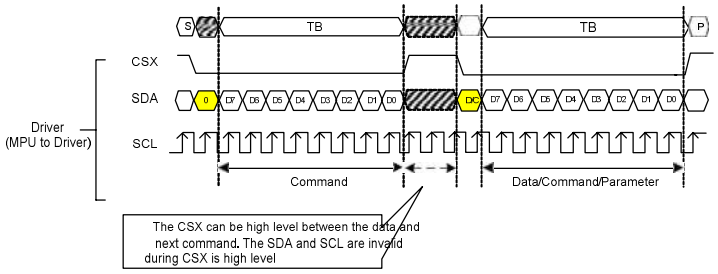
(4).Parameter-Pause-Parameter

Figure 24.



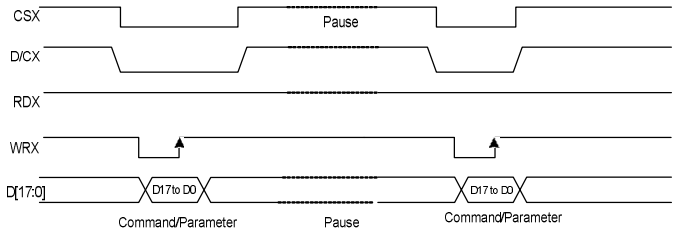
4.2.5. Serial Interface Pause (3_wire)

Figure 25.



4.2.6. Parallel Interface Pause

Figure 26.



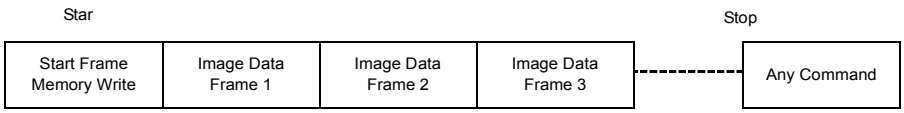
4.2.7. Data Transfer Mode

NV3002 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

4.2.7.1. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.

Figure 27.

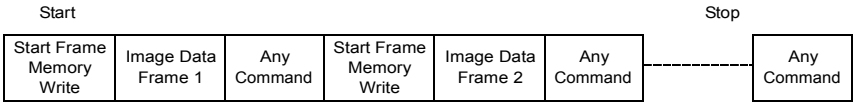


4.2.7.2. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is

sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.

Figure 28.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

4.3.Quad Serial Peripheral Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

Table 10.

IM3	IM2	IM1	IM 0	MCU-Interface Mode	CS X	D/CX	SC L	Function
1	0	1	0	1-wire	"L"			1)Write command, parameter or display data; 2)read command, parameter .
				4-wire	"L"			1)Write command, parameter or display data; 2)read command, parameter .

NV3002 supplies 1-wire and 4-wire bi-directional serial interfaces for communication between host and NV3002.Here 1-wire and 4-wire represent the number of data lines. The 1-wire serial mode consists of chip enabled input (CSX), serial clock input (SCL), and serial data Input/output (SIO0), The 4-wire serial mode consists of the chip enable input (CSX), the serial clock input (SCL), the serial data Input/output (SIO0(SDA))and serial data Input (SIO1(DCX)&SIO2(D0)&SIO3(D1)) for data transmission. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

4.3.1.Write Sequence

The write mode of the interface means that the host writes commands or data to NV3002. 1- Wire serial interface commands and data are written in the same way. The first is that the host processor drives CSX pin to low and Then set the first byte to

02H.Each bit of data is read by NV3002 on the rising edge of the SCL signal, and the data bit of data on the falling edge is set by the host on SDA.The 1-wire serial interface writes sequence described in the figure as below.

Figure 29

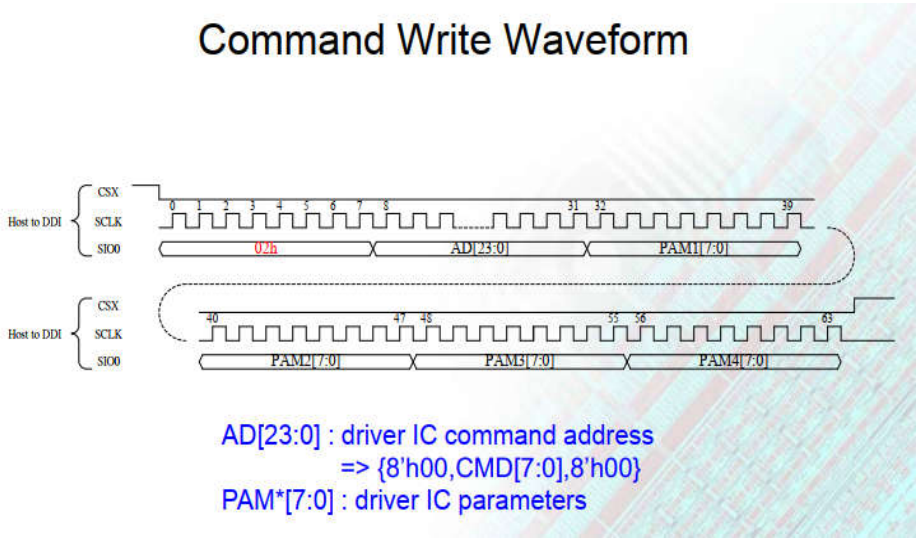
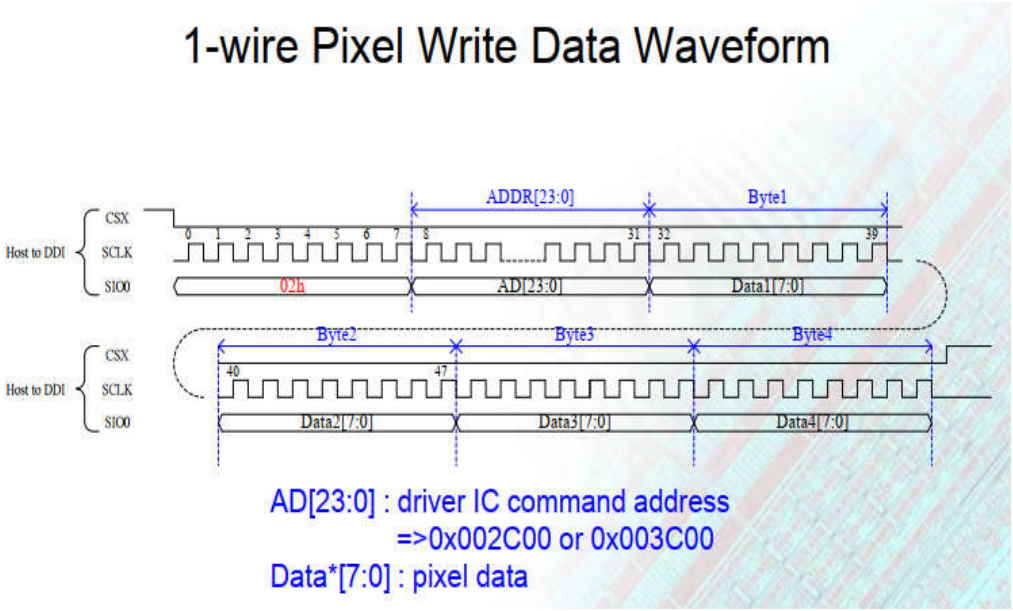


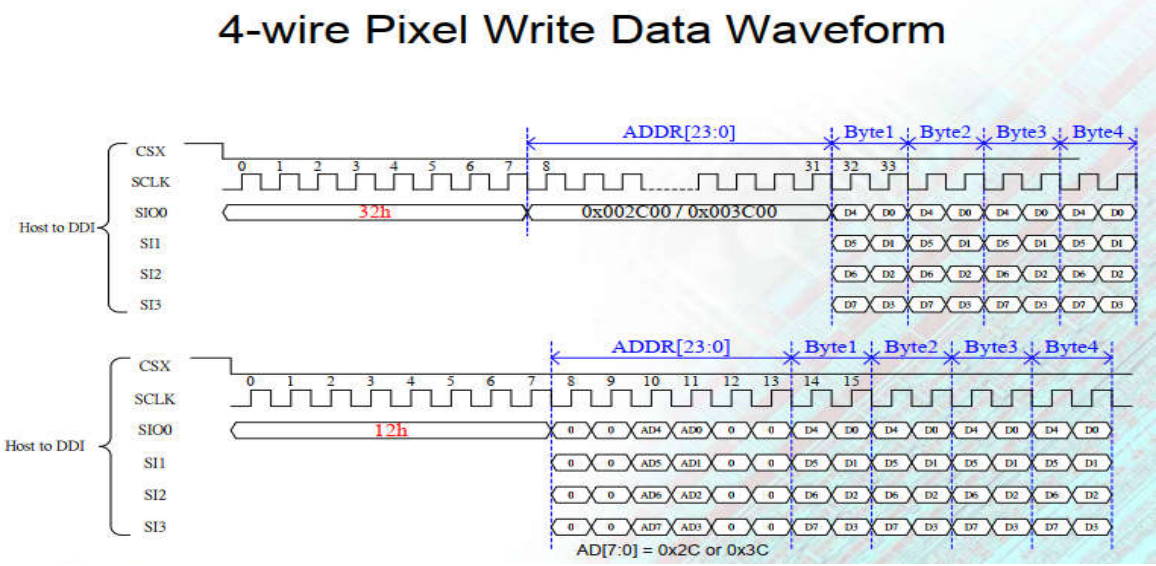
Figure 30



4-Wire serial interface commands and data are written in the same way. The first is that the host processor drives CSX pin to low and Then set the first byte to 12H or 32-H.Each bit of data is read by NV3002 on the rising edge of the SCL signal, and

the data bit of data on the falling edge is set by the host on SDA.The 1-wire serial interface writes sequence described in the figure as below.

Figure 31



4.3.2.Read Sequence

The read mode of interface means that the host reads register's parameter from NV3002. For a QSPI read, the host first sends a command that includes a header (03h), address bits, and data bits, and then transmits the following bytes in the opposite direction. The format of the specific sending command is as follows.

QSPI reads support only one wire of read. The specific reading method is that NV3002 stores SDA(input data) lock on the rising edge of SCL(serial clock), and then shifts SDA(output data) to the falling edge of SCL(serial clock).After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit.

Table 11.

Example 1:Read register 0AH that returns a single argument

Read CMD 0x03	IC CMD 0x000A00	IC Read Data 0x0C

Table 12.

Example 2: Read the 65H register that returns multiple parameters

Read CMD 0x03	IC CMD 0x006500	IC Read Data#1 0x01
IC Read Data#2 0x02	IC Read Data#1 0x02	

4.4. Display Data RAM (DDRAM)

NV3002 has an integrated 240x240x18-bit graphic type static RAM. This 129600-byte memory allows storing a 240xRGBx240 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

4.5. Display Data Format

NV3002 supplies 16-/8-bit parallel MCU interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-line serial interface . The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] .

4.5.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of NV3002 can be used by setting external pin as IM [3:0] to “1101”or“1001” for serial interface. The shown figure is the example of 3-line SPI interface.

Figure32.

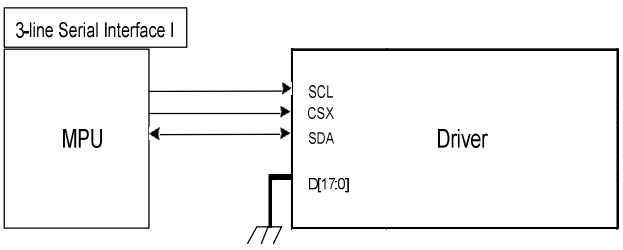
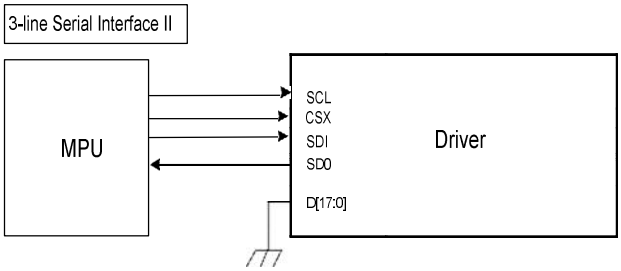


Figure33.



In 3-line serial interface, different display data format is available for three color depths supported by the LCM listed below.

-4k colors, RGB 4, 4, 4 -bits input.

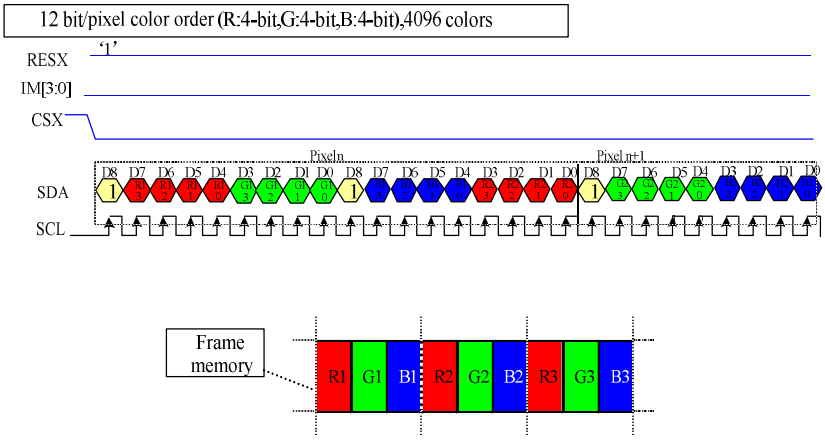
-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

Two pixel (3 sub-pixels) display data is sent by 3 byte transfers when DBI [2:0] bits of 3Ah register are set to “011”.

1). 4K-Colors:12-bit/pixel(RGB 4, 4, 4 -bits input).

Figure34.



Note 1: The pixel data with 12-bit color depth information.

Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

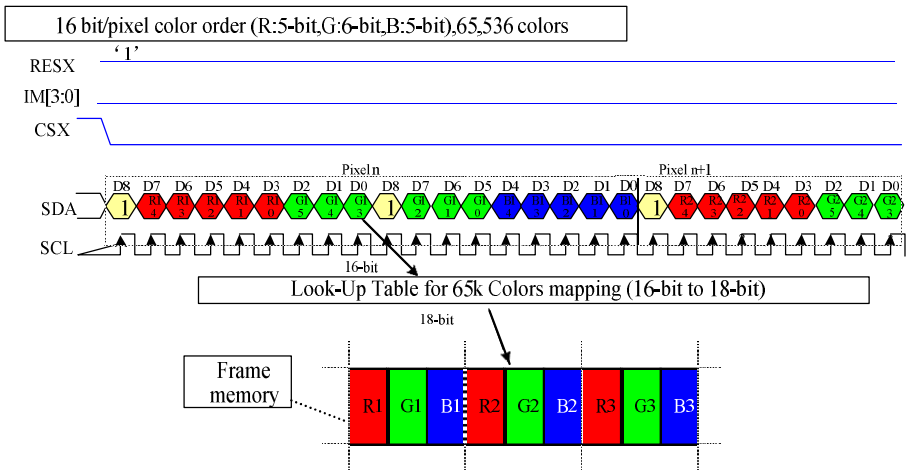
Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: ‘-‘= Don’t care –Can be set “0” or “1”.

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

2). 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

Figure35.



Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

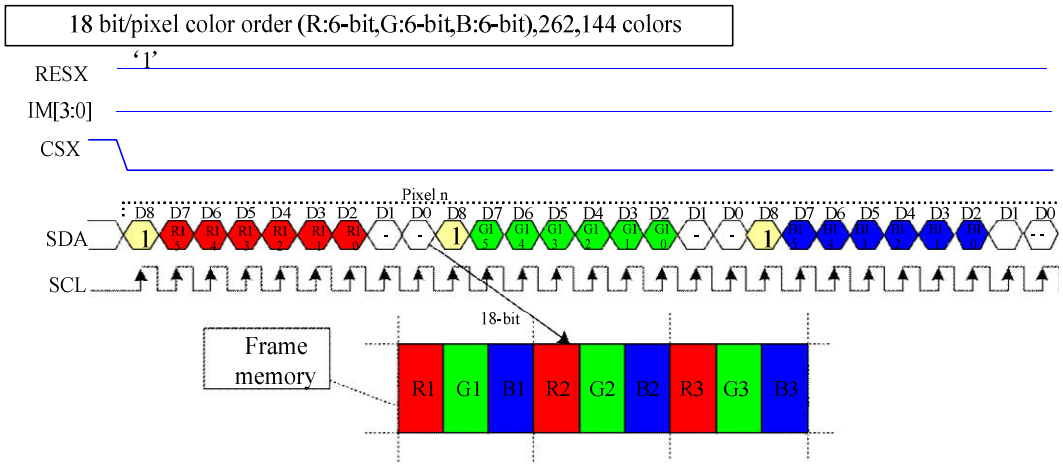
Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

One pixel (3 sub-pixels) display data is sent by 3 byte transfers when DBI [2:0] bits of 3Ah register are set to "110".

3). 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

Figure36.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1"

4.5.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of NV3002 can be used by setting external pin

as IM [3:0] to “1111” or”1011”for serial interface . The shown figure is the example of 4-line SPI interface.

Figure37.

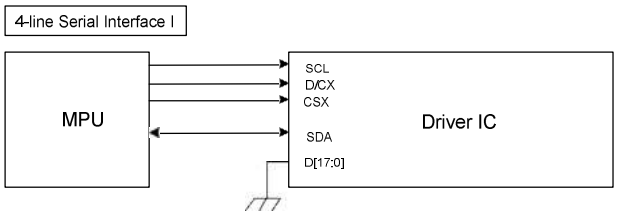
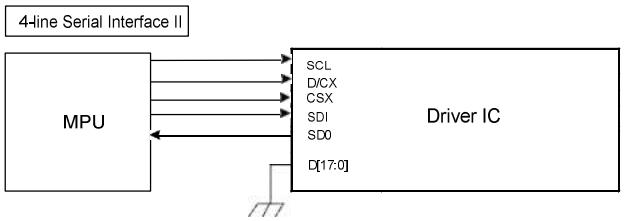


Figure38.



In 4-line serial interface, different display data format is available for three color depths supported by the LCM listed below.

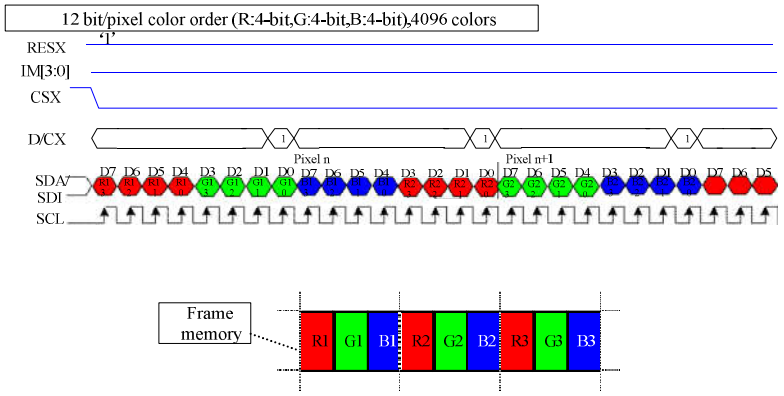
-4k colors, RGB 4, 4, 4 -bits input.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

Two pixel (3 sub-pixels) display data is sent by 3 byte transfers when DBI [2:0] bits of 3Ah register are set to “011”.

Figure39.



Note 1: The pixel data with 12-bit color depth information.

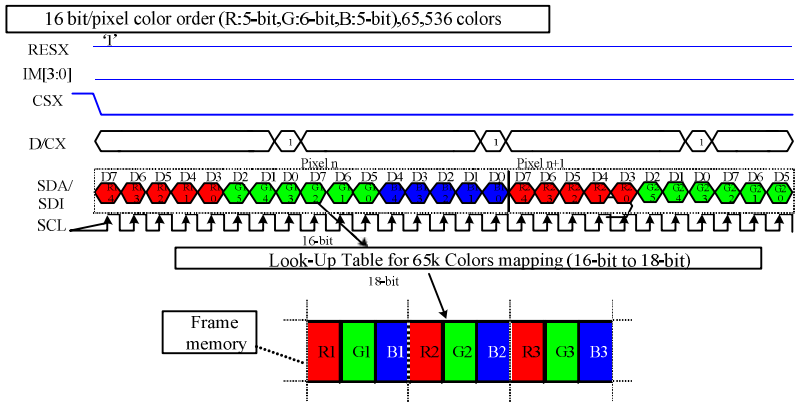
Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Figure40.



Note 1: The pixel data with 16-bit color depth information.

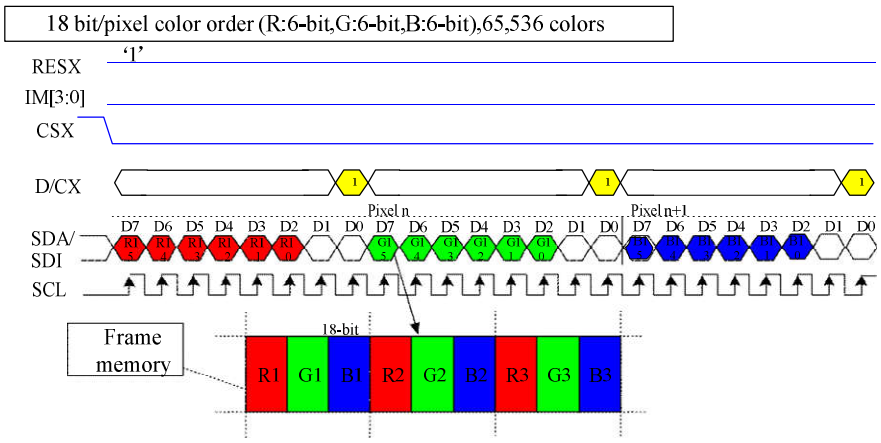
Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

One pixel (3 sub-pixels) display data is sent by 3 byte transfers when DBI [2:0] bits of 3Ah register are set to "110".

Figure41.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

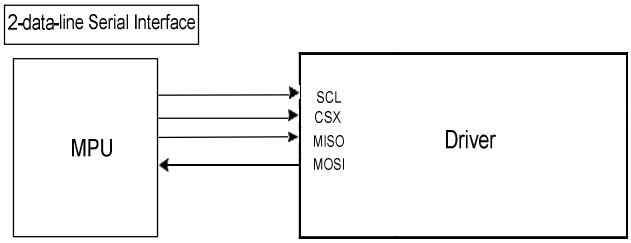
Note 4: '-'= Don't care –Can be set "0" or "1".

4.5.3. 2-data-line mode

2-data-line mode bus interfaces include CS, SCL,MOSI/MISO.The chip-select CS (active low) enables and disables the serial interface. SCL is the serial data clock. MOSI/MISO are serial data lines.

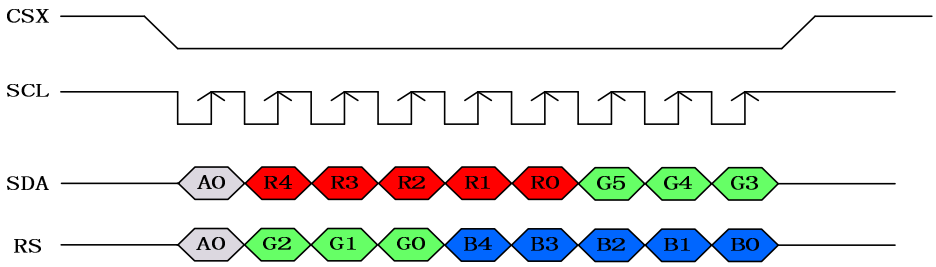
This mode only supports write RAM and is implemented by MOSI bus. The specific timing is shown in the figure below.

Figure42.



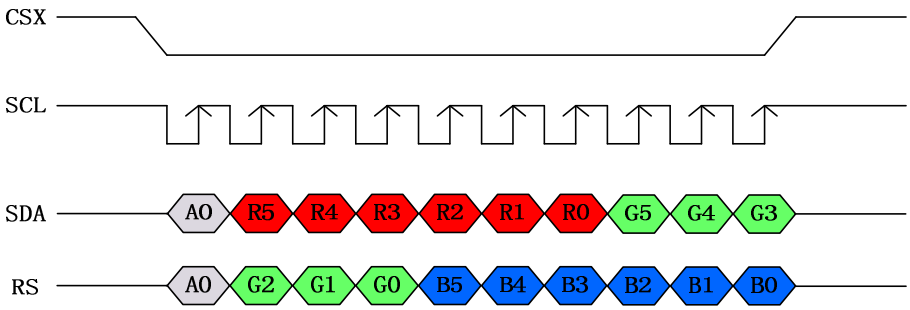
1). RGB565 1/1pixel/transition(65K color,dbi[2:0]='101')

Figure43：Display format 1



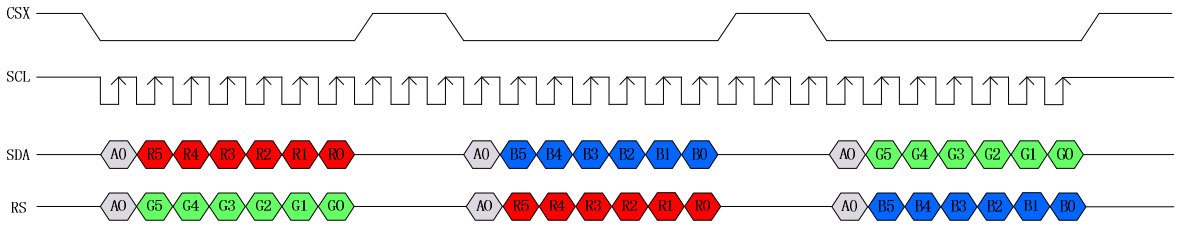
2). RGB666 1/1pixel/transition(262K color,dbi[2:0]=’110’,mdt[1:0]=’00’)

Figure44：Display format 1



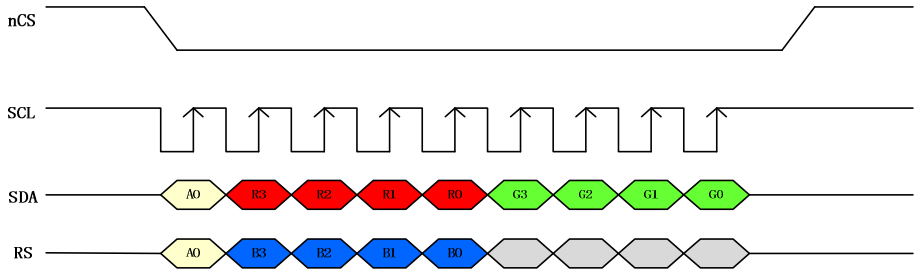
3). RGB6-6-6 2/3pixel/transition(262K color,dbi[2:0]=’110’,mdt[1:0]=’01’)

Figure45.



4) . RGB444 1/1pixel/transition(262K color,dbi[2:0]=’011’)

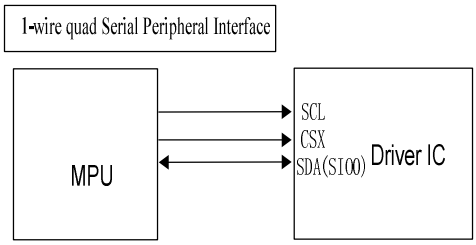
Figure46.



4.5.4. 1-wire quad Serial Peripheral Interface

The 1-wire quad serial bus interface of NV3002 can be used by setting external pin as IM [3:0] to “1010” for serial interface. The shown figure is the example of 1-wire quad SPI interface.

Figure47.



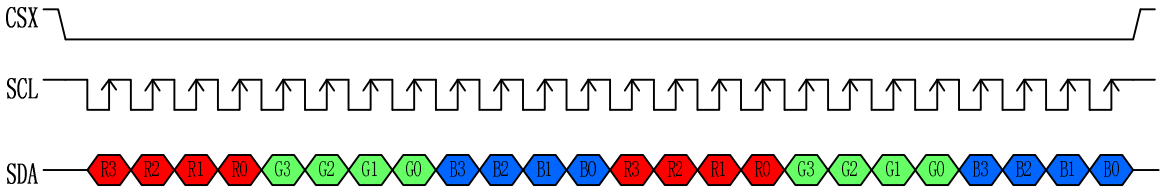
Different display data formats are available for three color depths supported by listed below.

- 4K-Colors, RGB 4, 4, 4 -bits input data.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1). 4K-Colors:12-bit/pixel(RGB 4, 4, 4 -bits input).

Two pixel (3 sub-pixels) display data is sent by 3 byte transfers when DBI [2:0] bits of 3Ah register are set to “011”.

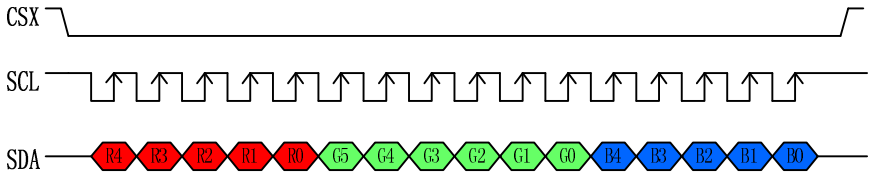
Figure48.



2) . 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

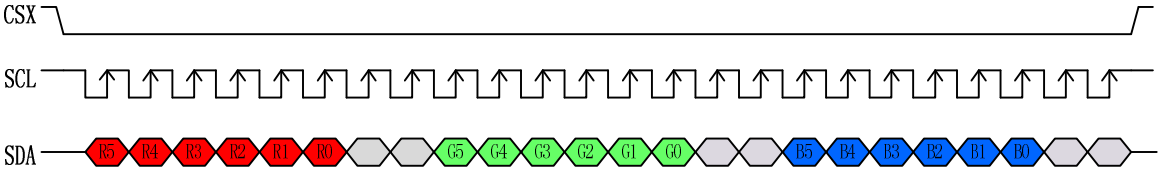
Figure49.



3). 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “110”.

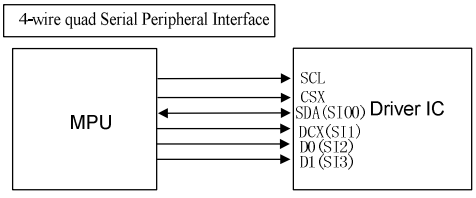
Figure50.



4.5.5. 4-wire quad Serial Peripheral Interface

The 4-wire quad serial bus interface of NV3002 can be used by setting external pin as IM [3:0] to “1010” for serial interface. The shown figure is the example of 4-wire quad SPI interface.

Figure51.



Different display data formats are available for three color depths supported by listed below,For RGB565 and RGB666 data formats, there are two modes of display..

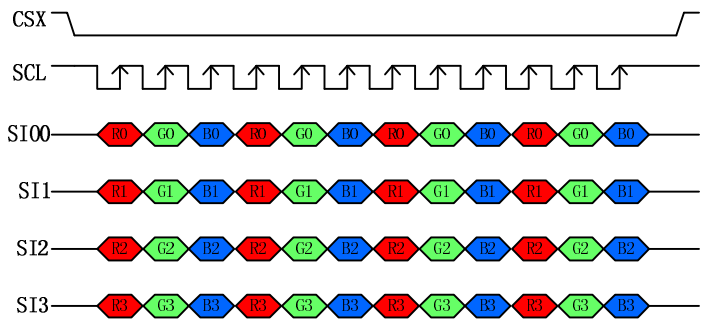
- 4K-Colors, RGB 4, 4, 4 -bits input data.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1). 4K-Colors:12-bit/pixel(RGB 4, 4, 4 -bits input).

Two pixel (3 sub-pixels) display data is sent by 3 byte transfers when DBI [2:0] bits of 3Ah register are set to “011”.

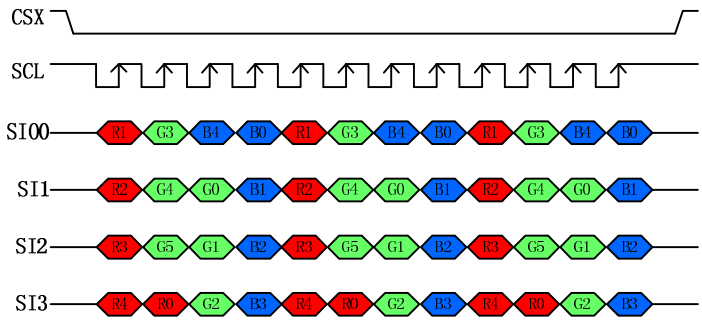
Figure52.



2). 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

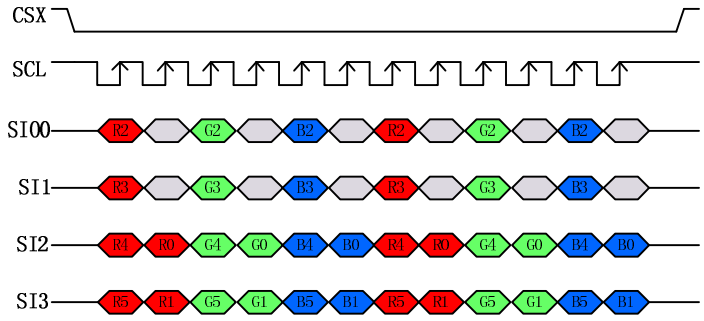
Figure53.



3). 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “110”.

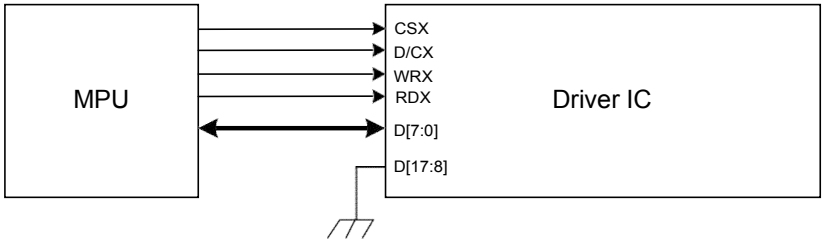
Figure54.



4.5.6. 8-bit Parallel MCU Interface

The 8080-Ⅰsystem 8-bit parallel bus interface of NV3002 can be used by setting external pin as IM [3:0] to“0100”..The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure55.



Different display data formats are available for three color depths supported by listed below.

- 4K-Colors, RGB 4, 4, 4 -bits input data.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1). 4K-Colors:12-bit/pixel(RGB 4, 4, 4 -bits input).

Two pixel (3 sub-pixels) display data is sent by 3 byte transfers when DBI [2:0] bits of 3Ah register are set to “011”.

Table 13.

Count	0	1	2	3	4	…	357	358	359	360
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R3	0B3	1R3	2R3	…	237G3	238R3	238B3	239G3
D6	C6	0R2	0B2	1G2	2R2	…	237G2	238R2	238B2	239G2

D5	C5	0R1	0B1	1G1	2R1	…	237G1	238R1	238B1	239G1
D4	C4	0R0	0B0	1G0	2R0	…	237G0	238R0	238B0	239G0
D3	C3	0R3	1R3	1B3	1R3	…	237B3	238G3	239R3	239B3
D2	C2	0G2	1R2	1B2	1G2	…	237B2	238G2	239R2	239B2
D1	C1	0G1	1R1	1B1	1G1	…	237B1	238G1	239R1	239B1
D0	C0	0G0	1R0	1B0	1G0	…	237B0	238G0	239R0	239B0

2). 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Table 14.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

3). 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

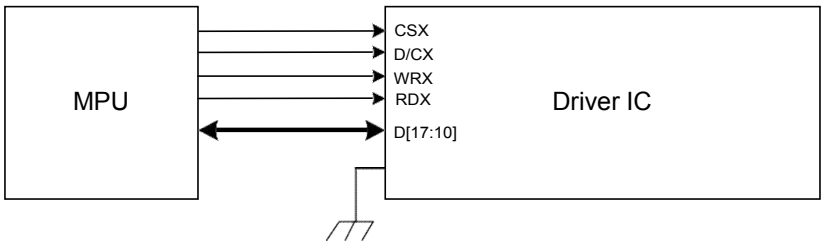
One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Table15.

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

The 8080-II system 8-bit parallel bus interface of NV3002 can be used by settings as IM [3:0] =”0000”. The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.

Figure56.



Different display data formats are available for three color depths supported by listed below.

- 4K-Colors, RGB 4, 4, 4 -bits input data.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

4). 4K-Colors:16-bit/pixel(RGB 4, 4, 4 -bits input).

Two pixel (3 sub-pixels) display data is sent by 3 byte transfers when DBI [2:0] bits of 3Ah register are set to “011”.

Table16.

Count	0	1	2	3	4	…	357	358	359	360
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R3	0B3	1R3	2R3	…	237G3	238R3	238B3	239G3
D16	C6	0R2	0B2	1G2	2R2	…	237G2	238R2	238B2	239G2
D15	C5	0R1	0B1	1G1	2R1	…	237G1	238R1	238B1	239G1
D14	C4	0R0	0B0	1G0	2R0	…	237G0	238R0	238B0	239G0
D13	C3	0R3	1R3	1B3	1R3	…	237B3	238G3	239R3	239B3
D12	C2	0G2	1R2	1B2	1G2	…	237B2	238G2	239R2	239B2
D11	C1	0G1	1R1	1B1	1G1	…	237B1	238G1	239R1	239B1
D10	C0	0G0	1R0	1B0	1G0	…	237B0	238G0	239R0	239B0

5). 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0]

bits of 3Ah register are set to “101”.

Table17.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D13	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D12	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

6).262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to“110”.

Table18.

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D17	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D14	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D11	C1				…			
D10	C0				…			

5. Function Description

5.1. Display data GRAM mapping

The display data RAM stores display dots and consists of 539460 bits . There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

GRAM address for display panel position as shown in the following table Table29.

(00,00)h	(00,01)h	…… …	(00, ED)h	(00, EE)h	(00,EF)h
(01,00)h	(01,01)h	…… …	(01, ED)h	(01, EE)h	(01, EF)h
(02,00)h	(02,01)h	…… …	(02, ED)h	(02, EE)h	(02, EF)h
(03,00)h	(03,01)h	…… …	(03, ED)h	(03, EE)h	(03, EF)h
. . .	. . .	. . .	. . .	. . .	. . .
(ED,00)h	(ED,01)h	…… …	(ED, ED)h	(ED, EE)h	(ED, EF)h
(EE,00)h	(EE,01)h	…… …	(EE, ED)h	(EE, EE)h	(EE, EF)h
(EF,00)h	(EF,01)h	…… …	(EF, ED)h	(EF, EE)h	(EF, EF)h

5.2. MCU to memory write/read direction

The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits D5, D6, and D7 as described below.

Figure59.

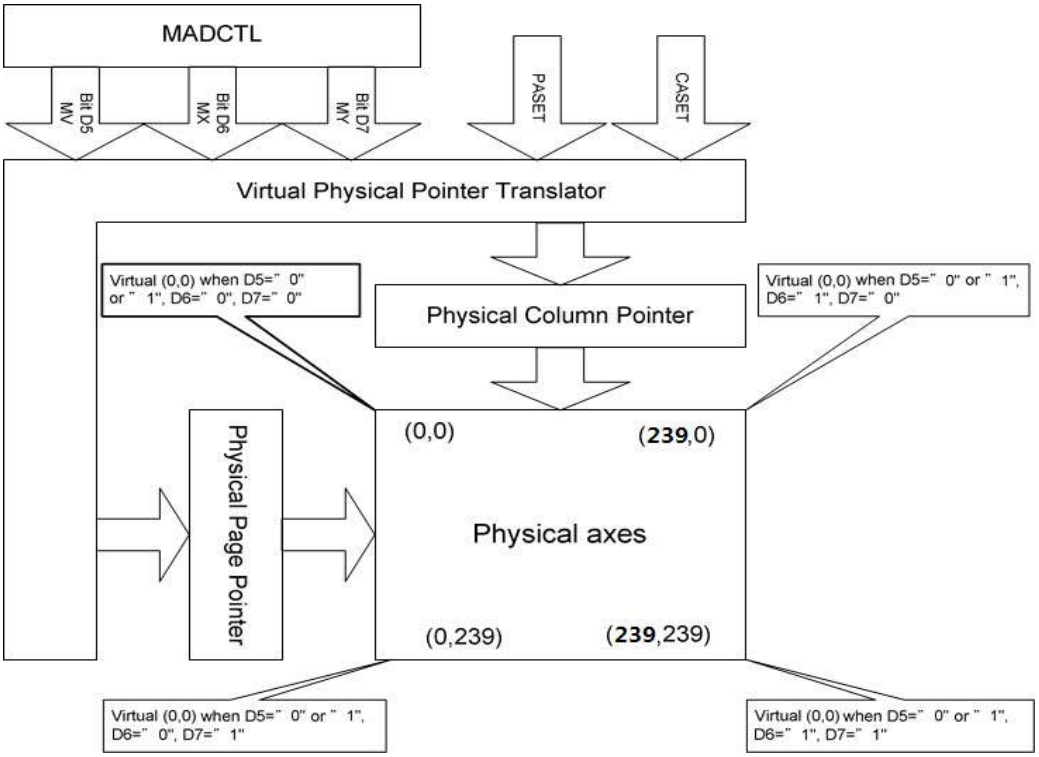


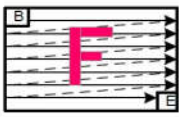
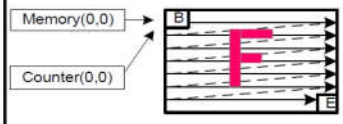
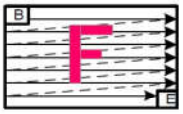
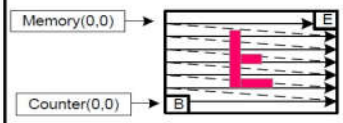
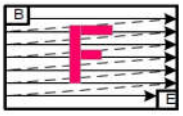
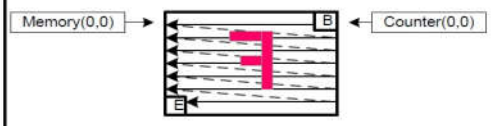
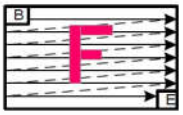
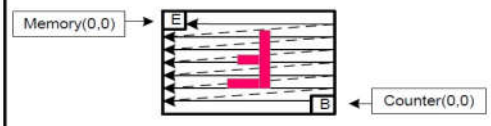
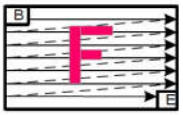
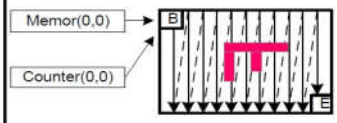
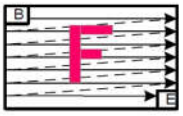
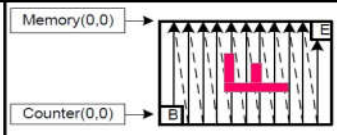
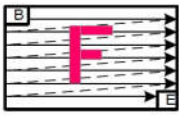
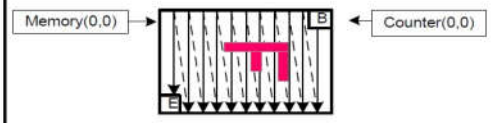
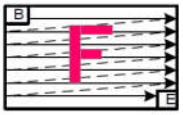
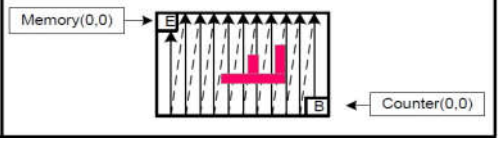
Table30.

D5	D6	D7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (239-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (239-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (239-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (239-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “Start column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than “End Column”	Return to “Start column”	Increment by 1
The Page counter is large than “End Page”	Return to “Start column”	Return to “Start Page”

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MCU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

5.3. GRAM to display address mapping

By setting the **SS**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS** , the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR**, the relation between the source output channel and the <R>,<G>,

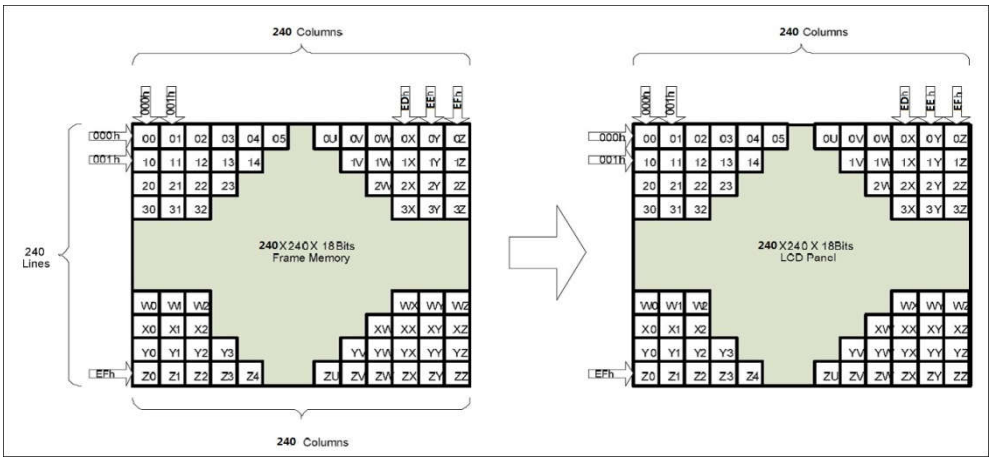
<B> dot allocation can be reversed for different LCD color filter arrangement.

The following Tables show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

GRAM X address and display panel position:

NV3002 supports three kinds of display mode: one is Normal Display Mode, the other is Partial Display Mode, and Scrolling Display Mode.

Figure 60.

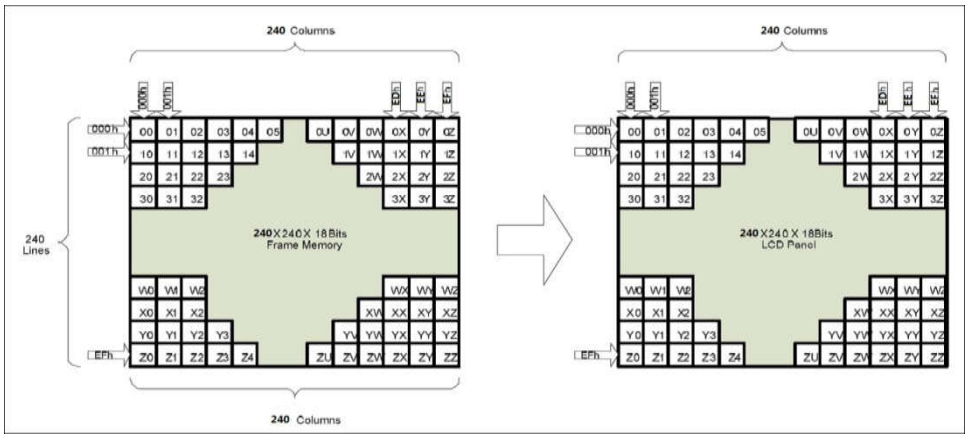


5.3.1. Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 00EFh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)

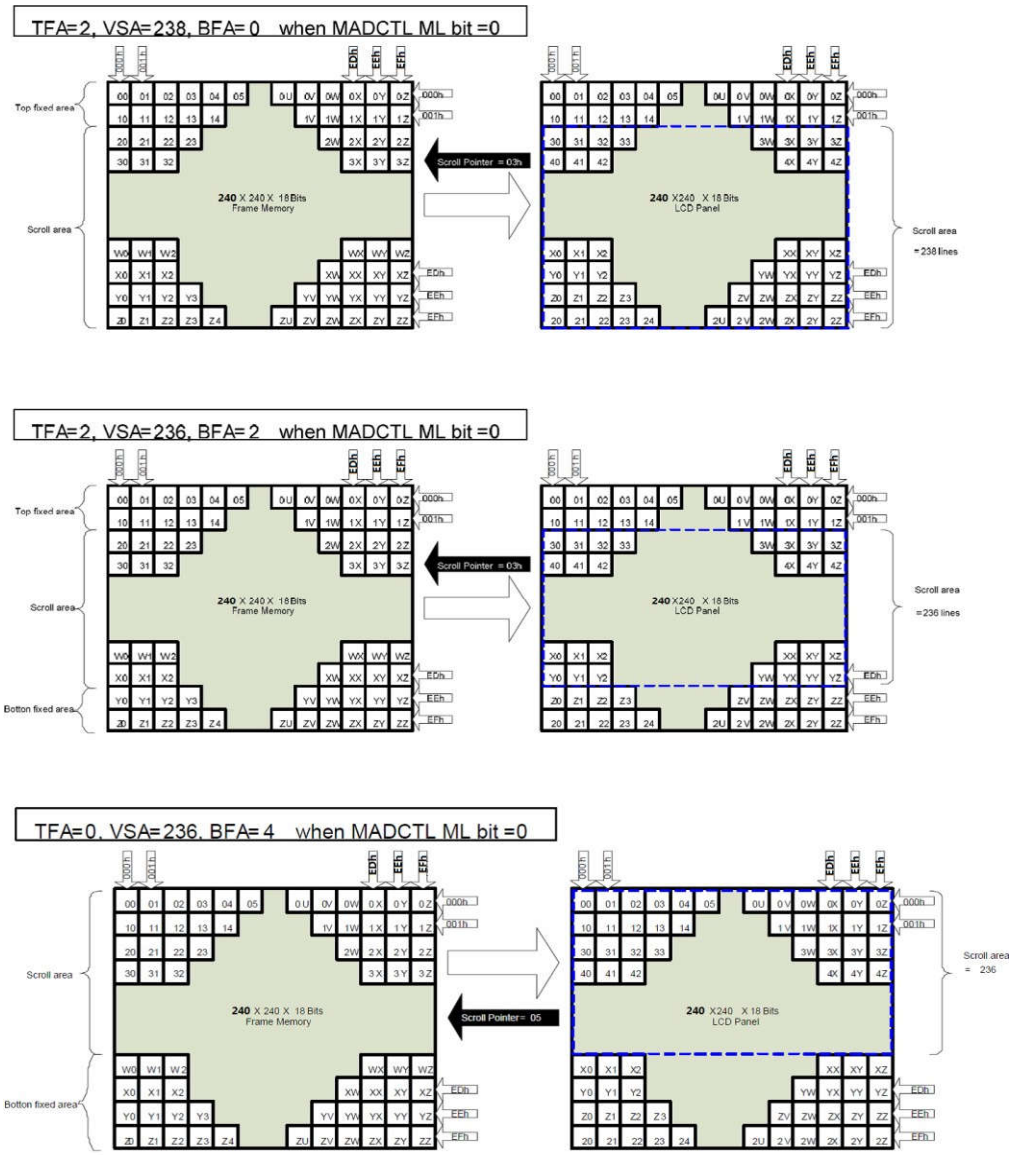
Figure61.



5.3.2. Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA ,BFA** bits (R33h) and **VSP** bits (R37h).

Figure62.



Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 240, Scrolling Mode is undefined.

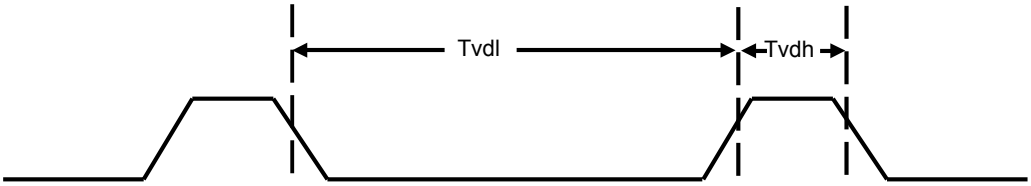
5.4. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame

Memory Writing when displaying video images.

5.4.1. Tearing effect line modes

Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only: Figure68.



Tvdh= The LCD display is not updated from the Frame Memory

Tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 240 H-sync pulses per field.

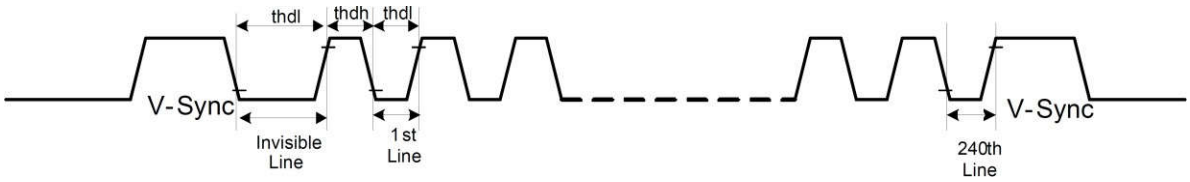


Figure69.

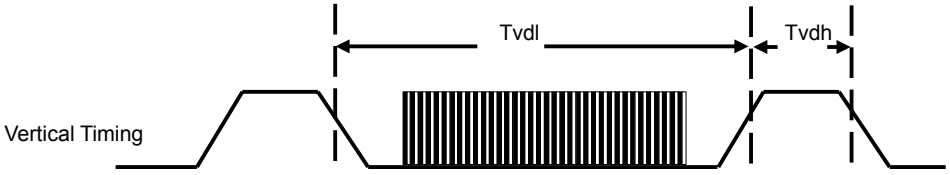
thdh= The LCD display is not updated from the Frame Memory

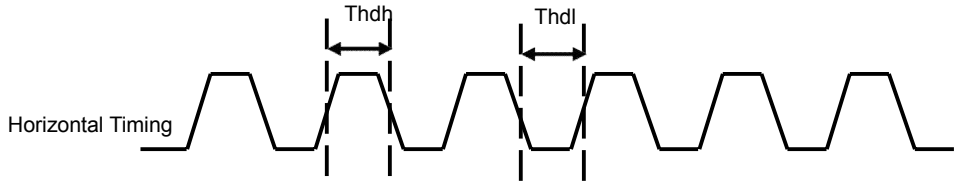
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

5.4.2. Tearing effect line timing

The Tearing Effect signal is described below.

Figure70.





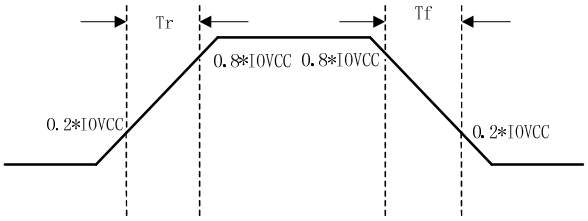
Idle Mode Off (Frame Rate = 20~75 Hz)

Table32.

Symbol	Parameter	Spec.			Description
		Min.	Max.	Unit	
Tvdl	Vertical Timing Low Duration	TBD	-	ms	-
Tvdh	Vertical Timing High Duration	1000	-	us	-
Thdl	Horizontal Timing Low Duration	TBD	-	us	-
Thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: Idle Mode Off (Frame Rate = 20~75 Hz) , The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Figure71.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

5.5. Source driver

Source driver of NV3002 contains 360 channels (S1~S360), is used for driving the source line of a-TFT LCD Panel. The source driver converts the digital data from GRAM into the analog voltage for 360 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.5. GIP driver

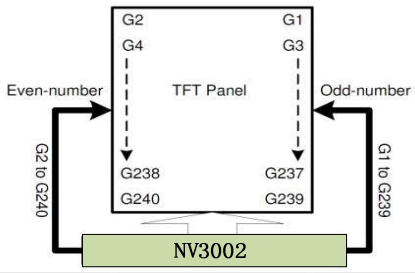
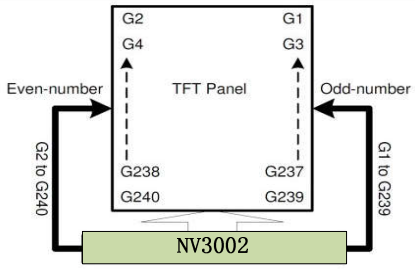
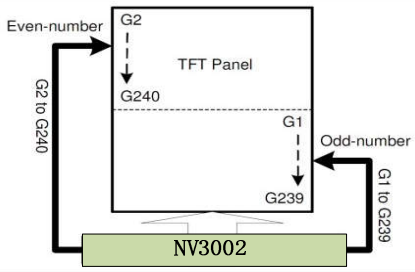
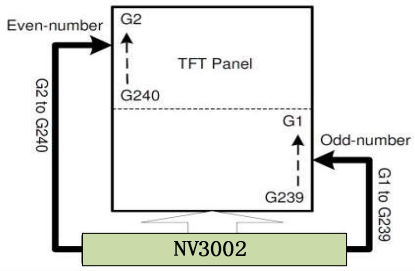
GIP driver of NV3002 contains a 32 channels (G1~G32), is used for generate dual-gate control signal on a-TFT LCD Panel. The GIP driver level is VGH when scan some line, VGL the other lines.

5.6. Scan mode setting

GS: Sets the direction of scan by the gate driver, The scan direction determined by GS = 0 can be reversed by setting GS = 1.

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

Table33.

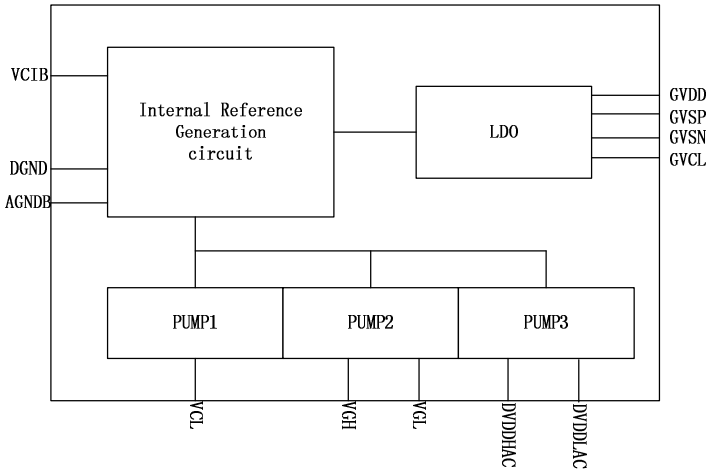
SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→G4→ …… ….→G237→G238→G239→G240
0	1		G240→G239->G238→G237→…… …. →G4→G3→G2→G1
1	0		G1→G3→……..→G237→G239→ G2→G4→……→G238→G240
1	1		G240→G238→……..→G4→G2→ G239→G237→……→G3→G1

5.7. LCD power generation circuit

5.7.1. Power supply circuit

The power circuit of NV3002 is used to generate supply voltages for LCD panel driving.

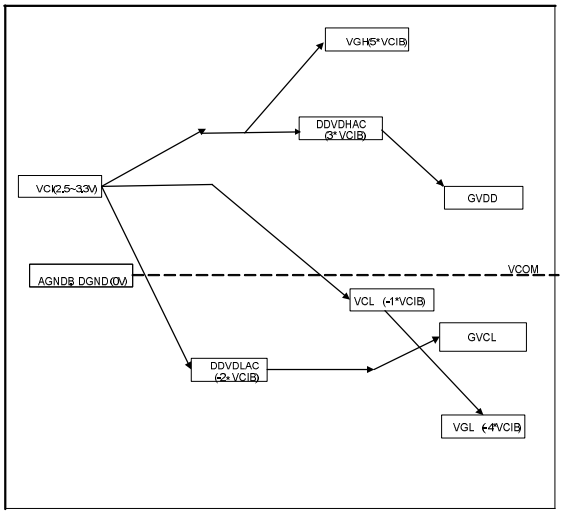
Figure72.



5.7.2. LCD power generation scheme

The boost voltage generated is shown as below.

Figure73.



LCD power generation scheme

5.8. Gamma Correction

NV3002 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make NV3002 available with liquid crystal panels of various characteristics.

Figure74.

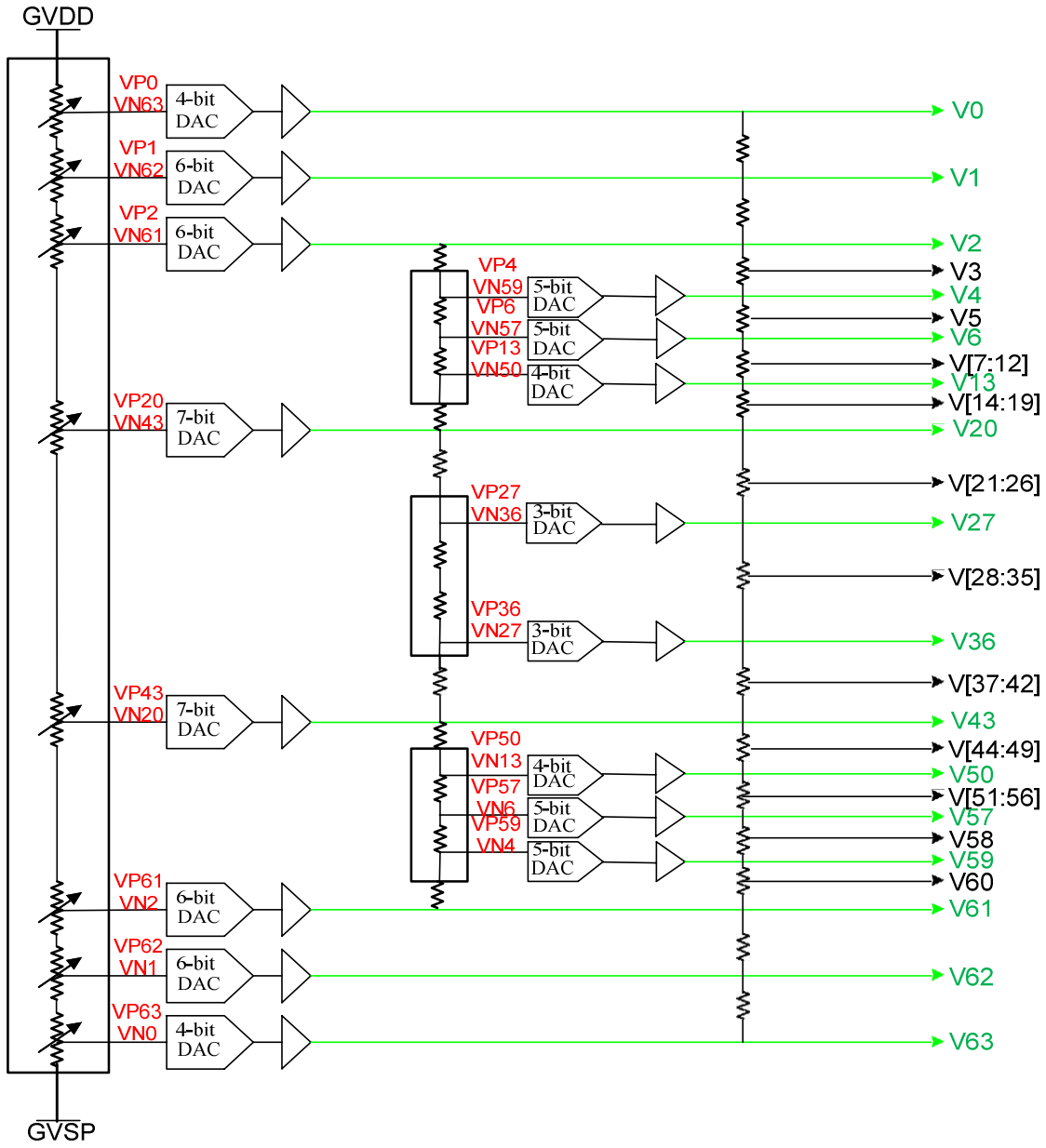
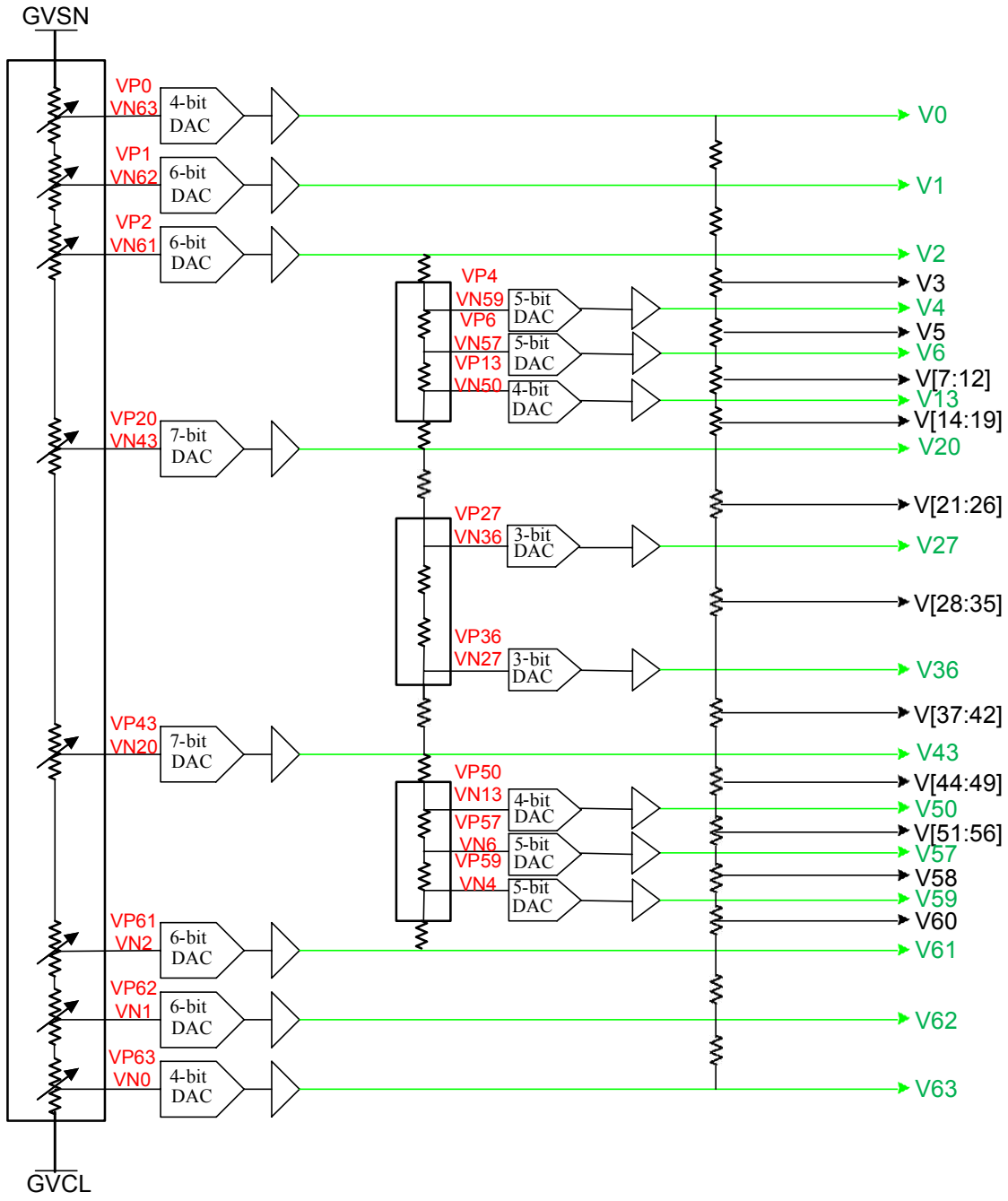
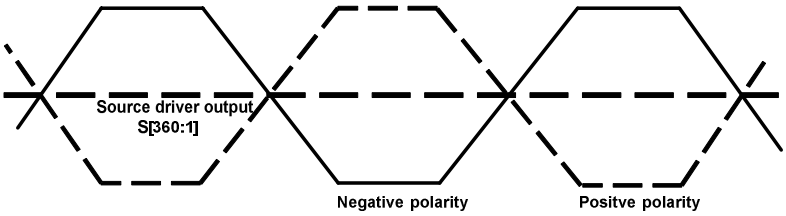


Figure75.



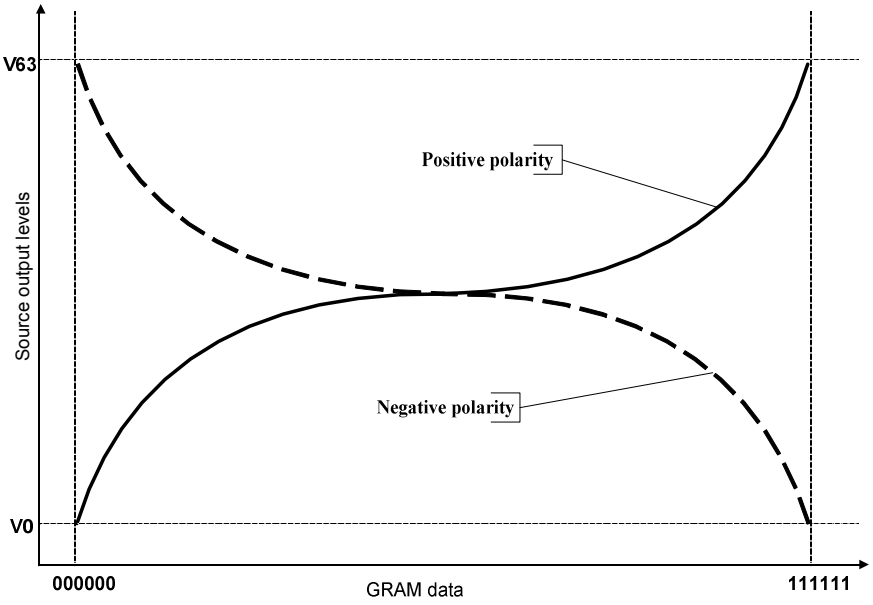
Grayscale Voltage Generation

Figure76. Dot inversion



Relationship between Source Output and VCOM

Figure77.



5.9. Power Level Definition

5.9.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.

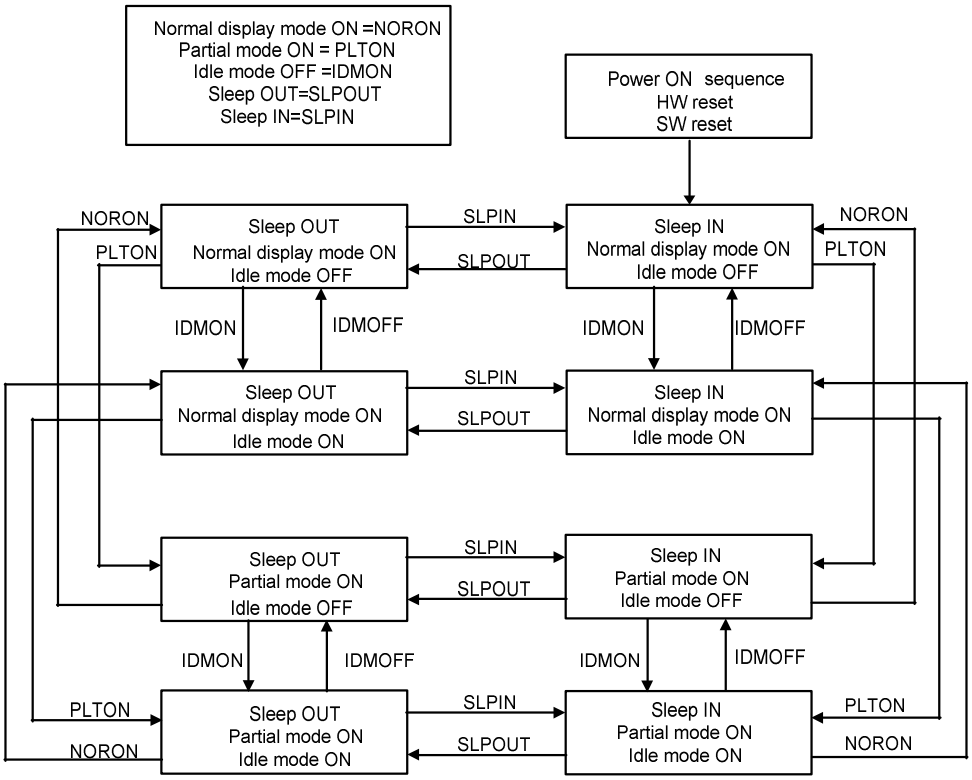
6. Power Off Mode.

In this mode, both VCIB and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

5.9.2. Power Flow Chart

Figure78.



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

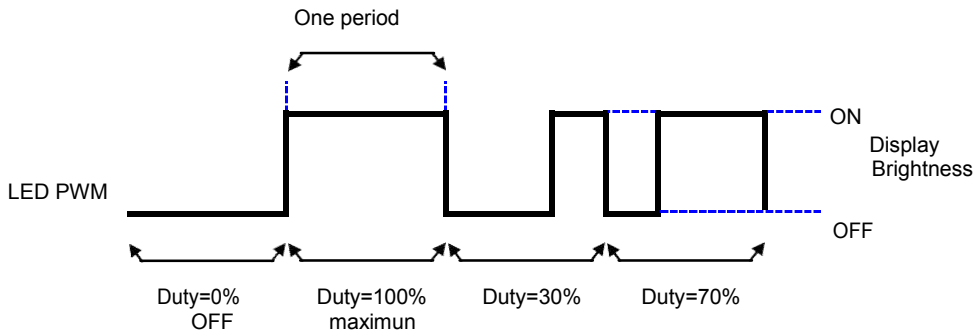
Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

5.9.3. Brightness control block

There is an external output signal from brightness block, LEDPWM to control the LED driver IC in order to control display brightness.

There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The LEDPWM duty is calculated as DBV[7:0]/255 x period (affected by OSC frequency).

For example: LEDPWM period = 3ms, and DBV[7:0] = '200DEC'. Then LEDPWM duty = 200 / 255=78.1%. Correspond to the LEDPWM period = 3 ms, the high-level of LEDPWM (high effective) = 2.344ms, and the low-level of LEDPWM = 0.656ms. Figure79.



LEDPWM output duty

5.10. Input/output pin state

5.10.1. Output pins

Table34.

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDA	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low
LEDPWM	Low	Low

Characteristics of output pins

5.10.2. Input pins

Table35.

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
RESX	Input valid	Input valid	Input valid	Input valid
CSX	Input invalid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input invalid

Characteristics of input pins

6. Command

6.1. Command List

NAME	ADDR	Access	D7	D6	D5	D4	D3	D2	D1	D0
NOP	00h	W								
RDDIDIF	04H	Multi-R	sys_id1[7:0]							
			sys_id2[7:0]							
			sys_id3[7:0]							
RDDST	09h	Multi-R	pump_en	sys_my	sys_mx	sys_mv	sys_ml	sys_bgr		
				dbi[2:0]			color8_en	ptl_on	slpout	normal_on
			scroll_on		inv_on	gs	ss	disp_en	te_on	
					telom					
SLPIN	10h	W								
SLPOUT	11h	W								
PARMON	12h	W								
NORMON	13h	W								
INVOFF	20h	W								
INVOFF	21h	W								
DISPOFF	28h	W								
DISPON	29h	W								
COLSET	2Ah	Multi-W								sc[8]
			sc[7:0]							
										ec[8]

			ec[7:0]						
ROWSET	2Bh	Multi-W							sp[8]
			sp[7:0]						
									ep[8]
			ep[7:0]						
MEMWR	2Ch	W							cmd_2c_start
MEMRD	2Eh	R							
PAREA	30h	Multi-W							sr[8]
			sr[7:0]						
									er[8]
			er[7:0]						
VSDEF	33h	Multi-W							tfa[8]
			tfa[7:0]						
									vsa[8
			vsa[7:0]						
									bfa[8]
			bfa[7:0]						
TEOFF	34h	W							
TEON	35h	W							telom
MADCTRL	36h	W	sys_my	sys_mx	sys_mv	sys_ml	sys_bgr		
VSSAD	37h	Multi-W							vsp[8]
			vsp[7:0]						
IDLEOFF	38h	W							

IDLEON	39h	W								
PFSET	3Ah	W						dbi[2:0]		
WRMEMC	3Ch	W								
IFCTRL1	40h	W				sdo_hiz				sda_sdo_en
IFCTRL2	41h	W							gd_cnt_mux	spi_2dat_en
IFCTRL3	42h	W				qspi_bgr			qspi_dummy	qspi_sbyte
IFCTRL4	43h	W			we_mod	endian	epf[1:0]		mdt[1:0]	
TECTRL1	44h	Multi-W								sts[8]
			sts[7:0]							
TECTRL2	45h	Multi-R								sts[8]
			sts[7:0]							
TECTRL3	46h	W				te_oe			te_pol	te_extend
TECTRL4	47h	Multi-W			te_v_start[5:0]					
				te_v_end[6:0]						
TECTRL5	48h	Multi-W			te_h_start[5:0]					
				te_h_end[6:0]						
SCANCTRL	49h	W						gs		ss
OTPCTRL1	4Ah	W		otp_ptm[1:0]		otp_pwe	otp_prd	otp_pprog	otp_vpp_sel	otp_vpp_src_sel
OTPCTRL2	4Bh	W	otp_pa[7:0]							
OTPCTRL3	4Ch	W	otp_pdin[7:0]							
OTPCTRL4	4Dh	R	otp_rd_dat[7:0]							
OTPCTRL5	4Eh	Multi-R	otp_crc[15:8]							
			otp_crc[7:0]							

USRMAD	4Fh	W	usr_my	usr_mx	usr_mv	usr_ml	usr_bgr			
RESCTRL1	50h	W						res_h_sel[2:0]		
RESCTRL2	51h	W	res_v_start[7:0]							
RESCTRL3	52h	W	res_v_num[7:0]							
ITCTRL1	53h	W	inter_vbp[7:0]							
ITCTRL2	54h	W	fr_div	inter_vfp[6:0]						
ITCTRL3	55h	W	inter_hbp[7:0]							
ITCTRL4	56h	W	inter_hfp[7:0]							
IBIASCTRL	57h	W						bias_adj[2:0]		
OSCCTRL	58h	W	osc_force_en				osc_trim[3:0]			
LVDCTRL	59h	W				lvd_en			lvd_sel[1:0]	
ALGCTRL1	5Ah	W	merge_disable	merge_times_porch_h[6:0]						
ALGCTRL2	5Bh	Multi-W	algo_pattern_en[15:8]							
			algo_pattern_en[7:0]							
RAMCTRL1	5Ch	W							mec_restart	mbist_en
RAMCTRL2	5Dh	W		pchsel_l	wlsel_l	scsel_l		pchsel_r	wlsel_r	scsel_r
RDBIST	5Eh	Multi-R	mec_restart	mbist_en	mbist_done	mbist_abort	l_mec_pxl1_hit	l_mec_pxl2_hit	r_mec_pxl1_hit	r_mec_pxl2_hit
							l_mec_pxl1_row[8]	l_mec_pxl2_row[8]	r_mec_pxl1_row[8]	r_mec_pxl2_row[8]
			l_mec_pxl1_row[7:0]							
			l_mec_pxl1_col[7:0]							
			l_mec_pxl2_row[7:0]							
			l_mec_pxl2_col[7:0]							
			r_mec_pxl1_row[7:0]							

			r_mec_pxl1_col[7:0]							
			r_mec_pxl2_row[7:0]							
			r_mec_pxl2_col[7:0]							
LBCTRL	5Fh	W		lb1_pchsel	lb1_wlsel	lb1_scsel		lb2_pchsel	lb2_wlsel	lb2_scsel
GAMCTRL1	60h	W					vrp0[3:0]			
GAMCTRL2	61h	W			vrp1[5:0]					
GAMCTRL3	63h	W				vrp4[4:0]				
GAMCTRL5	64h	W				vrp6[4:0]				
GAMCTRL6	65h	W				vrp13[3:0]				
GAMCTRL7	66h	W		vrp20[6:0]						
GAMCTRL8	67h	W		vrp27[2:0]				vrp36[2:0]		
GAMCTRL9	68h	W		vrp43[6:0]						
GAMCTRL10	69h	W					vrp50[3:0]			
GAMCTRL11	6Ah	W				vrp57[4:0]				
GAMCTRL12	6Bh	W					vrp59[4:0]			
GAMCTRL13	6Ch	W			vrp61[5:0]					
GAMCTRL14	6Dh	W			vrp62[5:0]					
GAMCTRL15	6Eh	W					vrp63[3:0]			
GAMCTRL16	6Fh	W			vj0p63[1:0]				vj1p63[1:0]	
GAMCTRL17	70h	W					vrn0[3:0]			
GAMCTRL18	71h	W			vrn1[5:0]					
GAMCTRL19	72h	W			vrn2[5:0]					
GAMCTRL20	73h	W				vrn4[4:0]				

GAMCTRL21	74h	W				vrn6[4:0]				
GAMCTRL22	75h	W					vrn13[3:0]			
GAMCTRL23	76h	W		vrn20[6:0]						
GAMCTRL24	77h	W		vrn27[2:0]			vrn36[2:0]			
GAMCTRL25	78h	W		vrn43[6:0]						
GAMCTRL26	79h	W					vrn50[3:0]			
GAMCTRL27	7Ah	W				vrn57[4:0]				
GAMCTRL28	7Bh	W				vrn59[4:0]				
GAMCTRL29	7Ch	W			vrn61[5:0]					
GAMCTRL30	7Dh	W			vrn62[5:0]					
GAMCTRL31	7Eh	W					vrn63[3:0]			
GAMCTRL32	7Fh	W			vj0n63[1:0]			vj1n63[1:0]		
RGLRCTRL1	80h	W				test_en		dvdd_adj[2:0]		
RGLRCTRL2	81h	W	bgr_adj[3:0]				vref_adj[3:0]			
VDDSCTRL	82h	W						vdds_trim[2:0]		
GLDOCTRL1	83h	W	gvcl_adj[7:0]							
GLDOCTRL2	84h	W	gvdd_ adj [7:0]							
GLDOCTRL3	85h	W		gvsp_ adj [6:0]						
GLDOCTRL5	87h	W		gvcl_vfb_trim[2:0]				gvdd_vfb_trim[2:0]		
ESDCTRL1	8Ah	W							esd_func_sel[1:0]	
ESDCTRL2	8Bh	W				esd_enable			esd_force_cs_1	esd_force_dc_1
ESDCTRL3	8Ch	R	esd_det[3:0]							esd_occured
RDOTPLD	8Eh	R						por	lvd	otp_loading

PWRCTRL1	8Fh	W			vgh_clk_sel[1:0]		vgl_clk_sel[1:0]	mv_clk_sel[1:0]
PWRCTRL2	90h	Multi-W	ddvdh_drain_row_on[8]	ddvdh_drain_row_off[8]			ddvdh_drain_frm_on[1:0]	ddvdh_drain_frm_off[1:0]
			ddvdh_drain_row_on[7:0]					
			ddvdh_drain_row_off[7:0]					
PWRCTRL3	91h	Multi-W	ddvdh_en_row_on[8]	ddvdh_en_row_off[8]			ddvdh_en_frm_on[1:0]	ddvdh_en_frm_off[1:0]
			ddvdh_en_row_on[7:0]					
			ddvdh_en_row_off[7:0]					
PWRCTRL4	92h	Multi-W	ddvdl_en_row_on[8]	ddvdl_en_row_off[8]			ddvdl_en_frm_on[1:0]	ddvdl_en_frm_off[1:0]
			ddvdl_en_row_on[7:0]					
			ddvdl_en_row_off[7:0]					
PWRCTRL5	93h	Multi-W	mv_disch_row_on[8]	mv_disch_row_off[8]			mv_disch_frm_on[1:0]	mv_disch_frm_off[1:0]
			mv_disch_row_on[7:0]					
			mv_disch_row_off[7:0]					
PWRCTRL6	94h	Multi-W	vgh_en_row_on[8]	vgh_en_row_off[8]			vgh_en_frm_on[1:0]	vgh_en_frm_off[1:0]
			vgh_en_row_on[7:0]					
			vgh_en_row_off[7:0]					
PWRCTRL7	95h	Multi-W	vgh_disch_row_on[8]	vgh_disch_row_off[8]			vgh_disch_frm_on[1:0]	vgh_disch_frm_off[1:0]
			vgh_disch_row_on[7:0]					
			vgh_disch_row_off[7:0]					
PWRCTRL8	96h	Multi-W	vgh_drain_row_on[8]	vgh_drain_row_off[8]			vgh_drain_frm_on[1:0]	vgh_drain_frm_off[1:0]
			vgh_drain_row_on[7:0]					
			vgh_drain_row_off[7:0]					
PWRCTR9	97h	Multi-W	vgl_en_row_on[8]	vgl_en_row_off[8]			vgl_en_frm_on[1:0]	vgl_en_frm_off[1:0]

			vgl_en_row_on[7:0]						
			vgl_en_row_off[7:0]						
PWRCTRL10	98h	Multi-W	vgl_disch_row_on[8]	vgl_disch_row_off[8]			vgl_disch_frm_on[1:0]	vgl_disch_frm_off[1:0]	
			vgl_disch_row_on[7:0]						
			vgl_disch_row_off[7:0]						
PWRCTRL11	99h	Multi-W	vgl_drain_row_on[8]	vgl_drain_row_off[8]			vgl_drain_frm_on[1:0]	vgl_drain_frm_off[1:0]	
			vgl_drain_row_on[7:0]						
			vgl_drain_row_off[7:0]						
PWRCTRL12	9Ah	W		ddvdh_btrs	ddvdh_btvs[1:0]		ddvdh_btvs_en		
PWRCTRL13	9Bh	W		ddvdl_btrs	ddvdl_btvs[1:0]		ddvdl_btvs_en		
PWRCTRL14	9Ch	W	vgh_noreg		vgh_bth[1:0]				
PWRCTRL15	9Dh	W	gam_sw[4:0]				vgh_set[2:0]		
PWRCTRL16	9Eh	W	vgl_btrs	vgl_noreg				vgl_set[2:0]	
PWRCTRL17	9Fh	Multi-W	gam_ref_bypass	bias_en_bypass	vdds_en_bypass	vref_en_bypass	vgl_drain_bypass	vgl_disch_bypass	gam_en_bypass	pump_ctrl_en
			vgl_en_bypass	vgh_drain_bypass	vgh_disch_bypass	vgh_en_bypass	mv_disch_bypass	ddvdl_en_bypass	ddvdh_en_bypass	ddvdh_drain_bypass
				chop_sw[4:0]					chop_ctrl	sd_en_bypass
GOACTRL	A0h	Multi-W	eck_diff_cnt[2:0]			eck_sel	map_sel[1:0]		goa_slpin_sel[1:0]	
			eck_cnt_num[7:0]							
VSTCTRL1	A1h	W	goa_vst1_shift[7:0]							
VSTCTRL2	A2h	W	goa_vst2_shift[7:0]							
VSTCTRL3	A3h	W	goa_vst3_shift[7:0]							
VSTCTRL4	A4h	W	goa_vst4_shift[7:0]							
VSTCTRL5	A5h	W	vst_gnd1_period[7:0]							

VSTCTRL6	A6h	W	vst_gnd2_period[7:0]							
VSTCTRL7	A6h	W	vst_vci_period[7:0]							
VSTCTRL8	A8h	W	goa_vst_tchop[8]	goa_vst_tglue[8]	vst_noverlap[1:0]		goa_vst_width[3:0]			
VSTCTRL9	A9h	W	goa_vst_tchop[7:0]							
VSTCTRL10	AAh	W	goa_vst_tglue[7:0]							
VENDCTRL1	ABh	Multi-W							goa_vend1_shift_start[9:8]	
			goa_vend1_shift_start[7:0]							
VENDCTRL2	ACh	Multi-W							goa_vend1_shift_end[9:8]	
			goa_vend1_shift_end[7:0]							
VENDCTRL3	ADh	Multi-W							goa_vend2_shift_start[9:8]	
			goa_vend2_shift_start[7:0]							
VENDCTRL4	AEh	Multi-W							goa_vend2_shift_end[9:8]	
			goa_vend2_shift_end[7:0]							
VENDCTRL5	AFh	Multi-W							goa_vend3_shift_start[9:8]	
			goa_vend3_shift_start[7:0]							
VENDCTRL6	B0h	Multi-W							goa_vend3_shift_end[9:8]	
			goa_vend3_shift_end[9:8]							
VENDCTRL7	B1h	Multi-W							goa_vend4_shift_start[9:8]	
			goa_vend4_shift_start[7:0]							
VENDCTRL8	B2h	Multi-W							goa_vend4_shift_end[9:8]	
			goa_vend4_shift_end[7:0]							
VENDCTRL9	B3h	W	vend_gnd1_period[7:0]							
VENDCTRL10	B4h	W	vend_gnd2_period[7:0]							

VENDCTRL11	B5h	W	vend_vci_period[7:0]						
VENDCTRL12	B6h	W	goa_vend_tchop[8]	goa_vend_tglue[8]	vend_noverlap[1:0]				bw_fw_sel
VENDCTRL13	B7h	W	goa_vend_tchop[7:0]						
VENDCTRL14	B8h	W	goa_vend_tglue[7:0]						
CLKCTRL1	B9h	W	goa_clk1_shift[7:0]						
CLKCTRL2	BAh	W	goa_clk2_shift[7:0]						
CLKCTRL3	BBh	W	goa_clk3_shift[7:0]						
CLKCTRL4	BCh	W	goa_clk4_shift[7:0]						
CLKCTRL5	BDh	W	goa_clk5_shift[7:0]						
CLKCTRL6	BEh	W	goa_clk6_shift[7:0]						
CLKCTRL7	BFh	W	goa_clk7_shift[7:0]						
CLKCTRL8	C0h	W	goa_clk8_shift[7:0]						
CLKCTRL9	C1h	W	clk_gnd1_period[7:0]						
CLKCTRL10	C2h	W	clk_gnd2_period[7:0]						
CLKCTRL11	C3h	W	lk_vci_period[7:0]						
CLKCTRL12	C4h	W	goa_clk_tchop[8]	goa_clk_tglue[8]	clk_noverlap[1:0]		goa_clk_width[3:0]		
CLKCTRL13	C5h	W	goa_clk_tchop[7:0]						
CLKCTRL14	C6h	W	goa_clk_tglue[7:0]						
CLKCTRL15	C7h	W					duty_block[3:0]		
CLKCTRL16	C8h	W	goa_clk1_switch[9:8]		goa_clk2_switch[9:8]		goa_clk3_switch[9:8]		goa_clk4_switch[9:8]
CLKCTRL17	C9h	W	goa_clk1_switch[7:0]						
CLKCTRL18	CAh	W	goa_clk2_switch[7:0]						
CLKCTRL19	CBh	W	goa_clk3_switch[7:0]						

CLKCTRL20	CCh	W	goa_clk4_switch[7:0]					
CLKCTRL21	CDh	W	goa_clk5_switch[9:8]		goa_clk6_switch[9:8]		goa_clk7_switch[9:8]	goa_clk8_switch[9:8]
CLKCTRL22	CEh	W	goa_clk5_switch[7:0]					
CLKCTRL23	CFh	W	goa_clk6_switch[7:0]					
CLKCTRL24	D0h	W	goa_clk7_switch[7:0]					
CLKCTRL25	D1h	W	goa_clk8_switch[7:0]					
RSTCTRL1	D2h	W	goa_rst_shift1[7:0]					
RSTCTRL2	D3h	Multi-W						goa_rst_shift2[9:8]
			goa_rst_shift2[7:0]					
RSTCTRL3	D4h	W	rst_gnd1_period[7:0]					
RSTCTRL4	D5h	W	rst_gnd2_period[7:0]					
RSTCTRL5	D6h	W	rst_vci_period[7:0]					
RSTCTRL6	D7h	W	goa_rst_tchop[8]	goa_rst_tglue[8]	rst_noverlap[1:0]		goa_rst_width[3:0]	
RSTCTRL7	D8h	W	goa_rst_tchop[7:0]					
RSTCTRL8	D9h	W	goa_rst_tglue[7:0]					
RDID1	DAh	R	sys_id1[7:0]					
RDID2	DBh	R	sys_id2[7:0]					
RDID3	DCh	R	sys_id3[7:0]					
WRID1	DDh	W	sys_id1[7:0]					
WRID2	DEh	W	sys_id2[7:0]					
WRID3	DFh	W	sys_id3[7:0]					
SOUCTRL1	E0h	W	ld_start[8]	ld_end[8]	srcpop_en_start[8]	srcpop_en_end[8]	srcnop_en_start[8]	srcnop_en_end[8]	fr_prec_start[8]	fr_prec_end[8]
SOUCTRL2	E1h	W	ld_start[7:0]					

SOUCTRL3	E2h	W	ld_end[7:0]							
SOUCTRL4	E3h	W	srcpop_en_start[7:0]							
SOUCTRL5	E4h	W	srcpop_en_end[7:0]							
SOUCTRL6	E5h	W	srcnop_en_start[7:0]							
SOUCTRL7	E6h	W	srcnop_en_end[7:0]							
SOUCTRL8	E7h	W	fr_prec_start[7:0]							
SOUCTRL9	E8h	W	fr_prec_end[7:0]							
SOUCTRL10	E9h	W	pol_ctrl	pol_init	ofc_ctrl	ofc_init	odd_even_ctrl	fr_sd_en_start[8]	fr_sd_en_end[8]	
SOUCTRL11	EAh	W	fr_sd_en_start[7:0]							
SOUCTRL12	EBh	W	fr_sd_en_end[7:0]							
SOUCTRL13	ECh	W	pol_switch[8]		be_prec_start[8]	be_prec_end[8]			be_sd_en_start[8]	be_sd_en_end[8]
SOUCTRL14	EDh	W	be_prec_start[7:0]							
SOUCTRL15	EEh	W	be_prec_end[7:0]							
SOUCTRL16	EFh	W	be_sd_en_start[7:0]							
SOUCTRL17	F0h	W	be_sd_en_end[7:0]							
SOUCTRL18	F1h	W	pol_switch[7:0]							
SOUCTRL19	F2h	W		pncs_en		goa_2143_en		rev	normal_black	pts
CPTEST1	F4h	W								cpe0
CPTEST2	F5h	W								cpe1
CPTEST3	F6h	W	cpdat[17:0]							
GVDDADJ	F7h	W				gvdd_otp[4:0]				
GVSPADJ	F8h	W							gvsp_otp[2:0]	
GVCLADJ	FAh	W				gvcl_otp[4:0]				

PADCTRL	FBh	W				osc_test_oe			ledpwm_oe	ledpwm
RDSTATE	FCh	R						cur_state[2:0]		
RD_PWR_STATUS	FDh	Multi-R		gam_en	regu_en	bgr_buf_en	vref_en	vdds_en	bias_en	gam_ref_en
							vgl_en	vgh_en	ddvdl_en	ddvdh_en

6.2. Description of Command 1

6.2.1. NOP (00h)

Command Set		NOP								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	No Parameter								00h
Description	This command is an empty command.									
Restriction	-									

6.2.2. Read display ID (04h)

Command Set		RD_SYSID								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-R	id1[7:0]								
2st Parameter		id2[7:0]								
3st Parameter		id3[7:0]								
Description	This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.									
Restriction	-									

6.2.3. Read display status (09h)

Command Set		RD_STATE								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-R	pump_en	sys_my	sys_mx	sys_mv	sys_ml	sys_bgr			/
2st Parameter			dbi[2:0]			color8_en	ptl_on	slpout	normal_on	/
3st Parameter		scroll_on		inv_on	gs	ss	disp_en	te_on		/
4st Parameter				telom						/
Description	pump_en: Booster Voltage Status. "0" = Booster Off; "1"=Booster On sys_my: Page Address Order. "0" = Top to Bottom (When memory data access control D7 = '0');									

	“1”= Bottom to Top (When memory data access control D7 = ‘1’) sys_mx: Column Address Order. “0” = Left to Right (When memory data access control D6 = ‘0’); “1”= Right to Left (When memory data access control D6 = ‘1’); sys_mv: Page/Column Order “0” = Normal Mode (When memory data access control D5 = ‘0’) “1”= Reverse Mode (When memory data access control D5 = ‘1’) sys_ml: Line Address Order “0” = LCD Refresh Top to Bottom (When memory data access control D4 = ‘0’) “1”= LCD Refresh Bottom to Top (When memory data access control D4 = ‘1’) sys_bgr: RGB/BGR Order “0” = RGB (When memory data access control D3 = ‘0’) “1”= BGR (When memory data access control D3 = ‘1’) dbi[2:0]: Interface color pixel format definition “011” = 12 Bit/Pixel(RGB 444) “101” = 16 Bit/Pixel(RGB 565) “110” = 18 Bit/Pixel(RGB 666) color8_en: Idle Mode On/Off “0” = Idle Mode Off “1”= Idle Mode On ptl_on: Partial Mode On/Off “0” = Partial Mode Off “1”= Partial Mode On Slpout: Sleep In/Out “0” = Sleep In Mode “1”= Sleep Out Mode normal_on: Display Normal ModeOn/Off “0” = Display Normal Mode Off “1”= Display Normal Mode On scroll_on: Vertical Scrolling Status “0” = Vertical Scrolling is Off “1”= Display Normal Mode On inv_on: Inversion Status “0” = Inversion is Off “1”= Inversion is On gs: Gate scan direction “0” = Gate scan direction is 0→239 “1”= Gate scan direction is 239→0 Ss: selects the shift direction of outputs of the source driver “0” = Source output S1→S360

	“1”= Source output S360→S1 disp_en: Display On/Off “0” = Display is Off “1”= Display is On te_on: Tearing Effect Line On/Off “0” = Tearing Effect Line Off “1”= Tearing Effect Line On Telom: Tearing Effect Output Line Mode “0” = Mode 1, V-Blanking only “1”= Mode 2, both H-Blanking and Vblanking
Restriction	-

6.2.4. Sleep In(10h)

Command Set		**SLPIN**								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	No Parameter								/
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. MCU interface and memory are still working and the memory keeps it’s contents.									
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120 msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.									
Register Availability										

Status	**Availability**
Normal Mode on,ldle Mode Off,Sleep Out	Yes
Normal Mode on,ldle Mode On,Sleep Out	Yes
Partial Mode on,ldle Mode Off,Sleep Out	Yes
Partial Mode on,ldle Mode On,Sleep Out	Yes
Sleep In	Yes

Default

Status	**Default Value(D7 to D0)**

	Power On Sequence: SLPIN SW Reset: SLPIN HW Reset: SLPIN

6.2.5. Sleep Out(11h)

Command Set		SLPOUT								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	No Parameter								/
Description	This command turns off sleep mode. In this mode e.g. the DC/DC converter is enabled. Intermal oscillator is started, and panel scanning is started.									
Restriction	This command has no effect when module is already in sleep out mode. Sleep Our Mode can only be left by the Sleep in Command (10h). It will be necessary to wait 5msec before sending next command; this is to allow time for the clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 120 msec and there cannot be any abnormal visual effect on the display image if faceory default and register values are same when this load is done and when the display module is already Sleep Out-mode. The display module is doing self-diagnostic function during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent. This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by HW Reset, Software Reset (01h), Sleep In (10h), or a NMI event trigger.									
Register Availability										

Status	Availability
Normal Mode on,ldle Mode Off,Sleep Out	Yes
Normal Mode on,ldle Mode On,Sleep Out	Yes
Partial Mode on,ldle Mode Off,Sleep Out	Yes
Partial Mode on,ldle Mode On,Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value(D7 to D0)
Power On Sequence	SLPOUT
SW Reset	SLPOUT
HW Reset	SLPOUT

6.2.6. Partial mode on (12h)

Command Set		PTLON								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	No Parameter								/
Description	This command turns on partial mode.The partial mode is described by the Partial Area command (30h). To leave Partial mode, the Normal Display On command (13h) should be written. X=Don't care Note: If a command is written in a frame cycle, the command becomes effective from the next frame.									
Restriction	This command has no effect during Partial mode is active.									
Register Availability										

Status	Availability
Normal Mode on,ldle Mode Off,Sleep Out	Yes
Normal Mode on,ldle Mode On,Sleep Out	Yes
Partial Mode on,ldle Mode Off,Sleep Out	Yes
Partial Mode on,ldle Mode On,Sleep Out	Yes
Sleep In	Yes

Default

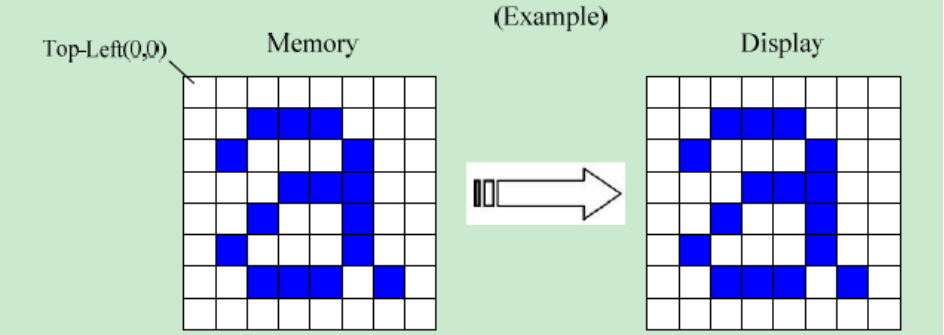
Status	Default Value(D7 to D0)
Power On Sequence	Normal Display On
SW Reset	Normal Display On
HW Reset	Normal Display On

6.2.7. Normal display mode on (13h)

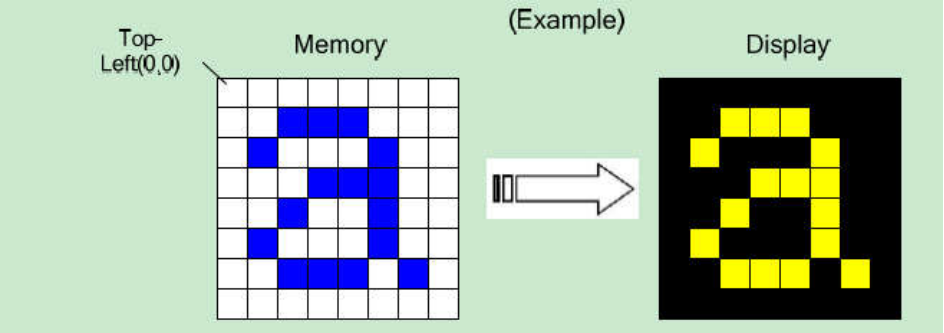
Command Set		NORMAL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	No Parameter								/
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. Exit from NORON by the Partial mode On command (12h) X = Don't care									

Restriction	

6.2.8. Display inversion off (20h)

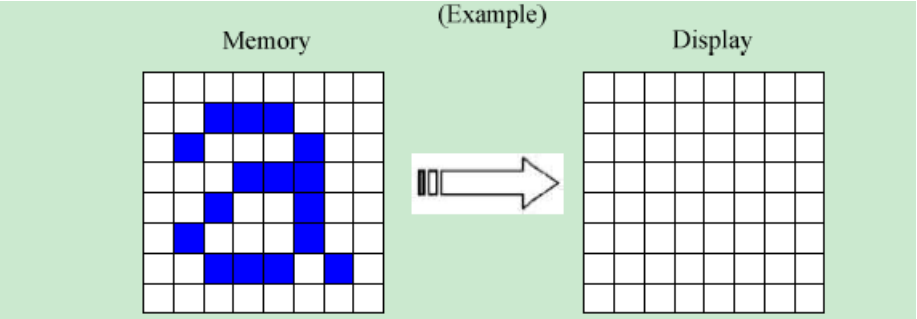
Command Set		INVOFF								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	No Parameter								/
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status. X = Don't care 									
Restriction	-									

6.2.9. Display inversion on(21h)

Command Set		INVON								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	No Parameter								/
Description	This command is used to enter into display inversion mode. This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display. This command doesn't change any other status. To exit Display inversion mode, the Display inversion OFF command (20h) should be written. X = Don't care 									

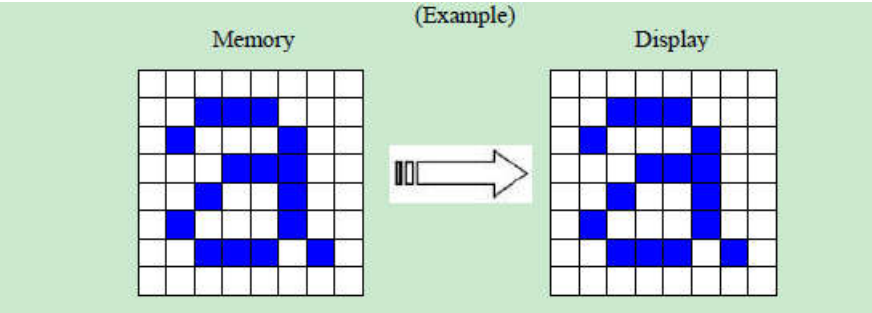
Restriction	-

6.2.10. Display off (28h)

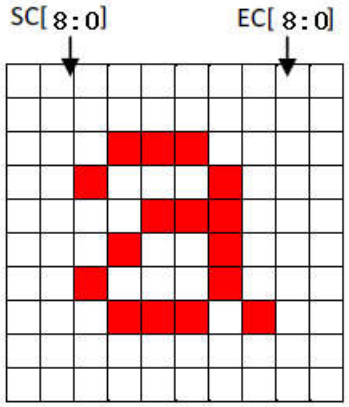
Command Set		DISPOFF								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	No Parameter								/
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. X = Don't care 									
Restriction	-									

6.2.11. Display on (29h)

Command Set		DISPON								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	No Parameter								/
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. X = Don't care									

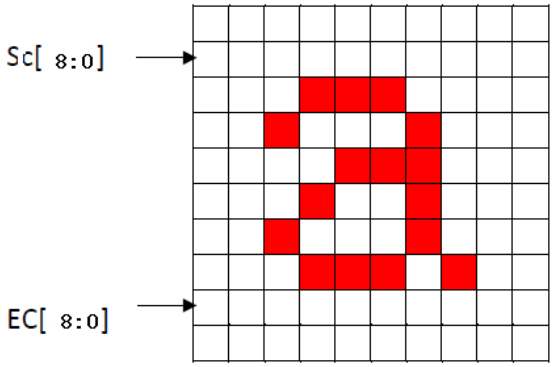
	
Restriction	-

6.2.12. Column address set (2Ah)

Command Set		COLSET								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-								sc[8]	00
2st Parameter	W	sc[7:0]								00
3st Parameter									ec[8]	00
4st Parameter		ec[7:0]								EF
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [8:0] and EC [8:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory. X = Don't care 									
Restriction	-									

6.2.13.Row address set (2Bh)

Command Set	ROWSET

Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
1st Parameter	Multi-W								sp[8]	00
2st Parameter		sp[7:0]								00
3st Parameter									ep[8]	00
4st Parameter		ep[7:0]								EF
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [8:0] and EP [8:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory. X = Don't care 									
Restriction	-									

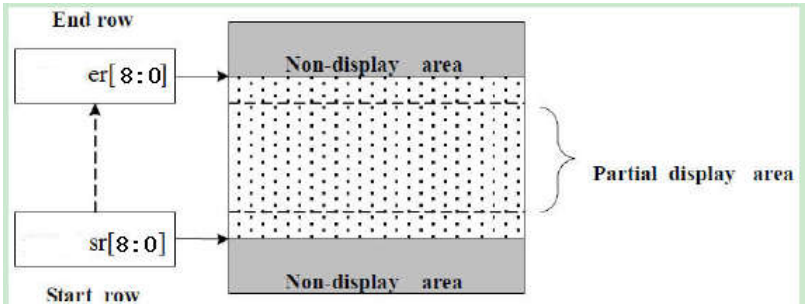
6.2.14. Memory write (2Ch)

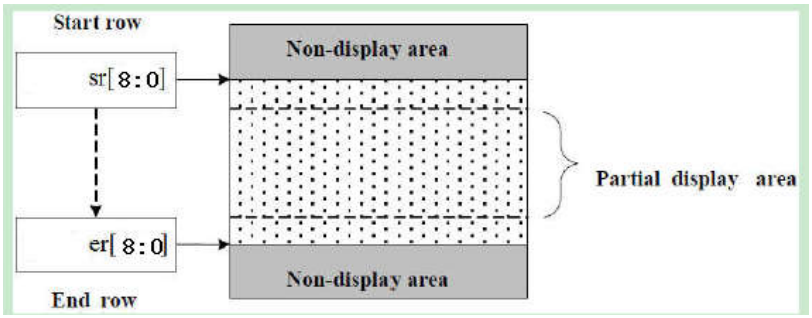
Command Set		MEMWR								
Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
1st Parameter	Write	No Parameter								
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] isstored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don't care.									
Restriction	-									

6.2.15. Memory read (2Eh)

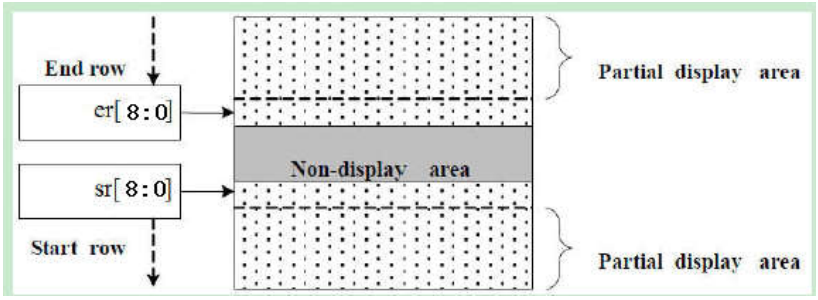
Command Set		MEMRD								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Read	No Parameter								
Description	This command is used to transfer data from frame memory to MPU. When this command is accepted, the column register and the page register are reset to the Start Column/Start page positions. The Start Column/Start page positions are different in accordance with MADCTL setting. Frame Read can be cancelled by sending any other command. The data color coding is fixed to 18-bit in reading function. Please see section 8.3.4.9 " Read Memory Data Color Coding" for color coding (18-bit cases), when there is used 8, 9, 16 and 18-bit data lines for image data.									
Restriction	-									

6.2.16. Partial area (30h)

Command Set		VSDEF								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W								sr[8]	00
2st Parameter		sr[7:0]								00
3st Parameter									er[8]	00
4st Parameter		er[7:0]								EF
Description	This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (sr[8:0]) and the second the End Row (er[8:0]), as illustrated in the figures below. sr[8:0] and er[8:0] refer to the Frame Memory row address counter. If End Row > Start Row, when MADCTL ml='1'.  If End Row > Start Row, when MADCTL ml='0'.									



If End Row < Start Row, when MADCTL ml='0'.



Restriction	-

6.2.17.Vertical scrolling definition (33h)

Command Set		PAREA								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W								tfa[8]	00
2st Parameter		tfa[7:0]								00
3st Parameter									vsa[8]	00
4st Parameter		vsa[7:0]								EF
5th Parameter									bfa[8]	00
6th Parameter		bfa[7:0]								00

Description

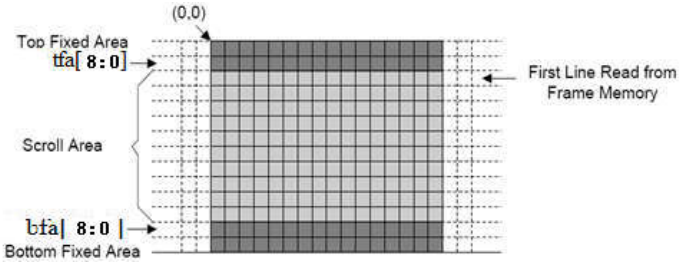
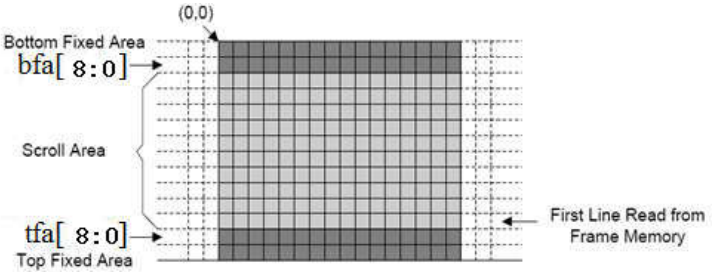
This command defines the Vertical Scrolling Area of the display.

When MADCTL ml = '0'

The 1st & 2nd parameter tfa[8:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter vsa[8:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter bfa[8:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). tfa[8:0], vsa[8:0] and bfa[8:0] refer to the

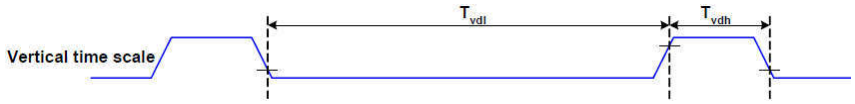
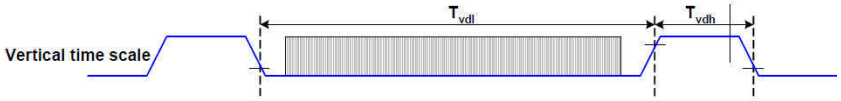
	Frame Memory Line Pointer.  **When MADCTL ml = '1'** The 1st & 2nd parameter tfa[8:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). The 3rd & 4th parameter vsa[8:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area. The 5th & 6th parameter bfa[8:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display). 
Restriction	

6.2.18. Te off (34h)

Command Set		TEOFF								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	No Parameter								/
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when tearing effect output is already off.									

6.2.19. Te on (35h)

Command Set	TEON

Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
1st Parameter	Write								telom	00
Description	This command is used to turn on the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ml. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. When telom =’0’: The Tearing Effect output line consists of V-Blanking information only:  When telom =’1’: The Tearing Effect output Line consists of both V-Blanking and HBlanking information:  Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.									
Restriction	This command has no effect when tearing effect output is already on.									

6.2.20. Memory access control (36h)

Command Set		MADCTRL								
Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
1st Parameter	Write	sys_my	sys_mx	sys_mv	sys_ml	sys_bgr				00
Description	This command defines read/write scanning direction of frame memory. <table><tr><th>Bit</th><th>Name</th><th>Description</th></tr><tr><td>D7</td><td>sys_my</td><td>Page Address Order</td></tr><tr><td>D6</td><td>sys_mx</td><td>Column Address Order</td></tr><tr><td>D5</td><td>sys_mv</td><td>Page/Column Order</td></tr><tr><td>D4</td><td>sys_ml</td><td>Line Address Order</td></tr><tr><td>D3</td><td>sys_bgr</td><td>RGB/BGR Order</td></tr></table>-Bit Assignment Bit D7- Page Address Order “0” = Top to Bottom (When MADCTL D7=”0”). “1” = Bottom to Top (When MADCTL D7=”1”). Bit D6- Column Address Order “0” = Left to Right (When MADCTL D6=”0”).									

“1” = Right to Left (When MADCTL D6=”1”).

Bit D5- Page/Column Order

“0” = Normal Mode (When MADCTL D5=”0”).

“1” = Reverse Mode (When MADCTL D5=”1”)

Bit D4- Line Address Order

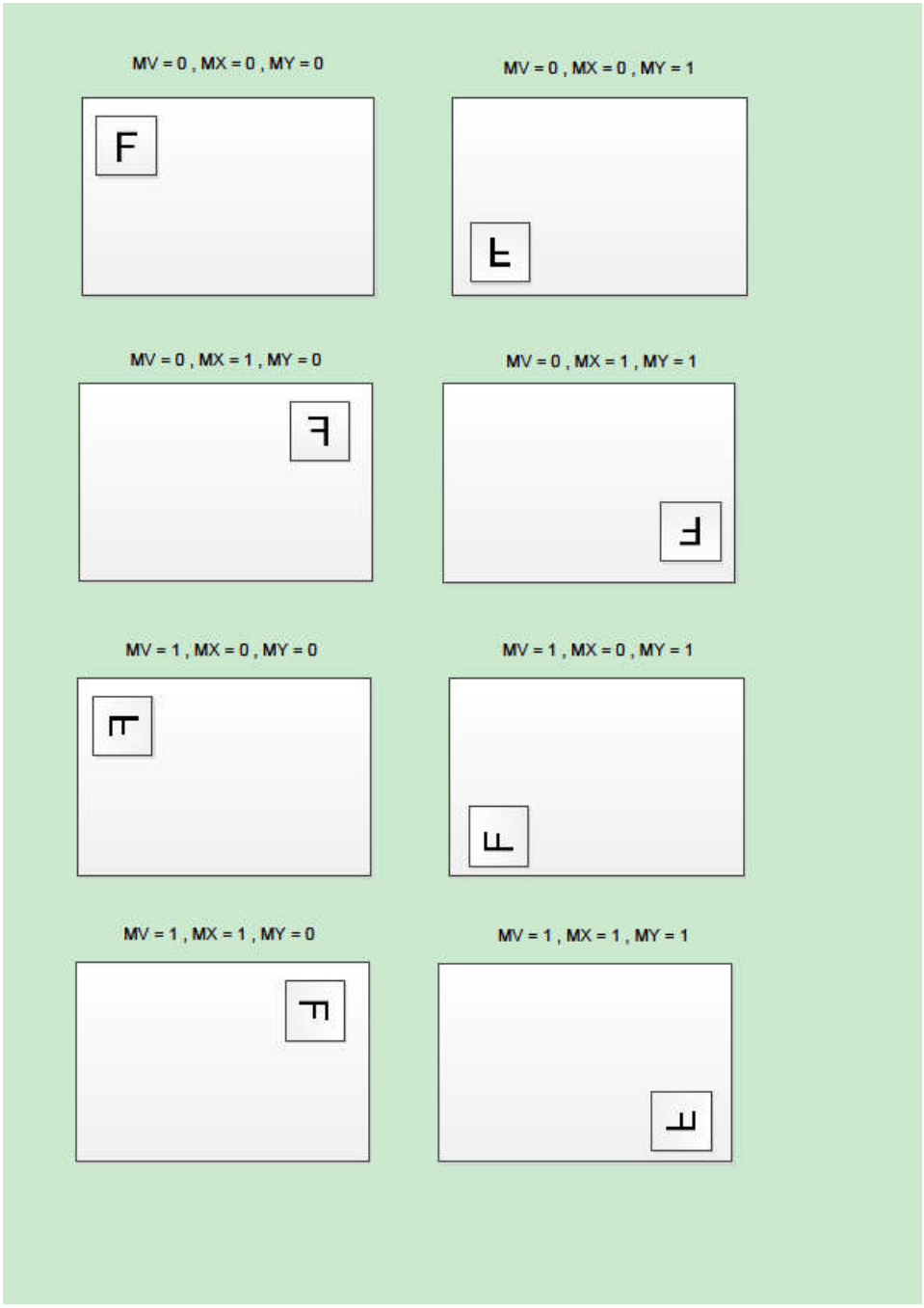
“0” = LCD Refresh Top to Bottom (When MADCTL D4=”0”)

“1” = LCD Refresh Bottom to Top (When MADCTL D4=”1”)

Bit D3- RGB/BGR Order

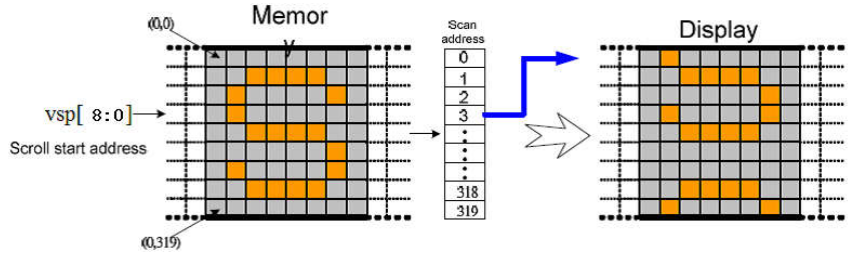
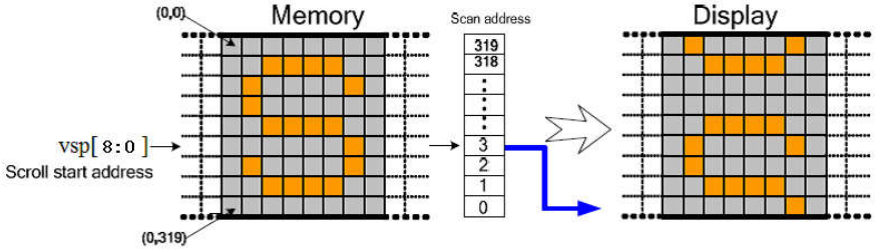
“0” = RGB (When MADCTL D3=”0”)

“1” = BGR (When MADCTL D3=”1”)



Restriction	-

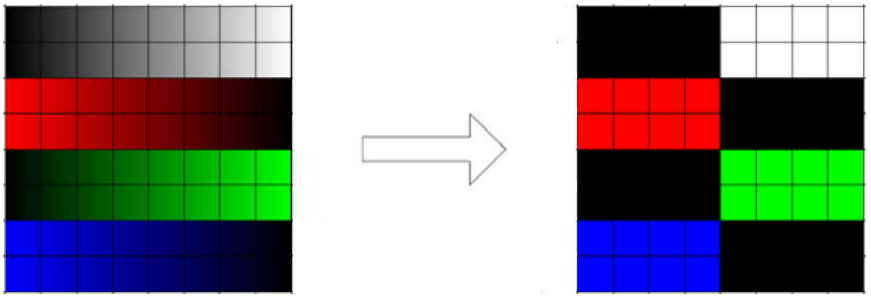
6.2.21. Vertical scrolling strat address (37h)

Command Set		VSSAD								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W								vsp[8]	00
2nd Parameter		vsp[7:0]								00
Description	This command is used together with Vertical scrolling (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical scrolling start address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below: When ml='0' Example: When Top Fixed Area = Bottom Fixed Area = 00, vertical scrolling area = 320 and vsp = '3'.  When ml='1' Example: When Top Fixed Area = Bottom Fixed Area = 00, vertical scrolling area = 320 and vsp = '3'.  Note: When new pointer position and picture data are sent, the result on the display will happen at the next panel scan to avoid tearing effect. Vsp refers to the Frame Memory line pointer.									
Restriction	Since the value of the vertical scrolling start address is absolute (with reference to the frame memory), it must not enter the fixed area (defined by vertical scrolling (33h)- otherwise undesirable image will be displayed on the panel).									

6.2.22. Idle mode off (38h)

Command Set		IDLEOFF								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	No parameter								/
Description	This command is used to recover from idle mode on. In the idle off mode 1. LCD can display 65k or 262k colors. 2. Normal frame frequency is applied.									
Restriction	This command has no effect when module is already in idle off mode.									

6.2.23. Idle mode on (39h)

Command Set		IDLEON								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	No parameter								/
Description	This command is used to enter into idle mode on. There will be no abnormal visible effect on the display mode change transition. In the idle on mode, 1. Color expression is reduced. The colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed. 2. 8-Color mode frame frequency is applied. 3. Exit from idle mode on by idle mode off (38h) command. Memory Pannel Display 									
Restriction	This command has no effect when module is already in idle on mode.									

6.2.24. Pixel format set (3Ah)

Command Set		PFSET								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**

<table>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td></td><td></td><td colspan="2">dbi[2:0]</td><td>06</td></tr>
<tr><td>Description</td><td colspan="9">dbi[2:0] is the pixel format of system interface.
<table><tr><th>dbi[2]</th><th>dbi[1]</th><th>dbi[0]</th><th>system interface format</th></tr><tr><td>0</td><td>0</td><td>0</td><td>reserved</td></tr><tr><td>0</td><td>0</td><td>1</td><td>reserved</td></tr><tr><td>0</td><td>1</td><td>0</td><td>reserved</td></tr><tr><td>0</td><td>1</td><td>1</td><td>12 bits/pixel</td></tr><tr><td>1</td><td>0</td><td>0</td><td>reserved</td></tr><tr><td>1</td><td>0</td><td>1</td><td>16 bits/pixel</td></tr><tr><td>1</td><td>1</td><td>0</td><td>18 bits/pixel</td></tr><tr><td>1</td><td>1</td><td>1</td><td>reserved</td></tr></table>“X”= Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="9">-</td></tr>
</table>

6.2.25. Write memory continue (3Ch)

<table>
<tr><th colspan="2">Command Set</th><th colspan="8">WRMEMC</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">No parameter</td><td>/</td></tr>
<tr><td>Description</td><td colspan="10">This command transfers image data from the host processor to the display module’s frame memory continuing from the pixel location following the previous write memory continue or memory write command.
If mv= ‘0’:
Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (caset_ec) value. The column register is then reset to caset_sc and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (paset_ep) value and the column register equals the caset_ec value, or the host processor sends another command. If the number of pixels exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1) the extra pixels are ignored.
If mv= ‘1’:
Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the end page (paset_ep) value. The page register is then reset to paset_sp and the column register is incremented. Pixels are written to the frame memory until the column register equals the end column (caset_ec) value and the page register equals the paset_ep value, or the host processor sends another command. If the number of pixels exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1) the extra pixels are ignored.</td></tr>
<tr><td>Restriction</td><td colspan="10">A memory write should follow a column address set or page address set to define the write</td></tr>
</table>

	address. Otherwise, data written with write memory continue is written to undefined addresses.

6.3. Description of Command 2

6.3.1. Interface control 1(40h)

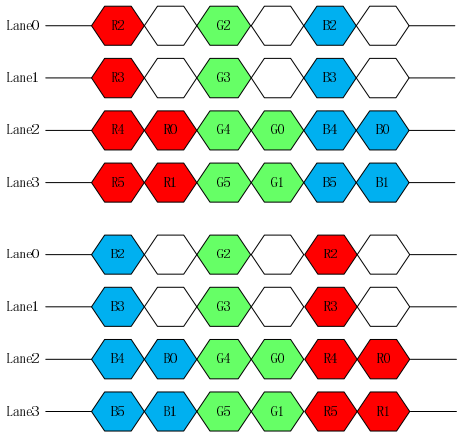
Command Set		IFCTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
40h	Write				sdo_hiz					00
Description	sdo_hiz : SDO enable signal. 1:enable 0:disable									
Restriction	-									

6.3.2. Interface control 2(41h)

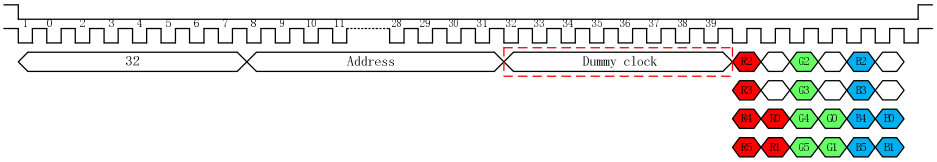
Command Set		IFCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
41h	Write								spi_2dat_en	00
Description	spi_2dat_en : spi 2-data line mode enable signal. 1:enable 0:disable									
Restriction	-									

6.3.3. Interface control 3(42h)

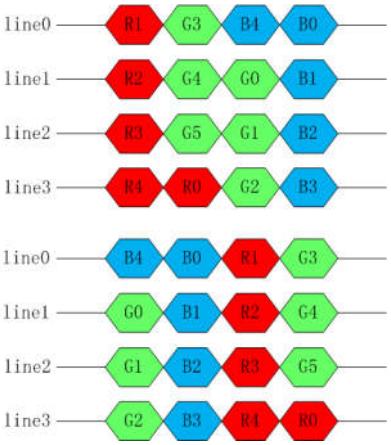
Command Set		IFCTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
42h	Write				qspi_bgr			qspi_dummy	qspi_sbyte	00
Description	When interface is Qspi: qspi_bgr : when op code = 8'h12 or 8'h32, and dbi(3AH) = 3'b110, this signal can change the order in which the sub-pixels are received.									



qspi_dummy : When op code = 8'h32, this signal determines whether there are 8 dummy clocks.



qspi_sbyte : When op code = 8'h12 or 8'h32, and dbi(3AH) = 3'b101, this signal can change the order of the received bytes.



Restriction	-

6.3.4. Interface control 4(43h)

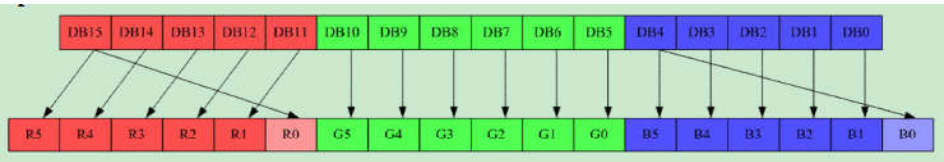
Command Set		IFCTRL4								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
43h	Write			we_mod	endian	epf[1:0]		mdt[1:0]		24
Description	we_mod : memory write control. we_mode = 0 : when the transfer number of data exceeds (ec-sc+1)*(sp+1), the exceeding data will be ignored.									

we_mode=1 : when the transfer number of data exceeds (ec-sc+1)*(sp+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

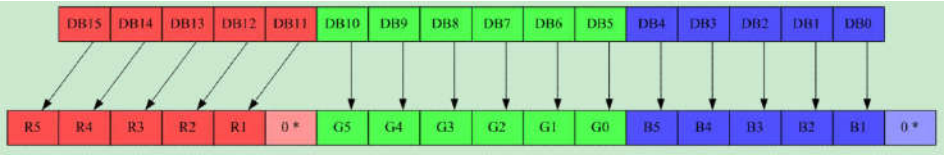
endian : When interface is MCU 8bit, and dbi(3AH) = 3'b101, this signal can change the order of the received bytes.

epf :

epf = 00



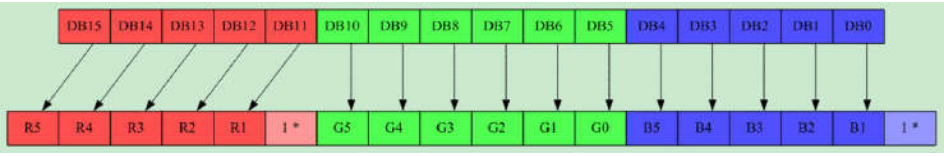
epf = 01



Note: Exception

1. R0 = 1 when R5~R1 = 1111
2. B0 = 1 when B4~B1 = 1111

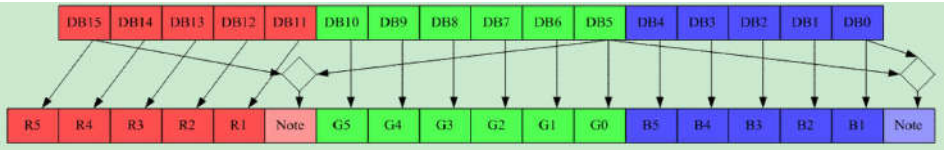
epf = 10



Note: Exception

1. R0 = 0 when R5~R1 = 0000
2. B0 = 0 when B4~B1 = 0000

epf = 11



Note:

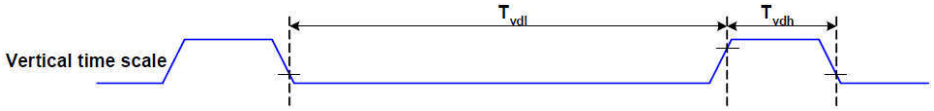
1. If DB15~DB11 = DB10~DB6, R0 = DB5, else R0 = DB15
2. If DB4~DB0 = DB10~DB16, B0 = DB5, else B0 = DB0

mdt : When interface is MCU 16bit, and dbi(3AH) = 3'b110, this signal select the method of display data transferring.

Restriction	-

6.3.5. Set tear scanline (44h)

Command Set		TECTRL1								
Command	**Write/**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**

	Read									
1st Parameter	Multi-W								sts[8]	00
2nd Parameter		sts[7:0]								00
Description	This command turns on the display module's tearing effect output signal on the TE signal line when the display module reaches line sts. The TE signal is not affected by changing mv. The tearing effect line on has one parameter that describes the tearing effect output line mode. The tearing effect output line consist of V-blanking information only.  Note: That set tear scanline with sts = '0' is equivalent to tearing effect line on with tear_mode= '0'. The tearing effect output line shall be low when the display module is in sleep mode.									
Restriction	-									

6.3.6.Get tear scanline (45h)

Command Set		TECTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-R								sts[8]	00
2nd Parameter		sts[7:0]								00
Description	The display module returns the current scanline gts, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.When in sleep in mode, the value returned by get scanline is undefined.									
Restriction	-									

6.3.7. Tearing effect control 1(46h)

Command Set		TECTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write							te_pol	te_extend	00
Description	te_pol : This signal can change TE polarity. te_extend : This signal enables the TE signal extension mode, which supports configuring the TE									

	waveform with register values.
Restriction	-

6.3.8. Tearing effect control 2(47h)

Command Set		TECTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W			te_v_start[5:0]						00
2nd Parameter			te_v_end[6:0]							00
Description	When the TE extension mode is turned on: te_v_start[5:0] : Specifies on which line of a frame the TE signal begins te_v_end[6:0] : Specify which line of a frame the te is closed.									
Restriction	-									

6.3.9. Tearing effect control 3(48h)

Command Set		TECTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W			te_h_start[5:0]						00
2nd Parameter			te_h_end[6:0]							00
Description	When the TE extension mode is turned on, and telom =1'b1: te_h_start[5:0] : Specifies which column of a row the TE signal begins. te_h_end[6:0] : Specifies from which column of a row the TE signal is closed.									
Restriction	-									

6.3.10. Scan direction control (49h)

Command Set		SCANCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write						gs		ss	01
Description	gs: Gate scan direction.gs="0": Gate scan direction is 0→479;gs="1": Gate scan direction is 479→0. ss: selects the shift direction of outputs of the source driver. 0: Source output S1→S360; 1: Source output S360→S1.									
Restriction	-									

6.3.11.OTP control 1(4Ah)

Command Set		OTPCTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
4Ah	Write		otp_ptm[1:0]		otp_pwe	otp_prd	otp_pprog	otp_vpp_sel	otp_vpp_src_sel	00
Description	otp_ptm[1:0] : test mode enable signal. otp_pwe : define program cycle. otp_prd : define read cycle. otp_pprog : program mode enable signal. otp_vpp_sel : select the work voltage (8V~8.5V during program cycle and 1.35V~1.65V in read cycle). otp_vpp_src_sel : The program voltage Source is provided by external or by the chip. 1: Program voltage Generate From Chip. 0 : Program voltage Generate From Outside.									
Restriction	-									

6.3.12.OTP control 2(4Bh)

Command Set		OTPCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
4Bh	Write	otp_pa[7:0]								00
Description	otp_pa[7:0] : Set the OTP program address.									
Restriction	-									

6.3.13.OTP control 3(4Ch)

Command Set		OTPCTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
4Ch	Write	otp_pdin[7:0]								00
Description	otp_pdin[7:0] : Specify OTP program data.									
Restriction	-									

6.3.14. OTP control 4(4Dh)

Command Set		OTPCTRL4								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	read	otp_rd_dat[7:0]								00
Description	otp_rd_dat[7:0] : Read OTP output data.									
Restriction	-									

6.3.15. Memory access control (4Fh)

Command Set		USRMAD								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	usr_my	usr_mx	usr_mv	usr_ml	usr_bgr				00

Description

This command defines read/write scanning direction of frame memory.

Bit	Name	Description
D7	usr_my	Page Address Order
D6	usr_mx	Column Address Order
D5	usr_mv	Page/Column Order
D4	usr_ml	Line Address Order
D3	usr_bgr	RGB/BGR Order

-Bit Assignment

Bit D7- Page Address Order

"0" = Top to Bottom (When MADCTL D7="0").

"1" = Bottom to Top (When MADCTL D7="1").

Bit D6- Column Address Order

"0" = Left to Right (When MADCTL D6="0").

"1" = Right to Left (When MADCTL D6="1").

Bit D5- Page/Column Order

"0" = Normal Mode (When MADCTL D5="0").

"1" = Reverse Mode (When MADCTL D5="1")

Bit D4- Line Address Order

"0" = LCD Refresh Top to Bottom (When MADCTL D4="0")

"1" = LCD Refresh Bottom to Top (When MADCTL D4="1")

Bit D3- RGB/BGR Order

"0" = RGB (When MADCTL D3="0")

	“1” = BGR (When MADCTL D3=”1”) The function is the same as 36H.
Restriction	-

6.3.16. Resolution select 1(50h)

Command Set		RESCTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
50h	Write						res_h_sel[2:0]			05
Description	res_h_sel[2:0] : Source channel selection. res_h_sel[2:0] | source channel 3'b000 | 80RGB 3'b001 | 120RGB 3'b010 | 128RGB 3'b011 | 144RGB 3'b100 | 160RGB 3'b101 | 240RGB									
Restriction	-									

6.3.17. Resolution select 2(51h)

Command Set		RESCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
51h	Write	res_v_start[7:0]								00
Description	res_v_start[7:0] : Specifies which line to start the display.									
Restriction	-									

6.3.18. Resolution select 3(52h)

Command Set		RESCTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
52h	Write	res_v_num[7:0]								78
Description	res_v_num[7:0] : Specifies the width of the display row.									
Restriction	-									

6.3.19. Internal timing control 1(53h)

Command Set		ITCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
53h	Write	inter_vbp[7:0]								04
Description	inter_vbp[7:0] : set internal vertical back-porch width.									
Restriction	-									

6.3.20. Internal timing control 2(54h)

Command Set		ITCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
54h	Write	fr_div	inter_vfp[6:0]							84
Description	fr_div : OSC frequency division multiplier selection. inter_vfp[7:0] : set internal vertical front-porch width.									
Restriction	-									

6.3.21. Internal timing control 3(55h)

Command Set		ITCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
55h	Write	inter_hbp[7:0]								19
Description	inter_hbp[7:0] : set internal horizontal back-porch width.									
Restriction	-									

6.3.22. Internal timing control 4(56h)

Command Set		ITCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
56h	Write	inter_hfp[7:0]								19
Description	inter_hfp[7:0] : set internal horizontal front-porch width.									
Restriction	-									

6.3.23. Ibias control (57h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="8">IBIASCTRL</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">bias_adj[2:0]</td><td>03</td></tr>
<tr><td>Description</td><td colspan="10">Bias_adj[2:0]: Bias for analog blocks
<table>
<tr><th>Bias_adj[2:0]</th><th>Ib(Unit: uA)</th><th>Bias_adj[2:0]</th><th>Ib(Unit: uA)</th></tr>
<tr><td>000</td><td>0.25</td><td>100</td><td>1.25</td></tr>
<tr><td>001</td><td>0.50</td><td>101</td><td>1.50</td></tr>
<tr><td>010</td><td>0.75</td><td>110</td><td>1.75</td></tr>
<tr><td>011</td><td>1.0</td><td>111</td><td>2.0</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

6.3.24. OSC control (58h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="8">OSCCTRL</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td>D2A_OSC _EN</td><td></td><td></td><td></td><td colspan="3">D2A_OSC_TRIM<3:0></td><td>08</td></tr>
<tr><td>Description</td><td colspan="10">D2A_OSC _EN: OSC enable signal.
<table>
<tr><th>D2A_OSC _EN</th><th>Description</th></tr>
<tr><td>0</td><td>Disable OSC</td></tr>
<tr><td>1</td><td>Enable OSC</td></tr>
</table>
D2A_OSC_TRIM<3:0>: OSC level adjustment
<table>
<tr><th>D2A_OSC_TRIM<3：0></th><th>Freq(Hz)</th><th>D2A_OSC_TRIM<3：0></th><th>Freq(Hz)</th></tr>
<tr><td>0000</td><td>1.18E+07</td><td>1000</td><td>1.10E+07</td></tr>
<tr><td>0001</td><td>1.25E+07</td><td>1001</td><td>1.06E+07</td></tr>
<tr><td>0010</td><td>1.31E+07</td><td>1010</td><td>1.02E+07</td></tr>
<tr><td>0011</td><td>1.40E+07</td><td>1011</td><td>9.95E+06</td></tr>
<tr><td>0100</td><td>1.49E+07</td><td>1100</td><td>1.04E+07</td></tr>
<tr><td>0101</td><td>1.64E+07</td><td>1101</td><td>9.55E+06</td></tr>
<tr><td>0110</td><td>1.70E+07</td><td>1110</td><td>9.10E+06</td></tr>
<tr><td>0111</td><td>1.78E+07</td><td>1111</td><td>8.64E+06</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

6.3.25. LVD control (59h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">LVDCTRL</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td></td><td></td><td></td><td>D2A_LVD_EN</td><td></td><td></td><td colspan="2">Lvd_sel<1:0></td><td>01</td></tr>
<tr><td>Description</td><td colspan="10">D2A_LVD_EN: LVD enable signal.
<table><tr><th>D2A_LVD_EN</th><th>Description</th></tr><tr><td>0</td><td>Disable LVD</td></tr><tr><td>1</td><td>Enable LVD</td></tr></table>Lvd_sel<1:0>: LVD threshold trimming selection signal
<table><tr><th>Lvd_sel<1:0></th><th>阈值电压</th></tr><tr><td>00</td><td>2.0</td></tr><tr><td>01</td><td>2.1</td></tr><tr><td>10</td><td>2.2</td></tr><tr><td>11</td><td>2.3</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

6.3.26. ALGCTRL1 (5Ah)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">ALGCTRL1</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td>Write</td><td>merge_disable</td><td colspan="8">merge_times_porch_h[6:0]</td><td>12</td></tr>
<tr><td>Description</td><td colspan="10">merge_disable : Close the window merge algorithm.
merge_times_porch_h[6:0] : Specify the number of Windows merged during H_Porch.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

6.3.27. ALGCTRL2 (5Bh)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">ALGCTRL2</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td rowspan="2">Multi-W</td><td colspan="9">algo_pattern_en[15:8]</td><td>FF</td></tr>
<tr><td>2nd Parameter</td><td colspan="9">algo_pattern_en[7:0]</td><td>FF</td></tr>
<tr><td>Description</td><td colspan="10">algo_pattern_en[15:0] : Enable signal of special pattern of algorithm.</td></tr>
</table>

Restriction	-

6.3.28. RAMCTRL 1(5Ch)

Command Set		RAMCTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
5Ch	Write							mec_restart	mbist_en	01
Description	mec_restart : When the memory bist is finished, turn the bist function back on at any time. mbist_en : Memory bist enable signal.									
Restriction	-									

6.3.29. RAMCTRL 2(5Dh)

Command Set		RAMCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
5Dh	Write		pchsel_l	wlsel_l	scsel_l		pchsel_r	wlsel_r	scsel_r	00
Description	pchsel_l/ pchsel_r: select the delay time to precharge the data line. wlsel_l/ : wlsel_r : select the delay time on word line. scsel_l/ scsel_r: select the delay time about read operation.									
Restriction	-									

6.3.30. RDBIST (5Eh)

Command Set		RDBIST								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-R	mec_restart	mbist_en	mbist_done	mbist_abort	l_mec_pxl1_hit	l_mec_pxl2_hit	r_mec_pxl1_hit	r_mec_pxl2_hit	/
2nd Parameter						l_mec_pxl1_row[8]	l_mec_pxl2_row[8]	r_mec_pxl1_row[8]	r_mec_pxl2_row[8]	/
3rd Parameter		l_mec_pxl1_row[7:0]								/

4th Parameter		l_mec_pxl1_col[7:0]	/
5 th Parameter		l_mec_pxl2_row[7:0]	/
6 th Parameter		l_mec_pxl2_col[7:0]	/
7 th Parameter		r_mec_pxl1_row[7:0]	/
8 th Parameter		r_mec_pxl1_col[7:0]	/
9 th Parameter		r_mec_pxl2_row[7:0]	/
10th Parameter		r_mec_pxl2_col[7:0]	/
Description	This read address returns memory bist result information : mec_restart : When the memory bist is finished, turn the bist function back on at any time. mbist_en : Memory bist enable signal. mbist_done : Memory bist finished flag. mbist_abort : A signal indicating that RAM has three or more bad spots. l_mec_pxl1_hit : The signal indicating the first bad point on the left side of RAM. l_mec_pxl2_hit : A signal indicating the second bad point on the left side of RAM. r_mec_pxl1_hit : A signal indicating the first bad spot on the right side of RAM. r_mec_pxl2_hit : A signal indicating the second bad spot on the right side of RAM. l_mec_pxl1_row[8:0] : The row where the first bad spot is on the left side of RAM. l_mec_pxl1_col[7:0] : The column where the first bad spot is on the left side of RAM. l_mec_pxl2_row[8:0] : The row where the second bad spot is on the left side of RAM. l_mec_pxl2_col[7:0] : The column where the second bad spot is on the left side of RAM. r_mec_pxl1_row[8:0] : The row where the first bad spot is on the right side of RAM. r_mec_pxl1_col[7:0] : The column where the first bad spot is on the right side of RAM. r_mec_pxl2_row[8:0] : The row where the second bad spot is on the right side of RAM. r_mec_pxl2_col[7:0] : The column where the second bad spot is on the right side of RAM.		
Restriction	-		

6.3.31. Linebuffer control (5Fh)

Command Set		LBCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write		lb1_pchsel	lb1_wlsel	lb1_scsel		lb2_pchsel	lb2_wlsel	lb2_scsel	00
Description	lb1_pchsel/ lb2_pchsel: select the delay time to precharge the data line. lb1_wlsel / lb2_wlsel: select the delay time on word line. lb1_scsel / lb2_scsel: select the delay time about read operation.									
Restriction	-									

6.4. Description of Command 3

6.4.1. Gamma control (60~7Fh)

Command Set		GAMCTRL								
Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
60h	Write					vrp0[3:0]				00h
61h	Write			vrp1[5:0]						03h
62h	Write			Vrp2[5:0]						07h
63h	Write				vrp4[4:0]					09h
64h	Write				vrp6[4:0]					09h
65h	Write					vrp13[3:0]				07h
66h	Write		vrp20[6:0]							2Ah
67h	Write		vrp27[2:0]				vrp36[2:0]			34h
68h	Write		vrp43[6:0]							45h
69h	Write					vrp50[3:0]				09h
6Ah	Write				vrp57[4:0]					11h
6Bh	Write				vrp59[4:0]					12h
6Ch	Write			vrp61[5:0]						3Ch
6Dh	Write			vrp62[5:0]						3Dh
6Eh	Write					vrp63[3:0]				0Dh
6Fh	Write			vj0p63[1:0]				vj1p63[1:0]		10h
70h	Write					vrn0[3:0]				00h
71h	Write			vrn1[5:0]						03h
72h	Write			vrn2[5:0]						07h
73h	Write				vrn4[4:0]					09h
74h	Write				vrn6[4:0]					09h
75h	Write					vrn13[3:0]				07h
76h	Write		vrn20[6:0]							2Ah
77h	Write		vrn27[2:0]				vrn36[2:0]			34h

78h	Write		vrn43[6:0]							45h
79h	Write					vrn50[3:0]				09h
7Ah	Write				vrn57[4:0]					11h
7Bh	Write				vrn59[4:0]					12h
7Ch	Write			vrn61[5:0]						3Ch
7Dh	Write			vrn62[5:0]						3Dh
7Eh	Write					vrn63[3:0]				0Dh
7Fh	Write			vj0n63[1:0]				vj1n63[1:0]		10h
Description	Gamma register trimming									
Restriction	-									

6.4.2. Regulator control (80~81h)

Command Set		RGLRCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
80h	Write				test_en		dvdd_adj[2:0]			00h
81h	Write	bgr_adj[3:0]				vref_adj[3:0]				00h

Description

Test_en: test enable signal

1: bgr, gvdd,gvcl,gvsp output to pad, these signal could be tested in pad.

0: test disable

dvdd_adj[2:0]: dvdd trimming signal

dvdd_adj[2:0]	DVDD (unit:V)	dvdd_adj[2:0]	DVDD (unit:V)
000	1.55	100	1.60
001	1.50	101	1.65
010	1.45	110	1.70
011	1.40	111	1.76

Restriction

bgr_adj[3:0]: bandgap trimming

bgr_adj[2:0]	VBG (unit:V)	bgr_adj[2:0]	VBG (unit:V)
0000	1.316	1000	1.325
0001	1.307	1001	1.334
0010	1.298	1010	1.343
0011	1.289	1011	1.352
0100	1.279	1100	1.361

	0101	1.270	1101	1.370
	0110	1.252	1110	1.388
	0111	1.234	1111	1.406

vref_adj[3:0]: vref trimming

vref_adj[2:0]	VREF (unit:V)	vref_adj[2:0]	VREF (unit:V)
0000	2.0	1000	2.03
0001	1.98	1001	2.05
0010	1.96	1010	2.07
0011	1.94	1011	2.09
0100	1.92	1100	2.11
0101	1.90	1101	2.13
0110	1.88	1110	2.15
0111	1.82	1111	2.19

6.4.3. VDDS control (82h)

Command Set		**RGLRCTRL**								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
82h	Write						vdds_trim[2:0]			00h
Description	Vdds_trim[2:0]: vdds trimming signal									

vdds_adj[2:0]	VDDS(unit:V)	vdds_adj[2:0]	VDDS (unit:V)
000	1.824	100	1.980
001	1.691	101	2.166
010	1.576	110	2.389
011	1.475	111	2.629

Restriction	

6.4.4. Gamma ldo control (83h)

Command Set		**GLDOCTRL1**								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
83h	Write	gvcl_adj[7:0]								9F
Description	GVCL LDO output voltage level adjustment:									

gvcl_adj[7:0]	GVCL	gvcl_adj[7:0]	GVCL	gvcl_adj[7:0]	GVCL	gvcl_adj[7:0]	GVCL
00000000	-4.94	01000000	-4.141	10000000	-3.341	11000000	-2.542
00000001	-4.929	01000001	-4.13	10000001	-3.33	11000001	-2.531

00000010	-4.917	01000010	-4.118	10000010	-3.318	11000010	-2.519
00000011	-4.906	01000011	-4.107	10000011	-3.307	11000011	-2.509
00000100	-4.89	01000100	-4.091	10000100	-3.291	11000100	-2.492
00000101	-4.879	01000101	-4.08	10000101	-3.28	11000101	-2.481
00000110	-4.867	01000110	-4.068	10000110	-3.268	11000110	-2.469
00000111	-4.856	01000111	-4.057	10000111	-3.257	11000111	-2.459
00001000	-4.842	01001000	-4.043	10001000	-3.243	11001000	-2.444
00001001	-4.831	01001001	-4.032	10001001	-3.232	11001001	-2.434
00001010	-4.819	01001010	-4.02	10001010	-3.22	11001010	-2.421
00001011	-4.808	01001011	-4.009	10001011	-3.209	11001011	-2.411
00001100	-4.789	01001100	-3.991	10001100	-3.19	11001100	-2.392
00001101	-4.779	01001101	-3.98	10001101	-3.18	11001101	-2.381
00001110	-4.766	01001110	-3.968	10001110	-3.167	11001110	-2.369
00001111	-4.756	01001111	-3.957	10001111	-3.157	11001111	-2.359
00010000	-4.741	01010000	-3.943	10010000	-3.142	11010000	-2.344
00010001	-4.731	01010001	-3.932	10010001	-3.132	11010001	-2.334
00010010	-4.719	01010010	-3.92	10010010	-3.12	11010010	-2.321
00010011	-4.708	01010011	-3.909	10010011	-3.109	11010011	-2.311
00010100	-4.691	01010100	-3.893	10010100	-3.093	11010100	-2.294
00010101	-4.681	01010101	-3.882	10010101	-3.082	11010101	-2.284
00010110	-4.669	01010110	-3.87	10010110	-3.07	11010110	-2.271
00010111	-4.658	01010111	-3.859	10010111	-3.059	11010111	-2.261
00011000	-4.644	01011000	-3.845	10011000	-3.045	11011000	-2.247
00011001	-4.633	01011001	-3.835	10011001	-3.034	11011001	-2.236
00011010	-4.621	01011010	-3.822	10011010	-3.022	11011010	-2.224
00011011	-4.61	01011011	-3.812	10011011	-3.011	11011011	-2.213
00011100	-4.589	01011100	-3.791	10011100	-2.99	11011100	-2.192
00011101	-4.578	01011101	-3.78	10011101	-2.98	11011101	-2.182
00011110	-4.566	01011110	-3.768	10011110	-2.967	11011110	-2.169
00011111	-4.555	01011111	-3.757	10011111	-2.957	11011111	-2.159
00100000	-4.541	01100000	-3.743	10100000	-2.942	11100000	-2.144
00100001	-4.531	01100001	-3.732	10100001	-2.932	11100001	-2.134
00100010	-4.518	01100010	-3.72	10100010	-2.919	11100010	-2.121
00100011	-4.508	01100011	-3.709	10100011	-2.909	11100011	-2.111
00100100	-4.491	01100100	-3.693	10100100	-2.892	11100100	-2.094
00100101	-4.481	01100101	-3.682	10100101	-2.882	11100101	-2.084
00100110	-4.468	01100110	-3.67	10100110	-2.869	11100110	-2.072
00100111	-4.458	01100111	-3.659	10100111	-2.859	11100111	-2.061
00101000	-4.443	01101000	-3.645	10101000	-2.844	11101000	-2.047
00101001	-4.433	01101001	-3.634	10101001	-2.834	11101001	-2.036
00101010	-4.42	01101010	-3.622	10101010	-2.822	11101010	-2.024
00101011	-4.41	01101011	-3.612	10101011	-2.811	11101011	-2.013

00101100	-4.391	01101100	-3.593	10101100	-2.792	11101100	-1.995
00101101	-4.381	01101101	-3.582	10101101	-2.782	11101101	-1.984
00101110	-4.368	01101110	-3.57	10101110	-2.769	11101110	-1.972
00101111	-4.358	01101111	-3.559	10101111	-2.759	11101111	-1.961
00110000	-4.343	01110000	-3.545	10110000	-2.744	11110000	-1.947
00110001	-4.333	01110001	-3.535	10110001	-2.734	11110001	-1.936
00110010	-4.32	01110010	-3.522	10110010	-2.722	11110010	-1.924
00110011	-4.31	01110011	-3.512	10110011	-2.711	11110011	-1.914
00110100	-4.293	01110100	-3.495	10110100	-2.695	11110100	-1.897
00110101	-4.283	01110101	-3.485	10110101	-2.684	11110101	-1.887
00110110	-4.271	01110110	-3.473	10110110	-2.672	11110110	-1.875
00110111	-4.26	01110111	-3.462	10110111	-2.661	11110111	-1.864
00111000	-4.246	01111000	-3.448	10111000	-2.647	11111000	-1.85
00111001	-4.235	01111001	-3.437	10111001	-2.636	11111001	-1.839
00111010	-4.223	01111010	-3.425	10111010	-2.624	11111010	-1.827
00111011	-4.212	01111011	-3.414	10111011	-2.614	11111011	-1.817
00111100	-4.189	01111100	-3.389	10111100	-2.59	11111100	-1.8045
00111101	-4.178	01111101	-3.378	10111101	-2.579	11111101	-1.792
00111110	-4.166	01111110	-3.366	10111110	-2.567	11111110	-1.7795
00111111	-4.155	01111111	-3.355	10111111	-2.556	11111111	-1.767

Restriction	-

6.4.5. Gamma ldo contro2 (84h)

Command Set		GLDOCTRL2								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
84h	Write	gvdd_adj[7:0]								C0

Description

GVDD LDO output voltage level adjustment:

gvdd_adj[7:0]	GVDD	gvdd_adj[7:0]	GVDD	gvdd_adj[7:0]	GVDD	gvdd_adj[7:0]	GVDD
00000000	3.5336	01000000	4.3307	10000000	5.1308	11000000	5.9304
00000001	3.5461	01000001	4.3424	10000001	5.1425	11000001	5.942
00000010	3.5586	01000010	4.3558	10000010	5.1558	11000010	5.9554
00000011	3.5711	01000011	4.3674	10000011	5.1674	11000011	5.967
00000100	3.5836	01000100	4.3799	10000100	5.1799	11000100	5.9795
00000101	3.5961	01000101	4.3915	10000101	5.1915	11000101	5.9911
00000110	3.6086	01000110	4.4083	10000110	5.2083	11000110	6.0079
00000111	3.6202	01000111	4.42	10000111	5.22	11000111	6.0196
00001000	3.6327	01001000	4.4325	10001000	5.2325	11001000	6.0321

00001001	3.6444	01001001	4.4441	10001001	5.2441	11001001	6.0437
00001010	3.6577	01001010	4.4575	10001010	5.2575	11001010	6.0571
00001011	3.6694	01001011	4.4691	10001011	5.2691	11001011	6.0687
00001100	3.6819	01001100	4.4816	10001100	5.2816	11001100	6.0812
00001101	3.6935	01001101	4.4933	10001101	5.2932	11001101	6.0928
00001110	3.7078	01001110	4.5076	10001110	5.3076	11001110	6.1071
00001111	3.7194	01001111	4.5192	10001111	5.3192	11001111	6.1188
00010000	3.7319	01010000	4.5317	10010000	5.3317	11010000	6.1313
00010001	3.7435	01010001	4.5433	10010001	5.3433	11010001	6.1429
00010010	3.7569	01010010	4.5567	10010010	5.3567	11010010	6.1563
00010011	3.7686	01010011	4.5684	10010011	5.3683	11010011	6.1679
00010100	3.7811	01010100	4.5809	10010100	5.3808	11010100	6.1804
00010101	3.7927	01010101	4.5925	10010101	5.3924	11010101	6.192
00010110	3.8079	01010110	4.6077	10010110	5.4076	11010110	6.2072
00010111	3.8195	01010111	4.6194	10010111	5.4193	11010111	6.2189
00011000	3.832	01011000	4.6318	10011000	5.4318	11011000	6.2313
00011001	3.8437	01011001	4.6435	10011001	5.4434	11011001	6.243
00011010	3.857	01011010	4.6569	10011010	5.4568	11011010	6.2564
00011011	3.8687	01011011	4.6685	10011011	5.4684	11011011	6.268
00011100	3.8812	01011100	4.681	10011100	5.4809	11011100	6.2805
00011101	3.8928	01011101	4.6927	10011101	5.4925	11011101	6.2921
00011110	3.9071	01011110	4.707	10011110	5.5068	11011110	6.3064
00011111	3.9187	01011111	4.7186	10011111	5.5184	11011111	6.318
00100000	3.9312	01100000	4.7311	10100000	5.5309	11100000	6.3305
00100001	3.9429	01100001	4.7428	10100001	5.5426	11100001	6.3421
00100010	3.9562	01100010	4.7561	10100010	5.556	11100010	6.3555
00100011	3.9679	01100011	4.7678	10100011	5.5676	11100011	6.3671
00100100	3.9804	01100100	4.7803	10100100	5.5801	11100100	6.3796
00100101	3.992	01100101	4.7919	10100101	5.5917	11100101	6.3913
00100110	4.0081	01100110	4.808	10100110	5.6078	11100110	6.4073
00100111	4.0197	01100111	4.8197	10100111	5.6194	11100111	6.419
00101000	4.0322	01101000	4.8322	10101000	5.6319	11101000	6.4315
00101001	4.0438	01101001	4.8438	10101001	5.6435	11101001	6.4431
00101010	4.0572	01101010	4.8572	10101010	5.6569	11101010	6.4565
00101011	4.0689	01101011	4.8689	10101011	5.6686	11101011	6.4681
00101100	4.0813	01101100	4.8814	10101100	5.681	11101100	6.4806
00101101	4.093	01101101	4.893	10101101	5.6927	11101101	6.4922
00101110	4.1073	01101110	4.9073	10101110	5.707	11101110	6.5065
00101111	4.1189	01101111	4.919	10101111	5.7186	11101111	6.5182
00110000	4.1314	01110000	4.9315	10110000	5.7311	11110000	6.5307
00110001	4.143	01110001	4.9431	10110001	5.7427	11110001	6.5423
00110010	4.1564	01110010	4.9565	10110010	5.7561	11110010	6.5557

00110011	4.1681	01110011	4.9682	10110011	5.7678	11110011	6.5673
00110100	4.1805	01110100	4.9807	10110100	5.7802	11110100	6.5798
00110101	4.1922	01110101	4.9923	10110101	5.7919	11110101	6.5915
00110110	4.2074	01110110	5.0075	10110110	5.8071	11110110	6.6067
00110111	4.219	01110111	5.0192	10110111	5.8187	11110111	6.6183
00111000	4.2315	01111000	5.0317	10111000	5.8312	11111000	6.6308
00111001	4.2432	01111001	5.0433	10111001	5.8428	11111001	6.6425
00111010	4.2565	01111010	5.0567	10111010	5.8562	11111010	6.656
00111011	4.2682	01111011	5.0683	10111011	5.8679	11111011	6.6677
00111100	4.2807	01111100	5.0808	10111100	5.8803	11111100	6.6802
00111101	4.2923	01111101	5.0924	10111101	5.8919	11111101	6.6918
00111110	4.3066	01111110	5.1067	10111110	5.9063	11111110	6.7059
00111111	4.3182	01111111	5.1183	10111111	5.9179	11111111	6.7171

Restriction	-

6.4.6. Gamma ldo contro3 (85h)

Command Set		GLDOCTRL3								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
85h	Write		vgsp_adj[6:0]							3F

Description

GVSP LDO output voltage level adjustment:

vgsp_adj[6:0]	VGSP	vgsp_adj[6:0]	VGSP	vgsp_adj[6:0]	VGSP	vgsp_adj[6:0]	VGSP
0000000	0.275	0100000	0.675	1000000	1.075	1100000	1.475
0000001	0.2875	0100001	0.6875	1000001	1.0875	1100001	1.4875
0000010	0.3	0100010	0.7	1000010	1.1	1100010	1.5
0000011	0.3125	0100011	0.7125	1000011	1.1125	1100011	1.5125
0000100	0.325	0100100	0.725	1000100	1.125	1100100	1.525
0000101	0.3375	0100101	0.7375	1000101	1.1375	1100101	1.5375
0000110	0.35	0100110	0.75	1000110	1.15	1100110	1.55
0000111	0.3625	0100111	0.7625	1000111	1.1625	1100111	1.5625
0001000	0.375	0101000	0.775	1001000	1.175	1101000	1.575
0001001	0.3875	0101001	0.7875	1001001	1.1875	1101001	1.5875
0001010	0.4	0101010	0.8	1001010	1.2	1101010	1.6
0001011	0.4125	0101011	0.8125	1001011	1.2125	1101011	1.6125
0001100	0.425	0101100	0.825	1001100	1.225	1101100	1.625
0001101	0.4375	0101101	0.8375	1001101	1.2375	1101101	1.6375
0001110	0.45	0101110	0.85	1001110	1.25	1101110	1.65
0001111	0.4625	0101111	0.8625	1001111	1.2625	1101111	1.6625
0010000	0.475	0110000	0.875	1010000	1.275	1110000	1.675

	0010001	0.4875	0110001	0.8875	1010001	1.2875	1110001	1.6875
	0010010	0.5	0110010	0.9	1010010	1.3	1110010	1.7
	0010011	0.5125	0110011	0.9125	1010011	1.3125	1110011	1.7125
	0010100	0.525	0110100	0.925	1010100	1.325	1110100	1.725
	0010101	0.5375	0110101	0.9375	1010101	1.3375	1110101	1.7375
	0010110	0.55	0110110	0.95	1010110	1.35	1110110	1.75
	0010111	0.5625	0110111	0.9625	1010111	1.3625	1110111	1.7625
	0011000	0.575	0111000	0.975	1011000	1.375	1111000	1.775
	0011001	0.5875	0111001	0.9875	1011001	1.3875	1111001	1.7875
	0011010	0.6	0111010	1	1011010	1.4	1111010	1.8
	0011011	0.6125	0111011	1.0125	1011011	1.4125	1111011	1.8125
	0011100	0.625	0111100	1.025	1011100	1.425	1111100	1.825
	0011101	0.6375	0111101	1.0375	1011101	1.4375	1111101	1.8375
	0011110	0.65	0111110	1.05	1011110	1.45	1111110	1.85
	0011111	0.6625	0111111	1.0625	1011111	1.4625	1111111	1.8625
Restriction	-							

6.4.7. Gamma ldo contro3 (87h)

Command Set		GLDOCTRL5								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
87h	Write		D2A_GVCL_VFB_TRIM<2：0>				D2A_GVDD_VFB_TRIM<2：0>			33
Description	D2A_GVDD_VFB_TRIM [2:0]:GVDD voltage trimming, default 011 D2A_GVCL_VFB_TRIM<2:0>：GVCL voltage trimming default 011									
Restriction										

D2A_GVDD_VFB_TRIM [2:0]	GVDD Output Voltage(V)
000	5.9517
001	5.9702
010	5.9890
011(default)	6.0074
100	6.0264
101	6.0456
110	6.0647
111	6.0837
…	19mV/Step

D2A_GVCL_VFB_TRIM [2:0]	GVCL Output Voltage(V)
000	-3.0582
001	-3.0424
010	-3.0267
011(default)	-3.0112
100	-2.9956
101	-2.9802
110	-2.965
111	-2.9498
…	15.6mV/Step

6.4.8. ESD control 1(8Ah)

Command Set		ESDCTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
8Ah	Write							esd_func_sel[1:0]		00
Description	esd_func_sel[1:0] : ESD function select signal.									
Restriction										

6.4.9. ESD control 2(8Bh)

Command Set		ESDCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
8Bh	Write	esd_enable	esd_rd_sram	esd_load_sram	esd_reload_otp	esd_force_analog_1	esd_force_clk_1	esd_force_cs_1	esd_force_dc_1	13
Description	esd_enable : ESD function enable signal. esd_rd_sram : Read sram protect bits to test register. esd_load_sram : Enable signal whether to load SRAM information after ESD occurs. esd_reload_otp : Enable signal for whether to reload OTP after ESD occurs. esd_force_analog_1 : Enable signal whether the analog power supply is protected after ESD occurs. esd_force_clk_1 : Enable signal whether to protect the interface clock after ESD occurs.									

	esd_force_cs_1 : Enable signal whether to protect the interface chip selection signal after ESD occurs. esd_force_dc_1 : Enable signal whether to protect interface DCX signal after ESD occurs.
Restriction	

6.4.10. ESD control 3(8Ch)

Command Set		ESDCTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Read	esd_det[3:0]							esd_occured	/
Description	When this address is read, the flag information is obtained whether or not ESD has occurred: esd_det[3:0] : Whether ESD has occurred in analog circuits. esd_occured : Has ESD occurred in digital circuits.									
Restriction										

6.4.11. RDOTPLD (8Eh)

Command Set		RDOTPLD								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Read						por	lvd	otp_loading	/
Description	When you read this address, you get some internal state information: por : Whether POR is occurring. lvd : Whether low voltage is detected. otp_loading : Whether the OTP is loading.									
Restriction										

6.4.12. Pump control 1(8Fh)

Command Set		PWRCTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
8Fh	Write			vgh_clk_sel[1:0]		vgl_clk_sel[1:0]		mv_clk_sel[1:0]		29
Description	vgh_clk_sel[1:0] : VGH circuit clock selection. vgl_clk_sel[1:0] : VGL circuit clock selection.									

	mv_clk_sel[1:0] : MV circuit clock selection.
Restriction	

6.4.13. Pump control 2(90h)

Command Set		PWRCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
90h	Multi-W	ddvdh_drain_row_on[8]	ddvdh_drain_row_off[8]			ddvdh_drain_frm_on[1:0]		ddvdh_drain_frm_off[1:0]		8B
		ddvdh_drain_row_on[7:0]								2C
		ddvdh_drain_row_off[7:0]								00
Description	ddvdh_drain_frm_on[1:0] : Roughly select the frame from which the ddvdh_drain starts. ddvdh_drain_frm_off[1:0] : Roughly select the frame from which the ddvdh_drain ends. ddvdh_drain_row_on[8:0] : Select exactly which row the ddvdh_drain starts. ddvdh_drain_row_off[8:0] : Select exactly which row the ddvdh_drain ends on.									
Restriction	-									

6.4.14.Pump control 3(91h)

Command Set		**PWRCTRL3**								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
91h	Multi-W	ddvdh_en_row_on[8]	ddvdh_en_row_off[8]			ddvdh_en_frm_on[1:0]		ddvdh_en_frm_off[1:0]		06
		ddvdh_en_row_on[7:0]								00
		ddvdh_en_row_off[7:0]								C8
Description	ddvdh_en_frm_on[1:0] : Roughly select the frame from which the ddvdh_en starts. ddvdh_en_frm_off[1:0] : Roughly select the frame from which the ddvdh_en ends. ddvdh_en_row_on[8:0] : Select exactly which row the ddvdh_en starts. ddvdh_en_row_off[8:0] : Select exactly which row the ddvdh_en ends on.									
Restriction	-									

6.4.15. Pump control 4(92h)

Command Set		PWRCTRL4								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
92h	Multi-W	ddvdl_en_row_on[8]	ddvdl_en_row_off[8]			ddvdl_en_frm_on[1:0]		ddvdl_en_frm_off[1:0]		06
		ddvdl_en_row_on[7:0]								00
		ddvdl_en_row_off[7:0]								C8
Description	ddvdl_en_frm_on[1:0] : Roughly select the frame from which the ddvdl_en starts. ddvdl_en_frm_off[1:0] : Roughly select the frame from which the ddvdl_en ends. ddvdl_en_row_on[8:0] : Select exactly which row the ddvdl_en starts. ddvdl_en_row_off[8:0] : Select exactly which row the ddvdl_en ends on.									
Restriction	-									

6.4.16. Pump control 5(93h)

Command Set		PWRCTRL5								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
93h	Multi-W	mv_disch_row_on[8]	mv_disch_row_off[8]			mv_disch_frm_on[1:0]		mv_disch_frm_off[1:0]		07
		mv_disch_row_on[7:0]								00
		mv_disch_row_off[7:0]								00
Description	mv_disch_frm_on[1:0] : Roughly select the frame from which the mv_disch starts. mv_disch_frm_off[1:0] : Roughly select the frame from which the mv_disch ends. mv_disch_row_on[8:0] : Select exactly which row the mv_disch starts. mv_disch_row_off[8:0] : Select exactly which row the mv_disch ends on.									
Restriction	-									

6.4.17. Pump control 6(94h)

Command Set		PWRCTRL6								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**

94h	Multi-W	vgh_en_row_on[8]	vgh_en_row_off[8]			vgh_en_frm_on[1:0]	vgh_en_frm_off[1:0]	48
		vgh_en_row_on[7:0]						64
		vgh_en_row_off[7:0]						2C
Description	vgh_en_frm_on[1:0] : Roughly select the frame from which the vgh_en starts. vgh_en_frm_off[1:0] : Roughly select the frame from which the vgh_en ends. vgh_en_row_on[8:0] : Select exactly which row the vgh_en starts. vgh_en_row_off[8:0] : Select exactly which row the vgh_en ends on.							
Restriction	-							

6.4.18. Pump control 7(95h)

Command Set		**PWRCTRL7**								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
95h	Multi-W	vgh_disch_row_on[8]	vgh_disch_row_off[8]			vgh_disch_frm_on[1:0]		vgh_disch_frm_off[1:0]		05
		vgh_disch_row_on[7:0]								64
		vgh_disch_row_off[7:0]								C8
Description	vgh_disch_frm_on[1:0] : Roughly select the frame from which the vgh_disch starts. vgh_disch_frm_off[1:0] : Roughly select the frame from which the vgh_disch ends. vgh_disch_row_on[8:0] : Select exactly which row the vgh_disch starts. vgh_disch_row_off[8:0] : Select exactly which row the vgh_disch ends on.									
Restriction	-									

6.4.19. Pump control 8(96h)

Command Set		**PWRCTRL8**								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
96h	Multi-W	vgh_drain_row_on[8]	vgh_drain_row_off[8]			vgh_drain_frm_on[1:0]		vgh_drain_frm_off[1:0]		05
		vgh_drain_row_on[7:0]								00

		vgh_drain_row_off[7:0]	64
Description	vgh_drain_frm_on[1:0] : Roughly select the frame from which the vgh_drain starts. vgh_drain_frm_off[1:0] : Roughly select the frame from which the vgh_drain ends. vgh_drain_row_on[8:0] : Select exactly which row the vgh_drain starts. vgh_drain_row_off[8:0] : Select exactly which row the vgh_drain ends on.		
Restriction	-		

6.4.20. Pump control 9(97h)

Command Set		**PWRCTRL9**								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
97h	Multi-W	vgl_en_row_on[8]	vgl_en_row_off[8]			vgl_en_frm_on[1:0]		vgl_en_frm_off[1:0]		C5
		vgl_en_row_on[7:0]								2C
		vgl_en_row_off[7:0]								2C
Description	vgl_en_frm_on[1:0] : Roughly select the frame from which the vgh_en starts. vgl_en_frm_off[1:0] : Roughly select the frame from which the vgh_en ends. vgl_en_row_on[8:0] : Select exactly which row the vgh_en starts. vgl_en_row_off[8:0] : Select exactly which row the vgh_en ends on.									
Restriction	-									

6.4.21. Pump control 10(98h)

Command Set		**PWRCTRL10**								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
98h	Multi-W	vgl_disch_row_on[8]	vgl_disch_row_off[8]			vgl_disch_frm_on[1:0]		vgl_disch_frm_off[1:0]		06
		vgl_disch_row_on[7:0]								00
		vgl_disch_row_off[7:0]								C8
Description	vgl_disch_frm_on[1:0] : Roughly select the frame from which the vgl_disch starts. vgl_disch_frm_off[1:0] : Roughly select the frame from which the vgl_disch ends. vgl_disch_row_on[8:0] : Select exactly which row the vgl_disch starts. vgl_disch_row_off[8:0] : Select exactly which row the vgl_disch ends on.									

Restriction	-

6.4.22. Pump control 11(99h)

Command Set		PWRCTRL11								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
99h	Multi-W	vgl_drain_row_on[8]	vgl_drain_row_off[8]			vgl_drain_frm_on[1:0]		vgl_drain_frm_off[1:0]		0A
		vgl_drain_row_on[7:0]								00
		vgl_drain_row_off[7:0]								64
Description	vgl_drain_frm_on[1:0] : Roughly select the frame from which the vgl_drain starts. vgl_drain_frm_off[1:0] : Roughly select the frame from which the vgl_drain ends. vgl_drain_row_on[8:0] : Select exactly which row the vgl_drain starts. vgl_drain_row_off[8:0] : Select exactly which row the vgl_drain ends on.									
Restriction	-									

6.4.23. Pump control 12(9Ah)

Command Set		PWRCTRL12								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
9Ah	Write		ddvdh_btrs	ddvdh_btvs[1:0]		ddvdh_btvs_en				68
Description	ddvdh_btrs: Select the DDVDH pump ratio. ddvdh_btvs[1:0]: Setting the clamp level of AVDD. ddvdh_btvs_en: Enable the clamp function of DDVDH.									
Restriction	-									

ddvdh_btrs	ratio
0	2*VCI
1	3*VCI

ddvdh_btvs[1:0]	DDVDH
00	6.2
01(def)	6.4
10	6.6
11	6.8

6.4.24. Pump control 13(9Bh)

<table>
<tr><th colspan="2">Command Set</th><th colspan="8">PWRCTRL13</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>9Bh</td><td>Write</td><td></td><td>ddvdl_ btrs</td><td colspan="2">ddvdl_btvs[1:0]</td><td>ddvdl_bt vs_en</td><td></td><td></td><td></td><td>68</td></tr>
<tr><td>Description</td><td colspan="10">ddvdl_btrs: Select the DDVDL pump ratio.
<table><tr><td>ddvdl_btrs</td><td>ratio</td></tr><tr><td>0</td><td>-1*VCI</td></tr><tr><td>1</td><td>-2*VCI</td></tr></table>ddvdl_btvs[1:0]: Setting the clamp level of DDVDL.
<table><tr><td>ddvdl_btvs[1:0]</td><td>DDVDL</td></tr><tr><td>00</td><td>-4</td></tr><tr><td>01</td><td>-4.4</td></tr><tr><td>10(def)</td><td>-4.8</td></tr><tr><td>11</td><td>-5</td></tr></table>ddvdl_btvs_en: Enable the clamp function of DDVDL.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

6.4.25. Pump control 14(9Ch)

<table>
<tr><th colspan="2">Command Set</th><th colspan="8">PWRCTRL14</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>9Ch</td><td>Write</td><td>vgh_no reg</td><td></td><td colspan="2">vgh_bth[1:0]</td><td></td><td></td><td></td><td></td><td>A0</td></tr>
<tr><td>Description</td><td colspan="10">vgh_noreg: Enable the clamp function of VGH.
<table><tr><td>vgh_noreg</td><td>Clamp</td></tr><tr><td>0</td><td>disable</td></tr><tr><td>1</td><td>enable</td></tr></table>vgh_bth[1:0]: Select the VGH pump ratio.
<table><tr><td>vgh_bth[1:0]</td><td>Ratio</td></tr><tr><td>00</td><td>5*VCIREG</td></tr><tr><td>01</td><td>6*VCIREG</td></tr><tr><td>10</td><td>7*VCIREG</td></tr><tr><td>11</td><td>8*VCIREG</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

6.4.26. Pump control 15(9Dh)

<table>
<tr><th colspan="2">Command Set</th><th colspan="8">PWRCTRL15</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>9Dh</td><td>Write</td><td colspan="5">gam_sw[4:0]</td><td colspan="3">vgh_set[2:0]</td><td>14</td></tr>
<tr><td>Description</td><td colspan="10">gam_sw[4:0] : Select the row from which the Gamma enable is turned on.
vgh_set[2:0]: Setting the clamp level of VGH.
<table>
<tr><th>vgh_set[2:0]</th><th>VGH</th></tr>
<tr><td>000</td><td>10.8</td></tr>
<tr><td>001</td><td>11.2</td></tr>
<tr><td>010</td><td>11.7</td></tr>
<tr><td>011</td><td>12.1</td></tr>
<tr><td>100</td><td>12.5</td></tr>
<tr><td>101</td><td>12.9</td></tr>
<tr><td>110</td><td>13.4</td></tr>
<tr><td>111</td><td>13.8</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

6.4.27. Pump control 16(9Eh)

<table>
<tr><th colspan="2">Command Set</th><th colspan="8">PWRCTRL16</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>9Eh</td><td>Write</td><td>vgl_btrs</td><td>vgl_noreg</td><td></td><td></td><td></td><td colspan="3">vgl_set[2:0]</td><td>C2</td></tr>
<tr><td>Description</td><td colspan="10">vgl_btrs: Select the VGH pump ratio.
<table>
<tr><th>vgl_btrs</th><th>VGH</th></tr>
<tr><td>0</td><td>5*VCI</td></tr>
<tr><td>1</td><td>6*VCI</td></tr>
</table>
vgl_noreg: Enable the clamp function of VGL.
<table>
<tr><th>vgl_noreg</th><th>Clamp</th></tr>
<tr><td>0</td><td>disable</td></tr>
<tr><td>1</td><td>enable</td></tr>
</table>
vgl_set[2:0]: Setting the clamp level of VGL.
<table>
<tr><th>vgl_set[2:0]</th><th>VGL</th></tr>
<tr><td>000</td><td>-8.9</td></tr>
<tr><td>001</td><td>-9.4</td></tr>
<tr><td>010</td><td>-9.9</td></tr>
<tr><td>011</td><td>-10.4</td></tr>
<tr><td>100</td><td>-10.9</td></tr>
<tr><td>101</td><td>-11.3</td></tr>
<tr><td>110</td><td>-11.8</td></tr>
<tr><td>111</td><td>-12.2</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

6.4.28. Pump control 17(9Fh)

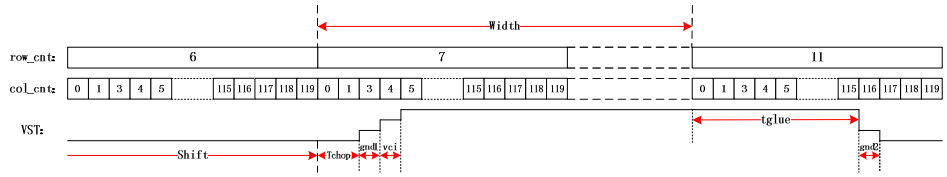
<table>
<tr><th colspan="2">Command Set</th><th colspan="9">PWRCTRL17</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td rowspan="3">9Fh</td><td rowspan="3">Multi-W</td><td>gam_ref_bypass</td><td>bias_en_bypass</td><td>vdds_en_bypass</td><td>vref_en_bypass</td><td>vgl_drain_bypass</td><td>vgl_disch_bypass</td><td>gam_en_bypass</td><td>pump_ctrl_en</td><td>00</td></tr>
<tr><td>vgl_en_bypass</td><td>vgh_drain_bypass</td><td>vgh_disch_bypass</td><td>vgh_en_bypass</td><td>mv_disch_bypass</td><td>ddvdl_en_bypass</td><td>ddvdh_en_bypass</td><td>ddvdh_drain_bypass</td><td>00</td></tr>
<tr><td colspan="6">chop_sw[4:0]</td><td>chop_ctrl</td><td>sd_en_bypass</td><td>04</td></tr>
<tr><td>Description</td><td colspan="10">When entering test mode, use the following signal to turn off the corresponding power supply:
pump_ctrl_en : Power master switch, can turn off all power supplies.
gam_ref_bypass : Turn off the gam_ref.
bias_en_bypass : Turn off the bias_en.
vdds_en_bypass : Turn off the vdds_en.
vref_en_bypass : Turn off the vref_en.
vgl_drain_bypass : Turn off the vgl_drain.
vgl_disch_bypass : Turn off the vgl_disch.
gam_en_bypass : Turn off the gam_en.
vgl_en_bypass : Turn off the vgl_en.
vgh_drain_bypass : Turn off the vgh_drain.
vgh_disch_bypass : Turn off the vgh_disch.
vgh_en_bypass : Turn off the vgh_en.
mv_disch_bypass : Turn off the mv_disch.
ddvdl_en_bypass : Turn off the ddvdl_en.
ddvdh_en_bypass : Turn off the ddvdh_en.
ddvdh_drain_bypass : Turn off the ddvdh_drain.
sd_en_bypass : Turn off the sd_en.
chop_sw[4:0] : Select gam_chop from which row to start the conversion.
chop_ctrl : gam_chop enable Signal.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

6.5. Description of Command 4

6.5.1. GOA control (A0h)

Command Set		GOACTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W	eck_diff_cnt[2:0]			eck_sel	map_sel[1:0]		goa_slpin_sel[1:0]		00
2nd Parameter		eck_cnt_num[7:0]								3C
Description	eck_diff_cnt[2:0] : Sets the conversion interval between eck and exck signals. eck_sel : Select eck output voltage. map_sel[1:0] : Select goa mapping mode. goa_slpin_sel[1:0] : When the current state is sleep in, Select the goa PAD output voltage. eck_cnt_num[7:0] : Set the cycle of eck and exck signal conversion.									
Restriction	-									

6.5.2. GOA VST control 1(A1h)

Command Set		VSTCTR1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A1	Write	goa_vst1_shift[7:0]								83
Description	goa_vst1_shift[7:0] : Specifies the row on which the VST begins. 									
Restriction	-									

6.5.3. GOA VST control 2(A2h)

Command Set		VSTCTR2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A2	Write	goa_vst2_shift[7:0]								83
Description	goa_vst2_shift[7:0] : Specifies the row on which the VST begins.									
Restriction	-									

6.5.4. GOA VST control 3(A3h)

Command Set		VSTCTR3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A3	Write	goa_vst3_shift[7:0]								00
Description	goa_vst3_shift[7:0] : Specifies the row on which the VST begins.									
Restriction	-									

6.5.5. GOA VST control 4(A4h)

Command Set		VSTCTR4								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A4	Write	goa_vst4_shift[7:0]								00
Description	goa_vst4_shift[7:0] : Specifies the row on which the VST begins.									
Restriction	-									

6.5.6. GOA VST control 5(A5h)

Command Set		VSTCTR5								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A5	Write	vst_gnd1_period[7:0]								14
Description	vst_gnd1_period[7:0] : Specifies the time when the VST voltage is raised to GND.									
Restriction	-									

6.5.7. GOA VST control 6(A6h)

Command Set		VSTCTR6								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A6	Write	vst_gnd2_period[7:0]								14
Description	vst_gnd2_period[7:0] : Specifies the time when the VST voltage will fall back to GND.									
Restriction	-									

6.5.8. GOA VST control 7(A7h)

Command Set		VSTCTR7								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A7	Write	vst_vci_period[7:0]								14
Description	vst_vci_period[7:0] : Specifies the time when the VST voltage is raised to VCI.									
Restriction	-									

6.5.9. GOA VST control 8(A8h)

Command Set		VSTCTR8								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A8	Write	goa_vst_tchop[8]	goa_vst_tglue[8]	vst_noverlap[1:0]		goa_vst_width[3:0]				03
Description	vst_noverlap[1:0] : VST switching interval between different power supplies. goa_vst_width[3:0] : The time interval during which the VST is maintained at the VGH voltage.									
Restriction	-									

6.5.10. GOA VST control 9(A9h)

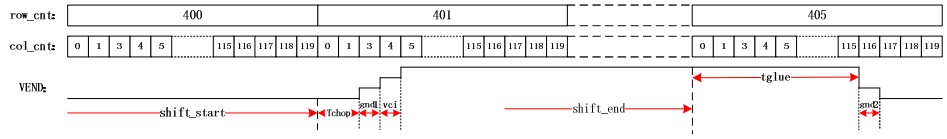
Command Set		VSTCTR9								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A9	Write	goa_vst_tchop[7:0]								00
Description	goa_vst_tchop[8:0] : Specifies which column the VST should be raised from.									
Restriction	-									

6.5.11. GOA VST control 10(AAh)

Command Set		VSTCTR10								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
AA	Write	goa_vst_tglue[7:0]								00
Description	goa_vst_tglue[8:0] : Specifies the column from which the VST starts to pull low.									

Restriction	-

6.5.12. GOA VEND control 1(ABh)

Command Set		VENDCTRL11								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
ABh	Multi-W							goa_vend1_shift_start[9:8]		01
		goa_vend1_shift_start[7:0]								EB
Description	goa_vend1_shift_start[9:0] : Specifies the row on which the VEND begins. 									
Restriction	-									

6.5.13. GOA VEND control 2(ACh)

Command Set		VENDCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
ACh	Multi-W							goa_vend1_shift_end[9:8]		01
		goa_vend1_shift_end[7:0]								EF
Description	goa_vend1_shift_end[9:0] : Specifies the row on which the VEND ends.									
Restriction	-									

6.5.14. GOA VEND control 3(ADh)

Command Set		VENDCTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
ADh	Multi-W							goa_vend2_shift_start[9:8]		01
		goa_vend2_shift_start[7:0]								EB
Description	goa_vend2_shift_start[9:0] : Specifies the row on which the VEND begins.									
Restriction	-									

6.5.15. GOA VEND control 4(AEh)

Command Set		VENDCTRL4								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
AEh	Multi-W							goa_vend2_shift_end[9:8]		01
		goa_vend2_shift_end[7:0]								EF
Description	goa_vend2_shift_end[9:0] : Specifies the row on which the VEND ends.									
Restriction	-									

6.5.16. GOA VEND control 5(AFh)

Command Set		VENDCTRL5								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
AFh	Multi-W							goa_vend3_shift_start[9:8]		00
		goa_vend3_shift_start[7:0]								00
Description	goa_vend3_shift_start[9:0] : Specifies the row on which the VEND begins.									
Restriction	-									

6.5.17. GOA VEND control 6(B0h)

Command Set		VENDCTRL6								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
B0h	Multi-W							goa_vend3_shift_end[9:8]		00
		goa_vend3_shift_end[7:0]								00
Description	goa_vend3_shift_end[9:0] : Specifies the row on which the VEND ends.									
Restriction	-									

6.5.18. GOA VEND control 7(B1h)

Command Set		VENDCTRL7								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**

B1h	Multi-W							goa_vend4_shift_start[9:8]	00
		goa_vend4_shift_start[7:0]							00
Description	goa_vend4_shift_start[9:0] : Specifies the row on which the VEND begins.								
Restriction	-								

6.5.19. GOA VEND control 8(B2h)

Command Set		VENDCTRL8								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
B2h	Multi-W							goa_vend4_shift_end[9:8]		00
		goa_vend4_shift_end[7:0]								00
Description	goa_vend4_shift_end[9:0] : Specifies the row on which the VEND ends.									
Restriction	-									

6.5.20. GOA VEND control 9(B3h)

Command Set		VENDCTRL9								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
B3h	Write	vend_gnd1_period[7:0]								14
Description	vend_gnd1_period[7:0] : Specifies the time when the VEND voltage is raised to GND.									
Restriction	-									

6.5.21. GOA VEND control 10(B4h)

Command Set		VENDCTRL10								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
B4h	Write	vend_gnd2_period[7:0]								14
Description	vend_gnd2_period[7:0] : Specifies the time when the VEND voltage will fall back to GND.									
Restriction	-									

6.5.22. GOA VEND control 11(B5h)

Command Set	VENDCTRL11

Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
B5h	Write	vend_vci_period[7:0]								14
Description	vend_vci_period[7:0] : Specifies the time when the VEND voltage is raised to VCI.									
Restriction	-									

6.5.23. GOA VEND control 12(B6h)

Command Set		VENDCTRL12								
Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
B6h	Write	goa_vend_tchop[8]	goa_vend_tglue[8]	vend_noverlap[1:0]					bw_fw_sel	00
Description	vend_noverlap[1:0] : VEND switching interval between different power supplies. bw_fw_sel : bw and fw voltage selection.									
Restriction	-									

6.5.24. GOA VEND control 13(B7h)

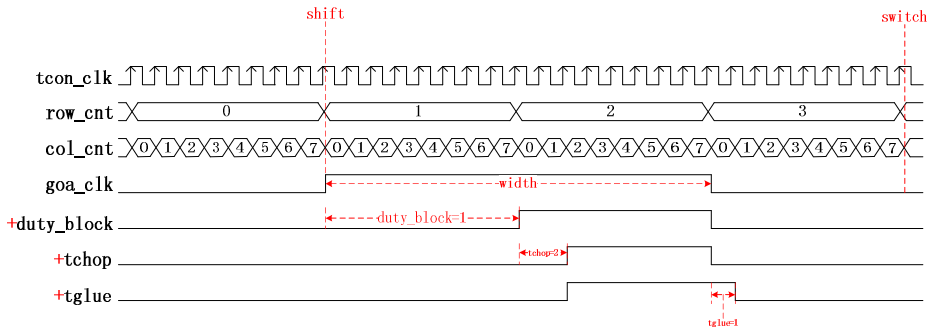
Command Set		VENDCTRL13								
Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
B7h	Write	goa_vend_tchop[7:0]								00
Description	goa_vend_tchop[8:0] : Specifies which column the VEND should be raised from.									
Restriction	-									

6.5.25. GOA VEND control 14(B8h)

Command Set		VENDCTRL14								
Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
B8h	Write	goa_vend_tglue[7:0]								00
Description	goa_vend_tglue[8:0] : Specifies the column from which the VEND signal starts to pull low.									
Restriction	-									

6.5.26. GOA CLK control 1(B9h)

Command Set	CLKCTRL1

Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
B9h	Write	goa_clk1_shift[7:0]								81
Description	goa_clk1_shift[7:0] : Specifies the row on which the CLK begins. 									
Restriction	-									

6.5.27. GOA CLK control 2(BAh)

Command Set		CLKCTRL2								
Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
BAh	Write	goa_clk2_shift[7:0]								81
Description	goa_clk2_shift[7:0] : Specifies the row on which the CLK begins.									
Restriction	-									

6.5.28. GOA CLK control 3(BBh)

Command Set		CLKCTRL3								
Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
BBh	Write	goa_clk3_shift[7:0]								01
Description	goa_clk3_shift[7:0] : Specifies the row on which the CLK begins.									
Restriction	-									

6.5.29. GOA CLK control 4(BCh)

Command Set		CLKCTRL4								
Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
BCh	Write	goa_clk4_shift[7:0]								01

Description	goa_clk4_shift[7:0] : Specifies the row on which the CLK begins.
Restriction	-

6.5.30. GOA CLK control 5(BDh)

Command Set		CLKCTRL5								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
BDh	Write	goa_clk5_shift[7:0]								03
Description	goa_clk5_shift[7:0] : Specifies the row on which the CLK begins.									
Restriction	-									

6.5.31. GOA CLK control 6(BEh)

Command Set		CLKCTRL6								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
BEh	Write	goa_clk6_shift[7:0]								03
Description	goa_clk6_shift[7:0] : Specifies the row on which the CLK begins.									
Restriction	-									

6.5.32. GOA CLK control 7(BFh)

Command Set		CLKCTRL7								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
BFh	Write	goa_clk7_shift[7:0]								05
Description	goa_clk7_shift[7:0] : Specifies the row on which the CLK begins.									
Restriction	-									

6.5.33. GOA CLK control 8(C0h)

Command Set		CLKCTRL8								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C0h	Write	goa_clk8_shift[7:0]								05
Description	goa_clk8_shift[7:0] : Specifies the row on which the CLK begins.									
Restriction	-									

6.5.34. GOA CLK control 9(C1h)

Command Set		CLKCTRL9								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C1h	Write	clk_gnd1_period[7:0]								14
Description	clk_gnd1_period[7:0] : Specifies the time when the CLK voltage is raised to GND.									
Restriction	-									

6.5.35. GOA CLK control 10(C2h)

Command Set		CLKCTRL10								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C2h	Write	clk_gnd2_period[7:0]								14
Description	clk_gnd2_period[7:0] : Specifies the time when the CLK voltage will fall back to GND.									
Restriction	-									

6.5.36. GOA CLK control 11(C3h)

Command Set		CLKCTRL11								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C3h	Write	clk_vci_period[7:0]								14
Description	clk_vci_period[7:0] : Specifies the time when the CLK voltage is raised to VCI.									
Restriction	-									

6.5.37. GOA CLK control 12(C4h)

Command Set		CLKCTRL12								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C4h	Write	goa_clk_tchop[8]	goa_clk_tglue[8]	clk_noverlap[1:0]		goa_clk_width[3:0]				03
Description	clk_noverlap[1:0] : CLK switching interval between different power supplies. goa_clk_width[3:0] : The time interval during which the CLK is maintained at the VGH voltage.									
Restriction	-									

6.5.38. GOA CLK control 13(C5h)

Command Set		CLKCTRL13								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C5h	Write	goa_clk_tchop[7:0]								00
Description	goa_clk_tchop[8:0] : Specifies which column the CLK should be raised from.									
Restriction	-									

6.5.39. GOA CLK control 14(C6h)

Command Set		CLKCTRL14								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C6h	Write	goa_clk_tglue[7:0]								00
Description	goa_clk_tglue[8:0] : Specifies the column from which the CLK starts to pull low.									
Restriction	-									

6.5.40. GOA CLK control 15(C7h)

Command Set		CLKCTRL15								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C7h	Write					duty_block[3:0]				00
Description	duty_block[3:0] : Set the duty cycle of CLK signal.									
Restriction	-									

6.5.41. GOA CLK control 16(C8h)

Command Set		CLKCTRL16								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C8h	Write	goa_clk1_switch [9:8]		goa_clk2_switch[9:8]		goa_clk3_switch[9:8]		goa_clk4_switch[9:8]		55
Description	The high level of the following register.									
Restriction	-									

6.5.42. GOA CLK control 17(C9h)

Command Set		CLKCTRL17								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C9h	Write	goa_clk1_switch[7:0]								E4
Description	goa_clk1_switch[9:0] : Set the CLK on which line to turn off.									
Restriction	-									

6.5.43. GOA CLK control 18(CAh)

Command Set		CLKCTRL18								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
CAh	Write	goa_clk2_switch[7:0]								E4
Description	goa_clk2_switch[9:0] : Set the CLK on which line to turn off.									
Restriction	-									

6.5.44. GOA CLK control 19(CBh)

Command Set		CLKCTRL19								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
CBh	Write	goa_clk3_switch[7:0]								E6
Description	goa_clk3_switch[9:0] : Set the CLK on which line to turn off.									
Restriction	-									

6.5.45. GOA CLK control 20(CCh)

Command Set		CLKCTRL20								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
CCh	Write	goa_clk4_switch[7:0]								E6
Description	goa_clk4_switch[9:0] : Set the CLK on which line to turn off.									
Restriction	-									

6.5.46. GOA CLK control 21(CDh)

Command Set		CLKCTRL21								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
CDh	Write	goa_clk5_switch [9:8]		goa_clk6_switch[9:8]		goa_clk7_switch[9:8]		goa_clk8_switch[9:8]		55
Description	The high level of the following register.									
Restriction	-									

6.5.47. GOA CLK control 22(CEh)

Command Set		CLKCTRL22								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
CEh	Write	goa_clk5_switch[7:0]								E8
Description	goa_clk5_switch[9:0] : Set the CLK on which line to turn off.									
Restriction	-									

6.5.48. GOA CLK control 23(CFh)

Command Set		CLKCTRL23								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
CFh	Write	goa_clk6_switch[7:0]								E8
Description	goa_clk6_switch[9:0] : Set the CLK on which line to turn off.									
Restriction	-									

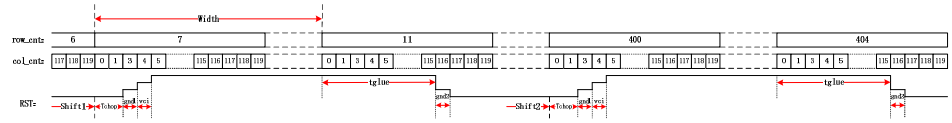
6.5.49. GOA CLK control 24(D0h)

Command Set		CLKCTRL24								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
D0h	Write	goa_clk7_switch[7:0]								EA
Description	goa_clk7_switch[9:0] : Set the CLK on which line to turn off.									
Restriction	-									

6.5.50. GOA CLK control 25(D1h)

Command Set		CLKCTRL25								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
D1h	Write	goa_clk8_switch[7:0]								EA
Description	goa_clk8_switch[9:0] : Set the CLK on which line to turn off.									
Restriction	-									

6.5.51. GOA RST control 1(D2h)

Command Set		RSTCTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
D2h	Write	goa_rst_shift1[7:0]								00
Description	goa_rst_shift1[7:0] : Specifies the row on which the RST begins. 									
Restriction	-									

6.5.52. GOA RST control 2(D3h)

Command Set		RSTCTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
D3h	Multi-W							goa_rst_shift2[9:8]		00
		goa_rst_shift2[7:0]								00
Description	goa_rst_shift2[9:0] : Specifies the row on which the RST begins.									
Restriction	-									

6.5.53. GOA RST control 4(D4h)

Command Set	RSTCTRL4

Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
D4h	Write	rst_gnd1_period[7:0]								14
Description	rst_gnd1_period[7:0] : Specifies the time when the RST voltage is raised to GND.									
Restriction	-									

6.5.54. GOA RST control 5(D5h)

Command Set		RSTCTRL5								
Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
D5h	Write	rst_gnd2_period[7:0]								14
Description	rst_gnd2_period[7:0] : Specifies the time when the RST voltage will fall back to GND.									
Restriction	-									

6.5.55. GOA RST control 6(D6h)

Command Set		RSTCTRL6								
Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
D6h	Write	rst_vci_period[7:0]								14
Description	rst_vci_period[7:0] : Specifies the time when the RST voltage is raised to VCI.									
Restriction	-									

6.5.56. GOA RST control 7(D7h)

Command Set		RSTCTRL7								
Command	Write/ Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
D7h	Write	goa_rst_tchop[8]	goa_rst_tglue[8]	rst_noverlap[1:0]		goa_rst_width[3:0]				03
Description	rst_noverlap[1:0] : RST switching interval between different power supplies. goa_rst_width[3:0] : The time interval during which the RST is maintained at the VGH voltage.									
Restriction	-									

6.5.57. GOA RST control 8(D8h)

Command Set		RSTCTRL8								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
D8h	Write	goa_rst_tchop[7:0]								0F
Description	goa_rst_tchop[7:0] : Specifies which column the RST should be raised from.									
Restriction	-									

6.5.58. GOA RST control 9(D9h)

Command Set		RSTCTRL9								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
D9h	Write	goa_rst_tglue[7:0]								0F
Description	goa_rst_tglue[7:0] : Specifies the column from which the CLK starts to pull low.									
Restriction	-									

6.5.59. Read ID1 (DAh)

Command Set		RDID1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Read	No Parameter								/
Description	id1 : LCD module/driver ID.									
Restriction	-									

6.5.60. Read ID2 (DBh)

Command Set		RDID2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Read	No Parameter								/
Description	id2 : LCD module/driver ID.									
Restriction	-									

6.5.61. Read ID3 (DCh)

Command Set		RDID3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Read	No Parameter								/
Description	Id3 : LCD module/driver ID.									
Restriction	-									

6.5.62. Write ID1 (DDh)

Command Set		WRID1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	id1[7:0]								00
Description	id1[7:0] : Set the LCD module/driver id1 through the interface.									
Restriction										

6.5.63. Write ID2 (DEh)

Command Set		WRID2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	id2[7:0]								30
Description	id2[7:0] : Set the LCD module/driver id1 through the interface.									
Restriction										

6.5.64. Write ID3 (DFh)

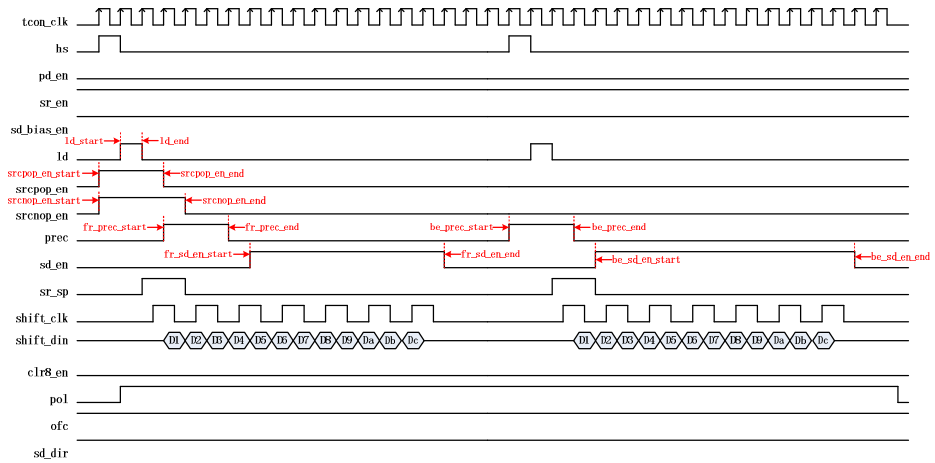
Command Set		WRID3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write	id3[7:0]								02
Description	Id3[7:0] : Set the LCD module/driver id1 through the interface.									
Restriction										

6.6. Description of Command 5

6.6.1. Source control 1(E0h)

Command Set		SOUCTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E0h	Write	ld_start[8]	ld_end[8]	srcpop_en_start[8]	srcpop_en_end[8]	srcnop_en_start[8]	srcnop_en_end[8]	fr_prec_start[8]	fr_prec_end[8]	00
Description	The high level of the following register.									
Restriction	-									

6.6.2. Source control 2(E1h)

Command Set		SOUCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E1h	Write	ld_start[7:0]								05
Description	ld_start[8:0] : Sets the starting column of the ld signal. 									
Restriction	-									

6.6.3. Source control 3(E2h)

Command Set		SOUCTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E2h	Write	ld_end[7:0]								06

Description	ld_end[8:0] : Sets the end column of the ld signal.
Restriction	-

6.6.4. Source control 4(E3h)

Command Set		SOUCTRL4								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E3h	Write	srcpop_en_start[7:0]								01
Description	srcpop_en_start[7:0] : Sets the starting column of the srcpop signal.									
Restriction	-									

6.6.5. Source control 5(E4h)

Command Set		SOUCTRL5								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E4h	Write	srcpop_en_end[7:0]								00
Description	srcpop_en_end[8:0] : Sets the end column of the srcpop signal.									
Restriction	-									

6.6.6. Source control 6(E5h)

Command Set		SOUCTRL6								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E5h	Write	srcnop_en_start[7:0]								01
Description	srcnop_en_start[8:0] : Sets the starting column of the srcnop signal.									
Restriction	-									

6.6.7. Source control 7(E6h)

Command Set		SOUCTRL7								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E6h	Write	srcnop_en_end[7:0]								1B
Description	srcnop_en_end[8:0] : Sets the end column of the srcnop signal.									
Restriction	-									

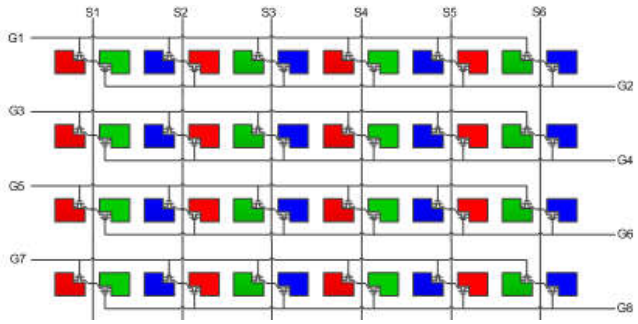
6.6.8. Source control 8(E7h)

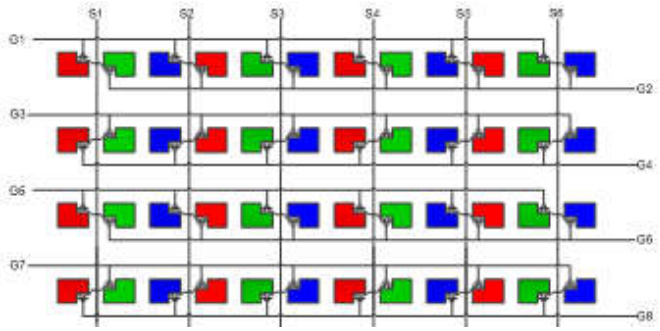
Command Set		SOUCTRL8								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E7h	Write	fr_prec_start[7:0]								12
Description	fr_prec_start[8:0] : Sets the starting column of the first half of the prec signal.									
Restriction	-									

6.6.9. Source control 9(E8h)

Command Set		SOUCTRL9								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E8h	Write	fr_prec_end[7:0]								22
Description	fr_prec_end[8:0] : Sets the end column of the first half of the prec signal.									
Restriction	-									

6.6.10. Source control 10(E9h)

Command Set		SOUCTRL10								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E9h	Write	pol_ctrl	pol_init	ofc_ctrl	ofc_init	odd_even_ctrl	fr_sd_en_start[8]	fr_sd_en_end[8]		20
Description	pol_ctrl : Dot inversion and column Inversion selection. pol_init : Set the initial value of the pol signal. ofc_ctrl : ofc signal enable. ofc_init : Set the initial value of the ofc signal. odd_even_ctrl : Selection of glass connection. 									

	
Restriction	-

6.6.11. Source control 11(EAh)

Command Set		SOUCTRL11								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
EAh	Write	fr_sd_en_start[7:0]								23
Description	fr_sd_en_start[8:0] : Sets the starting column of the first half of the sd_en signal.									
Restriction	-									

6.6.12. Source control 12(EBh)

Command Set		SOUCTRL12								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
EBh	Write	fr_sd_en_end[7:0]								A0
Description	fr_sd_en_end[8:0] : Sets the starting column of the first half of the sd_en signal.									
Restriction	-									

6.6.13. Source control 13(ECh)

Command Set		SOUCTRL13								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
ECh	Write	pol_switch[8]		be_prec_start[8]	be_prec_end[8]	chopper_sel[1:0]		be_sd_en_start[8]	be_sd_en_end[8]	00
Description	chopper_sel[1:0] : Select the mode of ofc signal.									
Restriction	-									

6.6.14. Source control 14(EDh)

Command Set		SOUCTRL14								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
EDh	Write	be_prec_start[7:0]								01
Description	be_prec_start[8:0] : Sets the starting column of the last half row of the prec signal.									
Restriction	-									

6.6.15. Source control 15(EEh)

Command Set		SOUCTRL15								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
EEh	Write	be_prec_end[7:0]								11
Description	be_prec_end[8:0] : Sets the end column of the last half row prec signal.									
Restriction	-									

6.6.16. Source control 16(EFh)

Command Set		SOUCTRL16								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
EFh	Write	be_sd_en_start[7:0]								12
Description	be_sd_en_start[8:0] : Sets the starting column of the last half row of the sd_en signal.									
Restriction	-									

6.6.17. Source control 17 (F0h)

Command Set		SOUCTRL17								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
F0h	Write	be_sd_en_end[7:0]								A0
Description	be_sd_en_end[8:0] : Sets the end column of the last half row sd_en signal.									
Restriction	-									

6.6.18. Source control 18(F1h)

Command Set		SOUCTRL18								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
F1h	Write	pol_switch[7:0]								00
Description	pol_switch[8:0] : Set the POL signal conversion location.									
Restriction	-									

6.6.19. Source control 19(F2h)

Command Set		SOUCTRL19								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
F2h	Write		pncs_en		goa_2143_en		rev	normal_black	pts	40
Description	pncs_en : pncs enable signal. goa_2143_en : goa 2143 mode enable signal. rev : Pixel reverse color control. normal_black : Select whether the screen is always white or always black. pts : Determine source output in a non-display area in the partial display mode.									
Restriction	-									

6.6.20. CP test 1(F4h)

Command Set		CPTEST1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
F4h	Write								cpe0	00
Description	cpe0 : Select whether the data to be written to RAM is cpdat or pxl_dat.									
Restriction	-									

6.6.21. CP test 2(F5h)

Command Set		CPTEST2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
F5h	Write								cpe1	00

Description	cpe1 : Select whether the data output to Source will be read RAM or written by the interface for CP testing.
Restriction	-

6.6.22. CP test 3(F6h)

Command Set		CPTEST3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
F6h	Write	cpdat[7:0]								00
Description	cpdat[7:0] : set cp test data.									
Restriction	-									

6.6.23. GVDD adjust (F7h)

Command Set		GVSPADJ								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
F8h	Write				gvdd_otp[4:0]					00
Description	gvdd_otp[4:0]:GVDD otp trimming. gvdd_otp[4] is its sign bit, gvdd_otp[3:0] is used to adjust the GVDD voltage. The value of GVDD valtage is depend on the sum of gvdd_adj[7:0] (84H) and gvdd_otp[4:0]. Eg: gvdd_otp = 5'h04 gvdd_adj = 8'hc0 GVDD = 8'hc0 + 5'h04 = 8'hc4 gvdd_otp = 5'h11 gvdd_adj = 8'hc0 GVDD = 8'hc0 - 5'h01 = 8'hbf									
Restriction	-									

6.6.24. GVSP adjust (F8h)

Command Set		GVSPADJ								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
F8h	Write						gvsp_otp[2:0]			00
Description	gvsp_otp[2:0]:GVSP otp trimming. gvsp_otp[[2] is its sign bit, gvsp_otp[1:0] is used to adjust the GVSP voltage. The value of GVSP valtage is depend on the sum of vgsp_adj[6:0](85H) and gvsp_otp[2:0] .									
Restriction	-									

6.6.25. GVCL adjust (FAh)

Command Set		GVCLADJ								
Command	**Write/Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
F8h	Write				gvcl_otp[4:0]					00
Description	gvcl_otp[4:0]:GVCL otp trimming. gvcl_otp [4] is its sign bit, gvcl_otp [3:0] is used to adjust the GVCL voltage. The final value of GVCL valtage is depend on the sum of gvcl_adj[7:0](83H) and gvcl_otp[4:0].									
Restriction	-									

6.6.26. Pad control (FBh)

Command Set		PADCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Read			atest_en	osc_test_oe			ledpwm_oe	ledpwm	03
Description	atest_en : Whether to enable the osc_clk dichotomal signal. Osc_test_oe : osc div test output enable. ledpwm_oe : ledpwm enable signal. ledpwm : The dimming signal.									
Restriction	-									

6.6.27. RDSTATE (FCh)

Command Set		RDSTATE								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Write						cur_state[2:0]			/
Description	cur_state[2:0] : Gets the current state information of the state machine.									
Restriction	-									

6.6.28. Read power status (FDh)

Command Set		RD_PWR_STATUS								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-R		gam_en	regu_en	bgr_buf_en	vref_en	vdds_en	bias_en	gam_ref_en	/
2nd Parameter						vgl_en	vgh_en	ddvdl_en	ddvdh_en	/
Description	Reading this address will fetch internal power information.									
Restriction	-									

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When NV3002 is used out of the absolute maximum ratings, NV3002 may be permanently damaged. To use NV3002 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, NV3002 will malfunction and cause poor reliability.

Table34.

Item	Symbol	Unit	Value
Supply voltage	VCIB	V	-0.3~+4.6
Supply voltage(Logic)	IOVCC	V	-0.3~+4.6
Supply voltage(Digital)	DVDD	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	-0.3~+32.0
Logic input voltage range	VIN	V	-0.3~IOVCC+0.3
Logic output voltage range	VO	V	-0.3~IOVCC+0.3
Operation temperature	Topr	℃	-35~+80
Storage temperature	Tstg	℃	-40~+100
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

7.2. DC Characteristics

General DC Characteristics

Table35.

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog OperatingVoltage	VCIB	V	Operating voltage	2.5	2.8	3.6	Note2
Logic Operating Voltage	IOVCC	V	I/O supply voltage	1.65	2.8	3.6	Note2
Digital Operating voltage	DVDD	V	Digital supply voltage	-	1.55	-	Note2
GateDriver High Voltage	VGH	V	-	10.8	-	13.8	Note3
Gate Driver Low Voltage	VGL	V	-	-8.9	-	-12.2	Note3
Driver SupplyVoltage	-	V	|VGH-VGL|	19.7	-	26	Note3
Input and Output							
Logic HighLevel Input Voltage	VIH	V	-	0.7* IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	DGND	-	0.3* IOVCC	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8* IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	DGND	-	0.2* IOVCC	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=IOVCC or DGND	-0.1	-	+0.1	Note1,2,3
Source Driver							
Source Output Range	Vsout	V	-	GVCL	-	GVDD	Note4

Note 1: IOVCC=1.65 to 3.6V, VCIB=2.5 to 3.6V, AGNDB=DGND=0V, Ta=-35 to 80 ℃

Note2: Please supply digital IOVCC voltage equal or less than analog VCIB voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC,

DE, SDA, SCL, IM3, IM2,IM1,IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

Note5: VCIB=2.8V

Note6: VCIB=2.8V

Note7: The Max. Value is between with Note 4 measure point and Gamma setting value

7.3. AC Characteristics

7.3.1. Display Parallel 8-bit Interface Timing Characteristics (8080-Ⅰ)

Figure80.

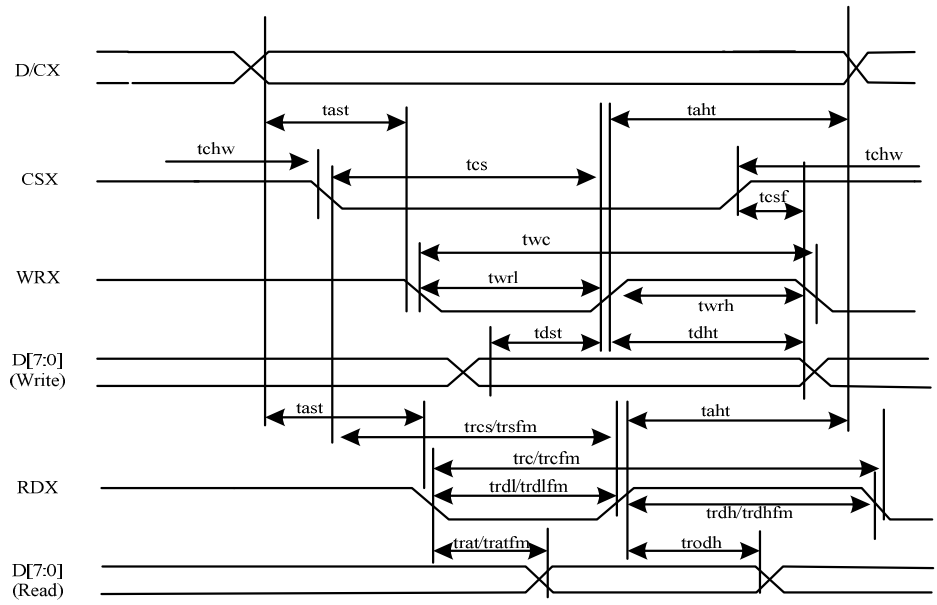


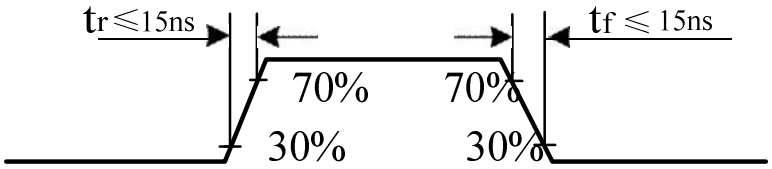
Table36

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	

WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	70	-	ns	
D[17:0], D[15:0],	tdst	Write data setup time	10	-	ns	For maximum CL=30pF
	tdht	Write data hold time	10	-	ns	
D[8:0], D[7:0]	trat	Read access time	-	40	ns	For minimum CL=8pF
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

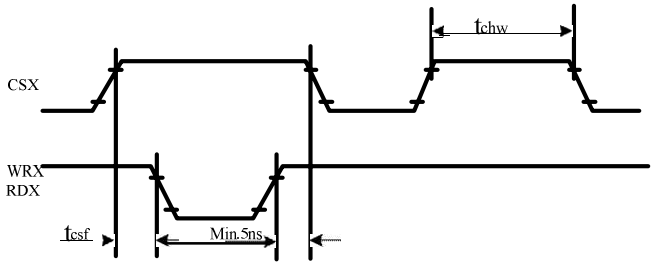
Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCIB=2.5V to 3.6V, DGND=0V

Figure81.



CSX timings :

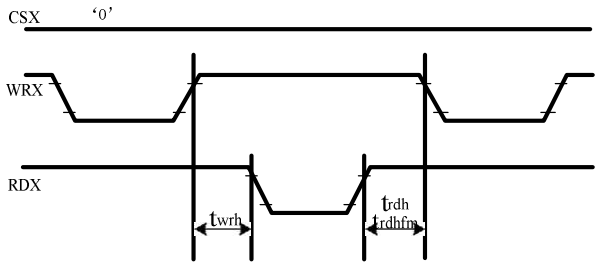
Figure82.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:

Figure83.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.3.2. Display Parallel 8-bit Interface Timing Characteristics (8080-Ⅱ)

Figure84.

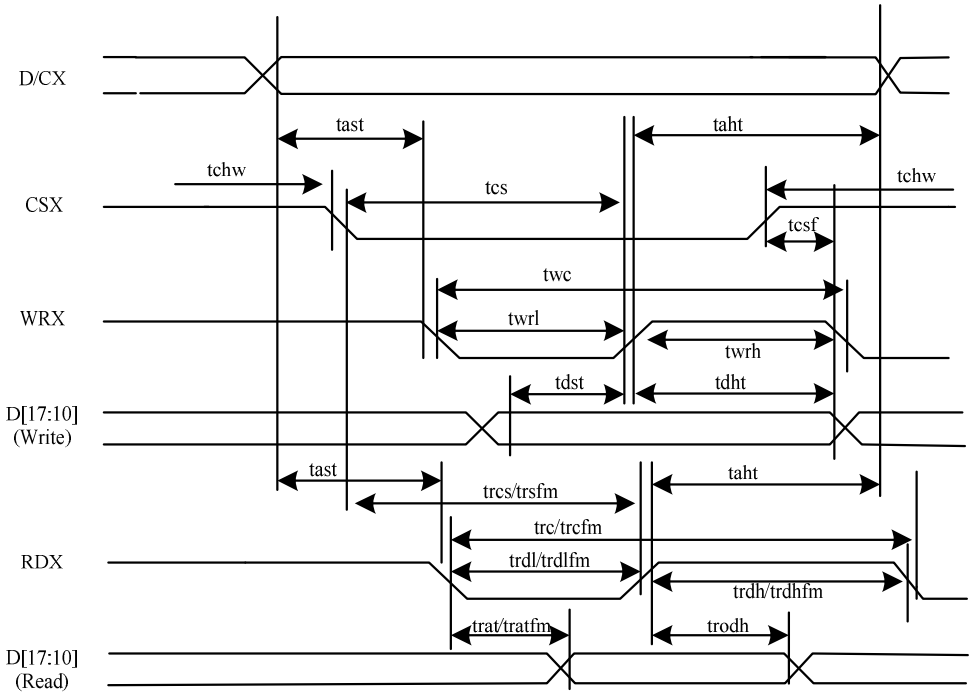


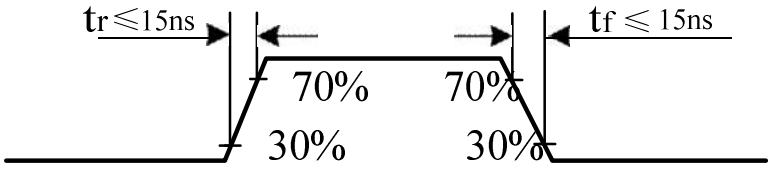
Table37.

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
	tchw	CSX "H" pulse width	0	-	ns	

CSX	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	70	-	ns	
D[17:0], D[17:10] &D[8:1], D[17:10] ,D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

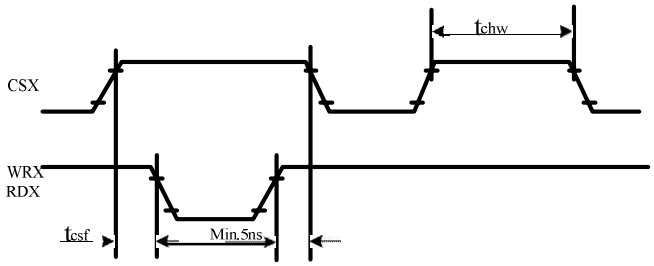
Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCIB=2.5V to 3.3V, DGND=0V

Figure85.



CSX timings :

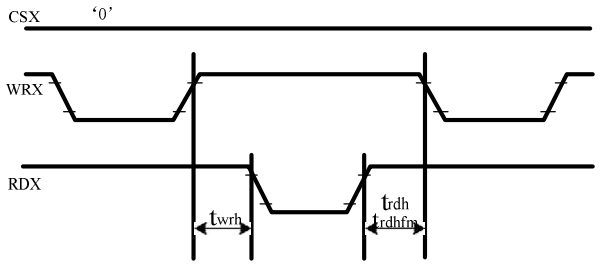
Figure86.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:

Figure87.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.3.3. Display Serial Interface Timing Characteristics (3-line SPI system)

Figure88.

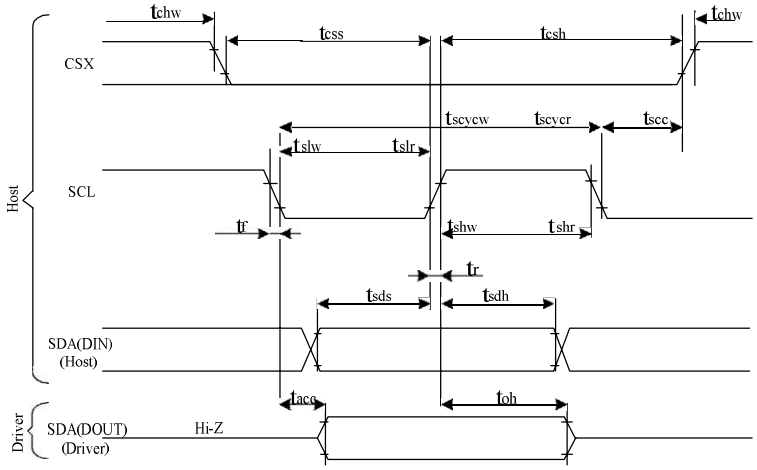


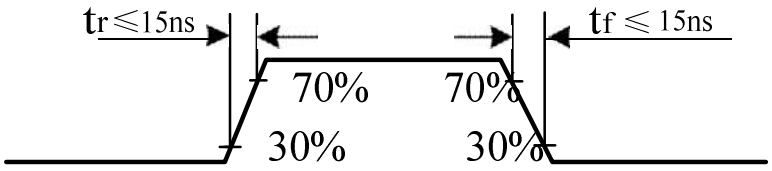
Table38.

Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	10	-	ns	
	tshw	SCL "H" Pulse Width (Write)	5	-	ns	
	tslw	SCL "L" Pulse Width (Write)	5	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	

	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	5	-	ns	
	tsdh	Data hold time (Write)	5	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	
CSX	tscc	SCL-CSX	10	-	ns	
	tchw	CSX "H" Pulse Width	10	-	ns	
	tcss	CSX-SCL Time	20	-	ns	
	tcsh		40	-	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCIB=2.5V to 3.3V, AGNDB=DGND=0V

Figure89.



7.3.4. Display Serial Interface Timing Characteristics (4-line SPI system)

Figure90.

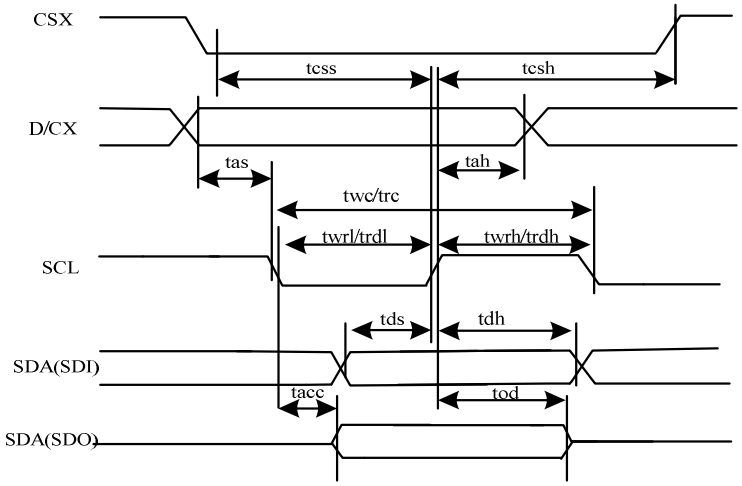


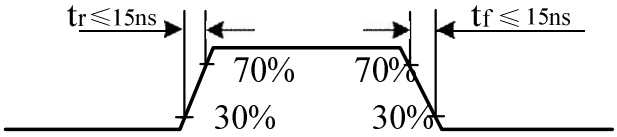
Table39.

Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	20	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	10	-	ns	
	twrh	SCL "H" Pulse Width (Write)	5	-	ns	
	twrl	SCL "L" Pulse Width (Write)	5	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	

	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	5	-	ns	
	tdh	Data hold time (Write)	5	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCIB=2.5V to 3.3V, AGNDB=DGND=0V

Figure91.



8. GENERATION REVISION HISTORY

REV.	EFFECTIVE DATE	DESCRIPTION OF CHANGES	PREPARED BY
1.0	2019-11-02	Frist Release	Dor
1.1	2020-05-14	Update pin name	Dor
1.2	2020-06-15	1. Update chip size 2. Update Pad location 3. Change AGNDR to DGND 4. Delete DDVDHDC	Dor