NV3022B Datasheet

A-Si TFT LCD Single Chip Driver
132RGBx162 Resolution and 262K color

Version 1.0
Jan 2019

Introduction

NV3022B is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 132RGBx162 dots, comprising a 396-channel source driver, a 162-channel gate driver, 48,114 bytes GRAM for graphic data of 132RGBx162 dots, and power supply circuit.

The NV3022B supports 18-/16-/9-/8-bit data bus interface and serial peripheral interfaces (SPI). It also supplies 18-bit, 16-bit or 6-bit RGB interface for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

NV3022B can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The NV3022B also supports a function to display in 8 colors idle mode, allowing for precise power control by software. So these features make the NV3022B an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP, on which long battery life is a major concern.

1. Features

- Display resolution options
  - 120(RGB) (H) X 160 (V)
  - 128(RGB) (H) X 128 (V)
  - 128(RGB) (H) X 160 (V)
  - 130(RGB) (H) X 130 (V)
  - 132(RGB) (H) X 132(V)
  - 132(RGB) (H) X 162 (V)
- LCD Driver Output Circuits
  - 396 source outputs
  - 162 gate outputs
  - Common electrode output
- AM-LCD driver with on-chip full display RAM: 34,749 bytes
- System Interfaces
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-series MCU
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 6800-series MCU
  - 6-bits, 16-bits, 18-bits RGB interface
  - 3-pin/4-pin serial interface
- Display color modes
  - Full color mode (idle mode off): 262K-colors
  - Reduced color modes (idle mode on): 8-colors
- On Chip Functions
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Line/frame inversion
  - Factory default value (Maker ID, Version ID, Module ID, etc) are stored on the display module

- Low–Power Consumption
  - Low operating power supplies
    - IOVCC = 1.65V ~ 3.6 V (interface I/O)
    - VCI = 2.5V ~ 4.8 V (analog)
- LCD Voltage Drive
  - Source/VCOM power supply voltage
    - AVDD – GND = 4.5V ~ 5.0V
    - VCL – GND = -1.0V ~ -3.0V
    - VCI1 － VCL ≦ 5.0V
  - Gate driver output voltage
    - VGH – GND = 10V ~ 16V
    - VGL – GND = -6V ~ -12V
    - VGH － VGL ≦ 30V
  - VCOM driver output voltage
    - VCOMH = 3.1725V ~ 4.41V
    - VCOML = -0.36V ~ -1.8225V
- Operate Temperature Range: -30℃ to 85℃

2. Pin Descriptions

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td colspan="3">Power Supply Pin</td></tr>
<tr><td>IOVCC</td><td>I</td><td>Power supply for interface logic circuits (1.65 ~ 3.6V)</td></tr>
<tr><td>VCI</td><td>I</td><td>Power supply for analog circuit.
Could connect to external power supply (VCI=2.5~4.8V).</td></tr>
<tr><td>VSSA</td><td>I</td><td>System Ground for Analog System and Booster Circuit.</td></tr>
<tr><td>VSS</td><td>I</td><td>System Ground for I/O System and Digital System.</td></tr>
<tr><td colspan="3">Interface Logic Pin</td></tr>
<tr><td>P68</td><td>I</td><td>8080/6800 MCU Interface Mode Selection
P68 = ‘1’ : Select 6800-MCU parallel interface
P68 = ‘0’ : Select 8080-MCU parallel interface
Note: If not used, please fix this pin at VSS level.</td></tr>
<tr><td>IM2
IM1
IM0</td><td>I</td><td>MCU Parallel interface bus and Serial interface select :
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>SPI4W</th><th>Interface Type</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>X</td><td>MCU 8-bit Parallel</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>X</td><td>MCU 16-bit Parallel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>X</td><td>MCU 9-bit Parallel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>X</td><td>MCU 18-bit Parallel</td></tr>
<tr><td>0</td><td>X</td><td>X</td><td>1</td><td>SPI 4 Wire Serial</td></tr>
<tr><td>0</td><td>X</td><td>X</td><td>0</td><td>SPI 3 Wire Serial</td></tr>
</table></td></tr>
<tr><td>SPI4W</td><td></td><td>SPI4W=’0’, 3-line SPI Enable.
SPI4W=’1’, 4-line SPI Enable.
If Not Used, Please fix this Pin at VSS Level.</td></tr>
<tr><td>RESX</td><td>I</td><td>Chip Reset Pin (“Low Active”)
Note: Keep this pin without glitch</td></tr>
<tr><td>CSX</td><td>I</td><td>Chip Select Pin (“Low Active”)
Pull down when chip accessable</td></tr>
<tr><td>DCX</td><td>I</td><td>Reuse Pin according parallel and serial interface:
➢ MCU Interface: Distinguish Data (‘1’) or Command (‘0’).
➢ SPI Interface: Used as ‘SCL’ clock pin.
If not used, please connect this pin to VSS.</td></tr>
<tr><td>RDX</td><td>I</td><td>➢ 8080-parallel interface: used as ‘Read’ enable.
➢ 6800-parallel interface:
1. when WRX=’0’ , RDX used as ‘write’ enable;
2. When WRX=’1’, RDX used as ‘Read’ enable.</td></tr>
<tr><td>WRX</td><td>I</td><td>➢ 8080-parallel interface, used as write enable.
➢ 6800-parallel interface, used to distinguish ‘write’ or ‘read’ operation.
➢ SPI 4-wire interface, used as D/CX.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>D[17:0]</td><td>I/O</td><td>➢ SPI without RGB interface : D[0] used as SDI/O, others don’t care;
➢ SPI with RGB interface : D[17:0] used as data bus;
➢ MCU interface : D[17:0] used as data bus;
Note : When RGB interface enable , SPI should use ‘SDA’ pin as SDI/O</td></tr>
<tr><td>TE</td><td>O</td><td>Tearing effect output pin to synchronize MCU to frame writing</td></tr>
<tr><td>TEST12/SDA</td><td>I/O</td><td>When RCM[1]=’1’,SDA is used for SPI write/read data line;
When RCM[0]=’0’,SDA is not used;</td></tr>
<tr><td>TEST8/PCLK</td><td>I</td><td>RGB interface pixel clock signal</td></tr>
<tr><td>TEST10/HS</td><td>I</td><td>RGB interface horizontal synchronization signal</td></tr>
<tr><td>TEST11/VS</td><td>I</td><td>RGB interface vertical synchronization signal</td></tr>
<tr><td>TEST9/DE</td><td>I</td><td>RGB interface data enable signal</td></tr>
<tr><td>OSC</td><td>O</td><td>OSC waveform output pin, for test purpose.</td></tr>
<tr><td colspan="3">Mode Selection Pin</td></tr>
<tr><td>GM2
GM1
GM0</td><td>I</td><td>Panel Resolution Selection Pins.
<table>
<tr><th>GM2</th><th>GM1</th><th>GM0</th><th>Descriptions</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>132RGBX162(S1~396 and G1~G162 output)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>128RGBX128(S7~390 and G2~G129 output)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>120RGBX160(S7~366 and G2~G161 output)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>128RGBX160(S7~390 and G2~G161 output)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>130RGBX130(S7~396 and G2~G131 output)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>132RGBX132(S1~396 and G2~G133 output)</td></tr>
</table></td></tr>
<tr><td>VPP</td><td>I</td><td>When writing NVM, it needs external power supply voltage (7.5V).</td></tr>
<tr><td colspan="3">Driver Output pins</td></tr>
<tr><td>S1~S396</td><td>O</td><td>Source driver output pins.</td></tr>
<tr><td>G1~G162</td><td>O</td><td>Gate driver output pins.</td></tr>
<tr><td>VDD</td><td>O</td><td>Test pin for internal digital logic Power supply</td></tr>
<tr><td>GVDD</td><td>O</td><td>A power supply for Grayscale Voltage Generator</td></tr>
<tr><td>DDVDH</td><td>O</td><td>A power supply pin for source driver block that is generated from power block. Output of booster 1 circuit (output of 2-times output of VCI).</td></tr>
<tr><td>VCL</td><td>O</td><td>A power supply pin for generating VCOML</td></tr>
<tr><td>VGH</td><td>O</td><td>Power supply for Gate Driver</td></tr>
<tr><td>VGL</td><td>O</td><td>Negative power supply for Gate Driver</td></tr>
<tr><td>VCOMH</td><td>O</td><td>The high level of VCOM AC voltage.</td></tr>
<tr><td>VCOML</td><td>O</td><td>The low level of VCOM AC voltage.</td></tr>
<tr><td>VCOM</td><td>O</td><td>TFT display common electrode power supply. Alternates between voltage levels between VCOMH-VCOML.
Registers set the alternating cycle for operating or halting VCOM.</td></tr>
<tr><td>TEST_C<3:0></td><td>O</td><td>Test pin, it is not accessible to user.must be open.</td></tr>
<tr><td>TESTOP[8:1]</td><td>O</td><td>Test pin, it is not accessible to user.must be open.</td></tr>
<tr><td>TEST1P</td><td>O</td><td>Test pin, it is not accessible to user.must be open.</td></tr>
<tr><td>TEST2P</td><td>O</td><td>Test pin, it is not accessible to user.must be open.</td></tr>
</table>

3. Bump Arrangement and Coordination

3.1. Bump Arrangement

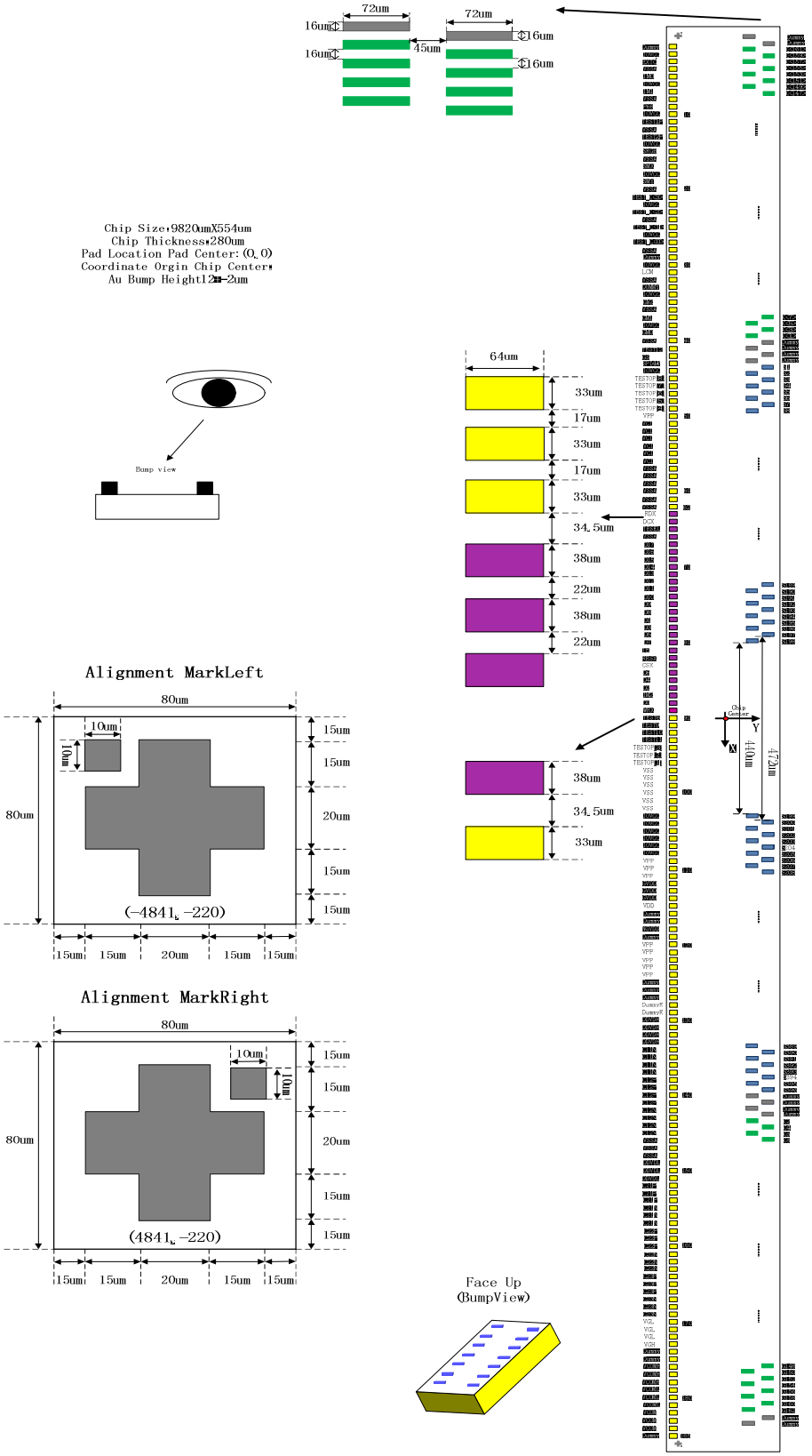


Figure 3-1 Pad Arrangement

3.2. Pin Connection

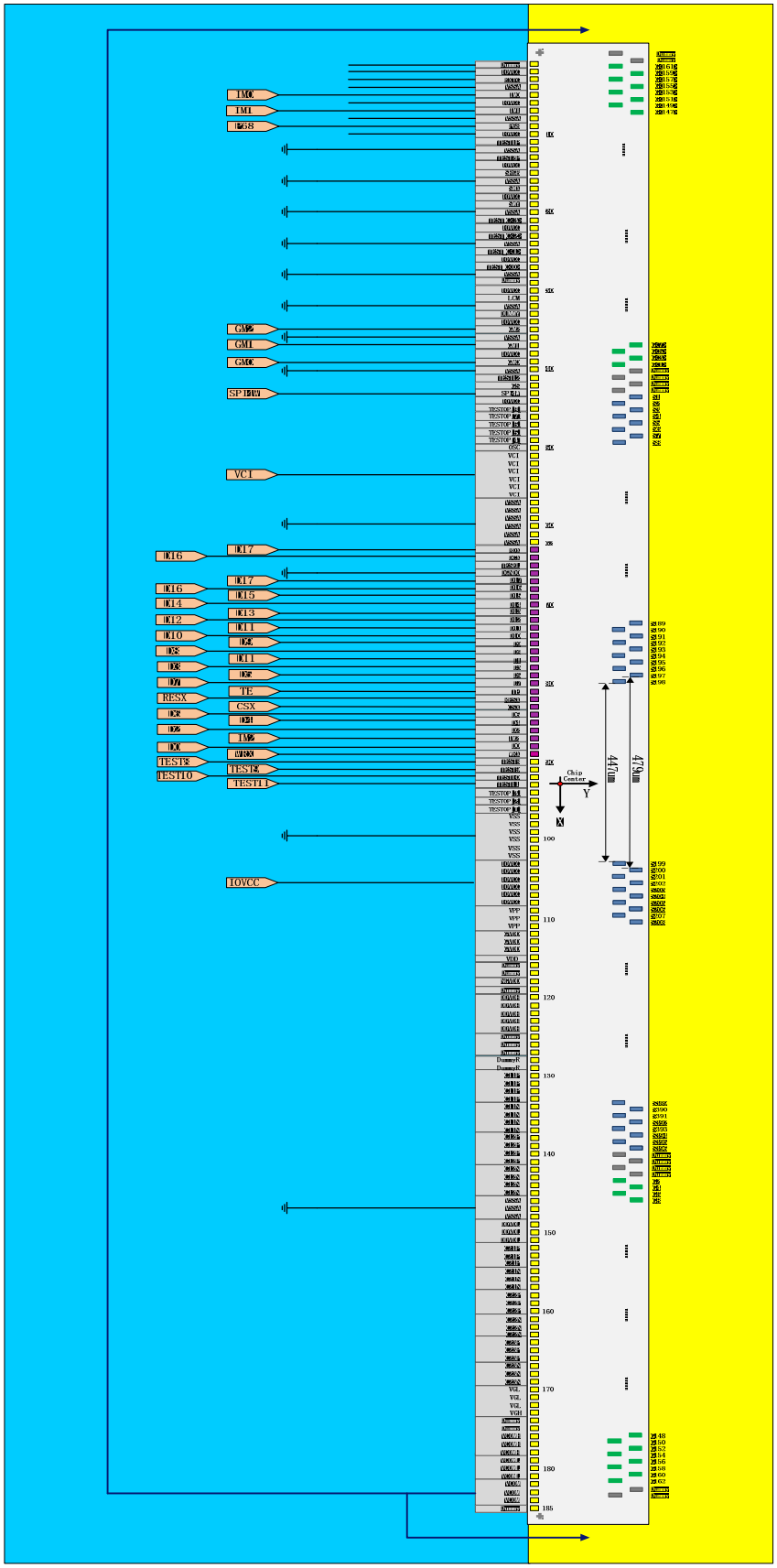


Figure 3-2 Pad Connection

3.3. Pad Coordination

No.	PAD Name	X	Y
1	Dummy	-4750	-231
2	IOVCC	-4700	-231
3	EXTC	-4650	-231
4	VSSA	-4600	-231
5	IM0	-4550	-231
6	IOVCC	-4500	-231
7	IM1	-4450	-231
8	VSSA	-4400	-231
9	P68	-4350	-231
10	IOVCC	-4300	-231
11	TEST1P	-4250	-231
12	VSSA	-4200	-231
13	TEST2P	-4150	-231
14	IOVCC	-4100	-231
15	SRGB	-4050	-231
16	VSSA	-4000	-231
17	SMX	-3950	-231
18	IOVCC	-3900	-231
19	SMY	-3850	-231
20	VSSA	-3800	-231
21	TEST_C<3>	-3750	-231
22	IOVCC	-3700	-231
23	TEST_C<2>	-3650	-231
24	VSSA	-3600	-231
25	TEST_C<1>	-3550	-231
26	IOVCC	-3500	-231
27	TEST_C<0>	-3450	-231
28	VSSA	-3400	-231
29	Dummy	-3350	-231
30	IOVCC	-3300	-231
31	LCM	-3250	-231
32	VSSA	-3200	-231
33	DUMMY	-3150	-231
34	IOVCC	-3100	-231
35	GM2	-3050	-231
36	VSSA	-3000	-231
37	GM1	-2950	-231
38	IOVCC	-2900	-231
39	GM0	-2850	-231
40	VSSA	-2800	-231
41	TEST12	-2750	-231
42	GS	-2700	-231
43	SPI4W	-2650	-231
44	IOVCC	-2600	-231
45	TESTOP[8]	-2550	-231
46	TESTOP[7]	-2500	-231
47	TESTOP[6]	-2450	-231
48	TESTOP[5]	-2400	-231
49	TESTOP[4]	-2350	-231
50	VPP	-2300	-231
51	VCI	-2250	-231
52	VCI	-2200	-231
53	VCI	-2150	-231
54	VCI	-2100	-231
55	VCI	-2050	-231
56	VCI	-2000	-231
57	VSSA	-1950	-231
58	VSSA	-1900	-231
59	VSSA	-1850	-231
60	VSSA	-1800	-231
61	VSSA	-1750	-231
62	VSSA	-1700	-231
63	RDX	-1630	-231
64	DCX	-1570	-231
65	TESEL	-1510	-231
66	VSSA	-1450	-231
67	D17	-1390	-231
68	D16	-1330	-231
69	D15	-1270	-231
70	D14	-1210	-231
71	D13	-1150	-231
72	D12	-1090	-231
73	D11	-1030	-231
74	D10	-970	-231
75	D9	-910	-231
76	D8	-850	-231
77	D1	-790	-231
78	D3	-730	-231
79	D5	-670	-231
80	D7	-610	-231
81	TE	-550	-231
82	RESX	-490	-231
83	CSX	-430	-231
84	D6	-370	-231
85	D4	-310	-231
86	D2	-250	-231
87	IM2	-190	-231
88	D0	-130	-231
89	WRX	-70	-231
90	TEST8	0	-231
91	TEST9	50	-231
92	TEST10	100	-231
93	TEST11	150	-231
94	TESTOP[3]	200	-231
95	TESTOP[2]	250	-231
96	TESTOP[1]	300	-231
97	VSS	350	-231
98	VSS	400	-231
99	VSS	450	-231
100	VSS	500	-231
101	VSS	550	-231
102	VSS	600	-231
103	IOVCC	650	-231
104	IOVCC	700	-231
105	IOVCC	750	-231
106	IOVCC	800	-231
107	IOVCC	850	-231
108	IOVCC	900	-231
109	VPP	950	-231
110	VPP	1000	-231
111	VPP	1050	-231
112	GVDD	1100	-231
113	GVDD	1150	-231
114	GVDD	1200	-231
115	VDD	1250	-231
116	Dummy	1300	-231
117	Dummy	1350	-231
118	NGVDD	1400	-231
119	Dummy	1450	-231
120	VPP	1500	-231
121	VPP	1550	-231
122	VPP	1600	-231
123	VPP	1650	-231
124	VPP	1700	-231
125	Dummy	1750	-231
126	Dummy	1800	-231
127	Dummy	1850	-231
128	DummyR	1900	-231
129	DummyR	1950	-231
130	DDVDH	2000	-231
131	DDVDH	2050	-231
132	DDVDH	2100	-231
133	DDVDH	2150	-231
134	C11N	2200	-231
135	C11N	2250	-231
136	C11N	2300	-231
137	C11N	2350	-231
138	C12P	2400	-231

No.	PAD Name	X	Y
139	C12P	2450	-231
140	C12P	2500	-231
141	C12P	2550	-231
142	C12N	2600	-231
143	C12N	2650	-231
144	C12N	2700	-231
145	C12N	2750	-231
146	VSSA	2800	-231
147	VSSA	2850	-231
148	VSSA	2900	-231
149	DDVDL	2950	-231
150	DDVDL	3000	-231
151	DDVDL	3050	-231
152	C21P	3100	-231
153	C21P	3150	-231
154	C21P	3200	-231
155	C21N	3250	-231
156	C21N	3300	-231
157	C21N	3350	-231
158	C22P	3400	-231
159	C22P	3450	-231
160	C22P	3500	-231
161	C22N	3550	-231
162	C22N	3600	-231
163	C22N	3650	-231
164	C23P	3700	-231
165	C23P	3750	-231
166	C23P	3800	-231
167	C23N	3850	-231
168	C23N	3900	-231
169	C23N	3950	-231
170	VGL	4000	-231
171	VGL	4050	-231
172	VGL	4100	-231
173	VGH	4150	-231
174	Dummy	4200	-231
175	Dummy	4250	-231
176	VCOMH	4300	-231
177	VCOMH	4350	-231
178	VCOMH	4400	-231
179	VCOML	4450	-231
180	VCOML	4500	-231
181	VCOML	4550	-231
182	VCOM	4600	-231
183	VCOM	4650	-231
184	VCOM	4700	-231
185	Dummy	4750	-231
186	Dummy	4772	110

No.	PAD Name	X	Y
187	Dummy	4756	227
188	G162	4740	110
189	G160	4724	227
190	G158	4708	110
191	G156	4692	227
192	G154	4676	110
193	G152	4660	227
194	G150	4644	110
195	G148	4628	227
196	G146	4612	110
197	G144	4596	227
198	G142	4580	110
199	G140	4564	227
200	G138	4548	110
201	G136	4532	227
202	G134	4516	110
203	G132	4500	227
204	G130	4484	110
205	G128	4468	227
206	G126	4452	110
207	G124	4436	227
208	G122	4420	110
209	G120	4404	227
210	G118	4388	110
211	G116	4372	227
212	G114	4356	110
213	G112	4340	227
214	G110	4324	110
215	G108	4308	227
216	G106	4292	110
217	G104	4276	227
218	G102	4260	110
219	G100	4244	227
220	G98	4228	110
221	G96	4212	227
222	G94	4196	110
223	G92	4180	227
224	G90	4164	110
225	G88	4148	227
226	G86	4132	110
227	G84	4116	227
228	G82	4100	110
229	G80	4084	227
230	G78	4068	110
231	G76	4052	227
232	G74	4036	110
233	G72	4020	227
234	G70	4004	110

No.	PAD Name	X	Y
235	G68	3988	227
236	G66	3972	110
237	G64	3956	227
238	G62	3940	110
239	G60	3924	227
240	G58	3908	110
241	G56	3892	227
242	G54	3876	110
243	G52	3860	227
244	G50	3844	110
245	G48	3828	227
246	G46	3812	110
247	G44	3796	227
248	G42	3780	110
249	G40	3764	227
250	G38	3748	110
251	G36	3732	227
252	G34	3716	110
253	G32	3700	227
254	G30	3684	110
255	G28	3668	227
256	G26	3652	110
257	G24	3636	227
258	G22	3620	110
259	G20	3604	227
260	G18	3588	110
261	G16	3572	227
262	G14	3556	110
263	G12	3540	227
264	G10	3524	110
265	G8	3508	227
266	G6	3492	110
267	G4	3476	227
268	G2	3460	110
269	Dummy	3444	227
270	Dummy	3428	110
271	Dummy	3412	227
272	Dummy	3396	110
273	S396	3380	227
274	S395	3364	110
275	S394	3348	227
276	S393	3332	110
277	S392	3316	227
278	S391	3300	110
279	S390	3284	227
280	S389	3268	110
281	S388	3252	227
282	S387	3236	110

No.	PAD Name	X	Y
283	S386	3220	227
284	S385	3204	110
285	S384	3188	227
286	S383	3172	110
287	S382	3156	227
288	S381	3140	110
289	S380	3124	227
290	S379	3108	110
291	S378	3092	227
292	S377	3076	110
293	S376	3060	227
294	S375	3044	110
295	S374	3028	227
296	S373	3012	110
297	S372	2996	227
298	S371	2980	110
299	S370	2964	227
300	S369	2948	110
301	S368	2932	227
302	S367	2916	110
303	S366	2900	227
304	S365	2884	110
305	S364	2868	227
306	S363	2852	110
307	S362	2836	227
308	S361	2820	110
309	S360	2804	227
310	S359	2788	110
311	S358	2772	227
312	S357	2756	110
313	S356	2740	227
314	S355	2724	110
315	S354	2708	227
316	S353	2692	110
317	S352	2676	227
318	S351	2660	110
319	S350	2644	227
320	S349	2628	110
321	S348	2612	227
322	S347	2596	110
323	S346	2580	227
324	S345	2564	110
325	S344	2548	227
326	S343	2532	110
327	S342	2516	227
328	S341	2500	110
329	S340	2484	227
330	S339	2468	110

No.	PAD Name	X	Y
331	S338	2452	227
332	S337	2436	110
333	S336	2420	227
334	S335	2404	110
335	S334	2388	227
336	S333	2372	110
337	S332	2356	227
338	S331	2340	110
339	S330	2324	227
340	S329	2308	110
341	S328	2292	227
342	S327	2276	110
343	S326	2260	227
344	S325	2244	110
345	S324	2228	227
346	S323	2212	110
347	S322	2196	227
348	S321	2180	110
349	S320	2164	227
350	S319	2148	110
351	S318	2132	227
352	S317	2116	110
353	S316	2100	227
354	S315	2084	110
355	S314	2068	227
356	S313	2052	110
357	S312	2036	227
358	S311	2020	110
359	S310	2004	227
360	S309	1988	110
361	S308	1972	227
362	S307	1956	110
363	S306	1940	227
364	S305	1924	110
365	S304	1908	227
366	S303	1892	110
367	S302	1876	227
368	S301	1860	110
369	S300	1844	227
370	S299	1828	110
371	S298	1812	227
372	S297	1796	110
373	S296	1780	227
374	S295	1764	110
375	S294	1748	227
376	S293	1732	110
377	S292	1716	227
378	S291	1700	110

No.	PAD Name	X	Y
379	S290	1684	227
380	S289	1668	110
381	S288	1652	227
382	S287	1636	110
383	S286	1620	227
384	S285	1604	110
385	S284	1588	227
386	S283	1572	110
387	S282	1556	227
388	S281	1540	110
389	S280	1524	227
390	S279	1508	110
391	S278	1492	227
392	S277	1476	110
393	S276	1460	227
394	S275	1444	110
395	S274	1428	227
396	S273	1412	110
397	S272	1396	227
398	S271	1380	110
399	S270	1364	227
400	S269	1348	110
401	S268	1332	227
402	S267	1316	110
403	S266	1300	227
404	S265	1284	110
405	S264	1268	227
406	S263	1252	110
407	S262	1236	227
408	S261	1220	110
409	S260	1204	227
410	S259	1188	110
411	S258	1172	227
412	S257	1156	110
413	S256	1140	227
414	S255	1124	110
415	S254	1108	227
416	S253	1092	110
417	S252	1076	227
418	S251	1060	110
419	S250	1044	227
420	S249	1028	110
421	S248	1012	227
422	S247	996	110
423	S246	980	227
424	S245	964	110
425	S244	948	227
426	S243	932	110

No.	PAD Name	X	Y
427	S242	916	227
428	S241	900	110
429	S240	884	227
430	S239	868	110
431	S238	852	227
432	S237	836	110
433	S236	820	227
434	S235	804	110
435	S234	788	227
436	S233	772	110
437	S232	756	227
438	S231	740	110
439	S230	724	227
440	S229	708	110
441	S228	692	227
442	S227	676	110
443	S226	660	227
444	S225	644	110
445	S224	628	227
446	S223	612	110
447	S222	596	227
448	S221	580	110
449	S220	564	227
450	S219	548	110
451	S218	532	227
452	S217	516	110
453	S216	500	227
454	S215	484	110
455	S214	468	227
456	S213	452	110
457	S212	436	227
458	S211	420	110
459	S210	404	227
460	S209	388	110
461	S208	372	227
462	S207	356	110
463	S206	340	227
464	S205	324	110
465	S204	308	227
466	S203	292	110
467	S202	276	227
468	S201	260	110
469	S200	244	227
470	S199	228	110
471	S198	-228	110
472	S197	-244	227
473	S196	-260	110
474	S195	-276	227
475	S194	-292	110
476	S193	-308	227
477	S192	-324	110
478	S191	-340	227
479	S190	-356	110
480	S189	-372	227
481	S188	-388	110
482	S187	-404	227
483	S186	-420	110
484	S185	-436	227
485	S184	-452	110
486	S183	-468	227
487	S182	-484	110
488	S181	-500	227
489	S180	-516	110
490	S179	-532	227
491	S178	-548	110
492	S177	-564	227
493	S176	-580	110
494	S175	-596	227
495	S174	-612	110
496	S173	-628	227
497	S172	-644	110
498	S171	-660	227
499	S170	-676	110
500	S169	-692	227
501	S168	-708	110
502	S167	-724	227
503	S166	-740	110
504	S165	-756	227
505	S164	-772	110
506	S163	-788	227
507	S162	-804	110
508	S161	-820	227
509	S160	-836	110
510	S159	-852	227
511	S158	-868	110
512	S157	-884	227
513	S156	-900	110
514	S155	-916	227
515	S154	-932	110
516	S153	-948	227
517	S152	-964	110
518	S151	-980	227
519	S150	-996	110
520	S149	-1012	227
521	S148	-1028	110
522	S147	-1044	227
523	S146	-1060	110
524	S145	-1076	227
525	S144	-1092	110
526	S143	-1108	227
527	S142	-1124	110
528	S141	-1140	227
529	S140	-1156	110
530	S139	-1172	227
531	S138	-1188	110
532	S137	-1204	227
533	S136	-1220	110
534	S135	-1236	227
535	S134	-1252	110
536	S133	-1268	227
537	S132	-1284	110
538	S131	-1300	227
539	S130	-1316	110
540	S129	-1332	227
541	S128	-1348	110
542	S127	-1364	227
543	S126	-1380	110
544	S125	-1396	227
545	S124	-1412	110
546	S123	-1428	227
547	S122	-1444	110
548	S121	-1460	227
549	S120	-1476	110
550	S119	-1492	227
551	S118	-1508	110
552	S117	-1524	227
553	S116	-1540	110
554	S115	-1556	227
555	S114	-1572	110
556	S113	-1588	227
557	S112	-1604	110
558	S111	-1620	227
559	S110	-1636	110
560	S109	-1652	227
561	S108	-1668	110
562	S107	-1684	227
563	S106	-1700	110
564	S105	-1716	227
565	S104	-1732	110
566	S103	-1748	227
567	S102	-1764	110
568	S101	-1780	227
569	S100	-1796	110
570	S99	-1812	227

No.	PAD Name	X	Y
571	S98	-1828	110
572	S97	-1844	227
573	S96	-1860	110
574	S95	-1876	227
575	S94	-1892	110
576	S93	-1908	227
577	S92	-1924	110
578	S91	-1940	227
579	S90	-1956	110
580	S89	-1972	227
581	S88	-1988	110
582	S87	-2004	227
583	S86	-2020	110
584	S85	-2036	227
585	S84	-2052	110
586	S83	-2068	227
587	S82	-2084	110
588	S81	-2100	227
589	S80	-2116	110
590	S79	-2132	227
591	S78	-2148	110
592	S77	-2164	227
593	S76	-2180	110
594	S75	-2196	227
595	S74	-2212	110
596	S73	-2228	227
597	S72	-2244	110
598	S71	-2260	227
599	S70	-2276	110
600	S69	-2292	227
601	S68	-2308	110
602	S67	-2324	227
603	S66	-2340	110
604	S65	-2356	227
605	S64	-2372	110
606	S63	-2388	227
607	S62	-2404	110
608	S61	-2420	227
609	S60	-2436	110
610	S59	-2452	227
611	S58	-2468	110
612	S57	-2484	227
613	S56	-2500	110
614	S55	-2516	227
615	S54	-2532	110
616	S53	-2548	227
617	S52	-2564	110
618	S51	-2580	227

No.	PAD Name	X	Y
619	S50	-2596	110
620	S49	-2612	227
621	S48	-2628	110
622	S47	-2644	227
623	S46	-2660	110
624	S45	-2676	227
625	S44	-2692	110
626	S43	-2708	227
627	S42	-2724	110
628	S41	-2740	227
629	S40	-2756	110
630	S39	-2772	227
631	S38	-2788	110
632	S37	-2804	227
633	S36	-2820	110
634	S35	-2836	227
635	S34	-2852	110
636	S33	-2868	227
637	S32	-2884	110
638	S31	-2900	227
639	S30	-2916	110
640	S29	-2932	227
641	S28	-2948	110
642	S27	-2964	227
643	S26	-2980	110
644	S25	-2996	227
645	S24	-3012	110
646	S23	-3028	227
647	S22	-3044	110
648	S21	-3060	227
649	S20	-3076	110
650	S19	-3092	227
651	S18	-3108	110
652	S17	-3124	227
653	S16	-3140	110
654	S15	-3156	227
655	S14	-3172	110
656	S13	-3188	227
657	S12	-3204	110
658	S11	-3220	227
659	S10	-3236	110
660	S9	-3252	227
661	S8	-3268	110
662	S7	-3284	227
663	S6	-3300	110
664	S5	-3316	227
665	S4	-3332	110
666	S3	-3348	227

No.	PAD Name	X	Y
667	S2	-3364	110
668	S1	-3380	227
669	Dummy	-3396	110
670	Dummy	-3412	227
671	Dummy	-3428	110
672	Dummy	-3444	227
673	G1	-3460	110
674	G3	-3476	227
675	G5	-3492	110
676	G7	-3508	227
677	G9	-3524	110
678	G11	-3540	227
679	G13	-3556	110
680	G15	-3572	227
681	G17	-3588	110
682	G19	-3604	227
683	G21	-3620	110
684	G23	-3636	227
685	G25	-3652	110
686	G27	-3668	227
687	G29	-3684	110
688	G31	-3700	227
689	G33	-3716	110
690	G35	-3732	227
691	G37	-3748	110
692	G39	-3764	227
693	G41	-3780	110
694	G43	-3796	227
695	G45	-3812	110
696	G47	-3828	227
697	G49	-3844	110
698	G51	-3860	227
699	G53	-3876	110
700	G55	-3892	227
701	G57	-3908	110
702	G59	-3924	227
703	G61	-3940	110
704	G63	-3956	227
705	G65	-3972	110
706	G67	-3988	227
707	G69	-4004	110
708	G71	-4020	227
709	G73	-4036	110
710	G75	-4052	227
711	G77	-4068	110
712	G79	-4084	227
713	G81	-4100	110
714	G83	-4116	227

No.	PAD Name	X	Y
715	G85	-4132	110
716	G87	-4148	227
717	G89	-4164	110
718	G91	-4180	227
719	G93	-4196	110
720	G95	-4212	227
721	G97	-4228	110
722	G99	-4244	227
723	G101	-4260	110
724	G103	-4276	227
725	G105	-4292	110
726	G107	-4308	227
727	G109	-4324	110
728	G111	-4340	227

No.	PAD Name	X	Y
729	G113	-4356	110
730	G115	-4372	227
731	G117	-4388	110
732	G119	-4404	227
733	G121	-4420	110
734	G123	-4436	227
735	G125	-4452	110
736	G127	-4468	227
737	G129	-4484	110
738	G131	-4500	227
739	G133	-4516	110
740	G135	-4532	227
741	G137	-4548	110
742	G139	-4564	227

No.	PAD Name	X	Y
743	G141	-4580	110
744	G143	-4596	227
745	G145	-4612	110
746	G147	-4628	227
747	G149	-4644	110
748	G151	-4660	227
749	G153	-4676	110
750	G155	-4692	227
751	G157	-4708	110
752	G159	-4724	227
753	G161	-4740	110
754	Dummy	-4756	227
755	Dummy	-4772	110

4. Interface Description

4.1. Interface Type Selection

The selection of a given interfaces are done by setting P68, IM2, IM1, and IM0 pins as show in below tables.

Table 4-1 Interface Type Selection

P68	IM2	IM1	IM0	Interface	Read Back Selection
X	0	X	X	Serial interface	Via the read instruction (8-bit , 24-bit and 32-bit read parameter)
0	1	0	0	8080 MCU 8-bit Parallel	RDX strobe (8-bit read data and 8-bit read parameter)
0	1	0	1	8080 MCU 16-bit Parallel	RDX strobe (16-bit read data and 8-bit read parameter)
0	1	1	0	8080 MCU 9-bit Parallel	RDX strobe (9-bit read data and 8-bit read parameter)
0	1	1	1	8080 MCU 18-bit Parallel	RDX strobe (18-bit read data and 8-bit read parameter)
1	1	0	0	6800 MCU 8-bit Parallel	RDX strobe (8-bit read data and 8-bit read parameter)
1	1	0	1	6800 MCU 16-bit Parallel	RDX strobe (9-bit read data and 8-bit read parameter)
1	1	1	0	6800 MCU 9-bit Parallel	RDX strobe (16-bit read data and 8-bit read parameter)
1	1	1	1	6800 MCU 18-bit Parallel	RDX strobe (18-bit read data and 8-bit read parameter)

4.2. Serial Interface

The Module uses a 3-wire 9-bit serial interface or 4-pins/8-bit bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pins serial use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output) and the 4-pins serial use: CSX (chip enable), D/CX (data/ command select), SCL (serial clock), and SDA (serial data input/output).

Table 4-2 Serial Interface Type Selection

IM2	4WSPI	Interface	Read back selection
0	0	3-Pins Serial Interface	Via the read instruction (8-bit , 24-bit and 32-bit read parameter)
0	1	4-Pins Serial Interface	Via the read instruction (8-bit , 24-bit and 32-bit read parameter)

4.2.1 Command/Data Write

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-pins serial data packet contains a control bit D/CX and a transmission byte, but in 4-pins serial case, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any orders to the Driver. The MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicated the start of data transmission.

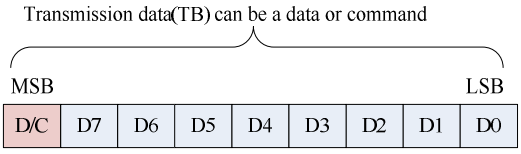


Figure 4-2-1-1 SPI 3-Wire Write Data Format

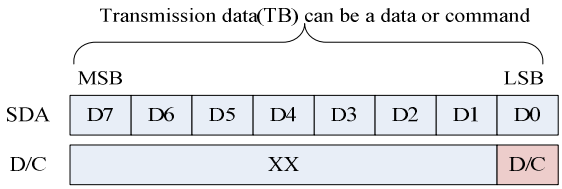


Figure 4-2-1-2 SPI 4-Wire Write Data Format

When CSX is “high”, SCL clock is ignored. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of SCL. D/CX indicates, whether the byte is command code (D/CX=’0’) or parameter/RAM data (D/CX=’1’). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-pin serial interface) or D7 (4-pins serial interface) of the next byte at the next rising edge of SCL.

4.2.2 Command/Data Read

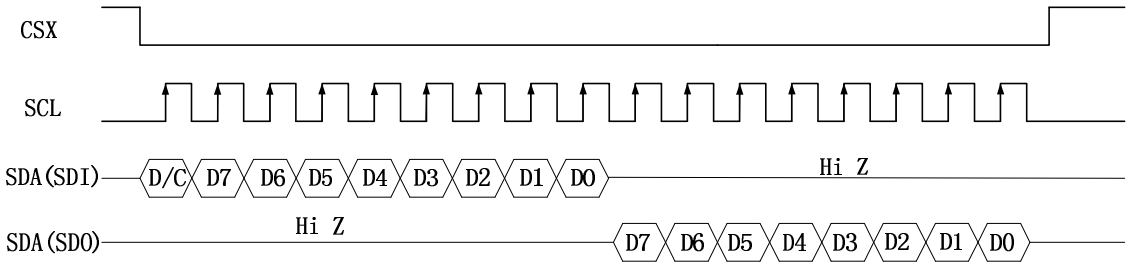


Figure 4-2-2-1 SPI 3-Wire 8-bit Read Operation
(For 'DAH/DBH/DCH/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh' Command)

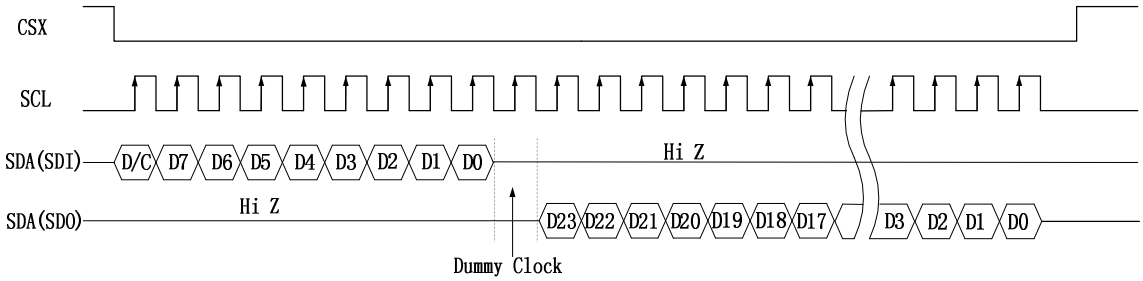


Figure 4-2-2-2 SPI 3-Wire 24-bit Read Operation
(For '04H' Command with one dummy clock)

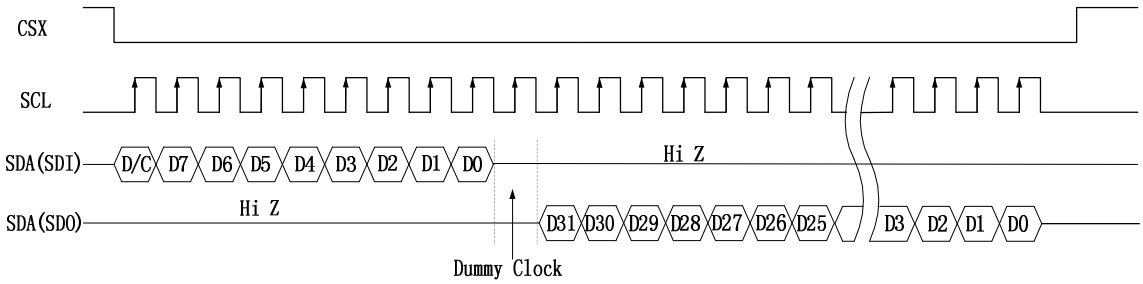


Figure 4-2-2-3 SPI 3-Wire 32-bit Read Operation
(For '09H' Command with one dummy clock)

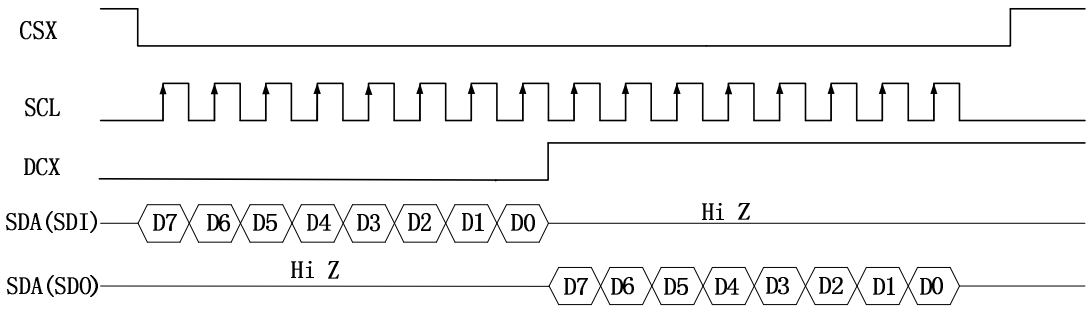


Figure 4-2-2-4 SPI 4-Wire 8-bit Read Operation
(For 'DAH/DBH/DCH/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh' Command)

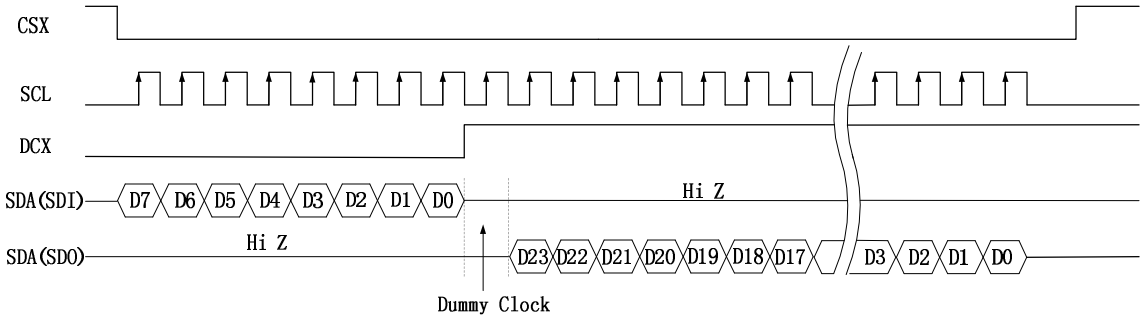


Figure 4-2-2-5 SPI 4-Wire 24-bit Read Operation
(For '04H' Command with one dummy clock)

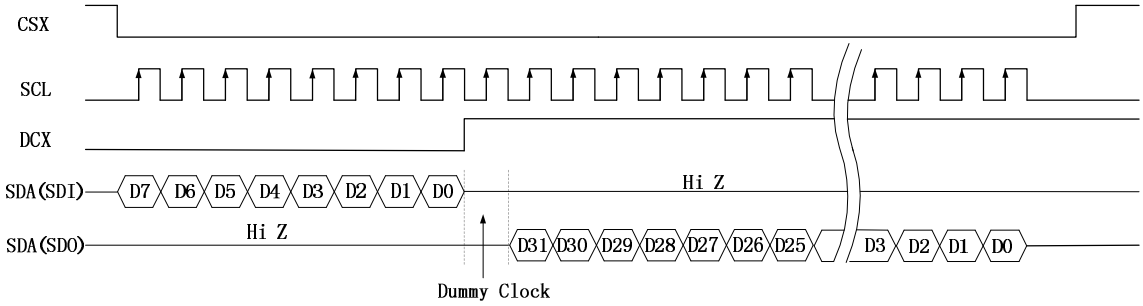


Figure 4-2-2-6 SPI 4-Wire 32-bit Read Operation
(For '09H' Command with one dummy clock)

4.3. 8080-Series Parallel Interface (P68='0')

The MCU uses an 11-wires 8-data parallel interface or 12-wires 9-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX (active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.

The graphics controller chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.

The 8080-series bi-direction interface can be used for communication between the micro- controller and LCD driver chip. The selection of this interface is done when P68 pin is low state (GND). Interface bus width can be selected with IM2, IM1 and IM0. The interface functions of 8080-series parallel interface are given in Table 4-3-1.

Table 4-3-1 8080 MCU Operation

P68	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
0	1	0	0	8-bit parallel	L	H	R	Write 8-bit command
					H	H	R	Write 8-bit display data or 8-bit parameter
					H	R	H	Read 8-bit display data or 8-bit parameter
0	1	0	1	16-bit parallel	L	H	R	Write 8-bit command
					H	H	R	Write 16-bit display data or 8-bit parameter
					H	R	H	Read 16-bit display data or 8-bit parameter
0	1	1	0	9-bit parallel	L	H	R	Write 8-bit command
					H	H	R	Write 9-bit display data or 8-bit parameter
					H	R	H	Read 9-bit display data or 8-bit parameter
0	1	1	1	18-bit parallel	L	H	R	Write 8-bit command
					H	H	R	Write 18-bit display data or 8-bit parameter
					H	R	H	Read 18-bit display data or 8-bit parameter

Note: Reading operation applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

4.3.1. Write Cycle/Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[17…0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (= ‘0’) and vice versa it is data (= ‘1’). The write cycle is described in the following figure.

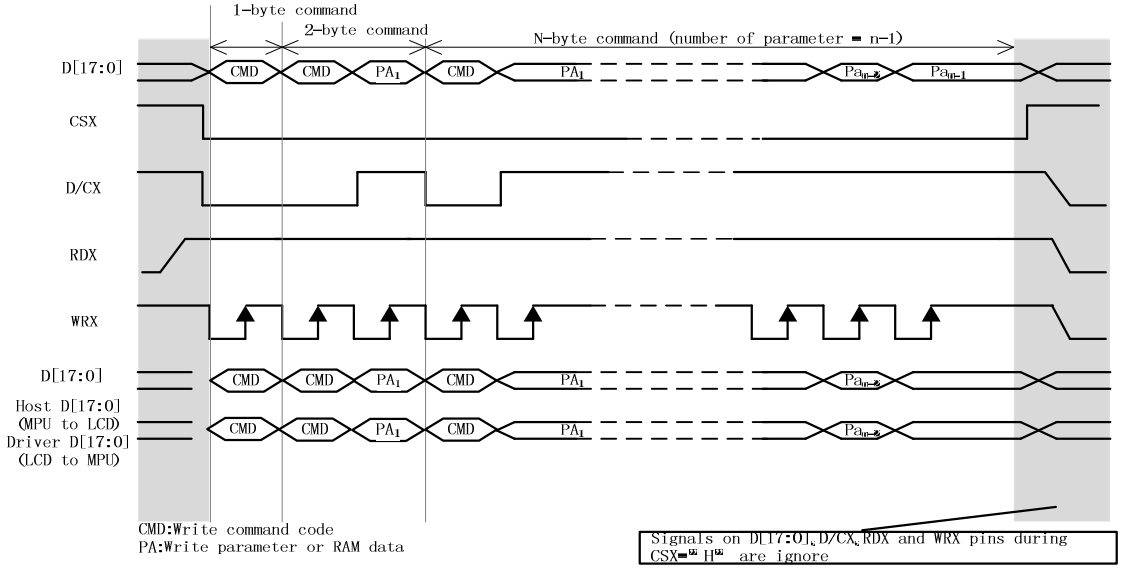


Figure 4-3-1 8080 MCU Write sequence

4.3.2. Read Cycle/Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from the display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

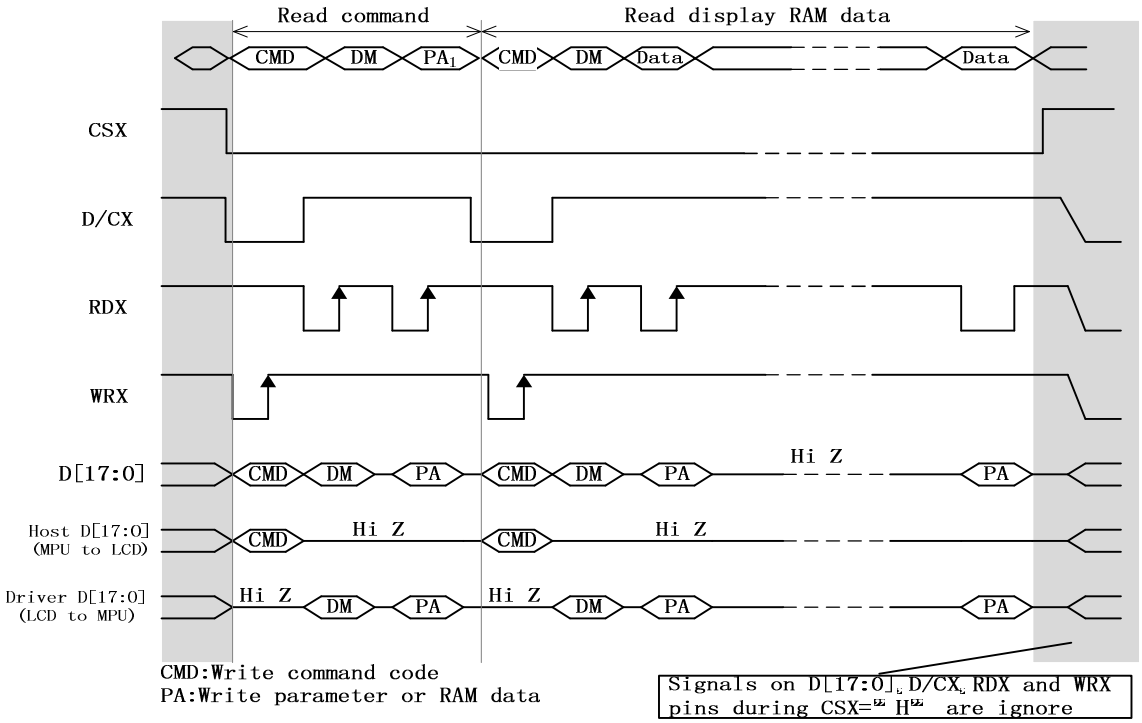


Figure 4-3-2 8080 Read sequence

4.4. 6800-Series Parallel Interface (P68='1')

The MCU uses a 11-wires 8-data parallel interface or 12-wires 9-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX (active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is read/write flag, RDX is the parallel data read/write enable and D[17:0] is parallel data.

The Graphics Controller Chip reads the data at the falling edge of RDX signal when WRX = '1' and writes the data at the falling of the RDX signal when R/WX='0'. The D/CX is the data or command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.

The 6800-series bi-direction interface can be used for communication between the micro- controller and LCD driver chip. The selection of this interface is done when P68 pin is high state (IOVCC). Interface bus width can be selected with IM2, IM1 and IM0. The interface functions of 6800-series parallel interface are given in Table 4-4-1.

Table 4-4-1 6800 MCU Operation

P68	IM2	IM1	IM0	Interface	D/CX	WRX	RDX	Function
1	1	0	0	8-bit parallel	L	L	F	Write 8-bit command
					H	L	F	Write 8-bit display data or 8-bit parameter
					H	H	F	Read 8-bit display data or 8-bit parameter
1	1	0	1	16-bit parallel	L	L	F	Write 8-bit command
					H	L	F	Write 16-bit display data or 8-bit parameter
					H	H	F	Read 16-bit display data or 8-bit parameter
1	1	1	0	9-bit parallel	L	L	F	Write 8-bit command
					H	L	F	Write 9-bit display data or 8-bit parameter
					H	H	F	Read 9-bit display data or 8-bit parameter
1	1	1	1	18-bit parallel	L	L	F	Write 8-bit command
					H	L	F	Write 18-bit display data or 8-bit parameter
					H	H	F	Read 18-bit display data or 8-bit parameter

Note: Reading operation applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

4.4.1. Write Cycle Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle consists of 3 control (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (D/CX= ‘0’), vice versa, it is data (D/CX= ‘1’).WRX work as write or read flag, WRX=’0’ stands for write operation, WRX=’1’ means read operation.The detail write cycle is described in the Figure 4-4-1.

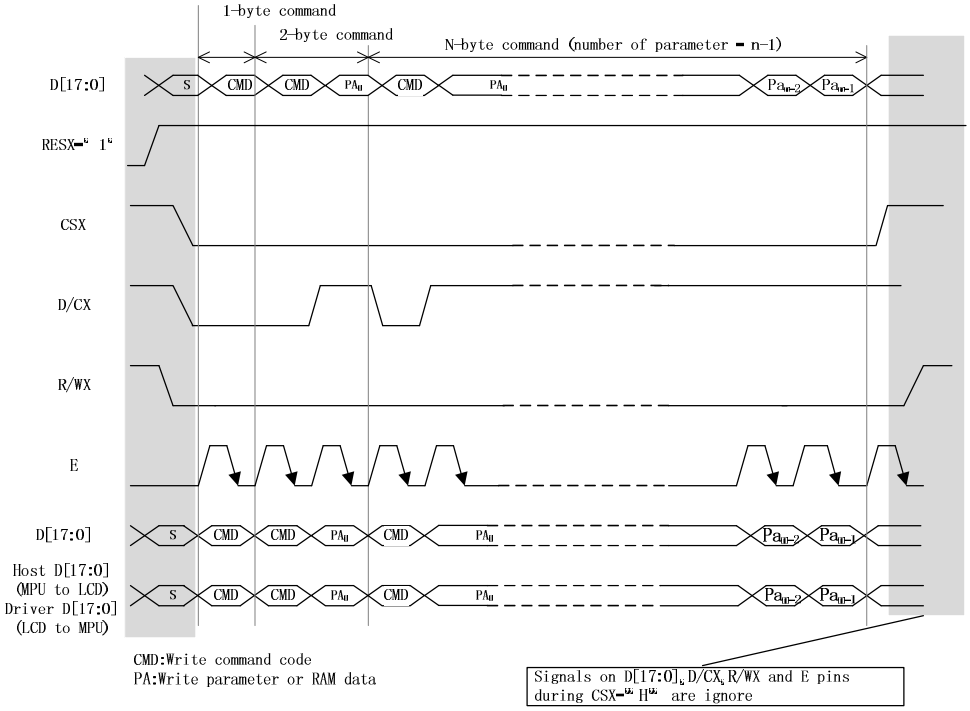


Figure 4-4-1 6800 Write Sequence

4.4.2. Read Cycle Sequence

The read cycle means that the host reads information (commend or/and data) to the display via the interface. Each read cycle consists of 3 control (D/CX, WRX, RDX) and data (D[17:0]). D/CX bit is control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low and vice versa it is data .WRX work as write or read flag,WRX='0' stands for write operation,WRX='1' means read operation.The detail read cycle is described in the figure Figure 4-4-2.

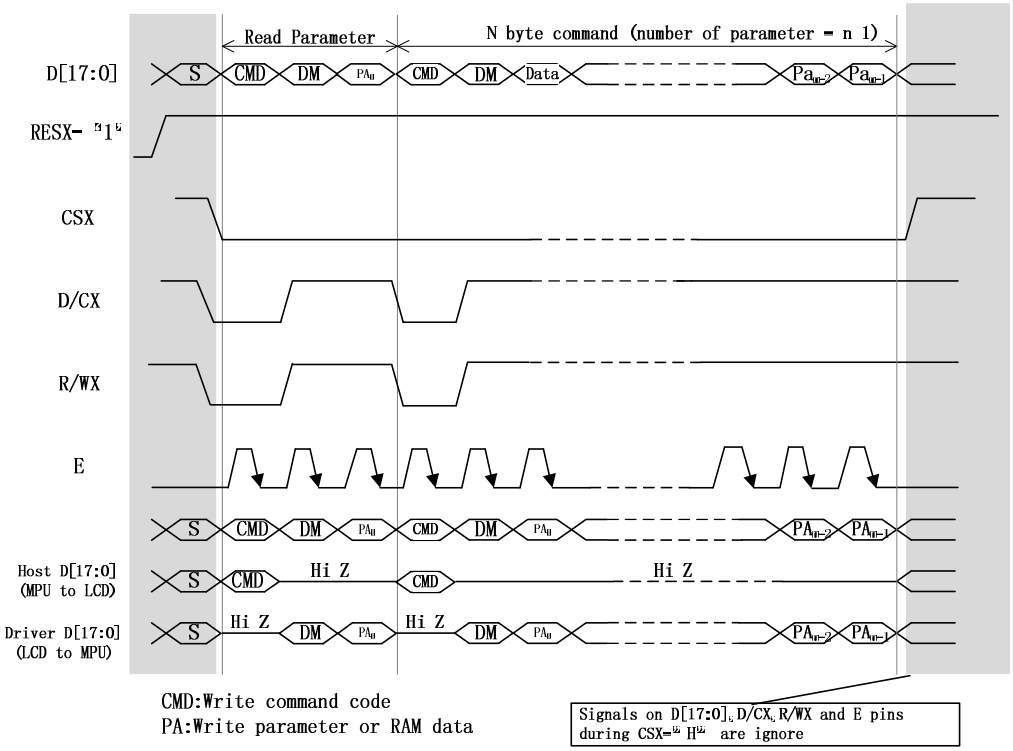


Figure 4-4-2 6800 Read Sequence

4.5. Serial Interface Recovery Function

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then Driver will reject the previous bits and should reset the interface that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example.

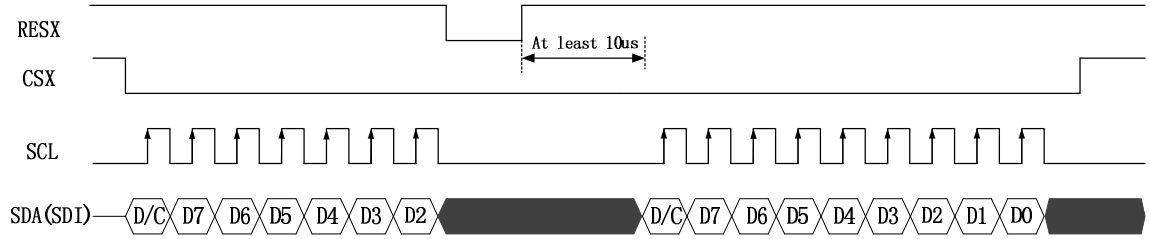


Figure 4-5-1 Serial interface recovery

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, Then the Driver will reject the previous bits and should reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example.

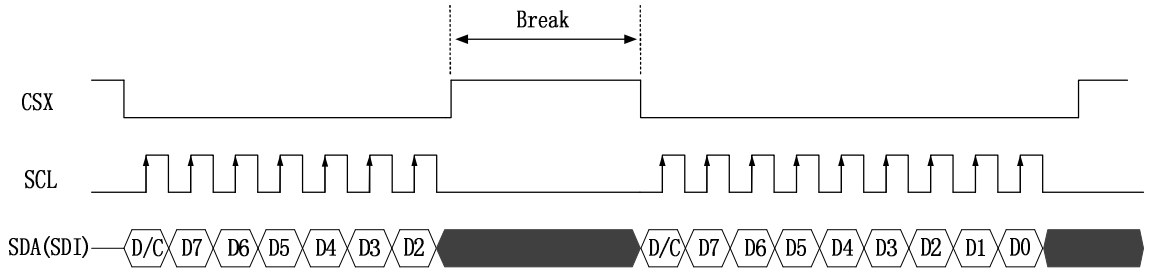


Figure 4-5-2 Serial interface recovery2

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as show below.

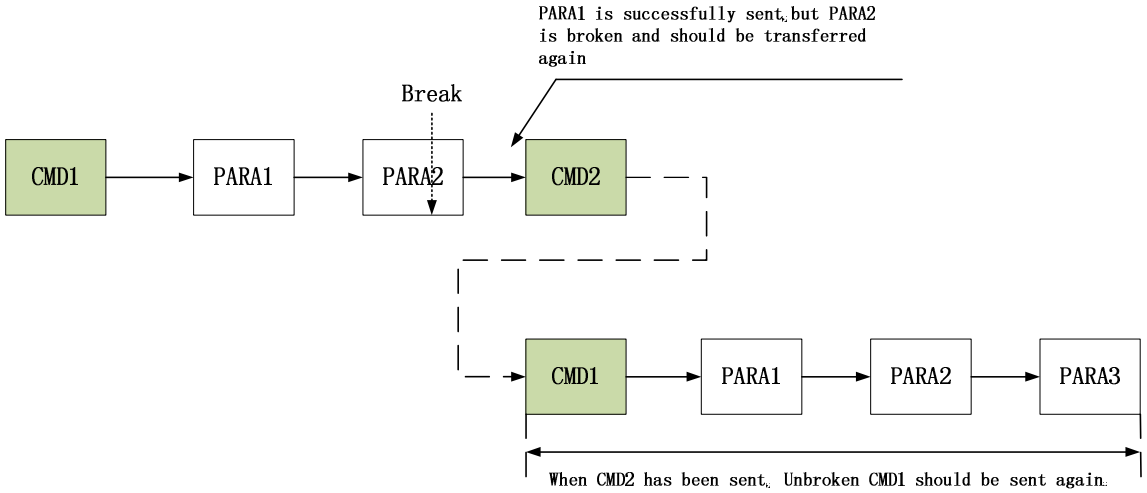


Figure 4-5-3 Serial interface recovery3

4.6. Display Data Transmission Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the Display Module will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below:

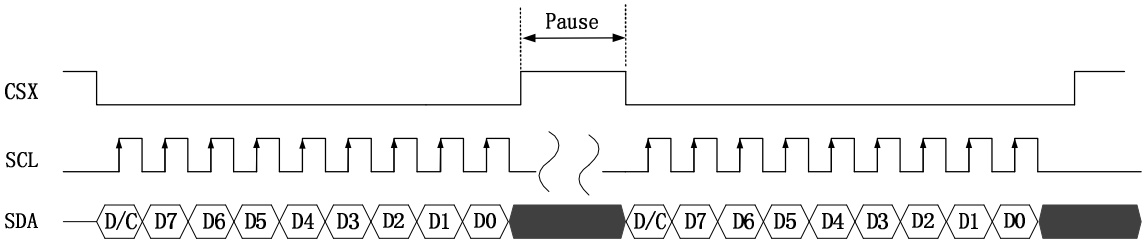


Figure 4-6 Serial interface recovery3

4.7. Display Data Transfer Mode

The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

Method1:

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

Start Frame Write	Image Data Frame1	Image Data Frame2	Image Data Frame3

Method2:

After image data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloading.

Start Frame Write	Image Data Frame1	Any Command	Start Frame Write	Image Data Frame2	Any Command	. . .	Any Command

4.8. RGB Interface

4.8.1. RGB Interface Selection

The RGB interface mode is available for NV3022B and the interface is selected by setting the VIPF[3:0] bits as following table.

Table 4-8-1 RGB Interface Selection

VIPF[3:0]				RGB Interface	Data Bus
0	1	1	0	18-bit RGB interface	D[17:0]
0	1	0	1	16-bit RGB interface	D[17:13],D[11:1]
1	1	1	0	6-bit RGB interface	D[7:2]
Others				Setting prohibited	

The display operation via RGB interface is synchronized with the VS, HS and PCLK signals. The RGB interface transfers the updated data to GRAM and the update area is defined by the window address function. The back porch and back porch are used to set the RGB interface timing.

- 18-bit data bus interface (D[17:0] is used) , VIPF[3:0] = 0110

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

- 16-bit data bus interface (D[17:13] and D[11:1] are used) , VIPF[3:0] = 0101

D17	D16	D15	D14	D13	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

- 6-bit data bus interface (D[7:2] is used) , VIPF[3] = 1110

First Transmission						Second Transmission						Third Transmission					
D7	D6	D5	D4	D3	D2	D7	D6	D5	D4	D3	D2	D7	D6	D5	D4	D3	D2
R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

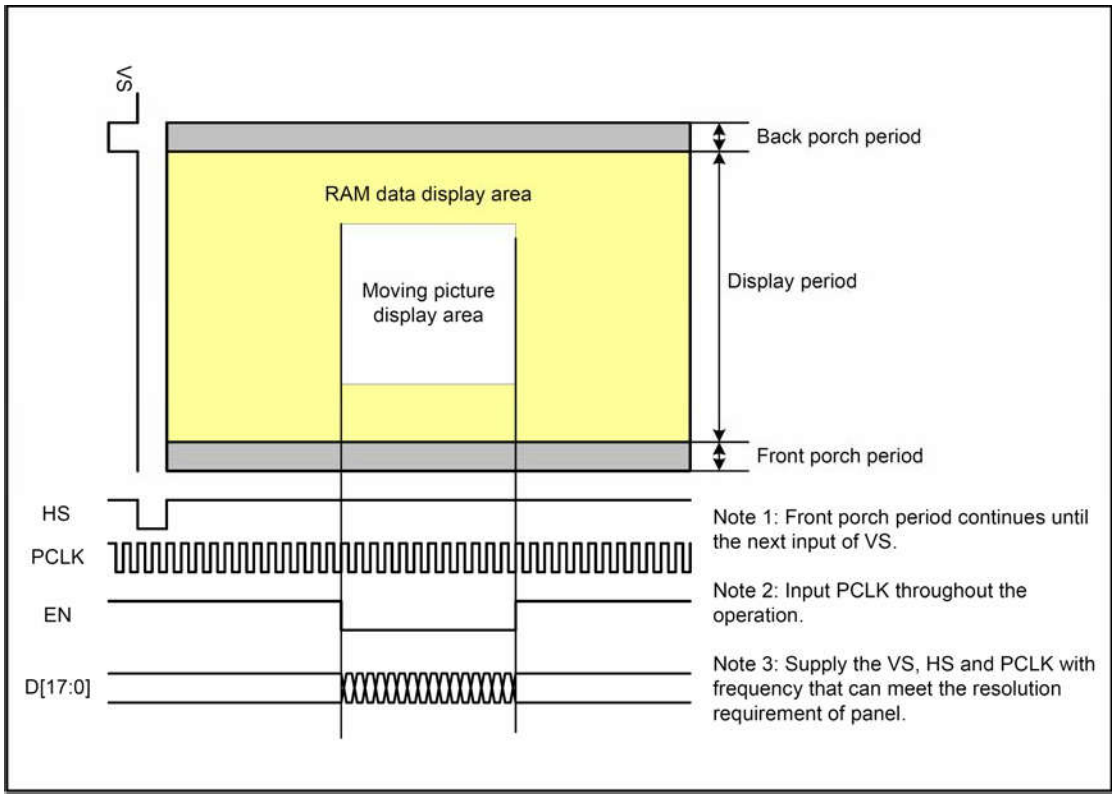
Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, EN and D[17:0] states when there is a rising edge of the PCLK. The PCLK can not be used as continues internal clock for other functions of the display module.

Vertical synchronization (VS) is used to tell when there is received a new

frame of the display. This is high enable and its state is read to the display module by a rising edge of the PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the PCLK signal. D[17:0] are used to tell what is the information of the image that is transferred on the display (When EN= ’1’ and there is a rising edge of PCLK). D[17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the PCLK signal.



4.8.2. RGB Interface Timing

The timing chart of Signals in 18-/16-bit RGB interface mode is shown as below:

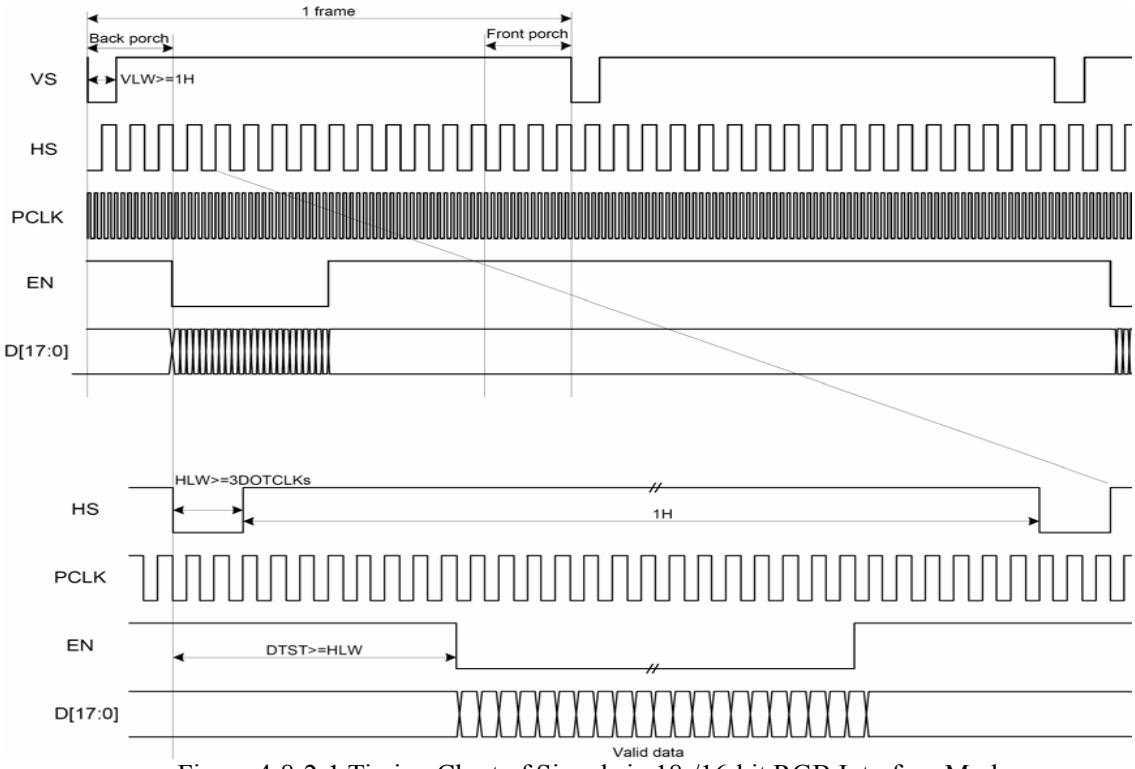


Figure 4-8-2-1 Timing Chart of Signals in 18-/16-bit RGB Interface Mode

The timing chart of 6-bit RGB interface mode is shown as below:

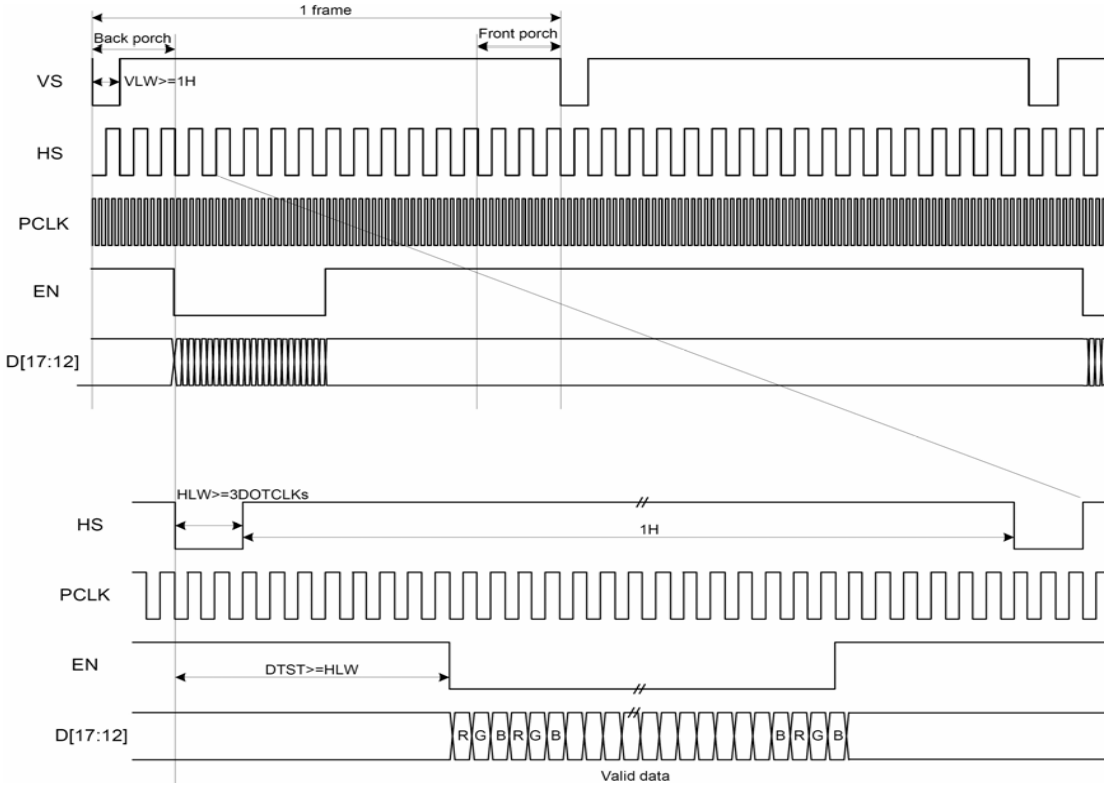


Figure 4-8-2-2 Timing Chart of Signals in 6-bit RGB Interface Mode

Note 1: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with PCLK.

Note 2: In 6-bit RGB interface mode, set the cycles of VS, HS and EN to 3 multiples of PCLK.

4.8.3 RGB Interface Mode Selection

NV3022B supplies a RGB interface with DE mode and can be selected by pull high external “RCM” pad.

When use RGB interface, writing data to frame memory is done by “PCLK” and Video Data Bus. So, controller (host) needn’t always transfer PCLK, VS, HS and DE signals to driver.

4.9. Display Data Color Coding

4.9.1. Serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.

- 4k colors, RGB 4-4-4-bits input
- 65K colors, RGB 5-6-5-bits input
- 262K colors, RGB 6-6-6-bits input

Data format and Reconstruct ways are shown as follow figures:

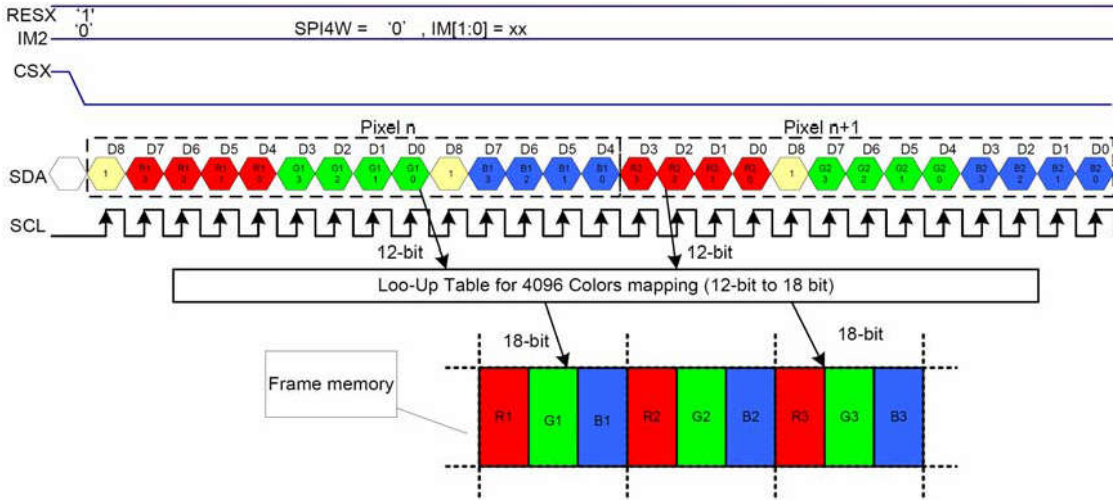


Figure 4-9-1-1 SPI 3-Wire 9-bit RGB4-4-4 Write Data Format

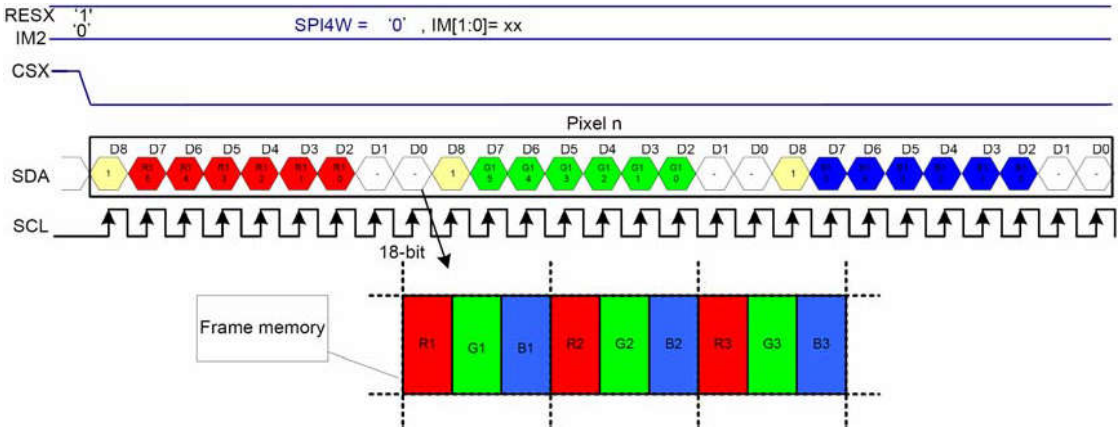


Figure 4-9-1-2 SPI 3-Wire 9-bit RGB6-6-6 Write Data Format

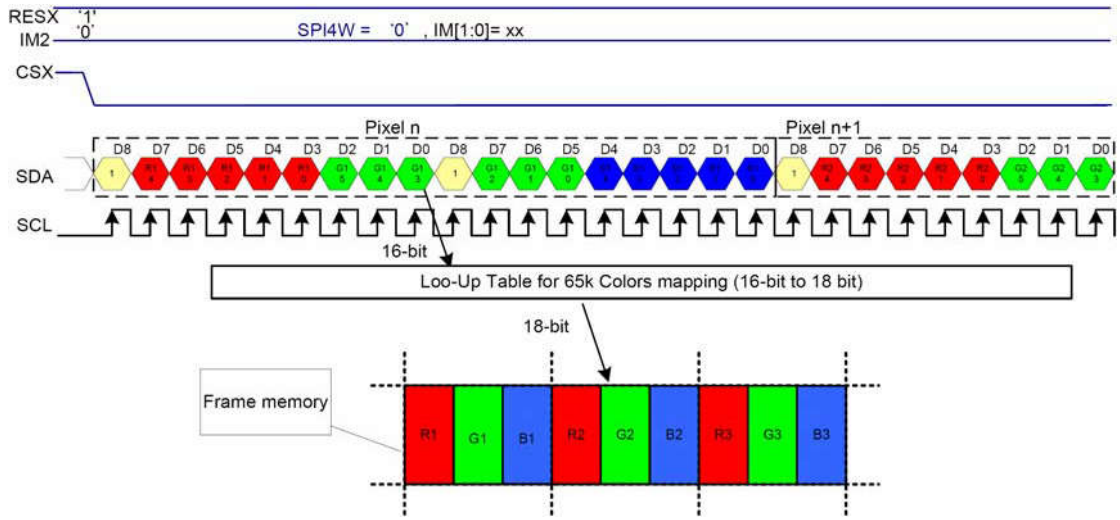


Figure 4-9-1-3 SPI 3-Wire 9-bit RGB5-6-5 Write Data Format

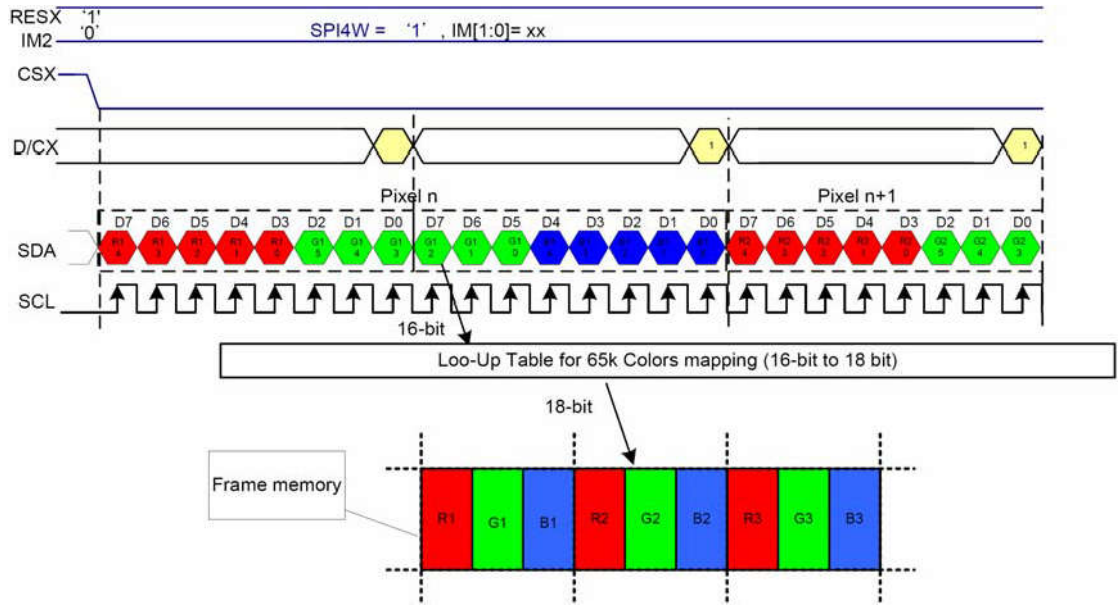


Figure 4-9-1-4 SPI 4-Wire 8-bit RGB5-6-5 Write Data Format

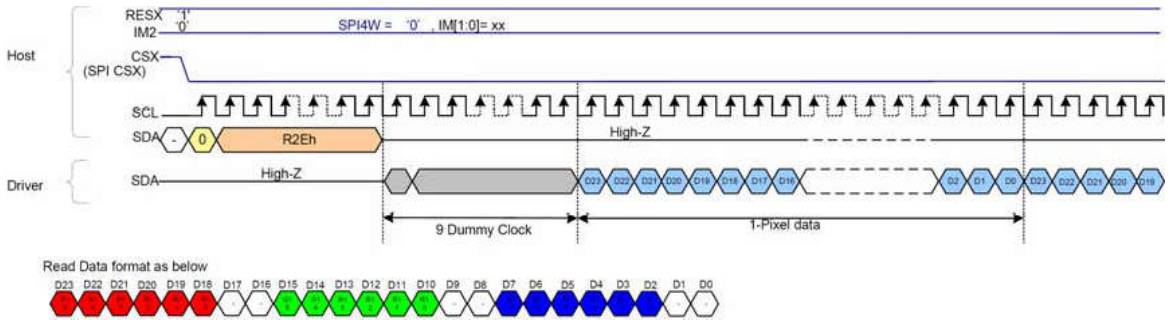


Figure 4-9-1-5 SPI 3-Wire Read Data Format

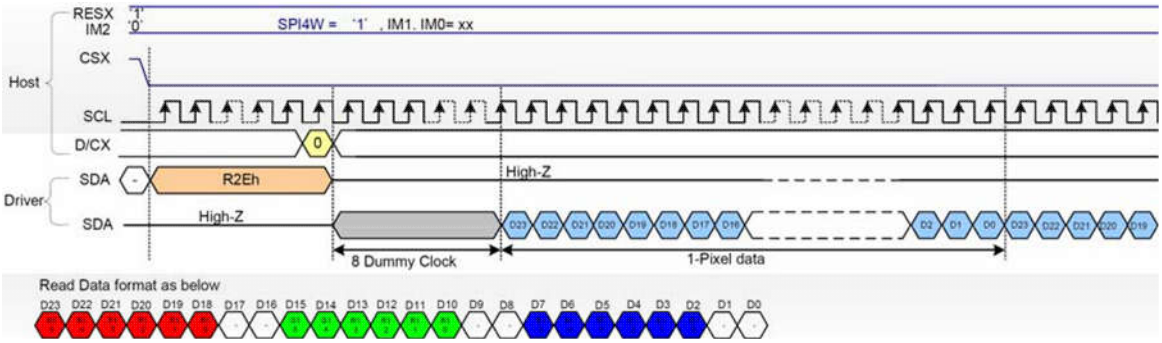


Figure 4-9-1-6 SPI 4-Wire Read Data Format

4.9.2. Parallel 8-bit Interface (IM=”100”)

Different display data formats are available for three colors depth supported by the LCM listed below.

- 4k colors, RGB 4-4-4-bits input
- 65K colors, RGB 5-6-5-bits input
- 262K colors, RGB 6-6-6-bits input

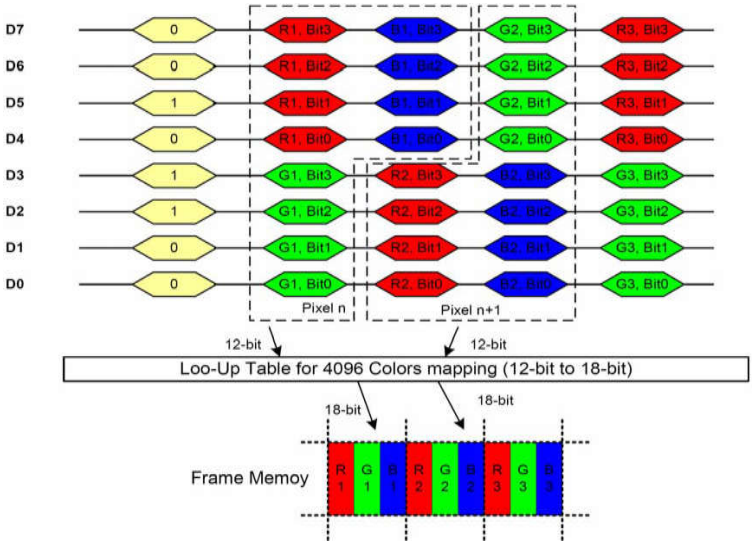


Figure 4-9-2-1 Two pixel (RGB4-4-4) in each three 8-bit write data packets

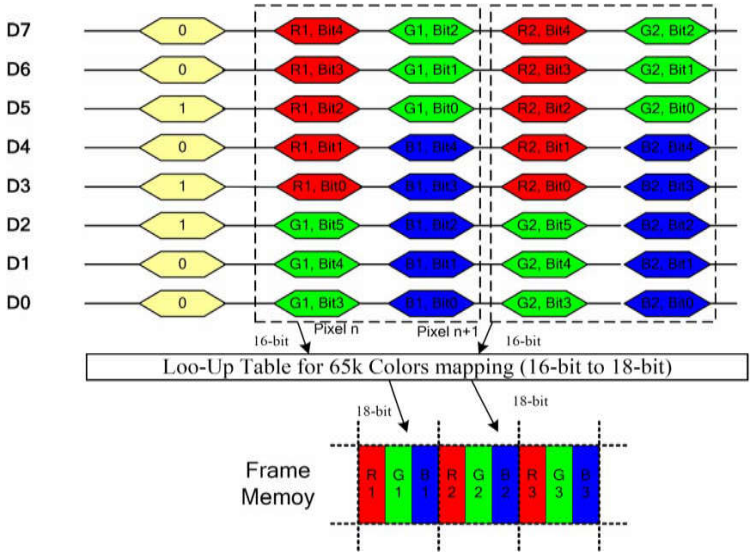


Figure 4-9-2-2 One pixel (RGB5-6-5) in each two 8-bit write data packets

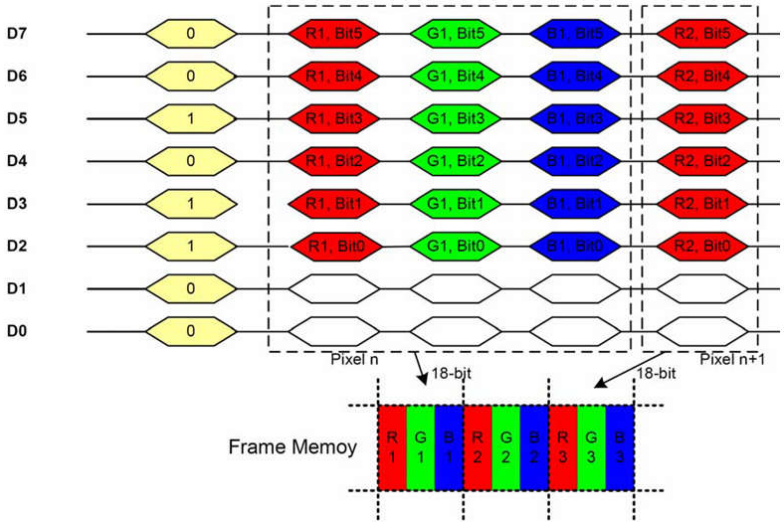


Figure 4-9-2-3 One pixel (RGB6-6-6) in each three 8-bit write data packets

4.9.3. Parallel 9-bit Interface (IM=”110”)

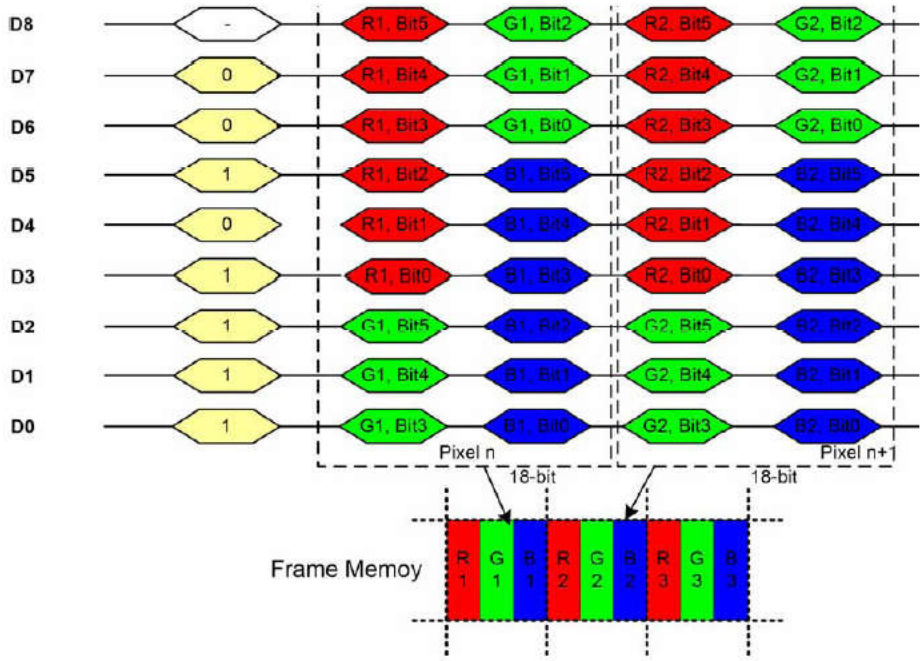


Figure 4-9-3 One pixel (RGB6-6-6) in each two 9-bit write data packets

4.9.4. Parallel 16-bit Interface (IM=”101”)

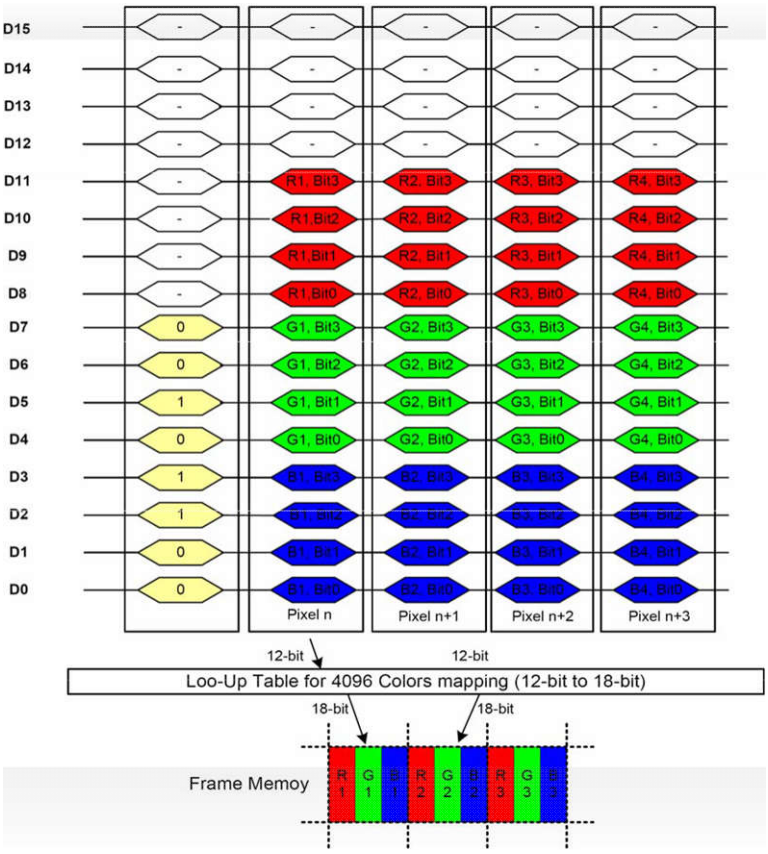


Figure 4-9-4-1 One pixel (RGB4-4-4) in each 16-bit write data packets

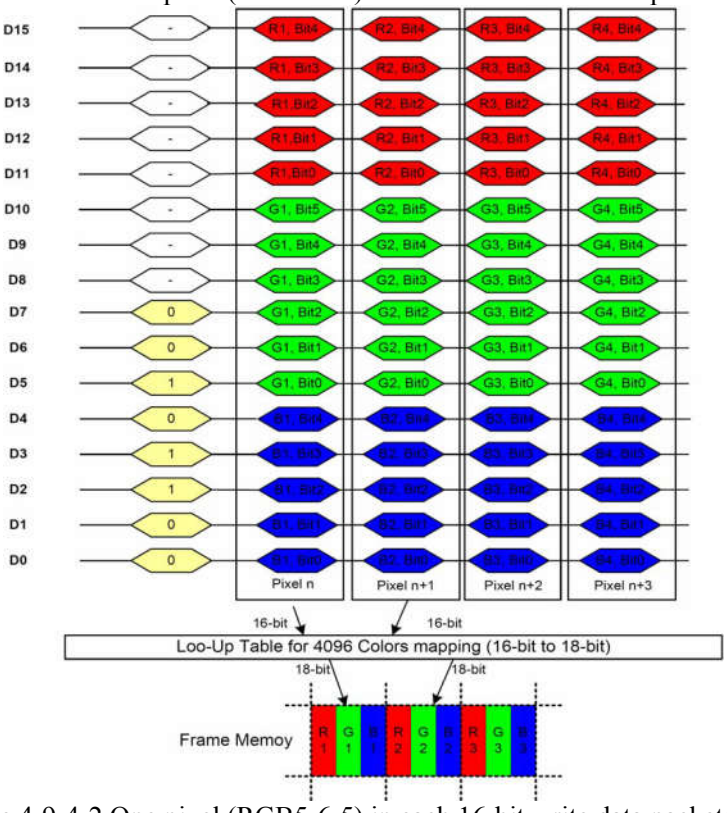


Figure 4-9-4-2 One pixel (RGB5-6-5) in each 16-bit write data packets

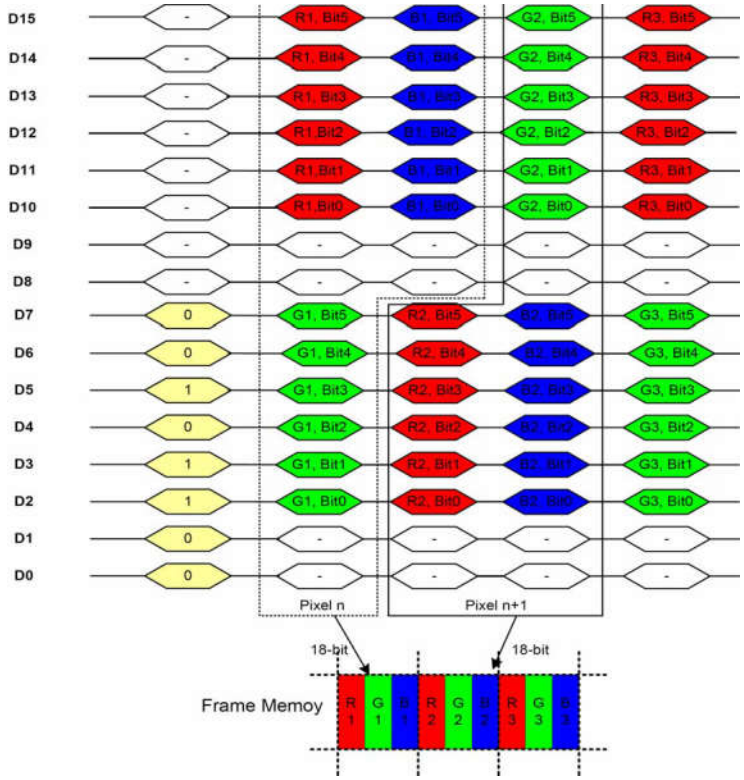


Figure 4-9-4-3 Two pixel (RGB6-6-6) in three16-bit write data packets

4.9.5. Parallel 18-bit Interface (IM=”111”)

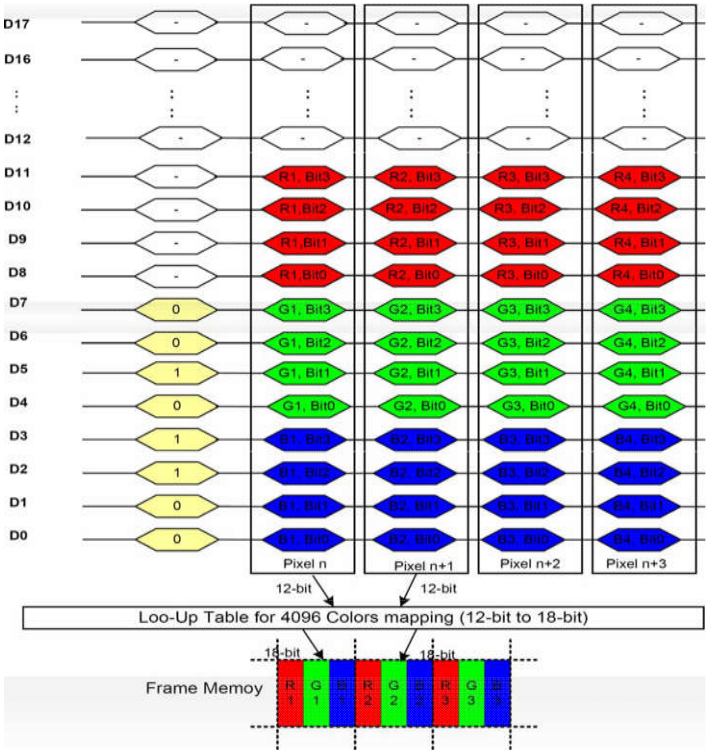


Figure 4-9-5-1 One pixel (RGB4-4-4) in one18-bit write data packets

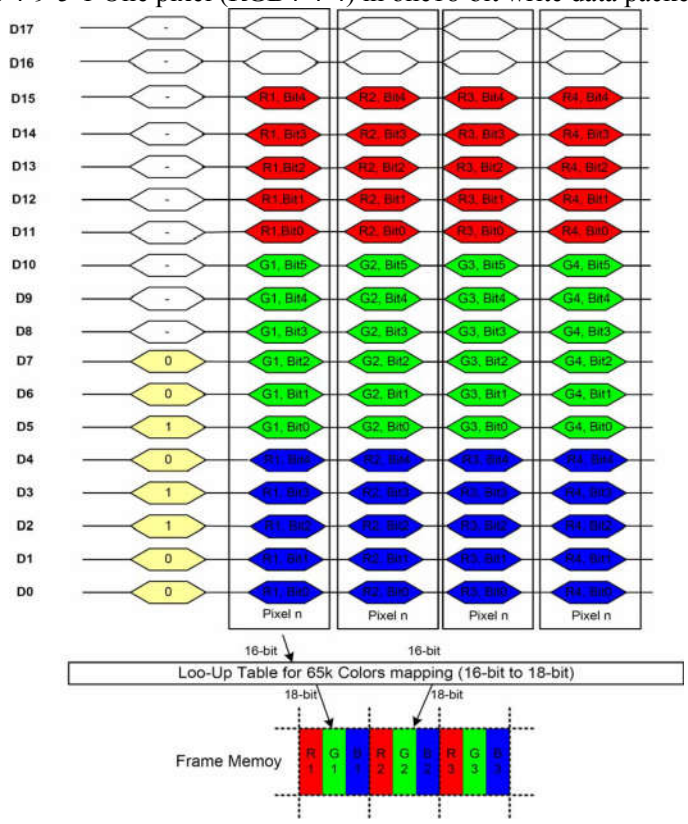


Figure 4-9-5-2 One pixel (RGB5-6-5) in one18-bit write data packets

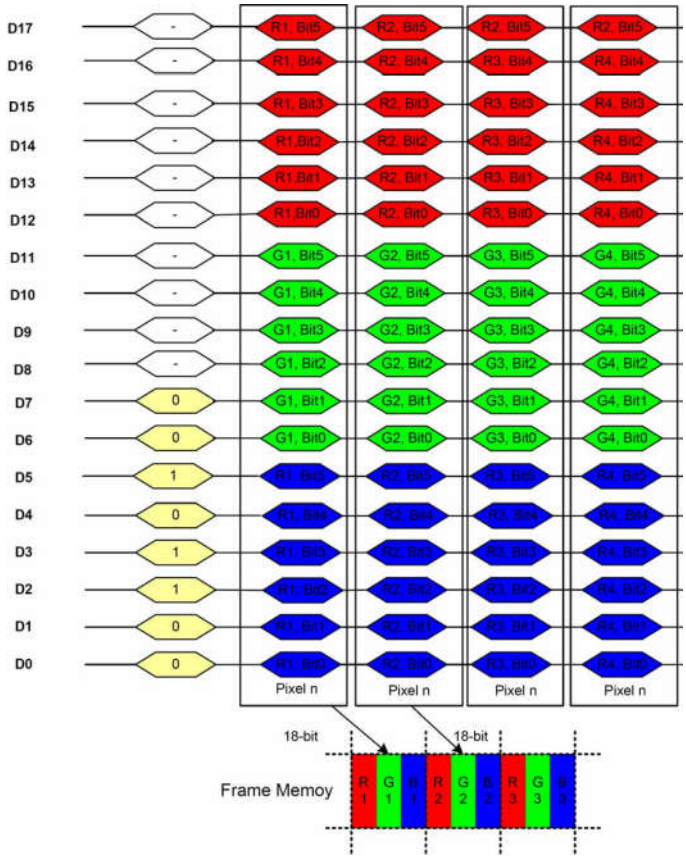
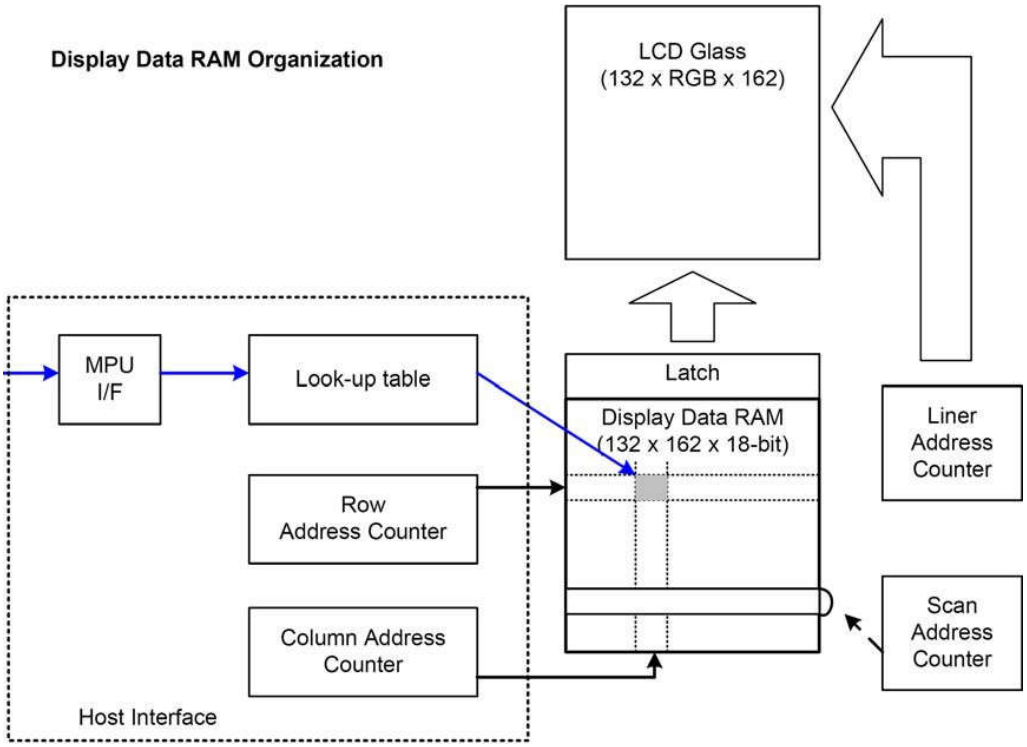


Figure 4-9-5-3 One pixel (RGB5-6-5) in one18-bit write data packets

5. Display Data with SRAM

5.1. SRAM Organization

The display data SRAM stores display dots and consists of 384,912 bits (132x18x162 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to “Source”. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



5.2. Memory To Display Mapping

Display data are writen in different direction according to different MX/MY settings, and scan read from SRAM also controlled by ML configuration.The detail as below figure shows:

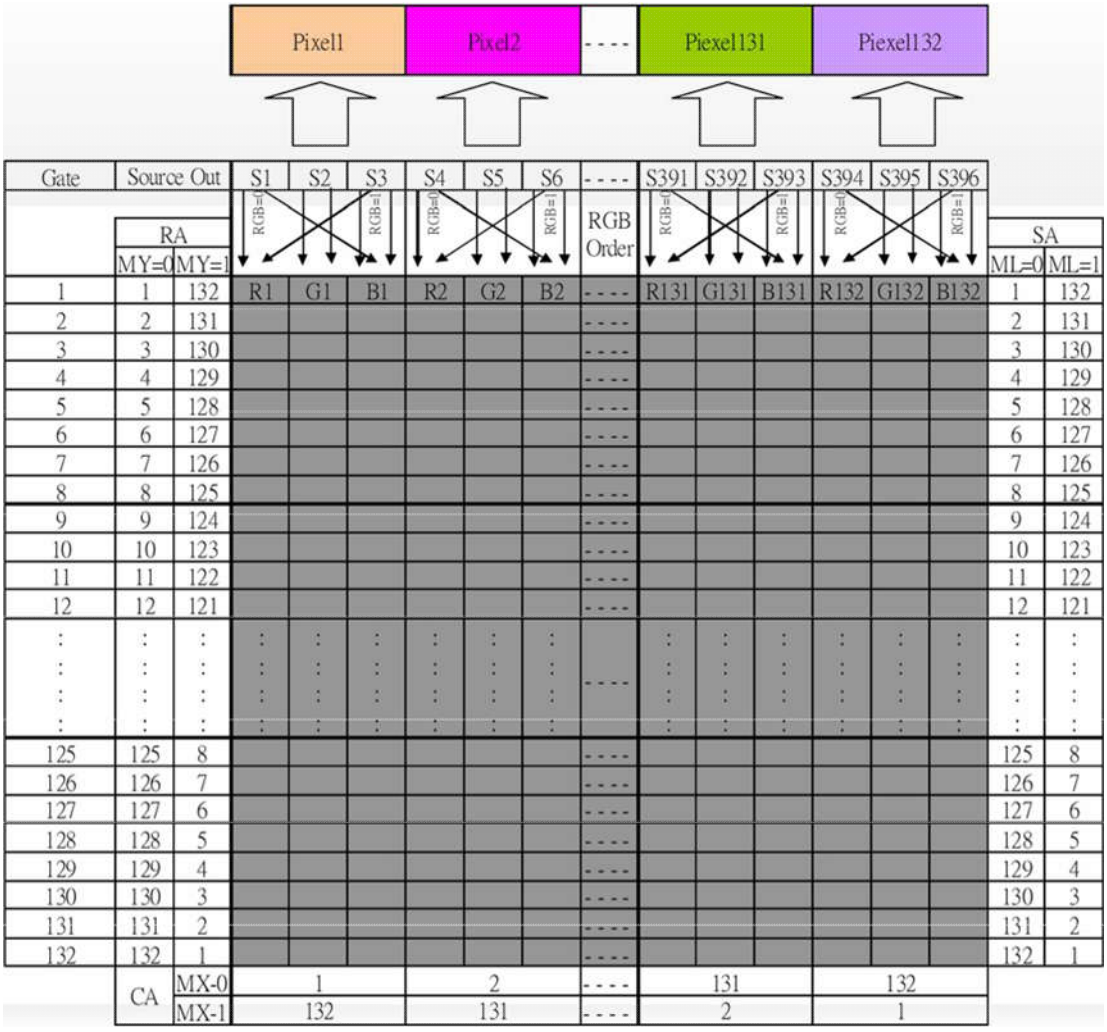


Figure 5-2 Display Data Mapping in SRAM

Note:

RA: Row Address
CA: Column Address
SA: Scan Address
MX: Mirror X-axis (Column address direction parameter), configured by MADCTL command
MY: Mirror Y-axis (Row address direction parameter), configured by MADCTL command
ML: Scan direction parameter, configured by MADCTL command
RGB: Red, Blue subpixel position change, configured by MADCTL command

5.3. MCU To SRAM Access Direction

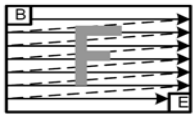
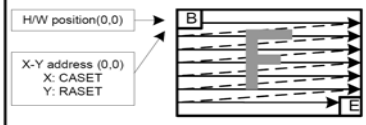
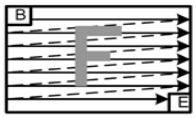
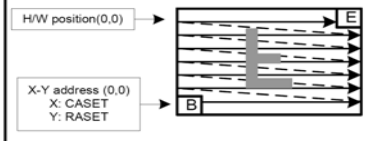
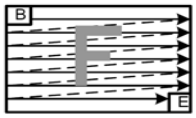
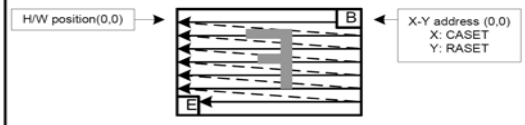
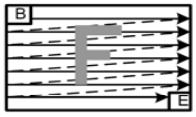
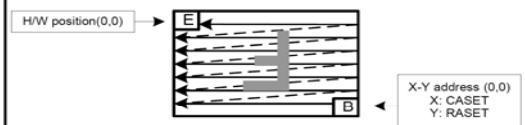
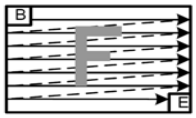
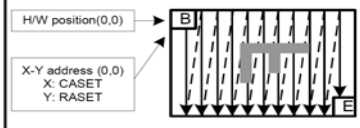
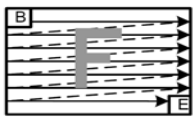
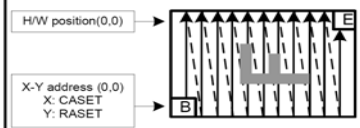
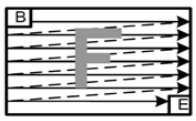
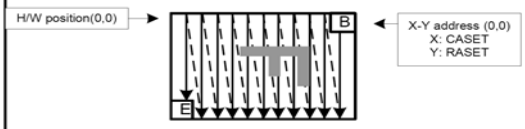
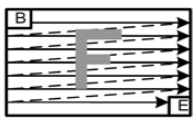
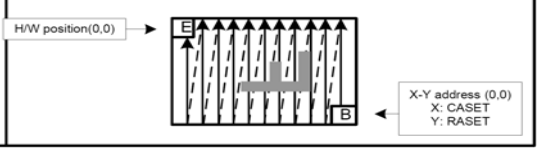
The address counter set the addresses of the display data RAM for writing and reading. Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. When GM=011, 132RGB x 162, the address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined into which will be written. The window is programmable via the command register XS, YS designating the start address and XE, YE designating the end address.

For example, the whole display contents will be written, the window is defined by the following values: XS=0(0h) YS=0(0h) and XE=131(83h), YE=161(A1h) In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address(X=XE), X wraps around to XS and Y increments to address the next row. After every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET” and “MADCTR”, define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Below table shows the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM. For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

Table 5-3 Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

Display Data Direction	MADCTR Parameter			Image in the Memory (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
XY Exchange	1	1	0		
XY Exchange	1	1	1		

6. Tearing Effect

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

6.1. Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync information only:

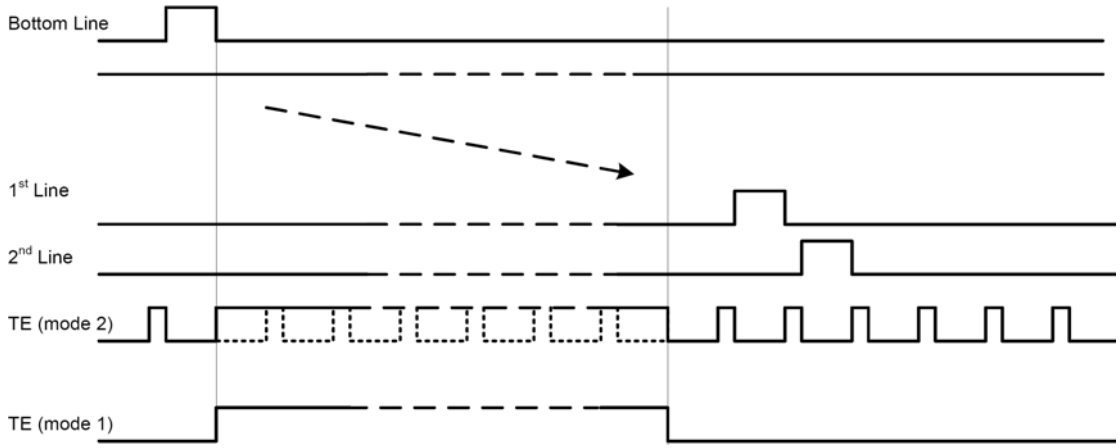
Tvdh = The LCD display is not updated from the Frame Memory.

Tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the Tearing Effect Output signal consists of V-Sync and H-Sync information, There are one V-sync and 162 H-sync pulses per field:

Thdh = The LCD display is not updated from the Frame Memory.

Thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

6.2. Tearing Effect Line Timing

The Tearing Effect signal is described below:

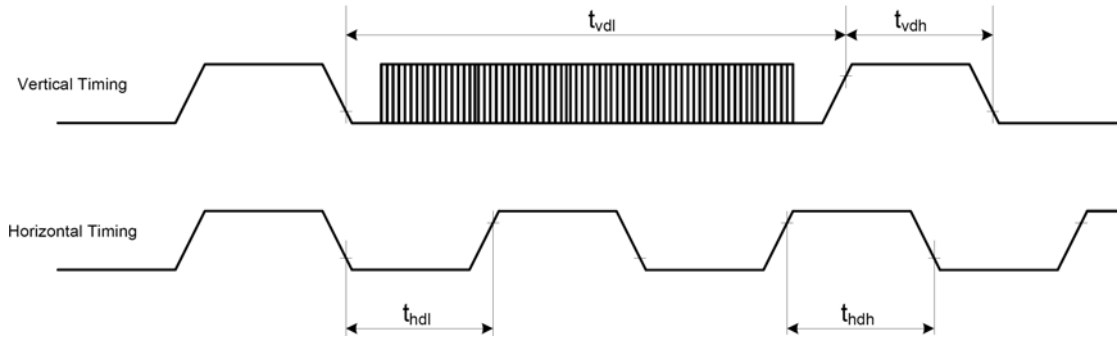


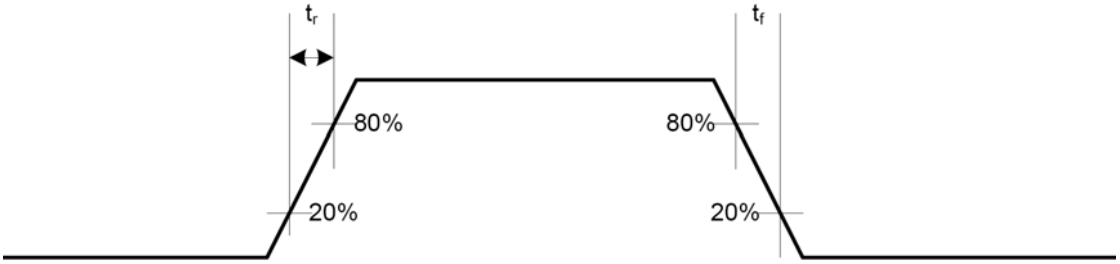
Table 6-2 AC characteristics of Tearing Effect Signal Idle Mode Off/On (Frame Rate = 58.9Hz)

Symbol	Parameter	MIN	MAX	Unit	Descritpion
tvdl	Vertical Timing Low Duration	13	-	Ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	33	-	µs	
thdh	Horizontal Timing High Duration	25	500	µs	

Notes:

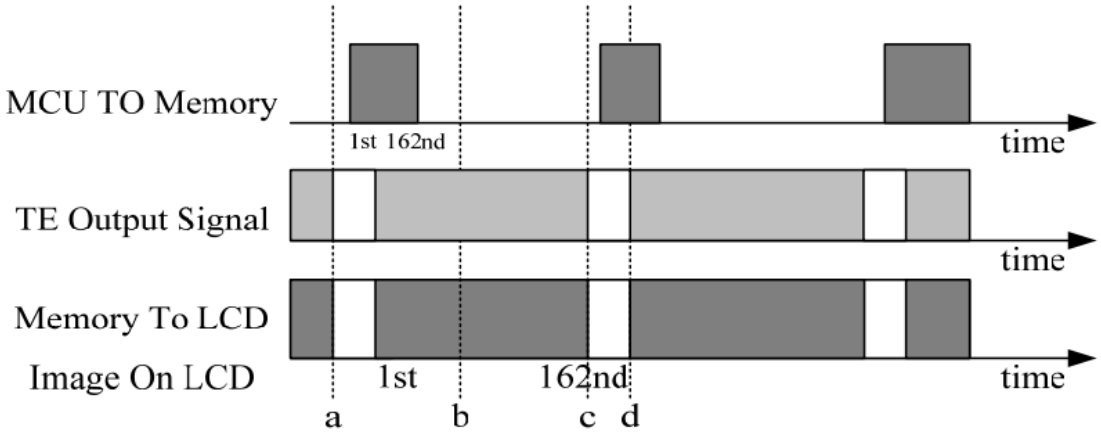
The timings in Table 7-2 apply when MADCTL B4=0

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



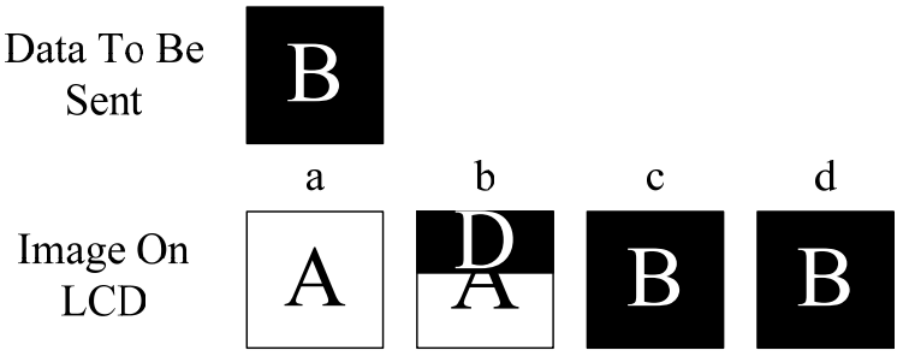
The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid Tearing Effect:

6.2.1. Example 1 MCU Write is Faster than Panel Read

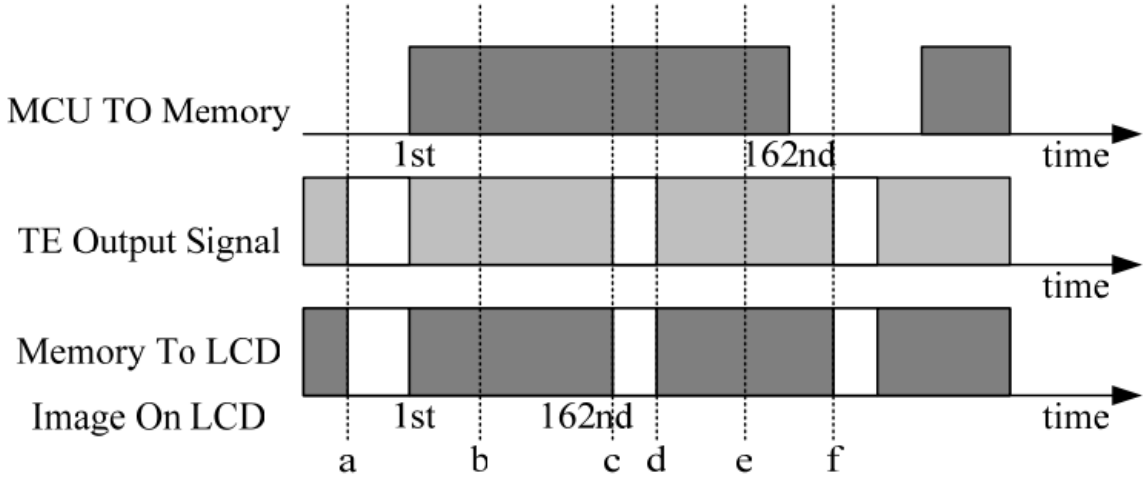


The MCU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MCU to Frame memory write position.

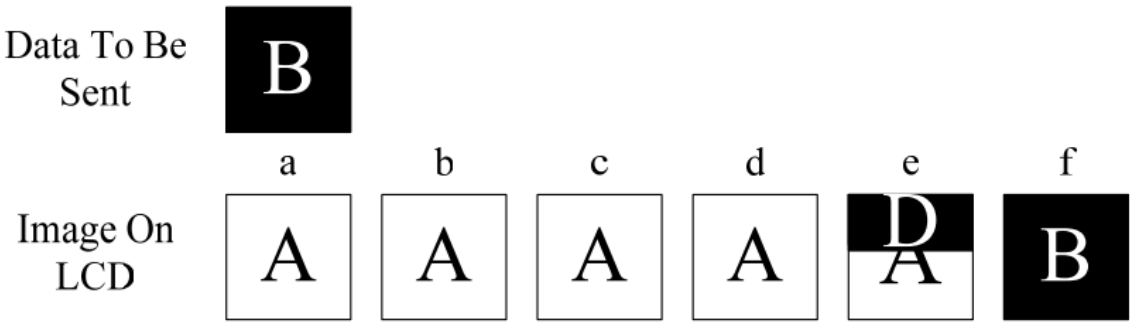
Frame refresh has a complete new image:



6.2.2. Example 2 MCU Write is slower than Panel Read



The MCU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MCU to Frame memory write position.



7. Power ON/OFF Sequence

IOVCC and VCI can be applied in any order.

VCI and IOVCC can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120 msec after RESX has been released.

During power off, if LCD is in the Sleep In Mode, IOVCC or VCI can be powered down minimum 0 msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Notes:

There will be no damage to the display module if the power sequences are not met.

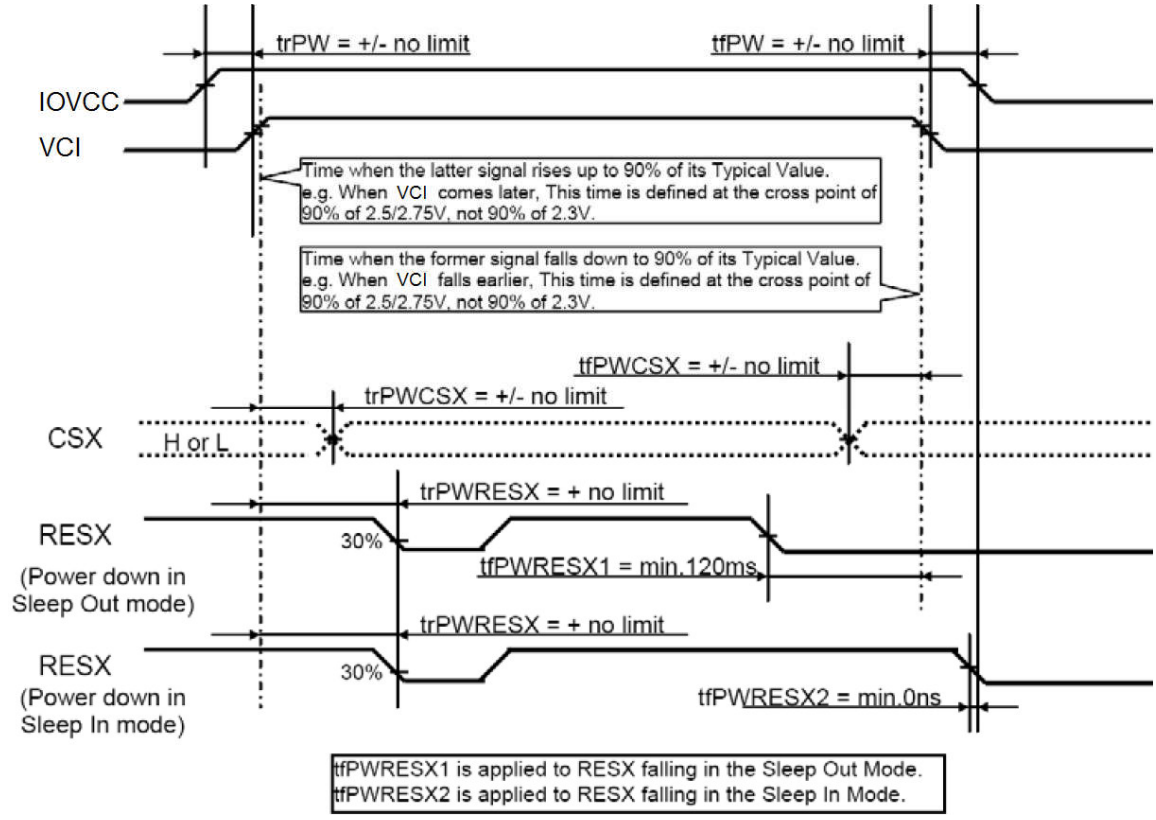
There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence as defined in Sections 8.1 and 8.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

7.1. Case 1 - RESX line is held high or Unstable by Host at Power On

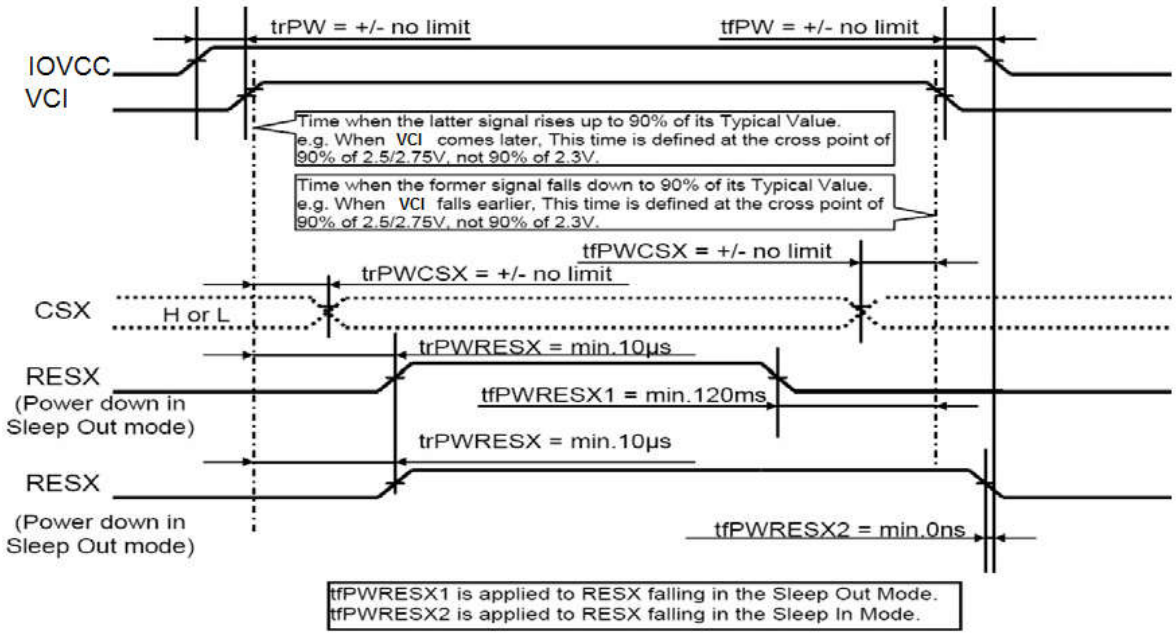
If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.2. Case 2 - RESX line is held low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10 µsec after both VCI and IOVCC have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. The display module must meet following requirements:

There cannot be any damages for the display module or the display module cannot cause any damages for the host or lines of the interface.

There cannot be any abnormal visible effects (= Display must be blank) within 1 second on the display and remains blank until “Power On Sequence” powers it up.

8. Power Level Definition

8.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out. In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out. In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out. In this mode, the full display area is used but with 8 colors.

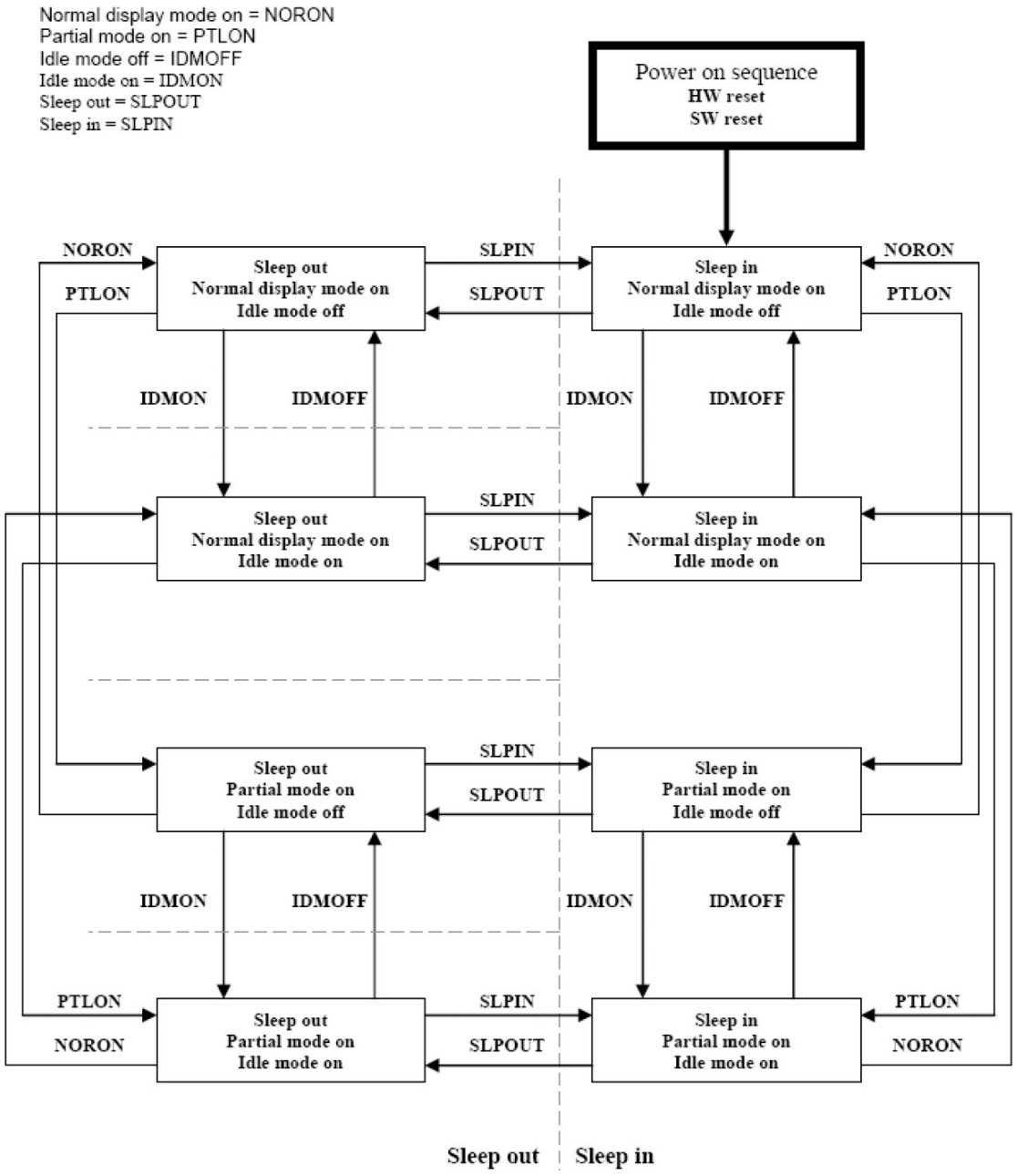
4. Partial Mode On, Idle Mode On, Sleep Out. In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode. In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.

6. Power Off Mode. In this mode, both VCI and IOVCC are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed. If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon

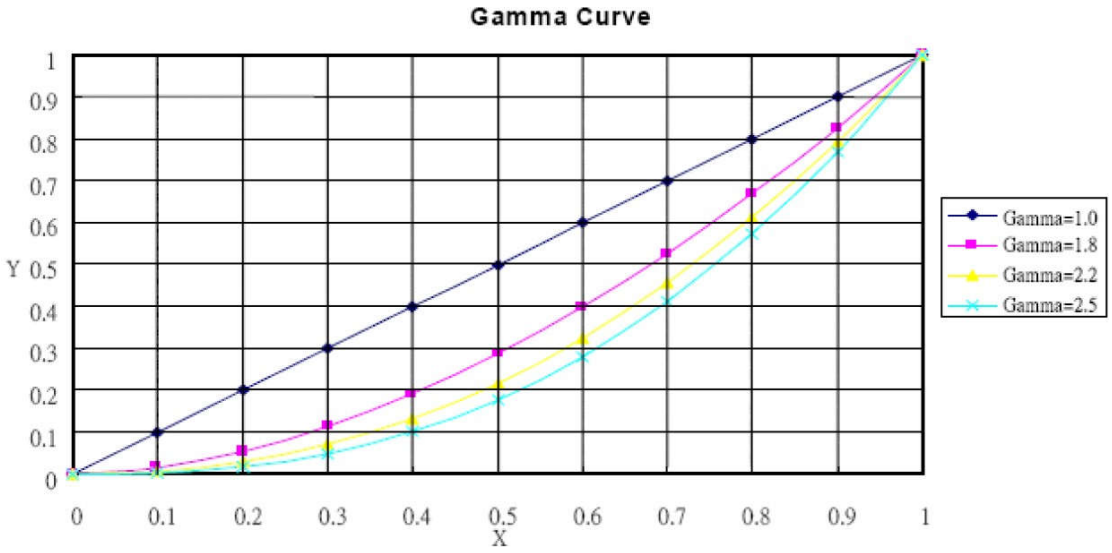
8.2. Power Flow Chart



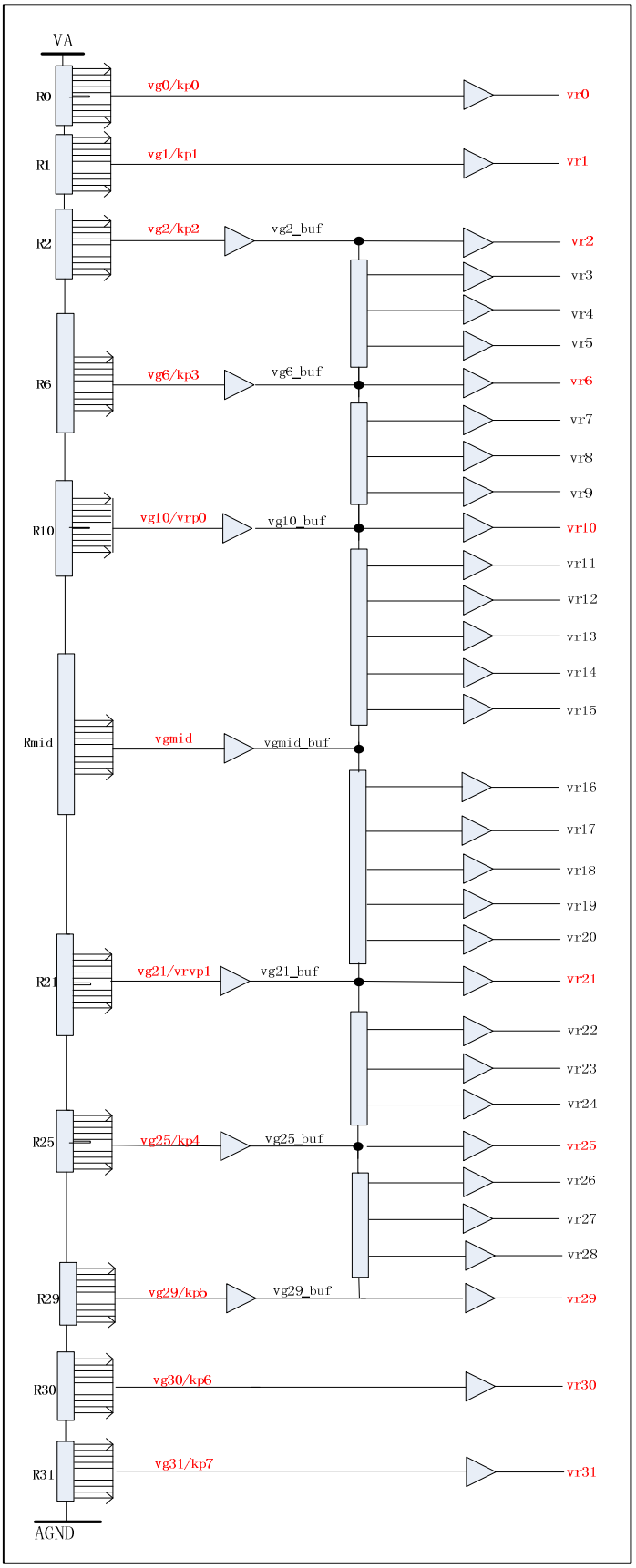
Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.
Note 2: There is not any limitation, which is not specified by Nokia, when there is changing from one power mode to another power mode.
Note 3: It is recommended that it should be enter Sleep in before power off.

9. Gamma Curve

9.1. Gamma curve according to the Gamma 1.0/1.8/2.2/2.5



9.2. Gamma Structure



10. Reset Function

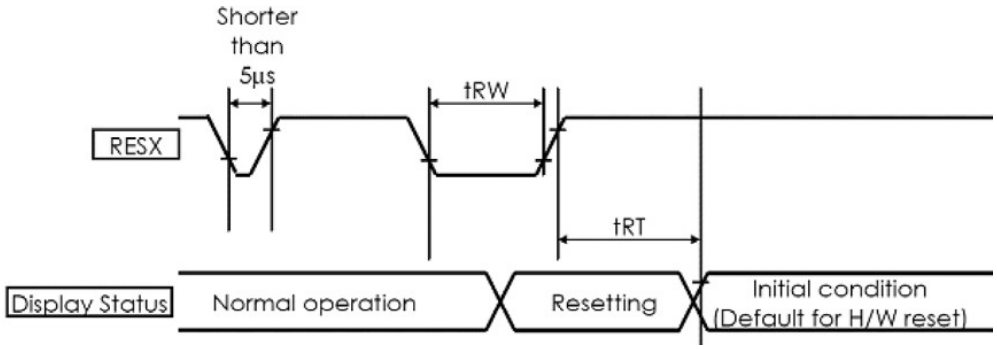
10.1. State of Register After Different Reset

The registers for resolution 128(RGB) x160 are initialized are listed below:

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column:Start Address(XS)	0000h	0000h	0000h
Column:End Address(XE)	007Fh	007Fh	007Fh
Row:Start Address(YS)	0000h	0000h	0000h
Row:End Address(YE)	009Fh	009Fh	009Fh
Gamma Setting	GC0	GC0	GC0
Color Set	262K	262K	262K
Partial:Start Address(PSL)	0000h	0000h	0000h
Partial:End Address(PEL)	009Fh	009Fh	009Fh
Scroll:Vertical scrolling	Off	Off	Off
Scroll:Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll:Scroll Area(VSA)	00A0h	00A0h	00A0h
Scroll:Bottom Fixed Area(BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing:On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RGB)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6(18-Bit/Pixel)	6(18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	0	0	No change
RDDCOLMOD	6(18-Bit/Pixel)	6(18-Bit/Pixel)	No change
RDDIM	00h	00h	No change
RDDSM	00h	00h	00h
RDDSER	00h	00h	00h
ID1	33h	33h	33h
ID2	30h	30h	30h
ID3	23h	23h	23h

Notes:
1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10μs after both VCI & IOVCC are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

10.2. Reset Timing



(VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 4.8V, Ta = -30 to 85℃)

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRW	Valid Reset low pulse width	RESX	10	-	-	-	us
tRT	Valid Reset Complete width	RESX	-	-	5	When reset applied during Sleep in mode	ms
		RESX	-	-	120	When reset applied during Sleep out mode	ms

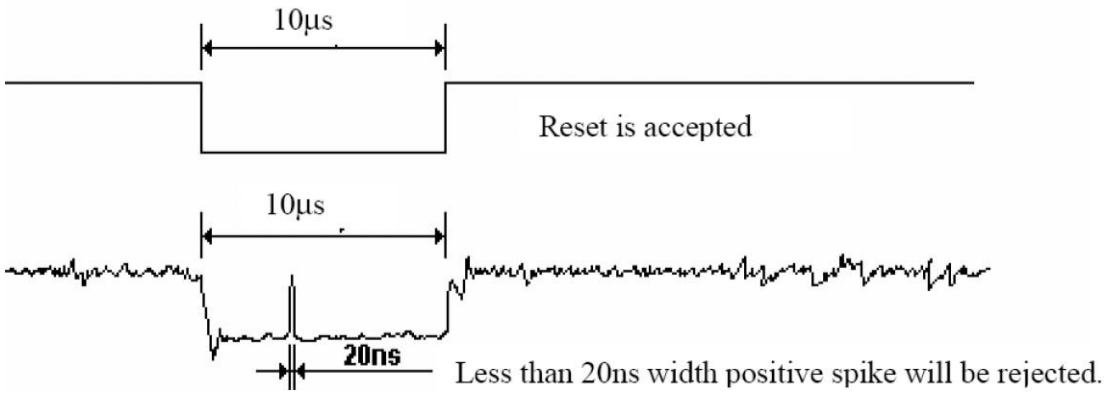
Note:

1> Spike due to an electrostatic discharge on RESX line does not cause system reset according to the table below.

RESX Pulse	Action
Shorten than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts(It depends on voltage and temperature condition)

2> During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In mode) and then return to Default condition for Hardware Reset.

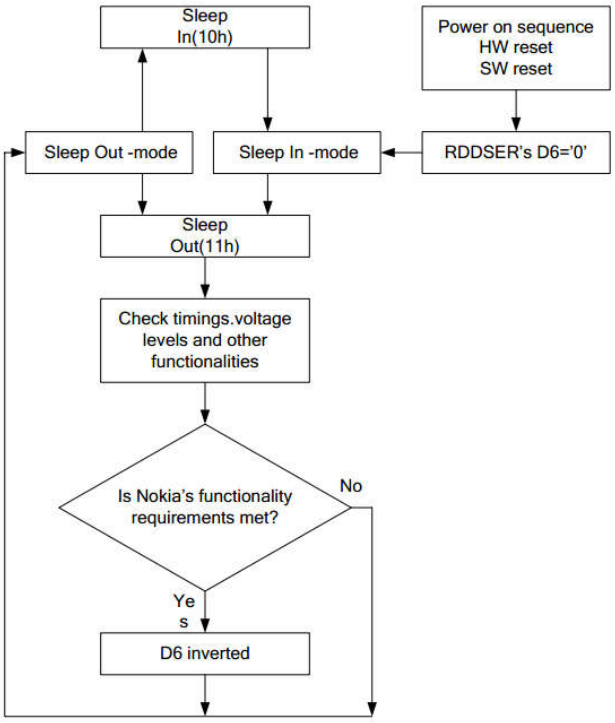
3> Spike Rejection also applies during a valid reset pulse as shown below:



4> It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

11. Sleep Out and Self-Diagnostic Functions of Display

Sleep Out-command (11h) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements. The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted a bit, which defined in command ("0Fh", The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted. The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out command, when there is changing from Sleep In mode to Sleep Out mode, before there is possible to check if Nokia's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out command is sent in Sleep Out mode.

12. Command

12.1. System Function Command List and Description

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x00	NOP	W	0	0	0	0	0	0	0	0
0x01	SWRESET	W	0	0	0	0	0	0	0	0
0x04	RDDID	R	sys_id1[7:0]							
			sys_id2[7:0]							
			sys_id3[7:0]							
0x09	RDDST	R	boost_on	my	mx	mv	ml	rgb		
			pixel_fmt[3:0]				idle_on	ptl_on	slpout	normal_on
			scroll_on	1'b0	invon	0	0	dispon	te_on	0
			0	0	telom	rgb_on				
0x0A	RDDPM	R	boost_on	idle_on	ptl_on	slpout	normal_on	dispon	0	0
0x0B	RDD_MADCTR	R	my	mx	mv	ml	sbgr	0	0	0
0x0C	RDD_COLMOD	R	vipf[3:0]				0	ifpf[2:0]		
0x0D	RDDIM	R	scroll_on	1'b0	invon	0	0	0	0	0
0x0E	RDDSM	R	te_on	telom	0	0	0	0	0	0
0x0F	RDDSDR	R	self_diag[4:0]				0	0	0	0
0x10	SLPIN	W								
0x11	SLPOUT	W								
0x12	PTLON	W								
0x13	NORON	W								
0x20	INVOFF	W								
0x21	INVON	W								
0x28	DISPOFF	W								
0x29	DISPON	W								
0x2A	CASET	W	col_st_set[7:0]							
			col_ed_set[7:0]							

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x2B	RASET	W	row_st_set[7:0]							
			row_ed_set[7:0]							
0x2C	RAMWR	W								
0x2E	RAMRD	W								
0x30	PTLAR	W	ptl_st_set[7:0]							
			ptl_ed_set[7:0]							
0x33	SCRLAR	W	tfa[7:0]							
			vsa[7:0]							
0x34	TEOFF	W								
0x35	TEON	W								TELOM
0x36	MADCTR	W	my	mx	mv	ml	rgb			
0x37	VSCSAD	W	ssa[7:0]							
0x38	IDMOFF	W								
0x39	IDMON	W								
0x3A	COLMOD	W	vipf[3:0]					ifpf[2:0]		
0xDA	RDID1	R	sys_id1[7:0]							
0xDB	RDID2	R	sys_id2[7:0]							
0xDC	RDID3	R	sys_id3[7:0]							

12.1.1. NOP (00h)

<table>
<tr><th>00H</th><th colspan="11">No Operation</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00H</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is an empty command. It does not have any effect on the display module. However it can be used to terminate Frame Memory White or Read as described in RAMWR (Memory White) and RAMRD (Memory Read) Commands.
X=Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="12">None</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
</table>

12.1.2. SWRESET (01h)

<table>
<tr><td>01H</td><td colspan="11">Software Reset</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01H</td></tr>
<tr><td>Parameter</td><td colspan="11">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)
Note: The Frame Memory contents are affected by this command.
X=Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="11">None</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
</table>

12.1.3. RDDID (04h)

<table>
<tr><th>04H</th><th colspan="12">Read Display ID</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>R</td><td>H</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>04H</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td colspan="8">SYS_ID1[7:0]</td><td>33H</td></tr>
<tr><td>Parameter3</td><td>H</td><td>R</td><td>H</td><td colspan="8">SYS_ID2[7:0]</td><td>30H</td></tr>
<tr><td>Parameter4</td><td>H</td><td>R</td><td>H</td><td colspan="8">SYS_ID3[7:0]</td><td>23H</td></tr>
<tr><td>Description</td><td colspan="12">This read byte returns 24-bit display identification.
The 1st Parameter is dummy read.
The 2st Parameter (SYS_ID1): LCD module’s manufacture ID.
The 3st Parameter (SYS_ID2): LCD module/driver version ID.
The 4st Parameter (SYS_ID3): LCD module/driver version ID.
Note: Commands RDDID1/2/3 (DAh, DBh, DCh) read data correspond to the parameters 1, 2, 3 of command 04h, respectively.</td></tr>
<tr><td>Restriction</td><td colspan="12">None</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>ID1</th><th>ID2</th><th>ID3</th></tr><tr><td>Power On Sequence</td><td>33h</td><td>30h</td><td>23h</td></tr><tr><td>SW Reset</td><td>33h</td><td>30h</td><td>23h</td></tr><tr><td>HW Reset</td><td>33h</td><td>30h</td><td>23h</td></tr></table></td></tr>
</table>

12.1.4. RDDST (09h)

09H	Read Display Status											
	D/CX	**RDX**	**WRX**	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	R	H	0	0	0	0	1	0	0	1	09H
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X
Parameter2	H	R	H	BOOST_ON	MY	MX	MV	ML	RGB	0	0	-
Parameter3	H	R	H	PIXEL_FMT[3:0]				IDLE_ON	PTL_ON	SLPOUT	NORMAL_ON	-
Parameter4	H	R	H	SCROLL_ON	0	INVON	0	0	DISPON	TE_ON	0	-
Parameter5	H	R	H	0	0	TELOM	RGB_ON					-

Description

Bit	Description	Value
BOOST_ON	Booster Voltage Status	“1”=Booster on,“0”=Booster off
MY	Row Address Order(MY)	“1”=Decrement. (Bottom to Top), when MADCTL (36h) D7=“1”
		“0”=Increment.(Bottom to Top),when MADCTL (36h) D7=“0”
MX	Column Adress Order(MX)	“1”=Decrement.(Right to Left),when MADCTL(36h)D6=“1”
		“0”=Increment.(Left to Right),when MADCTL(36h)D6=“0”
MV	Row/Column Exchange(MV)	“1”=Row/column exchange. when MADCTL (36h) D5=“1”
		“0”=Normal(MV=0).when MADCTL (36h) D5=“0”
ML	Vertical refresh Order(ML)	“1”=Decrement.(LCD refresh Bottom to Top, when MADCTL (36h) D4=“1”
		“0”=Increment.(LCD refresh Top to Bottom), when MADCTL(36h)D4=“0”
RGB	RGB/BGR Order(RGB)	“1”=BGR.when MADCTL(36h)D3=“1”
		“0”=RGB.when MADCTL(36h)D3=“0”
PIXEL_FMT[3:0]	Interface Color Pixel Format Definition	“0011”=12-bit/pixel
		“0101”=16-bit/pixel
		“0110”=18-bit/pixel
IDLE_ON	Ldle Mode On/Off	“1”=On,“0”=Off
PTL_ON	Partial Mode On/Off	“1”=On,“0”=Off
SLPOUT	Sleep In/Out	“1”=On,“0”=Off
NORMAL_ON	Display Normal Mode On/Off	“1”=Normal Display,“0”=Normal Display Off
SCROLL_ON	Vertical Scrolling Status	“1”=Scroll On,“0”=Scroll Off
INVON	Inversion Status	“1”=On,“0”=Off
DISPON	Display On/Off	“1”=On,“0”=Off

<table>
<tr><td></td><td>
<table>
<tr><td>TE_ON</td><td>Tearing effect line on/off</td><td>“1”=On,“0”=Off</td></tr>
<tr><td>TELOM</td><td>Tearing effect line mode</td><td>“0”=mode1,“1”=mode2,</td></tr>
<tr><td>RGB_ON</td><td>RGB interfacee flag</td><td>“0x1A”=RGB ON,”0x00”=RGB OFF</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td>None</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value(ST31 to ST0)</th></tr>
<tr><th>ST[31-24]</th><th>ST[23-16]</th><th>ST[15-8]</th><th>ST[7-0]</th></tr>
<tr><td>Power on Sequence</td><td>0000-0100</td><td>0110-0001</td><td>0000-0000</td><td>0000-0000</td></tr>
<tr><td>SW Reset</td><td>0xxx-xxx0</td><td>0xxx-0001</td><td>0000-0000</td><td>0000-0000</td></tr>
<tr><td>HW Reset</td><td>0000-0000</td><td>0110-0001</td><td>0000-0000</td><td>0000-0000</td></tr>
</table>
</td></tr>
</table>

12.1.5. RDDPM (0Ah)

<table>
<tr><th>0AH</th><th colspan="12">Read Display Power Mode</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>R</td><td>H</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0AH</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td>BOOST_ON</td><td>IDLE_ON</td><td>PTL_ON</td><td>SLPOUT</td><td>NORMAL_ON</td><td>DISPON</td><td>0</td><td>0</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>BOOST_ON</td><td>Booster Voltage Status</td><td>“1”=Booster On
“0”Booster Off</td></tr>
<tr><td>IDLE_ON</td><td>Idle mode On/Off</td><td>“1”=Idle mode On
“0”=Idle mode Off</td></tr>
<tr><td>PTL_ON</td><td>Partial Mode On/Off</td><td>“1”=Partial Mode On
“0”=Partial Mode Off</td></tr>
<tr><td>SLPOUT</td><td>Sleep In/Off</td><td>“1”=Sleep Out
“0”=Sleep In</td></tr>
<tr><td>NORMAL_ON</td><td>Display Normal Mode On/Off</td><td>“1”=Normal Display
“0”=Partial Display</td></tr>
<tr><td>DISPON</td><td>Display On/Off</td><td>“1”=Display On
“0”=Display Off</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="12">None</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>0000_1000(08h)</td></tr>
<tr><td>SW Reset</td><td>0000_1000(08h)</td></tr>
<tr><td>HW Reset</td><td>0000_1000(08h)</td></tr>
</table>
</td></tr>
</table>

12.1.6. RDDMADCTL (0Bh)

<table>
<tr><td>0BH</td><td colspan="11">Read Display MADCTL</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>R</td><td>H</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0BH</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td>MY</td><td>MX</td><td>MV</td><td>ML</td><td>SBGR</td><td>0</td><td>0</td><td>0</td><td>-</td></tr>
<tr><td>Description</td><td colspan="11">
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>MY</td><td>Page Address Order</td><td>“1”=Decrement,“0”=Increment</td></tr>
<tr><td>MX</td><td>Column Adress Order</td><td>“1”=Decrement,“0”=Increment</td></tr>
<tr><td>MV</td><td>Page/Column Order</td><td>“1”=Row/column exchange (MV=1)
“0”=Normal(MV=0)</td></tr>
<tr><td>ML</td><td>Line Address Order</td><td>“1”=LCD Refresh Botton to top
“0”=LCD Refresh top to Botton</td></tr>
<tr><td>SBGR</td><td>RGB/BGR Order</td><td>“1”=BGR, “0”=RGB</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="11">None</td></tr>
<tr><td>Register Availability</td><td colspan="11">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="11">
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h08</td></tr>
<tr><td>SW Reset</td><td>8’h08</td></tr>
<tr><td>HW Reset</td><td>8’h08</td></tr>
</table>
</td></tr>
</table>

12.1.7. RDDCOLMOD (0Ch)

<table>
<tr><td>0CH</td><td colspan="12">Read Display Pixel Format</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>R</td><td>H</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0CH</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td colspan="4">VIPF[3:0]</td><td>0</td><td colspan="3">IFPF[2:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">The 1st Parameter is dummy read.
<table>
<tr><th colspan="2">Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>VIPF3</td><td rowspan="4">RGB Interface Color Fomat</td><td rowspan="4">0101=16 bit/pixel(1 time data transfer)
0110=18 bit/pixel(1 time data transfer)
1110=18 bit/pixel(3 times data transfer)
The other=not defined</td></tr>
<tr><td>D6</td><td>VIPF2</td></tr>
<tr><td>D5</td><td>VIPF1</td></tr>
<tr><td>D4</td><td>VIPF0</td></tr>
<tr><td>D3</td><td>D3</td><td></td><td>“0”（Not Used)</td></tr>
<tr><td>D2</td><td>IFPF2</td><td rowspan="3">Control Interface Color Fomat</td><td rowspan="3">“011”=12 bit/pixel
“101”=16 bit/pixel
“110”=18 bit/pixel
The other=not defined</td></tr>
<tr><td>D1</td><td>IFPF1</td></tr>
<tr><td>D0</td><td>IFPF0</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">None</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>0110_0110(18bit/pixel)</td></tr>
<tr><td>SW Reset</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>0110_0110(18bit/pixel)</td></tr>
</table></td></tr>
</table>

12.1.8. RDDIM (0Dh)

<table>
<tr><td>0DH</td><td colspan="12">Read Display Image Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>R</td><td>H</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0DH</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td>SCROLL_ON</td><td>0</td><td>INVON</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">The 1st Parameter is dummy read.
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Scrolling On/Off</td><td>“1”=Scrolling is On
“0”=Scrolling is Off</td></tr>
<tr><td>D5</td><td>Inversion On/Off</td><td>“1”=Inversion is On
“0”=Inversion is Off</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">None</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>SW Reset</td><td>8’h00</td></tr>
<tr><td>HW Reset</td><td>8’h00</td></tr>
</table></td></tr>
</table>

12.1.9. RDDSM (0Eh)

<table>
<tr><td>0EH</td><td colspan="11">Read Display Signal Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>R</td><td>H</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0EH</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td>TE_ON</td><td>TELOM</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-</td></tr>
<tr><td>Description</td><td colspan="11">The 1st Parameter is dummy read.
<table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>D7</td><td>Tearing Effect Line On/Off</td><td>“0”=Off, “1”= On</td></tr><tr><td>D6</td><td>Tearing Effect Line Mode</td><td>“0”=Mode1,“1”= Mode2</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="11">None</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

12.1.10. RDDSDR (0Fh)

<table>
<tr><th>0FH</th><th colspan="12">Read Display Self-Diagnostic Result</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>R</td><td>H</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0FH</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td colspan="4">SELF_DIAG[3:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">The 1st Parameter is dummy read.
If internal function work correctly, send this command will get an inverted result every time.</td></tr>
<tr><td>Restriction</td><td colspan="12">None</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>SLPIN</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

12.1.11. SLPIN (10h)

<table>
<tr><th>10H</th><th colspan="12">Sleep In</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10H</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command causes the LCD module to enter the minimum power consumption mode.
In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.
MCU interface and memory are still working and the memory keeps it’s contents.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).
It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120 msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>SLPIN</td></tr><tr><td>SW Reset</td><td>SLPIN</td></tr><tr><td>HW Reset</td><td>SLPIN</td></tr></table></td></tr>
</table>

12.1.12. SLPOUT(11h)

<table>
<tr><th>11H</th><th colspan="12">Sleep Out</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11H</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command turns off sleep mode.
In this mode e.g. the DC/DC converter is enabled. Internal oscillator is started, and panel scanning is started.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in sleep out mode. Sleep Our Mode can only be left by the Sleep in Command (10h).
It will be necessary to wait 5msec before sending next command; this is to allow time for the clock circuits to stabilize.
The display module loads all display supplier’s factory default values to the registers during this 120 msec and there cannot be any abnormal visual effect on the display image if faceory default and register values are same when this load is done and when the display module is already Sleep Out-mode.
The display module is doing self-diagnostic function during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.
This command has no effect when module is already in sleep out mode.
Sleep Out Mode can only be left by HW Reset, Software Reset (01h), Sleep In (10h), or a NMI event trigger.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>SLPOUT</td></tr><tr><td>SW Reset</td><td>SLPOUT</td></tr><tr><td>HW Reset</td><td>SLPOUT</td></tr></table></td></tr>
</table>

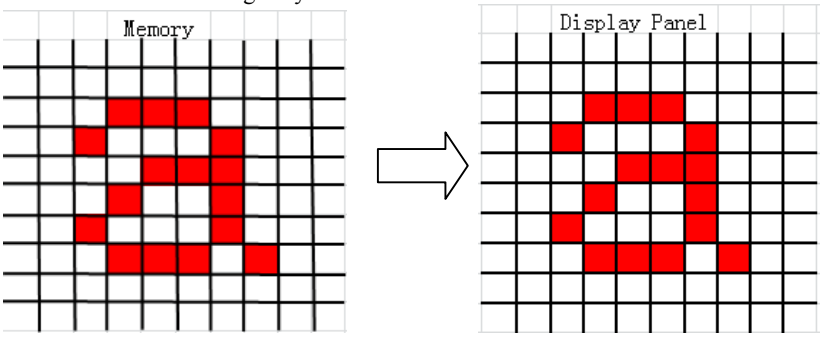
12.1.13. PTLON (12h)

<table>
<tr><th>12H</th><th colspan="11">Partial Display Mode On</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12H</td></tr>
<tr><td>Parameter</td><td colspan="11">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">This command turns on partial mode.The partial mode is described by the Partial Area command (30h).
To leave Partial mode, the Normal Display On command (13h) should be written.
X=Don’t care
Note: If a command is written in a frame cycle, the command becomes effective from the next frame.</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect during Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Normal Display On</td></tr><tr><td>SW Reset</td><td>Normal Display On</td></tr><tr><td>HW Reset</td><td>Normal Display On</td></tr></table></td></tr>
</table>

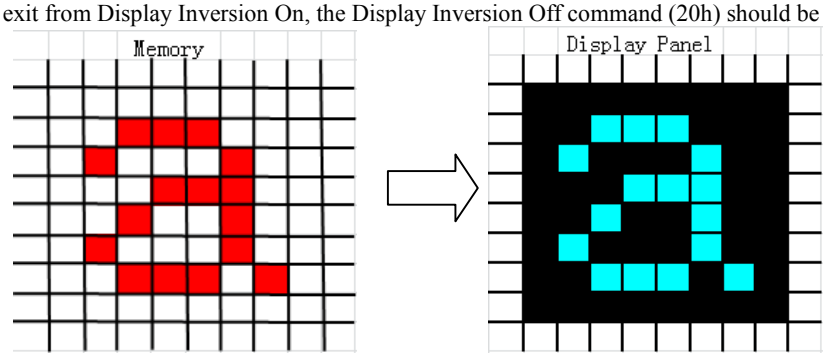
12.1.14. NORON (13h)

<table>
<tr><th>13H</th><th colspan="11">Normal Display Mode On</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13H</td></tr>
<tr><td>Parameter</td><td colspan="11">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">This command returns the display to normal mode.
Normal display mode on means Partial mode off and Scroll mode off.
Exit from NORON by the Partial mode On command (12h)
X=Don’t care
Note: If a command is written in a frame cycle, the command becomes effective from the next frame.</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Normal Display On</td></tr><tr><td>SW Reset</td><td>Normal Display On</td></tr><tr><td>HW Reset</td><td>Normal Display On</td></tr></table></td></tr>
</table>

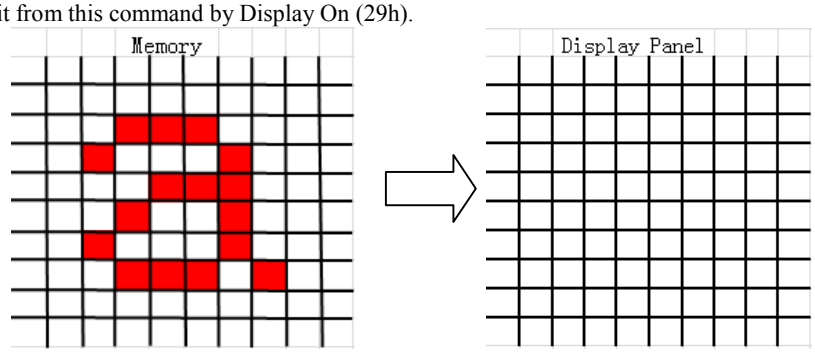
12.1.15. INVOFF (20h)

<table>
<tr><th>20H</th><th colspan="11">Display Inversion Off</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>20H</td></tr>
<tr><td>Parameter</td><td colspan="11">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to recover from display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.
 
</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when module is already in inversion off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="11"><table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>Normal Display On</td></tr>
<tr><td>SW Reset</td><td>Normal Display On</td></tr>
<tr><td>HW Reset</td><td>Normal Display On</td></tr>
</table></td></tr>
</table>

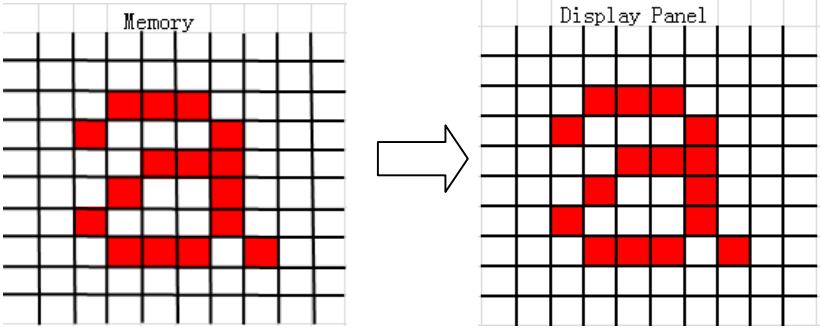
12.1.16. INVON (21h)

<table>
<tr><th>21H</th><th colspan="11">Display Inversion On</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21H</td></tr>
<tr><td>Parameter</td><td colspan="11">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to enter into display inversion mode.
This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.
This command does not change any other status.
To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.
  </td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when module is already in inversion on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Normal Display On</td></tr><tr><td>SW Reset</td><td>Normal Display On</td></tr><tr><td>HW Reset</td><td>Normal Display On</td></tr></table></td></tr>
</table>

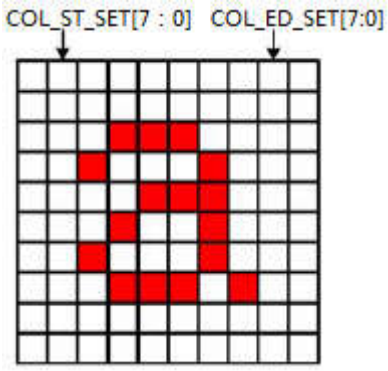
12.1.17. DISPOFF (28h)

<table>
<tr><th>28H</th><th colspan="11">Display Off</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28H</td></tr>
<tr><td>Parameter</td><td colspan="11">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.
Exit from this command by Display On (29h).
 
</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when module is already in display off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="11"><table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>Display Off</td></tr>
<tr><td>SW Reset</td><td>Display Off</td></tr>
<tr><td>HW Reset</td><td>Display Off</td></tr>
</table></td></tr>
</table>

12.1.18 DISPON (29h)

<table>
<tr><th>29H</th><th colspan="11">Display On</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29H</td></tr>
<tr><td>Parameter</td><td colspan="11">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to recover from DISPLAY OFF mode. Output from the Frame Memorry is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
 
</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="11"><table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>Display On</td></tr>
<tr><td>SW Reset</td><td>Display On</td></tr>
<tr><td>HW Reset</td><td>Display On</td></tr>
</table></td></tr>
</table>

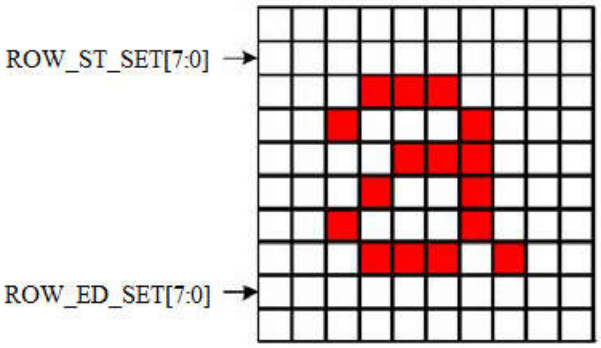
12.1.19 CASET (2Ah)

<table>
<tr><th>2AH</th><th colspan="12">Column Address Set</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2AH</td></tr>
<tr><td>Parameter1</td><td>H</td><td>H</td><td>R</td><td colspan="8">COL_ST_SET[15:8]</td><td>00H</td></tr>
<tr><td>Parameter2</td><td>H</td><td>H</td><td>R</td><td colspan="8">COL_ST_SET[7:0]</td><td>00H</td></tr>
<tr><td>Parameter3</td><td>H</td><td>H</td><td>R</td><td colspan="8">COL_ED_SET[15:8]</td><td>00H</td></tr>
<tr><td>Parameter4</td><td>H</td><td>H</td><td>R</td><td colspan="8">COL_ED_SET[7:0]</td><td>83H</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The value of COL_ST_SET[7:0] and COL_ED_SET[7:0] are referred when RAMWR command comes.
Each value represents one column line in the Frame Memory.
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">XS[7:0] always must be equal to or less than XE[7:0].
When XS[7:0] or XE[7:0] is greater than maximum row address like below, data of out of range wull be ignored.
1. 132x132 memory base(GM=’101’)
(Parameter range:0≦XS[7:0]≦XE[7:0]≦131(0083H)):MV=”0”
(Parameter range:0≦XS[7:0]≦XE[7:0]≦131(0083H)):MV=”1”
2. 130x130 memory base(GM=’100’)
(Parameter range:0≦XS[7:0]≦XE[7:0]≦129(0081H)):MV=”0”
(Parameter range:0≦XS[7:0]≦XE[7:0]≦129(0081H)):MV=”1”
3. 128x160 memory base(GM=’011’)
(Parameter range:0≦XS[7:0]≦XE[7:0]≦127(007FH)):MV=”0”
(Parameter range:0≦XS[7:0]≦XE[7:0]≦159(009FH)):MV=”1”
4. 120x160 memory base(GM=’010’)
(Parameter range:0≦XS[7:0]≦XE[7:0]≦119(0077H)):MV=”0”
(Parameter range:0≦XS[7:0]≦XE[7:0]≦159(009FH)):MV=”1”
5. 128x128 memory base(GM=’001’)
(Parameter range:0≦XS[7:0]≦XE[7:0]≦127(007FH)):MV=”0”
(Parameter range:0≦XS[7:0]≦XE[7:0]≦127(007FH)):MV=”1”
6. 132x162 memory base(GM=’000’)
(Parameter range:0≦XS[7:0]≦XE[7:0]≦131(0083H)):MV=”0”
(Parameter range:0≦XS[7:0]≦XE[7:0]≦127(00A1H)):MV=”1”</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr></table></td></tr>
</table>

	Sleep In: Yes
Default	

Status	Default Value		
(132x132 GM=”101”)	XS[7:0]	XE[7:0]	EX[7:0](MV=1)
Power On Sequence	0000h	0083h(131)	
S/W Reset	0000h	0083h(131)	0083h(131)
H/W Reset	0000h	0083h(131)	
Status	**Default Value**		
(130x130 GM=”100”)	XS[7:0]	XE[7:0]	EX[7:0](MV=1)
Power On Sequence	0000h	0081h(129)	
S/W Reset	0000h	0081h(129)	0081h(129)
H/W Reset	0000h	0081h(129)	
Status	**Default Value**		
(128x160 GM=”011”)	XS[7:0]	XE[7:0]	EX[7:0](MV=1)
Power On Sequence	0000h	007Fh(127)	
S/W Reset	0000h	007Fh(127)	009Fh(159)
H/W Reset	0000h	007Fh(127)	
Status	**Default Value**		
(120x160 GM=”010”)	XS[7:0]	XE[7:0]	EX[7:0](MV=1)
Power On Sequence	0000h	0077h(119)	
S/W Reset	0000h	007Fh(119)	009Fh(159)
H/W Reset	0000h	0077h(119)	
Status	**Default Value**		
(128x128 GM=”001”)	XS[7:0]	XE[7:0]	EX[7:0](MV=1)
Power On Sequence	0000h	007Fh(127)	
S/W Reset	0000h	007Fh(127)	009Fh(127)
H/W Reset	0000h	0077h(119)	
Status	**Default Value**		
(132x162 GM=”000”)	XS[7:0]	XE[7:0]	EX[7:0](MV=1)
Power On Sequence	0000h	0083h(131)	
S/W Reset	0000h	0083h(131)	00A1h(161)
HW Reset	0000h	0083H(131)	

12.1.20 RASET (2Bh)

<table>
<tr><th>2BH</th><th colspan="12">Row Address Set</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>2BH</td></tr>
<tr><td>Parameter1</td><td>H</td><td>H</td><td>R</td><td colspan="8">ROW_ST_SET[15:8]</td><td>00H</td></tr>
<tr><td>Parameter2</td><td>H</td><td>H</td><td>R</td><td colspan="8">ROW_ST_SET[7:0]</td><td>00H</td></tr>
<tr><td>Parameter3</td><td>H</td><td>H</td><td>R</td><td colspan="8">ROW_ED_SET[15:8]</td><td>00H</td></tr>
<tr><td>Parameter4</td><td>H</td><td>H</td><td>R</td><td colspan="8">ROW_ED_SET[7:0]</td><td>A1H</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The value of ROW_ST_SET[7:0] and ROW_ED_SET[7:0] are referred when RAMWR command comes.
Each value represents one Page line in the Frame Memory.
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">YS[7:0] always must be equal to or less than EP[7:0].
When YS[7:0] or YE[7:0] is greater than maximum row address like below,data of out of range wull be ignored.
132x132 memory base(GM=’101’)
(Parameter range:0≦YS[7:0]≦YE[7:0]≦131(0083H)):MV=”0”
(Parameter range:0≦YS[7:0]≦YE[7:0]≦131(0083H)):MV=”1”
130x130 memory base(GM=’100’)
(Parameter range:0≦YS[7:0]≦YE[7:0]≦129(0081H)):MV=”0”
(Parameter range:0≦YS[7:0]≦YE[7:0]≦129(0081H)):MV=”1”
128x160 memory base(GM=’011’)
(Parameter range:0≦YS[7:0]≦YE[7:0]≦159(009FH)):MV=”0”
(Parameter range:0≦YS[7:0]≦YE[7:0]≦127(009FH)):MV=”1”
120x160 memory base(GM=’010’)
(Parameter range:0≦YS[7:0]≦YE[7:0]≦159(009FH)):MV=”0”
(Parameter range:0≦YS[7:0]≦YE[7:0]≦119(007FH)):MV=”1”
128x128 memory base(GM=’001’)
(Parameter range:0≦YS[7:0]≦YE[7:0]≦127(007FH)):MV=”0”
(Parameter range:0≦YS[7:0]≦YE[7:0]≦127(007FH)):MV=”1”
132x162 memory base(GM=’000’)
(Parameter range:0≦YS[7:0]≦YE[7:0]≦161(00A1H)):MV=”0”
(Parameter range:0≦YS[7:0]≦YE[7:0]≦131(0083H)):MV=”1”</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr></table></td></tr>
</table>

	Partial Mode on,ldle Mode On,Sleep Out		Yes
	Sleep In		Yes

Default

Status	**Default Value**		
(132x132 GM=”101”)	YS[7:0]	YE[7:0]	YX[7:0](MV=1)
Power On Sequence	0000h	83h(131)	
S/W Reset	0000h	83h(131)	83h(131)
H/W Reset	0000h	83h(131)	
Status	**Default Value**		
(130x130 GM=”100”)	YS[7:0]	YE[7:0]	YX[7:0](MV=1)
Power On Sequence	0000h	81h(129)	
S/W Reset	0000h	81h(129)	81h(129)
H/W Reset	0000h	81h(129)	
Status	**Default Value**		
(128x160 GM=”011”)	YS[7:0]	YE[7:0]	YX[7:0](MV=1)
Power On Sequence	00h	9Fh(159)	
S/W Reset	00h	9Fh(159)	7Fh(127)
H/W Reset	00h	9Fh(159)	
Status	**Default Value**		
(120x160 GM=”010”)	YS[7:0]	YE[7:0]	YX[7:0](MV=1)
Power On Sequence	00h	9Fh(159)	
S/W Reset	00h	9Fh(159)	77h(119)
H/W Reset	00h	9Fh(159)	
Status	**Default Value**		
(128x128 GM=”001”)	YS[7:0]	YE[7:0]	YX[7:0](MV=1)
Power On Sequence	00h	7Fh(127)	
S/W Reset	00h	7Fh(127)	7Fh(127)
H/W Reset	00h	7Fh(127)	
Status	**Default Value**		
(132x162 GM=”000”)	YS[7:0]	YE[7:0]	YX[7:0](MV=1)
Power On Sequence	00h	A1h(161)	
S/W Reset	00h	A1h(161)	83h(131)
HW Reset	00h	A1h(161)	

12.1.21 RAMWR (2Ch)

<table>
<tr><th>2CH</th><th colspan="12">Memory Write</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2CH</td></tr>
<tr><td>1st Parameter</td><td>H</td><td>H</td><td>R</td><td colspan="8">D[7:0]</td><td>-</td></tr>
<tr><td>|</td><td>H</td><td>H</td><td>R</td><td colspan="8">D[7:0]</td><td>-</td></tr>
<tr><td>Nth Parameter</td><td>H</td><td>H</td><td>R</td><td colspan="8">D[7:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to transfer data from MCU to frame memory.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.
The Start Column /Start Page positions are different in accordance with MADCTL setting.
Then D[7:0] is stored in frame memory and the column refister and the row register incremented.
Sending any other command can stop frame Write.</td></tr>
<tr><td>Restriction</td><td colspan="12">In all color modes, there is no restriction on length of parameters.
1. 132x132 memory base (GM=”101”)
132x132x18-bit memory can be written by this command.
Memorry range(0000h,0000h)->(0083h,083h)
2. 130x130 memory base (GM=”100”)
130x130x18-bit memory can be written by this command.
Memorry range(0000h,0000h)->(0081h,081h)
3. 128x160 memory base (GM=”011”)
128x160x18-bit memory can be written by this command.
Memorry range(0000h,0000h)->(007Fh,09Fh)
4. 120x160 memory base (GM=”010”)
120x160x18-bit memory can be written by this command.
Memorry range(0000h,0000h)->(0077h,09Fh)
5. 128x128 memory base (GM=”001”)
128x128x18-bit memory can be written by this command.
Memorry range(0000h,0000h)->(007Fh,007Fh)
6. 132x162 memory base (GM=”000”)
132x162x18-bit memory can be written by this command.
Memorry range(0000h,0000h)->(0083h,00A1h)</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>HW Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

12.1.22 RAMRD (2Eh)

<table>
<tr><th>2EH</th><th colspan="12">Memory Read</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>R</td><td>H</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>2EH</td></tr>
<tr><td>1st Parameter</td><td>H</td><td>R</td><td>H</td><td colspan="8">D[7:0]</td><td>–</td></tr>
<tr><td>|</td><td>H</td><td>H</td><td>R</td><td colspan="8">D[7:0]</td><td>–</td></tr>
<tr><td>Nth Parameter</td><td>H</td><td>H</td><td>R</td><td colspan="8">D[7:0]</td><td>–</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to transfer data from frame memory to MCU.
This command makes no change to other driver status.
When this command is accepted, the column register and then row register are reset to the Start Column/Start Row positions.
The Start Column/Start Row positions are different in accordance with MADCTL setting.
Then D[7:0] is read back from the frame memory and the column register and the register incremented.
Frame Read can be stopped by sending any other command.
Display Data Format for color coding (18 bit cases), when there is used 8,9,16 or 18 data line for image data.</td></tr>
<tr><td>Restriction</td><td colspan="12">In all color modes, the Frame Read is always 24 bit so there is no restriction on length of parameters.
Note: Memory Read is only possible via the Parallel Interface.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>HW Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

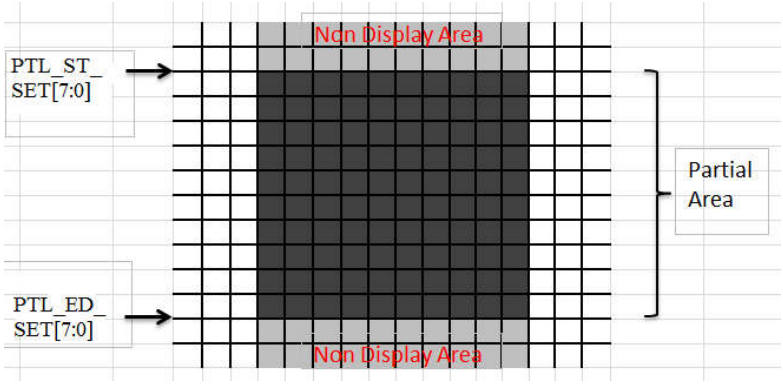
12.1.23 PTLAR(30h)

30H	Partial Area											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	0	0	1	1	0	0	0	0	30H
Parameter1	H	H	R	PTL_ST_SET[15:8]								00H
Parameter2	H	H	R	PTL_ST_SET[7:0]								00H
Parameter3	H	H	R	PTL_ED_SET[15:8]								00H
Parameter4	H	H	R	PTL_ED_SET[7:0]								a1H

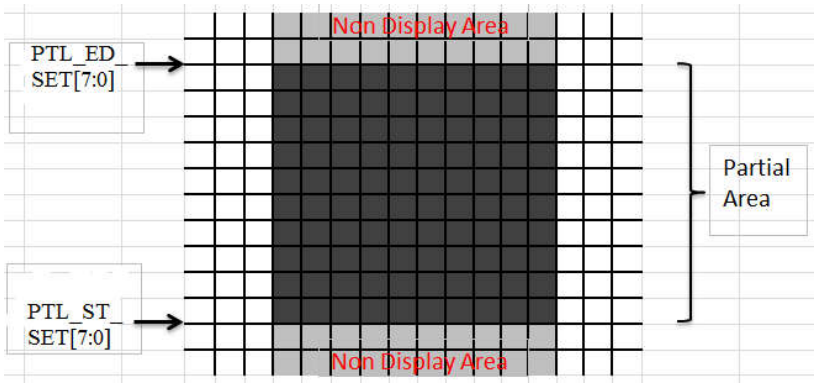
Description

This command defines the partial mode's display area.There are 4 parameters associated with this command, the first defines the Start Row(PSL) and the second the End Row(PEL),as illustrated in the figure below.PSL and PEL refer to the Frame Memory Line Pointer.

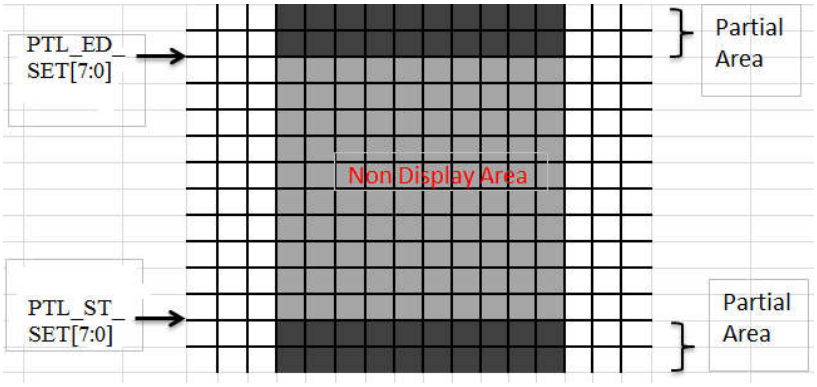
If End Row>Start Row when MADCTL B4=0:



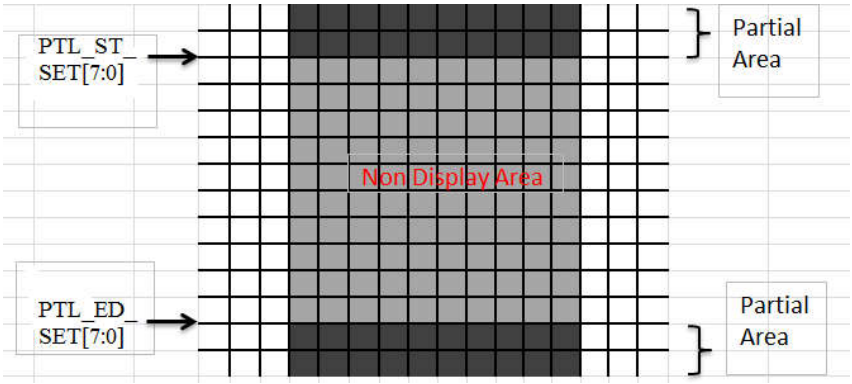
If End Row>Start Row when MADCTL ML=1:



If End Row<Start Row when MADCTL ML=0:



If End Row<Start Row when MADCTL ML=1:



If End Row=Start Row then the Partial Area will be one row deep.

Restriction	No Restriction

Register Availability

Status	Availability
Normal Mode on,ldle Mode Off,Sleep Out	Yes
Normal Mode on,ldle Mode On,Sleep Out	Yes
Partial Mode on,ldle Mode Off,Sleep Out	Yes
Partial Mode on,ldle Mode On,Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value						
	PSL[7:0]	PEL[7:0]					
GM	"xxx"	"101"	"100"	"011"	"010"	"001"	"000"
Power On Sequence	00h	83h	81h	9Fh	9Fh	7Fh	A1h
SW Reset	00h	83h	81h	9Fh	9Fh	7Fh	A1h
HW Reset	00h	83h	81h	9Fh	9Fh	7Fh	A1h

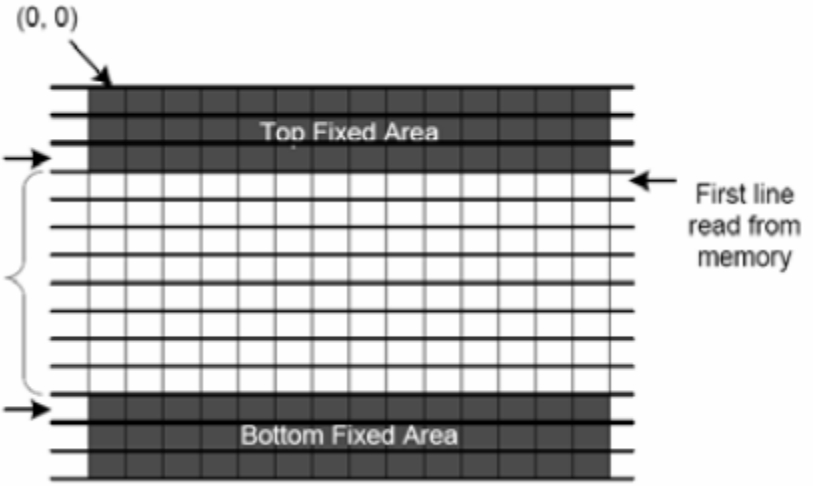
12.1.24 SCRLAR (33h)

33H	Scroll Area											
	D/CX	**RDX**	**WRX**	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	0	0	1	1	0	0	1	1	33H
Parameter1	H	H	R	TFA[15:8]								00H
Parameter2	H	H	R	TFA[7:0]								00H
Parameter3	H	H	R	VSA[15:8]								00H
Parameter4	H	H	R	VSA[7:0]								00H

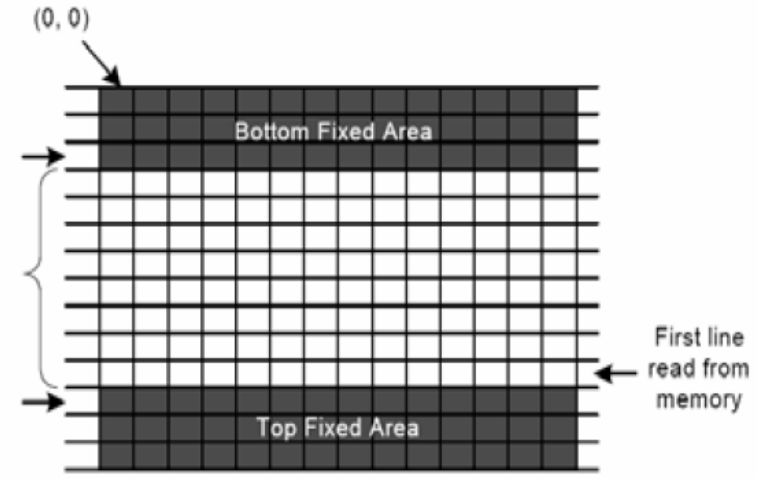
Description

This command defines the Vertical Scrolling Area of the display.
When MADCTL ML=0
The 1st &2nd parameter TFA[7:0]describes the Top Fixed Area (in No.of lines from TOP of the Frame Memory and Display).
The 3rd &4th parameter VSA[7:0]describes the height of the Vertical Scrolling Area(in No.of lines of the Frame Memory[not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

TFA, VSA refer to the Frame Memory Line Point.



When MADCTL ML=1
The 1st &2nd parameter TFA[7:0] describes the Top Fixed Area (in No.of lines from Bottom of the Frame Memory and Display).
The 3rd &4th parameter VSA[7:0] describes the height of the Vertical Sxrolling Area (in No.of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.



Restriction

The condition is (TFA+VSA+BFA)=128 in 128RGBx128(GM=”001”)
The condition is (TFA+VSA+BFA)=130 in 130RGBx130(GM=”100”)
The condition is (TFA+VSA+BFA)=132 in 132RGBx132(GM=”101”)
The condition is (TFA+VSA+BFA)=160 in 128RGBx160(GM=”011”)
or 120 RGB x 160 (GM=”010”)
The condition is (TFA+VSA+BFA)=162 in 132RGBx162(GM=”000”)
Otherwise Scrolling mode is undefined.
In Vertical Scrol Mode,MADCTL parameter MV should be set to “0”
this affects the Frame memory Write.

Register Availability

Status	Availability
Normal Mode on,ldle Mode Off,Sleep Out	Yes
Normal Mode on,ldle Mode On,Sleep Out	Yes
Partial Mode on,ldle Mode Off,Sleep Out	Yes
Partial Mode on,ldle Mode On,Sleep Out	Yes
Sleep In	Yes

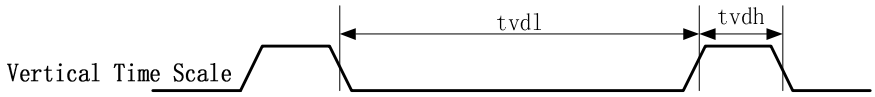
Default

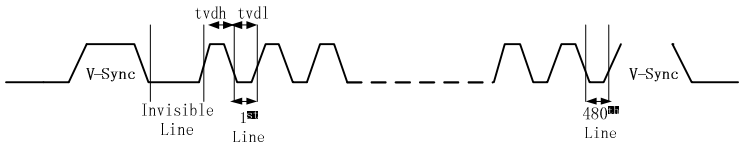
Status	Defalut Value						
	TFA[7:0]	VSA[7:0]					
GM	"xx"	"101"	"100"	"011"	"010"	"001"	"000"
Power On Sequence	00h	83h	81h	A0h	A0h	80h	A2h
SW Reset	00h	83h	81h	A0h	A0h	80h	A2h
HW Reset	00h	83h	81h	A0h	A0h	80h	A2h

12.1.25 TEOFF (34h)

<table>
<tr><th>34H</th><th colspan="12">Tearing Effect Line Off</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34H</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to turn OFF (Active Low) the Tearing Effect output single from the TE signal line.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
</table>

12.1.26 TEON (35h)

<table>
<tr><th>35H</th><th colspan="11">Tearing Effect Line On</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>TELOM</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to turn ON the Tearing Effect output signal from the TE signal line.This output is not affected by charging MADCTL bit ML.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don’t Care).
When TELOM=0:
The Tearing Effect Output line consists of V-Blanking information only:
 

When TELOM =1:
The Tearing Effect Output line consists of both V-Blanking and H-Blanking information:
 

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active LOW.
Display Data Format for color coding (18 bit cases), when there is used 8,9,16 or 18 data line for image data.</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when Tearing Effect output is already ON.</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Tearing effect off & M=0</td></tr><tr><td>SW Reset</td><td>Tearing effect off & M=0</td></tr><tr><td>HW Reset</td><td>Tearing effect off & M=0</td></tr></table></td></tr>
</table>

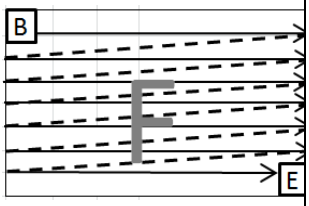
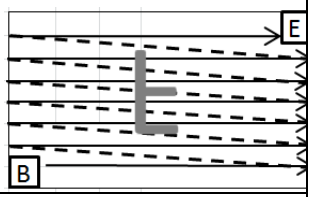
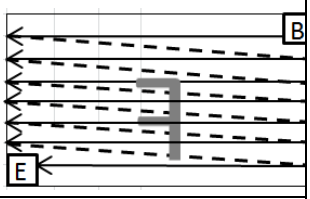
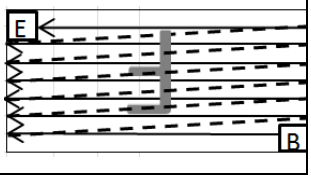
12.1.27 MADCTR (36h)

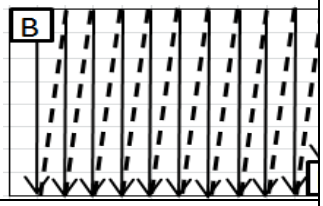
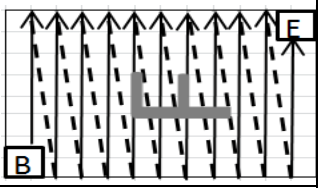
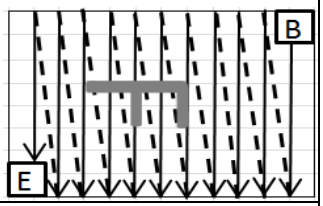
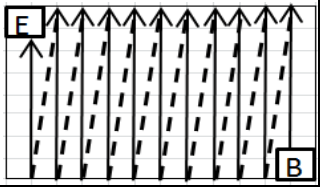
36H	Memory Data Access Control											
	D/CX	**RDX**	**WRX**	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	0	0	1	1	0	1	1	0	36H
Parameter	H	H	R	MY	MX	MV	ML	RGB	0	0	0	08H

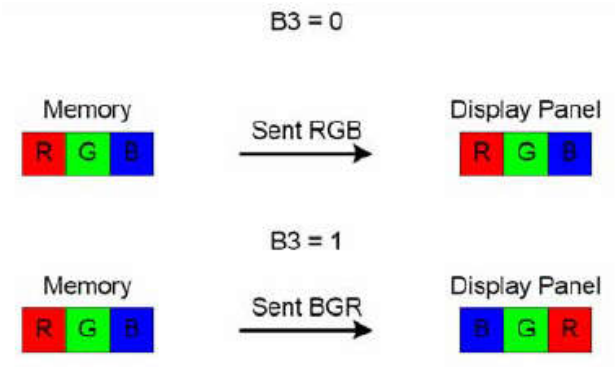
Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.
Bit Assignment

Bit	Description	Value
MY	Row Address Order	These 3 bits controls MPU to memory write/read direction.
MX	Column Address Order	
MV	Page/Column Selection	
ML	Vertical Order	LCD Vertical refresh direction control
RGB	RGB/BGR Order	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel

B5	B6	B7	Image in Frame Memory
0	0	0	
0	0	1	
0	1	0	
0	1	1	

B5	B6	B7	Image in Frame Memory
1	0	0	
1	0	1	
1	1	0	
1	1	1	

<table>
<tr><td></td><td> 
</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>08H</td></tr>
<tr><td>SW Reset</td><td>08H</td></tr>
<tr><td>HW Reset</td><td>08H</td></tr>
</table>
</td></tr>
</table>

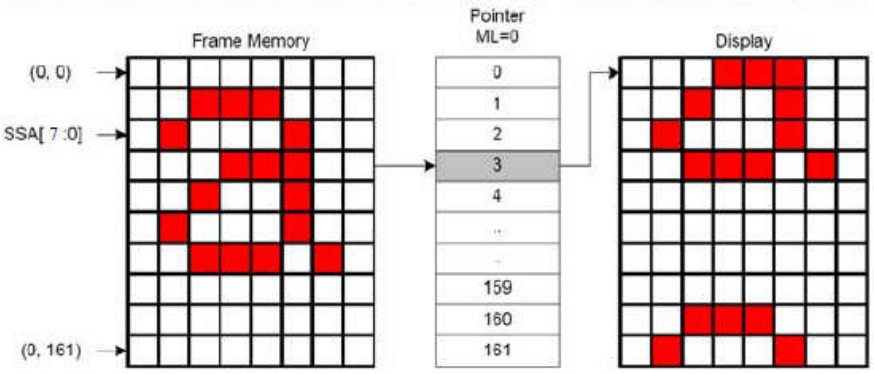
12.1.28 VSCSAD (37h)

37H	Vertical Scroll Start Address of RAM											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	0	0	1	1	0	1	1	1	37H
Parameter1	H	H	R	SSA[15:8]								00H
Parameter2	H	H	R	SSA[7:0]								00H

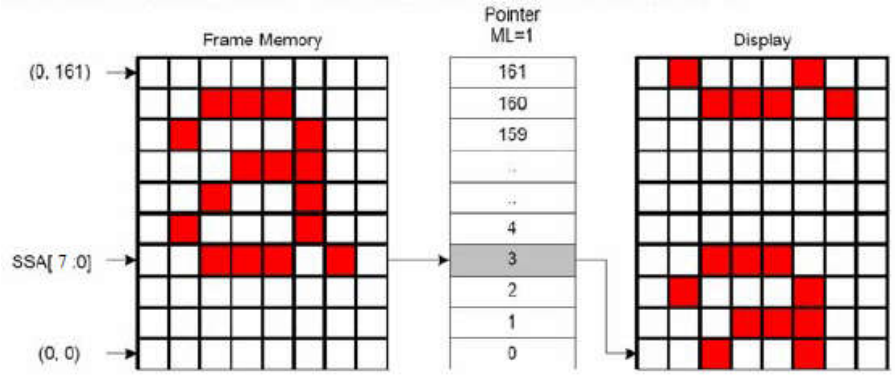
Description

This command is used together with Vertical Scrolling Definition(33h).These two command describe the scrolling area and scrolling mode.
The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last lin of the Top Fixed Area on thd display as illustrated below.
This command Start the scrolling.

When MADCTL ML=0
Exanple: GM=000,132RGBx162
When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=162 and Vertical Scrolling Pointer SSA=”3”.



When MADCTL ML=1
Exanple:GM=000,132RGBx162
When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=162 and SSA=”3”.



Note:
When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. SSA refers to the Frame Memory scan address.
When new Pointer position and Picture Data, internal system works as 128x128 and maximum scan address becomes 127 internal of 161.

Restriction

Register Availability

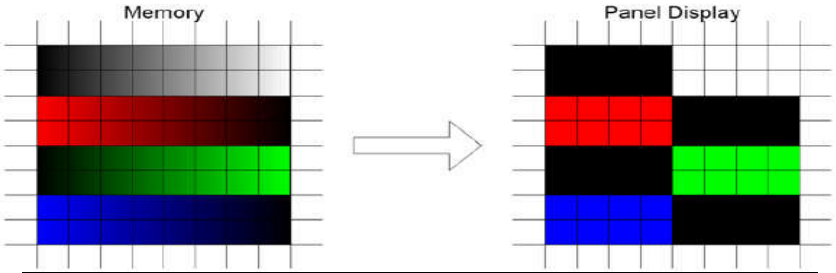
Status	Availability

	Normal Mode on,ldle Mode Off,Sleep Out: Yes Normal Mode on,ldle Mode On,Sleep Out: Yes Partial Mode on,ldle Mode Off,Sleep Out: Yes Partial Mode on,ldle Mode On,Sleep Out: Yes Sleep In: Yes
Default	**Status** / **Default Value** Power On Sequence: 8'h00 SW Reset: 8'h00 HW Reset: 8'h00

12.1.29 IDMOFF (38h)

<table>
<tr><td>38H</td><td colspan="11">Idle Mode Off</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38H</td></tr>
<tr><td>Parameter</td><td colspan="11">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">This commad is used to recover from Idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the Idle off mode
1, LCD can display maximum 4096, 65k, 262k colors.
2, Normal frame frequency is applied.</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when module is already in Idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>SW Reset</td><td>Idle Mode Off</td></tr><tr><td>HW Reset</td><td>Idle Mode Off</td></tr></table></td></tr>
</table>

12.1.30 IDMON (39h)

<table>
<tr><th>39H</th><th colspan="11">Idle Mode On</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39H</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to enter into Idle mode on.
There will be no abnormal visible effect on the display mode change tranition.
In the Idle mode.
Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
8-Color mode frame frequency is applied.
Exit from IDMON by Idle Mode Off (38h) command.
 

<table>
<tr><th>Reduced Color</th><th>R[5:0]</th><th>G[5:0]</th><th>B[5:0]</th></tr>
<tr><td>Black</td><td>0XXXX</td><td>0XXXX</td><td>0XXXX</td></tr>
<tr><td>Blue</td><td>0XXXX</td><td>0XXXX</td><td>1XXXX</td></tr>
<tr><td>Red</td><td>1XXXX</td><td>0XXXX</td><td>0XXXX</td></tr>
<tr><td>Magenta</td><td>1XXXX</td><td>0XXXX</td><td>1XXXX</td></tr>
<tr><td>Green</td><td>0XXXX</td><td>1XXXX</td><td>0XXXX</td></tr>
<tr><td>Cyan</td><td>0XXXX</td><td>1XXXX</td><td>1XXXX</td></tr>
<tr><td>Yellow</td><td>1XXXX</td><td>1XXXX</td><td>0XXXX</td></tr>
<tr><td>White</td><td>1XXXX</td><td>1XXXX</td><td>1XXXX</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in idle on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>Idle Mode On</td></tr>
<tr><td>SW Reset</td><td>Idle Mode On</td></tr>
<tr><td>HW Reset</td><td>Idle Mode On</td></tr>
</table></td></tr>
</table>

12.1.31 COLMOD (3Ah)

<table>
<tr><th>3AH</th><th colspan="12">Interface Color Mode Set</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3AH</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td colspan="5">VIPF[3:0]</td><td>0</td><td colspan="3">IFPF[2:0]</td><td>66H</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define the format of RGB picture data,which is to be transferred via the MCU interface.The formats are shown in the table:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>VIPF3</td><td rowspan="4">RGB Interface Color Format</td><td rowspan="4">"0101"=16 bit/pixel(1 time data transfer)
"0110"=18 bit/pixel(1 time data transfer)
"1110"=18 bit/pixel(3 time data transfer)
The others=not defined</td></tr>
<tr><td>VIPF2</td></tr>
<tr><td>VIPF1</td></tr>
<tr><td>VIPF0</td></tr>
<tr><td>D3</td><td></td><td>"0"(Not Used)</td></tr>
<tr><td>IFPF2</td><td rowspan="3">Control Interface Color Format</td><td rowspan="3">"011"=12 bit/pixel
"101"=16 bit/pixel
"110"=18 bit/pixel
The others=not defined</td></tr>
<tr><td>IFPF1</td></tr>
<tr><td>IFPF0</td></tr>
</table>
Note:
1. In 12-bits /Pixel, 16-bits/Pixel mode, the LUT is applied to transfer data into the Frame Memory.
2. When VIPF[3:0]=1110, 6-bits data width of 3-times transfer is used to transmin 1 pixel data with the 18-bits color depth information.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in Idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h66</td></tr>
<tr><td>SW Reset</td><td>8’h66</td></tr>
<tr><td>HW Reset</td><td>8’h66</td></tr>
</table></td></tr>
</table>

12.1.32 RDID1 (DAh)

DAH	Read ID1 Value											
	D/CX	**RDX**	**WRX**	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	1	0	1	1	0	1	0	DAH
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X
Parameter2	H	R	H	SYS_ID1[7:0]								33H
Description	The 1st Parameter is dummy read. This read byte return 8-bit LCD module's ID. The parameter(SYS_ID7- SYS_ID0): LCD module manufacturer ID											
Restriction	Should set "FF=A5" before configure this registers											
Register Availability												

Status	Availability
Normal Mode on,ldle Mode Off,Sleep Out	Yes
Normal Mode on,ldle Mode On,Sleep Out	Yes
Partial Mode on,ldle Mode Off,Sleep Out	Yes
Partial Mode on,ldle Mode On,Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value(D7 to D0)
Power On Sequence	8'h33
SW Reset	8'h33
HW Reset	8'h33

12.1.33 RDID2 (DBh)

<table>
<tr><th>DBH</th><th colspan="12">Read ID2 Value</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>DBH</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td colspan="8">SYS_ID2[7:0]</td><td>30H</td></tr>
<tr><td>Description</td><td colspan="12">The 1st Parameter is dummy read.
This read byte return 8-bit LCD module’s ID.</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h30</td></tr><tr><td>SW Reset</td><td>8’h30</td></tr><tr><td>HW Reset</td><td>8’h30</td></tr></table></td></tr>
</table>

12.1.34 RDID3 (DCh)

<table>
<tr><th>DCH</th><th colspan="12">Read ID3 Value</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>DCH</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td colspan="8">SYS_ID3[7:0]</td><td>23H</td></tr>
<tr><td>Description</td><td colspan="12">The 1st Parameter is dummy read.
This read byte return 8-bit LCD module’s ID.</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h23</td></tr><tr><td>SW Reset</td><td>8’h23</td></tr><tr><td>HW Reset</td><td>8’h23</td></tr></table></td></tr>
</table>

12.2 Panel Function Command List and Description

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x3D	SPI2SET	W					spi2line_en		spi2line_mode[1:0]	
0x51	PWCTR 1	W				ddvdh_clp_en		ddvdh_clamp[2:0]		
0x52	PWCTR 2	W				vgh_clp_en			vgh_clamp[1:0]	
0x53	PWCTR 3	W				vgl_clp_en			vgl_clamp[1:0]	
0x61	FRMCTR1	W	hbp[7:0]							
0x62	FRMCTR2	W	hfp[7:0]							
0x63	FRMCTR3	W		vbp[6:0]						
0x64	FRMCTR4	W		vfp[6:0]						
0x82	RGBCTR	W					dpi_dp	dpi_ep	dpi_hsp	dpi_vsp
0x84	GATEST	W	gate_st[7:0]							
0x85	GATEED	W	gate_ed[7:0]							
0x87	PWCTR 4	W				vrh[4:0]				
0x88	VMCTR 1	W			vcm[5:0]					
0x89	VMCTR 2	W			vcom_vdv[5:0]					
0x93	SRCSET	W				ndl			src_en_sel	polar_sel
0x94	SRCST	W	src_st[7:0]							
0x95	PCHGST	W	pchg_st[7:0]							
0xB1	PWCTR 5	W					bth[1:0]		btl[1:0]	
0xB2	PWCTR 6	W	ddvdh_clk_sel[1:0]		vgh_clk_sel[1:0]		vgl_clk_sel[1:0]		vcl_clk_sel[1:0]	
0xB6	VMBIAS	W							vcom_bias_fix[1:0]	
0xC3	REV	W				src_ss				gate_gs
0xC4	VDD18	W					regu_ad[2:0]			
0xD1	RDOTP 1	R	otp_rd_dat[7:0]							
0xD2	RDO	R	otp_rd_dat[15:8]							

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
	TP 2									
0xD3	RDO TP 3	R	otp_rd_dat[23:16]							
0xD4	RDO TP 4	R	otp_rd_dat[31:24]							
0xE1	OTPC TR 1	W			otp_ptm[1:0]		otp_vpp_sel	otp_prog	otp_wr_en	otp_rd_en
0xE2	OTPC TR 2	W		otp_addr[6:0]						
0xE3	OTPC TR 3	W	otp_wr_dat[7:0]							
0xE4	OTPC TR 4	W							otp_esd_en	otp_slpout_en

12.2.1 SPI2SET (3Dh)

<table>
<tr><th>3DH</th><th colspan="12">SPI 2 Line Set</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>3DH</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>SPI2LINE_EN</td><td>0</td><td colspan="2">SPI2LINE_MODE[1:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="12">SPI2LINE_EN: Enable SPI two data line function. “0” is ON,”1” is OFF;
SPI2LINE_MODE[1:0]: Select different data combination on data lines.

<table><tr><th>MODE[1:0]</th><th>Pixel format</th><th>Transmit method</th></tr><tr><td>00</td><td rowspan="2">5-6-5</td><td rowspan="2">One transmit per pixel</td></tr><tr><td>11</td></tr><tr><td>01</td><td>6-6-6</td><td>One transmit per pixel</td></tr><tr><td>10</td><td>6-6-6</td><td>Three transmits each two pixels</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

;

12.2.2 PWCTR1 (51h)

<table>
<tr><th>51H</th><th colspan="12">Power Control 1</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>51H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>DDVDH_CLP_EN</td><td>0</td><td colspan="3">DDVDH_CLAMP[2:0]</td><td>13H</td></tr>
<tr><td>Description</td><td colspan="12">DDVDH_CLP_EN: This command is used to define DDVDH clamp enable.

<table>
<tr><th>DDVDH_CLP_EN</th><th>Description</th></tr>
<tr><td>0</td><td>Disable the clamp</td></tr>
<tr><td>1</td><td>Enable the clamp</td></tr>
</table>

DDVDH_CLAMP[2:0]: This command is used to define DDVDH clamp value
<table>
<tr><th>DDVDH_CLAMP[1:0]</th><th>DDVDH (V)</th></tr>
<tr><td>000</td><td>4.5</td></tr>
<tr><td>001</td><td>4.6</td></tr>
<tr><td>010</td><td>4.7</td></tr>
<tr><td>011</td><td>4.8</td></tr>
<tr><td>100</td><td>4.9</td></tr>
<tr><td>101</td><td>5</td></tr>
<tr><td>110</td><td>5.1</td></tr>
<tr><td>111</td><td>5.2</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h13</td></tr>
<tr><td>SW Reset</td><td>8’h13</td></tr>
<tr><td>HW Reset</td><td>8’h13</td></tr>
</table></td></tr>
</table>

12.2.3 PWCTR 2 (52h)

<table>
<tr><td>52H</td><td colspan="12">Power Control 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>52H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>VGH_CLP_EN</td><td>0</td><td>0</td><td colspan="2">VGH_CLAMP[1:0]</td><td>13H</td></tr>
<tr><td>Description</td><td colspan="12">VGH_CLP_EN: This command is used to define VGH clamp enable.
<table>
<tr><th>VGH_CLP_EN</th><th>Description</th></tr>
<tr><td>0</td><td>Disable the clamp</td></tr>
<tr><td>1</td><td>Enable the clamp</td></tr>
</table>
VGH_CLAMP[1:0]: This command is used to define VGH clamp value.
<table>
<tr><th>VGH_CLAMP[1:0]</th><th>VGH (unit:V)</th></tr>
<tr><td>00</td><td>10</td></tr>
<tr><td>01</td><td>12</td></tr>
<tr><td>10</td><td>13.5</td></tr>
<tr><td>11</td><td>15</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h13</td></tr>
<tr><td>SW Reset</td><td>8’h13</td></tr>
<tr><td>HW Reset</td><td>8’h13</td></tr>
</table></td></tr>
</table>

12.2.4 PWCTR 3 (53h)

<table>
<tr><td>53H</td><td colspan="12">Power Control 3</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>53H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>VGL_CLP_EN</td><td>0</td><td>0</td><td colspan="2">VGL_CLAMP[1:0]</td><td>10H</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to set the VGL clamp voltage.
<table>
<tr><th>VGL_CLAMP[1]</th><th>VGL_CLAMP[0]</th><th>VGL</th></tr>
<tr><td>0</td><td>0</td><td>-7.5</td></tr>
<tr><td>0</td><td>1</td><td>-10</td></tr>
<tr><td>1</td><td>0</td><td>-12.5</td></tr>
<tr><td>1</td><td>1</td><td>-13</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h10</td></tr>
<tr><td>SW Reset</td><td>8’h10</td></tr>
<tr><td>HW Reset</td><td>8’h10</td></tr>
</table></td></tr>
</table>

12.2.5 FRMCTR 1 (61h)

<table>
<tr><td>61H</td><td colspan="12">Frame Rate Control 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>61H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td colspan="8">HBP[7:0]</td><td>05H</td></tr>
<tr><td>Description</td><td colspan="12">Internal frame rate control register, used to enlarge horizontal scan cycle.
Frame rate=fosc/2*(131+HBP+HFP)*(162+VBP+VFP)
Fosc=6MHz</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h05</td></tr><tr><td>SW Reset</td><td>8’h05</td></tr><tr><td>HW Reset</td><td>8’h05</td></tr></table></td></tr>
</table>

12.2.6 FRMCTR 2 (62h)

<table>
<tr><td>62H</td><td colspan="12">Frame Rate Control 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>62H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td colspan="8">HFP[7:0]</td><td>05H</td></tr>
<tr><td>Description</td><td colspan="12">Internal frame rate control register, used to enlarge horizontal scan cycle.
Frame rate=fosc/2*(131+HBP+HFP)*(162+VBP+VFP)
Fosc=6MHz</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h05</td></tr><tr><td>SW Reset</td><td>8’h05</td></tr><tr><td>HW Reset</td><td>8’h05</td></tr></table></td></tr>
</table>

12.2.7 FRMCTR 3 (63h)

<table>
<tr><td>63H</td><td colspan="12">Frame Rate Control 3</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>63H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td colspan="7">VBP[6:0]</td><td>02H</td></tr>
<tr><td>Description</td><td colspan="12">Internal frame rate control register, used to enlarge vertical scan cycle.
Frame rate=fosc/2*(131+HBP+HFP)*(162+VBP+VFP)
Fosc=6MHz</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h02</td></tr><tr><td>SW Reset</td><td>8’h02</td></tr><tr><td>HW Reset</td><td>8’h02</td></tr></table></td></tr>
</table>

12.2.8 FRMCTR 4 (64h)

<table>
<tr><td>64H</td><td colspan="12">Frame Rate Control 4</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>64H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td colspan="7">VFP[6:0]</td><td>02H</td></tr>
<tr><td>Description</td><td colspan="12">Internal frame rate control register, used to enlarge vertical scan cycle.
Frame rate=fosc/2*(131+HBP+HFP)*(162+VBP+VFP)
Fosc=6MHz</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h02</td></tr><tr><td>SW Reset</td><td>8’h02</td></tr><tr><td>HW Reset</td><td>8’h02</td></tr></table></td></tr>
</table>

12.2.9 RGBCTR (82h)

<table>
<tr><td>82H</td><td colspan="12">RGB Interface Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>82H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DPI_DP</td><td>DPI_EP</td><td>DPI_HSP</td><td>DPI_VSP</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="12">DPI_DP : PCLK polarity (“1”= data fetched at falling time, “0”= data fetched at rising time);
DPI_EP : DE polarity (“1”= Low enable, “0”=High enable)
DPI_HSP: HS polarity(“1”=Low level sync clock, “0”=High level sync clock)
DPI_VSP: VS polarity(“1”=Low level sync clock, “0”=High level sync clock)</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

12.2.10 GATEST (84h)

<table>
<tr><td>84H</td><td colspan="12">GATE START SETTING</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>84H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td colspan="8">GATE_ST[7:0]</td><td>14H</td></tr>
<tr><td>Description</td><td colspan="12">Gate enables start position setting.</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h14</td></tr><tr><td>SW Reset</td><td>8’h14</td></tr><tr><td>HW Reset</td><td>8’h14</td></tr></table></td></tr>
</table>

12.2.11 GATEED (85h)

<table>
<tr><td>85H</td><td colspan="12">GATE END SETTING</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>85H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td colspan="8">GATE_ED[7:0]</td><td>78H</td></tr>
<tr><td>Description</td><td colspan="12">Gate enables end position setting.</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h78</td></tr><tr><td>SW Reset</td><td>8’h78</td></tr><tr><td>HW Reset</td><td>8’h78</td></tr></table></td></tr>
</table>

12.2.12 PWCTR 4 (87h)

<table>
<tr><td>87H</td><td colspan="12">Power Control 4</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>87H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td colspan="5">VRH[4:0]</td><td>17H</td></tr>
<tr><td>Description</td><td colspan="12">VRH[4:0]: This command is used to define GVDD trimming value.
<table>
<tr><th>VRH[4:0]</th><th>GVDD</th><th>VRH[4:0]</th><th>GVDD</th></tr>
<tr><td>00100</td><td>3.55</td><td>10000</td><td>4.15</td></tr>
<tr><td>00101</td><td>3.60</td><td>10001</td><td>4.20</td></tr>
<tr><td>00110</td><td>3.65</td><td>10010</td><td>4.25</td></tr>
<tr><td>00111</td><td>3.70</td><td>10011</td><td>4.30</td></tr>
<tr><td>01000</td><td>3.75</td><td>10100</td><td>4.35</td></tr>
<tr><td>01001</td><td>3.80</td><td>10101</td><td>4.40</td></tr>
<tr><td>01010</td><td>3.85</td><td>10110</td><td>4.45</td></tr>
<tr><td>01011</td><td>3.90</td><td>10111</td><td>4.50</td></tr>
<tr><td>01100</td><td>3.95</td><td>11000</td><td>4.55</td></tr>
<tr><td>01101</td><td>4.00</td><td>11001</td><td>4.60</td></tr>
<tr><td>01110</td><td>4.05</td><td>11010</td><td>4.65</td></tr>
<tr><td>01111</td><td>4.10</td><td>11011</td><td>4.70</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h17</td></tr>
<tr><td>SW Reset</td><td>8’h17</td></tr>
<tr><td>HW Reset</td><td>8’h17</td></tr>
</table></td></tr>
</table>

12.2.13 VMCTR 1 (88h)

88H	VCOM Control 1											
	D/CX	**RDX**	**WRX**	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	0	0	0	1	0	0	0	88H
Parameter	H	H	R	0	0	VCM[5:0]						17H

Description

VCM[5:0]: This command is used to define VCOMH trimming value.

VCM[5:0]	VCOMH	VCM[5:0]	VCOMH
000100	3.1725	100000	3.8025
000101	3.195	100001	3.825
000110	3.2175	100010	3.8475
000111	3.24	100011	3.87
001000	3.2625	100100	3.8925
001001	3.285	100101	3.915
001010	3.3075	100110	3.9375
001011	3.33	100111	3.96
001100	3.3525	101000	3.9825
001101	3.375	101001	4.005
001110	3.3975	101010	4.0275
001111	3.42	101011	4.05
010000	3.4425	101100	4.0725
010001	3.465	101101	4.095
010010	3.4875	101110	4.1175
010011	3.51	101111	4.14
010100	3.5325	110000	4.1625
010101	3.555	110001	4.185
010110	3.5775	110010	4.2075
010111	**3.6**	110011	4.23
011000	3.6225	110100	4.2525
011001	3.645	110101	4.275
011010	3.6675	110110	4.2975
011011	3.69	110111	4.32
011100	3.7125	111000	4.3425
011101	3.735	111001	4.365
011110	3.7575	111010	4.3875
011111	3.78	111011	4.41

Restriction: Should set “FF=A5” before configure this registers

Register Availability

Status	Availability
Normal Mode on,ldle Mode Off,Sleep Out	Yes
Normal Mode on,ldle Mode On,Sleep Out	Yes
Partial Mode on,ldle Mode Off,Sleep Out	Yes

<table>
<tr><td></td><td>
<table>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h13</td></tr>
<tr><td>SW Reset</td><td>8’h13</td></tr>
<tr><td>HW Reset</td><td>8’h13</td></tr>
</table>
</td></tr>
</table>

12.2.14 VMCTR 2 (89h)

89H	VCOM Control 2											
	D/CX	**RDX**	**WRX**	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	0	0	0	1	0	0	1	89H
Parameter	H	H	R	0	0	VCOM_VDV[5:0]						1cH

Description

VCOM_VDV[5:0]: This command is used to define VCOML trimming value.

VCOM_VDV[5:0]	VCOML	VCOM_VDV[5:0]	VCOML
000100	-0.36	100000	-1.1025
000101	-0.405	100001	-1.125
000110	-0.45	100010	-1.1475
000111	-0.495	100011	-1.17
001000	-0.54	100100	-1.1925
001001	-0.585	100101	-1.215
001010	-0.6075	100110	-1.2375
001011	-0.63	100111	-1.26
001100	-0.6525	101000	-1.2825
001101	-0.675	101001	-1.305
001110	-0.6975	101010	-1.3275
001111	-0.72	101011	-1.35
010000	-0.7425	101100	-1.3725
010001	-0.765	101101	-1.395
010010	-0.7875	101110	-1.4175
010011	-0.81	101111	-1.44
010100	-0.8325	110000	-1.4625
010101	-0.855	110001	-1.485
010110	-0.8775	110010	-1.5075
010111	-0.9	110011	-1.53
011000	-0.9225	110100	-1.5525
011001	-0.945	110101	-1.575
011010	-0.9675	110110	-1.5975
011011	-0.99	110111	-1.6425
011100	**-1.0125**	111000	-1.6875
011101	-1.035	111001	-1.7325
011110	-1.0575	111010	-1.7775
011111	-1.08	111011	-1.8225

Note: This value need VCOMH set in 3.5V

Restriction: Should set “FF=A5” before configure this registers

Register Availability

Status	Availability
Normal Mode on,ldle Mode Off,Sleep Out	Yes
Normal Mode on,ldle Mode On,Sleep Out	Yes
Partial Mode on,ldle Mode Off,Sleep Out	Yes
Partial Mode on,ldle Mode On,Sleep Out	Yes
Sleep In	Yes

<table>
<tr><td></td><td></td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h0F</td></tr>
<tr><td>SW Reset</td><td>8’h0F</td></tr>
<tr><td>HW Reset</td><td>8’h0F</td></tr>
</table>
</td></tr>
</table>

12.2.15 SRCSET (93h)

<table>
<tr><td>93H</td><td colspan="12">SOURCE SET</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>93H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>NDL</td><td>0</td><td>0</td><td>SRC_EN_SEL</td><td>POLAR_SEL</td><td>10H</td></tr>
<tr><td>Description</td><td colspan="12">NDL: Select max or min voltage to clear screen.
SRC_EN_SEL: Decide if the source enable is open during v-porch area. “1” is OPEN, “0” is CLOSE;
POLAR_SEL:”1” is line inverse, “0” is frame inverse</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h10</td></tr><tr><td>SW Reset</td><td>8’h10</td></tr><tr><td>HW Reset</td><td>8’h10</td></tr></table></td></tr>
</table>

12.2.16 SRCST (94h)

<table>
<tr><td>94H</td><td colspan="12">SOURCE START SETTING</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>94H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td colspan="8">SRC_ST[7:0]</td><td>10H</td></tr>
<tr><td>Description</td><td colspan="12">src_out_ctrl start position setting.</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h0A</td></tr><tr><td>SW Reset</td><td>8’h0A</td></tr><tr><td>HW Reset</td><td>8’h0A</td></tr></table></td></tr>
</table>

12.2.17 PCHGST (95h)

<table>
<tr><td>95H</td><td colspan="11">SOURCE PRECHARGE START SETTING</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>95H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td colspan="8">PCHG_ST[7:0]</td><td>03H</td></tr>
<tr><td>Description</td><td colspan="12">Source pre-charge start position setting.</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h03</td></tr><tr><td>SW Reset</td><td>8’h03</td></tr><tr><td>HW Reset</td><td>8’h03</td></tr></table></td></tr>
</table>

12.2.18 PWCTR 5 (B1h)

<table>
<tr><td>B1H</td><td colspan="12">Power Control 5</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>B1H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">BTH[1:0]</td><td colspan="2">BTL[1:0]</td><td>0FH</td></tr>
<tr><td>Description</td><td colspan="12">BTH[1:0]: is used to define the ratio in VGH pump.
<table>
<tr><th>BTH[1:0]</th><th>BTH[1:0]</th><th>VGH</th></tr>
<tr><td>0</td><td>0</td><td>4*VCI</td></tr>
<tr><td>0</td><td>1</td><td>5*VCI</td></tr>
<tr><td>1</td><td>0</td><td>6*VCI</td></tr>
<tr><td>1</td><td>1</td><td>6*VCI</td></tr>
</table>
BTL[1:0]: is used to define the ratio in VGL pump.
<table>
<tr><th>BTL[1:0]</th><th>BTL[1:0]</th><th>VGL</th></tr>
<tr><td>0</td><td>0</td><td>-3*VCI</td></tr>
<tr><td>0</td><td>1</td><td>-4*VCI</td></tr>
<tr><td>1</td><td>0</td><td>-5*VCI</td></tr>
<tr><td>1</td><td>1</td><td>-5*VCI</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h0F</td></tr>
<tr><td>SW Reset</td><td>8’h0F</td></tr>
<tr><td>HW Reset</td><td>8’h0F</td></tr>
</table></td></tr>
</table>

12.2.19 PWCTR 6 (B2h)

<table>
<tr><td>B2H</td><td colspan="12">Power Control 6</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>B2H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td colspan="2">ddvdh_clk_sel[1:0]</td><td colspan="2">vgh_clk_sel[1:0]</td><td colspan="2">vgl_clk_sel[1:0]</td><td colspan="2">vcl_clk_sel[1:0]</td><td>96H</td></tr>
<tr><td>Description</td><td colspan="12">
ddvdh_clk_sel[1:0] is used to set the operation frequency of DDVDH pump.
<table>
<tr><th>ddvdh_clk_sel [1]</th><th>ddvdh_clk_sel [0]</th><th>Frequency</th></tr>
<tr><td>0</td><td>0</td><td>1 * OSC</td></tr>
<tr><td>0</td><td>1</td><td>1/2 * OSC</td></tr>
<tr><td>1</td><td>0</td><td>1/4 * OSC</td></tr>
<tr><td>1</td><td>1</td><td>1/8 * OSC</td></tr>
</table>
vgh_clk_sel [1:0] is used to set the operation frequency of VGH pump.
<table>
<tr><th>vgh_clk_sel [1]</th><th>vgh_clk_sel [0]</th><th>Frequency</th></tr>
<tr><td>0</td><td>0</td><td>1 * OSC</td></tr>
<tr><td>0</td><td>1</td><td>1/2 * OSC</td></tr>
<tr><td>1</td><td>0</td><td>1/4 * OSC</td></tr>
<tr><td>1</td><td>1</td><td>1/8 * OSC</td></tr>
</table>
vgl_clk_sel [1:0] is used to set the operation frequency of VGL pump.
<table>
<tr><th>vgl_clk_sel [1]</th><th>vgl_clk_sel [0]</th><th>Frequency</th></tr>
<tr><td>0</td><td>0</td><td>1 * OSC</td></tr>
<tr><td>0</td><td>1</td><td>1/2 * OSC</td></tr>
<tr><td>1</td><td>0</td><td>1/4 * OSC</td></tr>
<tr><td>1</td><td>1</td><td>1/8 * OSC</td></tr>
</table>
vcl_clk_sel[1:0] is used to set the operation frequency of VCL pump.
<table>
<tr><th>vcl_clk_sel [1]</th><th>vcl_clk_sel [0]</th><th>Frequency</th></tr>
<tr><td>0</td><td>0</td><td>1 * OSC</td></tr>
<tr><td>0</td><td>1</td><td>1/2 * OSC</td></tr>
<tr><td>1</td><td>0</td><td>1/4 * OSC</td></tr>
<tr><td>1</td><td>1</td><td>1/8 * OSC</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
</table>
</td></tr>
</table>

		Power On Sequence	8’h00
		SW Reset	8’h00
		HW Reset	8’h00

12.2.20 CHOP (B5h)

<table>
<tr><td>B5H</td><td colspan="12">CHOP SET</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>B5H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td colspan="2">CHOP_SEL[1:0]</td><td>GAM_FLW_FIX</td><td>0</td><td colspan="2">GAM_BIAS_FIX[1:0]</td><td>30H</td></tr>
<tr><td>Description</td><td colspan="12">CHOPPER_SEL: Gamma chopper function option.
<table>
<tr><th>CHOP_SEL[1:0]</th><th>Description</th></tr>
<tr><td>00</td><td>2 frame chopper</td></tr>
<tr><td>01</td><td>1 line chopper (1 frame chopper polarity change)</td></tr>
<tr><td>10</td><td>1 line chopper (2 frame chopper polarity change)</td></tr>
<tr><td>11</td><td>NONE</td></tr>
</table>
Gam_bias_fix[1:0] is used to adjust gamma op’s bias current, default =00.
Gam_flw_fix is used to change gamma op’s driver capacity, default =0.</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>SW Reset</td><td>8’h00</td></tr>
<tr><td>HW Reset</td><td>8’h00</td></tr>
</table>
</td></tr>
</table>

12.2.21 VMBIAS (B6h)

<table>
<tr><td>B6H</td><td colspan="11">VCOM BIAS</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td></td><td>B6H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">VCOM_BIAS_FIX[1:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="12">VCOM_BIAS_FIX[1:0]: This command is used to define the VCOM bias
<table>
<tr><th>VCOM_BIAS_FIX[1:0]</th><th>Description</th></tr>
<tr><td>00</td><td>I</td></tr>
<tr><td>01</td><td>1/2*I</td></tr>
<tr><td>10</td><td>2*I</td></tr>
<tr><td>11</td><td>3/2*I</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>SW Reset</td><td>8’h00</td></tr>
<tr><td>HW Reset</td><td>8’h00</td></tr>
</table></td></tr>
</table>

12.2.22 REV (C3h)

<table>
<tr><th>C3H</th><th colspan="12">REV</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>C3H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>SRC_SS</td><td>0</td><td>0</td><td>0</td><td>GATE_GS</td><td>10H</td></tr>
<tr><td>Description</td><td colspan="12">SRC_SS: source reverse scan control. “1” is reverse, “0” is normal.
GATE_GS: gate reverse scan control. “1” is reverse, “0” is normal.</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h10</td></tr><tr><td>SW Reset</td><td>8’h10</td></tr><tr><td>HW Reset</td><td>8’h10</td></tr></table></td></tr>
</table>

12.2.23 VDD18 (C4h)

<table>
<tr><th>C4H</th><th colspan="11">VDD18 Set</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>C4H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">REGU_AD[2:0]</td><td>0</td><td>08H</td></tr>
<tr><td>Description</td><td colspan="12">REGU_AD[2:0]: vdd18 trimming signal.
<table>
<tr><th>REGU_AD[2:0]</th><th>VDD18</th></tr>
<tr><td>000</td><td>1.60</td></tr>
<tr><td>001</td><td>1.67</td></tr>
<tr><td>010</td><td>1.74</td></tr>
<tr><td>011</td><td>1.80</td></tr>
<tr><td>100</td><td>1.85</td></tr>
<tr><td>101</td><td>1.90</td></tr>
<tr><td>110</td><td>1.96</td></tr>
<tr><td>111</td><td>2.11</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value(D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>8’h08</td></tr>
<tr><td>SW Reset</td><td>8’h08</td></tr>
<tr><td>HW Reset</td><td>8’h08</td></tr>
</table></td></tr>
</table>

12.2.24 RDOTP 1 (D1h)

<table>
<tr><th>D1H</th><th colspan="12">Read OTP Data 1</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>D1H</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td colspan="8">OTP_RD_DAT[7:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">OTP read data[7:0]</td></tr>
<tr><td>Restriction</td><td colspan="12">The 1st Parameter is dummy read.
Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

12.2.25 RDOTP 2 (D2h)

<table>
<tr><th>D2H</th><th colspan="12">Read OTP Data 2</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>D2H</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td colspan="8">OTP_RD_DAT[15:8]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">The 1st Parameter is dummy read.
OTP read data[15:8]</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

12.2.26 RDOTP 3 (D3h)

<table>
<tr><th>D3H</th><th colspan="12">Read OTP Data 3</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>D3H</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td colspan="8">OTP_RD_DAT[23:16]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">The 1st Parameter is dummy read.
OTP read data[23:16]</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

12.2.27 RDOTP 4 (D4h)

<table>
<tr><th>D4H</th><th colspan="12">Read OTP Data 4</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>D4H</td></tr>
<tr><td>Parameter1</td><td>H</td><td>R</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Parameter2</td><td>H</td><td>R</td><td>H</td><td colspan="8">OTP_RD_DAT[31:24]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">The 1st Parameter is dummy read.
OTP read data[31:24]</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

12.2.28 OTPCTR 1 (E1h)

E1H	OTP Control 1											
	D/CX	**RDX**	**WRX**	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	1	1	0	0	0	0	1	E1H
Parameter	H	H	R	0	0	OTP_PTM[1:0]		OTP_VPP_SEL	OTP_PROG	OTP_WR_EN	OTP_RD_EN	00H
Description	Detail operations refer to OTP datasheet.											
Restriction	Should set “FF=A5” before configure this registers											
Register Availability												

Status	Availability
Normal Mode on,ldle Mode Off,Sleep Out	Yes
Normal Mode on,ldle Mode On,Sleep Out	Yes
Partial Mode on,ldle Mode Off,Sleep Out	Yes
Partial Mode on,ldle Mode On,Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value(D7 to D0)
Power On Sequence	8’h00
SW Reset	8’h00
HW Reset	8’h00

12.2.29 OTPCTR 2 (E2h)

<table>
<tr><th>E2H</th><th colspan="12">OTP Control 2</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>E2H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td colspan="7">OTP_ADDR[6:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="12">Detail operations refer to OTP datasheet.</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

12.2.30 OTPCTR 3 (E3h)

<table>
<tr><th>E3H</th><th colspan="12">OTP Control 3</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>E3H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td colspan="8">OTP_WR_DAT[7:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="12">Detail operations refer to OTP datasheet.</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

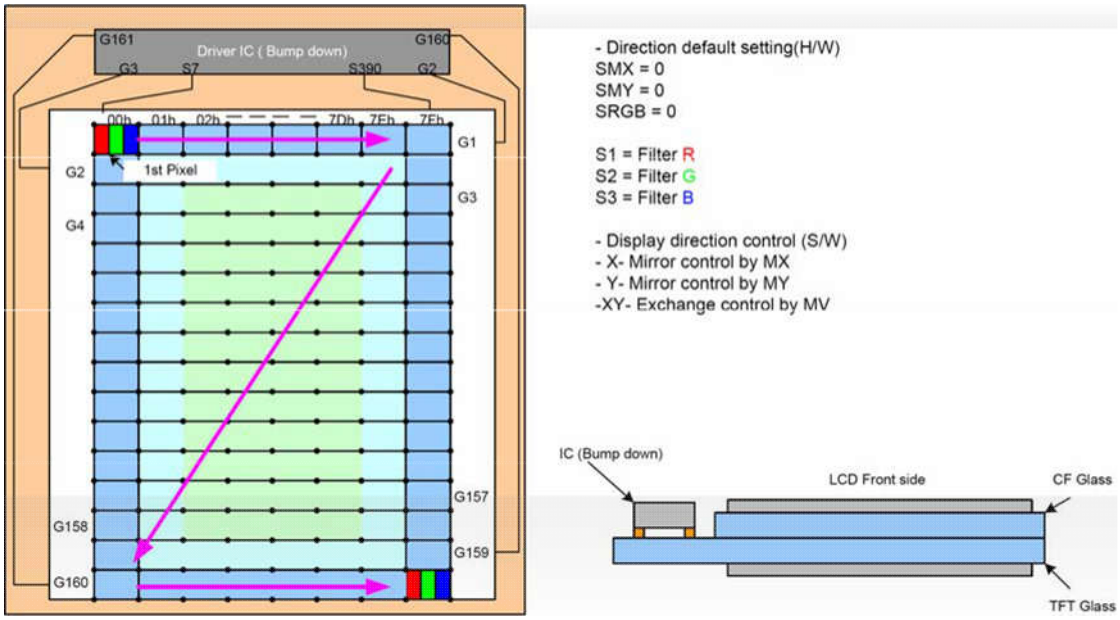
12.2.31 OTPCTR 4 (E4h)

<table>
<tr><th>E4H</th><th colspan="12">OTP Control 4</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>L</td><td>H</td><td>R</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>E4H</td></tr>
<tr><td>Parameter</td><td>H</td><td>H</td><td>R</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>OTP_ESD_EN</td><td>OTP_SLPOUT_EN</td><td>02H</td></tr>
<tr><td>Description</td><td colspan="12">OTP_ESD_EN: The switch to decide if reload OTP after ESD triggered.
OTP_SLPOUT_EN: The switch to decide if reload OTP after SLPOUT command.</td></tr>
<tr><td>Restriction</td><td colspan="12">Should set “FF=A5” before configure this registers</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on,ldle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>8’h03</td></tr><tr><td>SW Reset</td><td>8’h03</td></tr><tr><td>HW Reset</td><td>8’h03</td></tr></table></td></tr>
</table>

13. Example Panel Connection (GM=”011”)

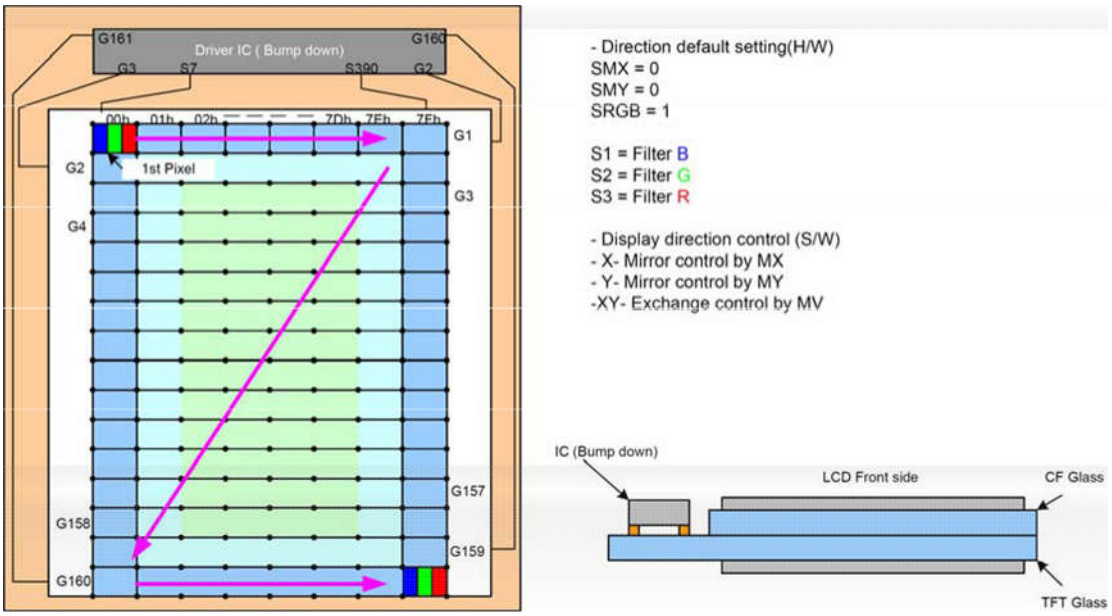
CASE 1: First pixel is at left_top of the panel

RGB order is “R.G.B”



CASE 2: First pixel is at left_top of the panel

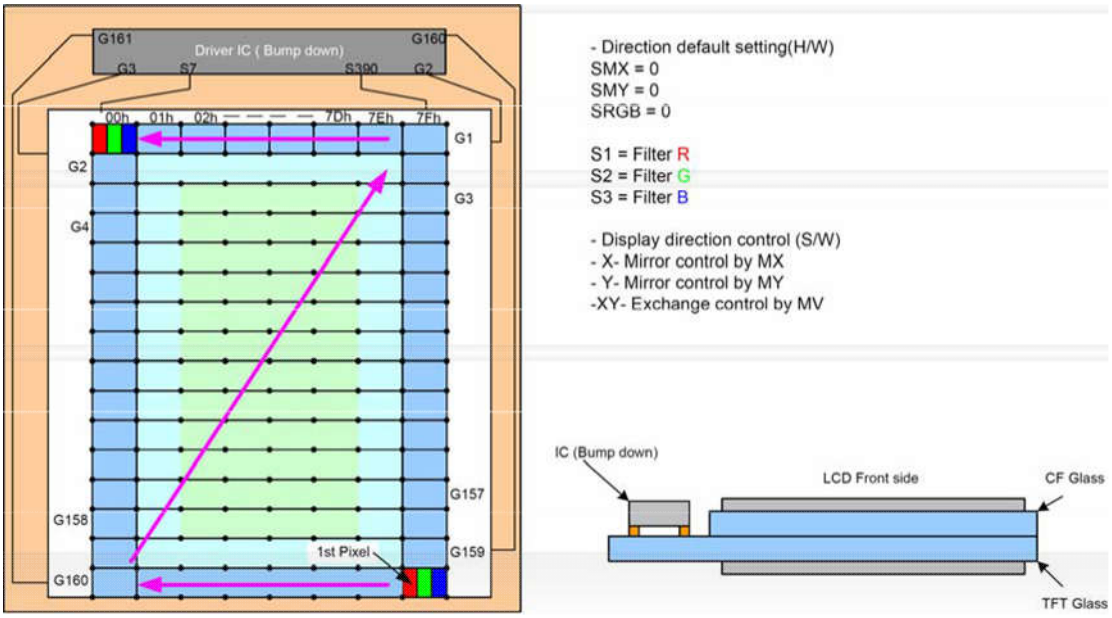
RGB order is “B.G.R”



CASE 3: First pixel is at Right_bottom of the panel
RGB order is “R.G.B”

CASE 3: First pixel is at Right_bottom of the panel

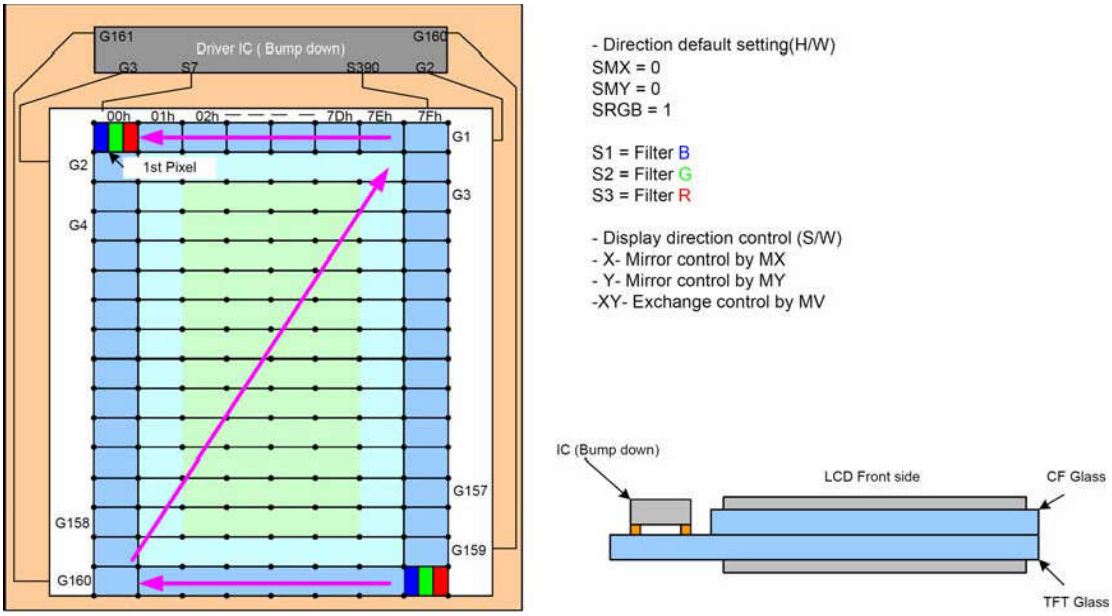
RGB order is “R.G.B”



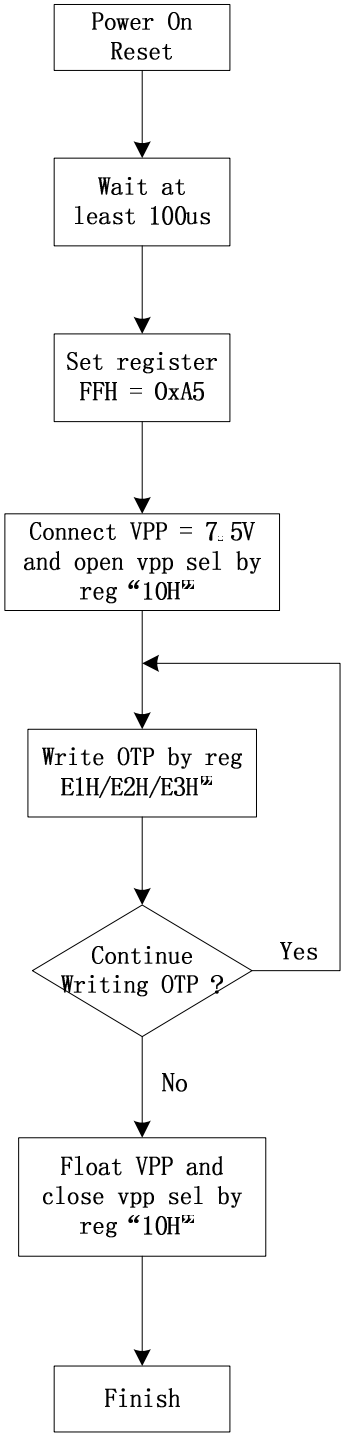
CASE 4: First pixel is at Right_bottom of the panel

RGB order is “B.G.R”

CASE 3: First pixel is at Right_bottom of the panel
RGB order is “R.G.B”



14. OTP Flow


Power On Reset
Wait at least 100us
Set register FFH = 0xA5
Connect VPP = 7.5V and open vpp sel by reg "10H"
Write OTP by reg E1H/E2H/E3H"
Continue Writing OTP ?
Yes
No
Float VPP and close vpp sel by reg "10H"
Finish

15. Electrical Characteristics

15.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When NV3022B is used out of the absolute maximum ratings, the NV3022B may be permanently damaged. So working within the following electrical characteristics limit is strongly recommended during normal operation.

Item	Symbol	Unit	Value Note
Supply voltage	VCI	V	-0.3~+4.8
Supply voltage(Logic)	IOVCC	V	-0.3~+3.6
Supply voltage(Digital)	VCC	V	-0.3~+2.4
Driver supply voltage	VGH-VGL	V	-0.3~+30.0
Logic input voltage range	VIN	V	-0.3~IOVCC+0.3
Logic output voltage range	VO	V	-0.3~IOVCC+0.3
Operation temperature	Topr	℃	-35~+85
Storage temperature	Tstg	℃	-55~+110

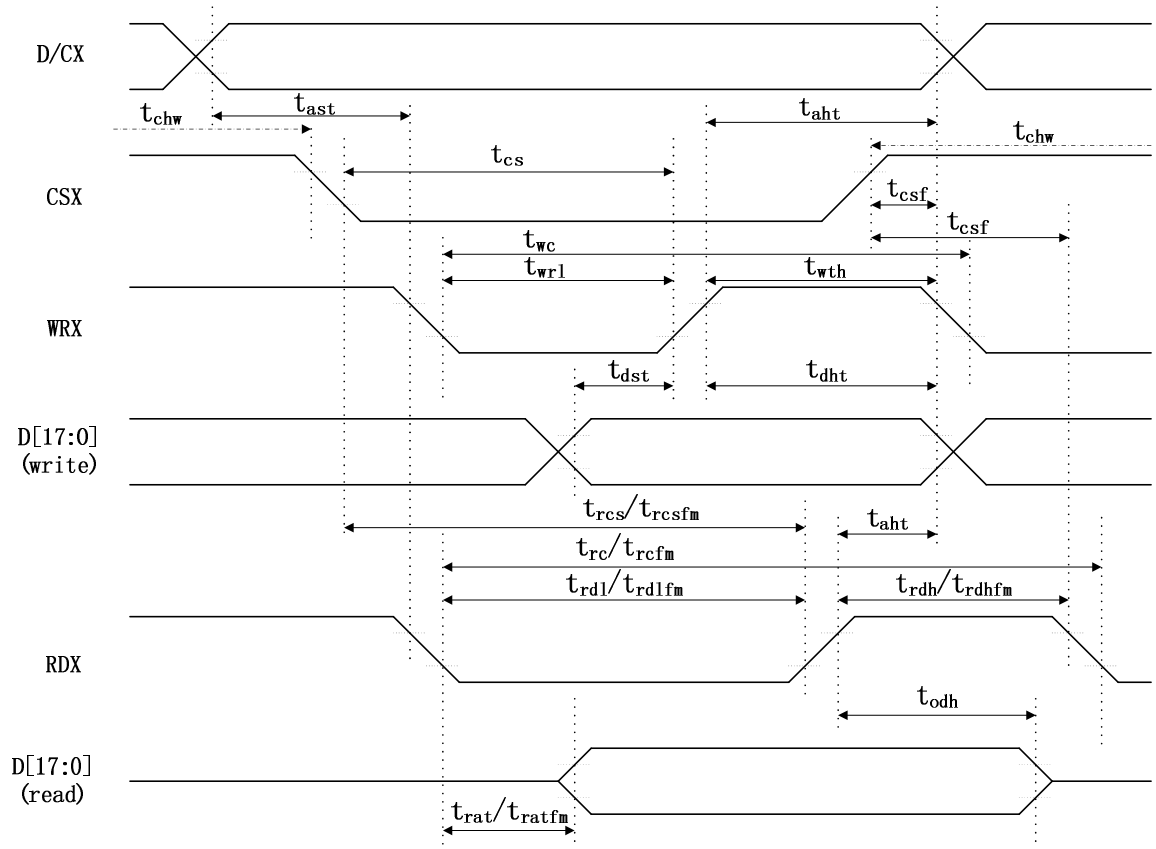
15.2. DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power & Operation Voltage							
Analog Operation Voltage	VCI	V	Operation Voltage	2.5	2.75	4.8	Note 2
Logic Operation Voltage	IOVCC	V	I/O Supply Voltage	1.65	1.8	3.6	Note 2
Digital Operation Voltage	VCC	V	Digital Supply Voltage		1.8		Note 2
Gate Driver High Voltage	VGH	V		10		16	Note 3
Gate Driver Low Voltage	VGL	V		-16		-7.5	Note 3
Driver Supply Voltage		V	|VGH-VGL|	19		32	Note 3
Input/Output							
Logic High Level Input Voltage	VIH	V		0.7IOVCC		IOVCC	Note 1,2,3
Logic Low Level Input Voltage	VIL	V		VSS		0.3IOVCC	Note 1,2,3
Logic High Level Output Voltage	VOH	V	IOH=-1.0mA	0.8IOVCC		IOVCC	Note 1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSS		0.2IOVCC	Note 1,2,3
Logic Input Leakage Current	IIL	uA	VIN=IOVCC or VSS	-0.1		0.1	Note 1,2,3
VCOM Operation							
VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5		5	Note 3
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5		0	Note 3
VCOM Amplitude Voltage	VOMA	V	|VCOMH-VCOML|	4		5.5	Note 3
Source Driver							
Source Output Range	Vsout	V		0.5		AVDD-0.1	Note 4
Gama Reference Voltage	GVDD	V		3		4.9	Note 3

Note 1: IOVCC=1.65 to 3.3V, VCI=2.5 to 4.8V, AGND=GND=0V, Ta=-30 to 70 (to +85 ℃ ℃ no damage)
Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage. (IOVCC≦VCI)
Note2, 3, 4: When the measurements are performed with LCD module. Measurement Points are like below.
Note3: CSX, RDX, WRX, D[23:0], D/CX, RESX, TE, PCLK, VS, HS, DE, SDA, SCL, GM2, GM1, GM0, RCM1, RCM0, P68, IM2, IM1, IM0, SRGB, REV, SMX, SMY, RL, TB, IDM, SHUT, PREG, GS and Test pins.
Note5: Source channel loading = 10pF/channel, Gate channel loading = 50pF/channel

15.3. AC Characteristics

15.3.1 Parallel MCU 18/16/9/8-bit BUS



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 15.3.1 AC characteristics of parallel MCU I/F in asynchronous mode

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
D/CX	TAST	Address Setup Time	0		ns	
	THAT	Address Hold Time (W/R)	10		ns	
CSX	TCHW	“S” “H” Pulse Width	0		ns	
	TCS	Chip Select Setup Time(W)	10		ns	
	TRCS	Chip Select Setup Time (Read ID)	45		ns	
	TRCSFM	Chip Select Setup Time (Read FM)	355		ns	
	TCSF	Chip Select Wait Time (W/R)	10		ns	
WRX	TWC	Write Cycle	66		ns	
	TWRH	Control Pulse H Duration	15		ns	
	TWRL	Control Pulse L Duration	15		ns	
RDX	TRC	Read Cycle(ID)	160		ns	When Read ID
	TRDH	Control Pulse H Duration(ID)	90		ns	
	TRDL	Control Pulse L	45		ns	

		Duration(ID)				
RDX	TRCFM	Read Cycle(FM)	450		ns	When Read From Frame Memory
	TRDHFM	Control Pulse H Duration(FM)	90		ns	
	TRDLFM	Control Pulse L Duration(FM)	355		ns	
D[17:0]	TDST	Data Setup Time	10		ns	CLmax=30pF Clmin=8pF
	TDHT	Data Hold Time	10		ns	
	TRAT	Read Access Time(ID)		40	ns	
	TRATFM	Read Access Time(FM)		340	ns	
	TODH	Output Disable Time	20	80	ns	

Note 1: IOVCC 1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=GND=0V, Ta=-30 to 70 °C (to +85°C no damage)
Note 2: This input signal rise time and fall time (tr, tf) is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals

15.3.2 Display Serial Interface(SPI)

15.3.2.1 SPI 3-Wire Interface

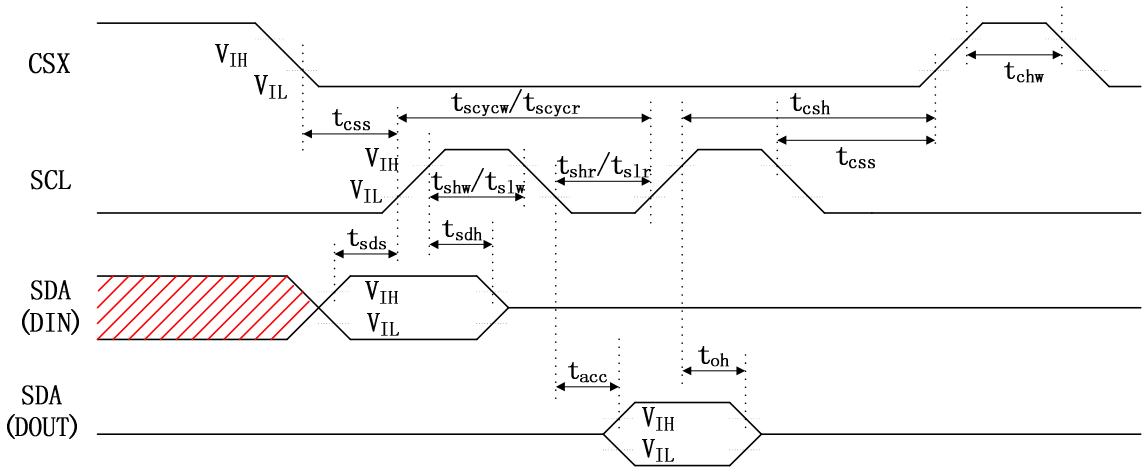


Table 15.3.2.1: 3-pin Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
CSX	TCSS	Chip Select Setup Time	10		ns	
	TCSH	Chip Select Hold Time	30		ns	
	TCHW	Chip Select “H” Pulse Width	30		ns	
SCL	TSCYCW	Serial Clock Cycle(Write)	66		ns	
	TSHW	S”L””H” Pulse Width(Write)	15		ns	
	TSLW	S”L””L” Pulse Width(Write)	15		ns	
	TSCYCR	Serial Clock	150		ns	

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
		Cycle(Read)				
	TSHR	S”L””H” Pulse Width(Read)	60		ns	
	TSLR	S”L””L” Pulse Width(Read)	60		ns	
SDA(DIN) /(DOUT)	TSDS	Data Setup Time	15		ns	
	TSDH	Data Hold Time	5		ns	
	TACC	Access Time	5	50	ns	CLmax=30pF CLmin=8pF
	TOH	Output Disable Time	10		ns	

Note 1: IOVCC=1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=GND=0V. Ta=-30 to 70℃ (to +85℃ no damage)
Note 2: The input signal rise time and fall time(tr, tf) is specified at 15 ns or less. Logic high and low levels are specified as 10% and 90% of IOVCC for Input signals.

15.3.2.2 SPI 4-Wire Interface

Table 15.3.2.2: 4 pin Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
CSX	TCSS	Chip Select Setup Time	10		ns	
	TCSH	Chip Select Hold Time	30		ns	
	TCHW	Chip Select “H” Pulse Width	30		ns	
SCL	TSCYCW	Serial Clock Cycle(Write)	66		ns	
	TSHW	S”L””H” Pulse Width(Write)	15		ns	
	TSLW	S”L””L” Pulse Width(Write)	15		ns	
	TSCYCR	Serial Clock Cycle(Read)	150		ns	
	TSHR	S”L””H” Pulse Width(Read)	60		ns	
	TSLR	S”L””L” Pulse Width(Read)	60		ns	
D/CX	TDCS	D/CX Setup Time	5		ns	
	TDCH	D/CX Hold Time	5		ns	
SDA(DIN) (DOUT)	TSDS	Data Setup Time	15		ns	
	TSDH	Data Hold Time	5		ns	
	TACC	Access Time	5	50	ns	CLmax=30pF CLmin=8pF
	TOH	Output Disable Time	10		ns	

Note 1: IOVCC=1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=GND=0V. Ta=-30 to 70℃ (to +85℃ no damage)
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. Logic high and low levels are specified as 10% and 90% of IOVCC for Input signals.

15.3.3 Parallel RGB 18/16/6-bit BUS

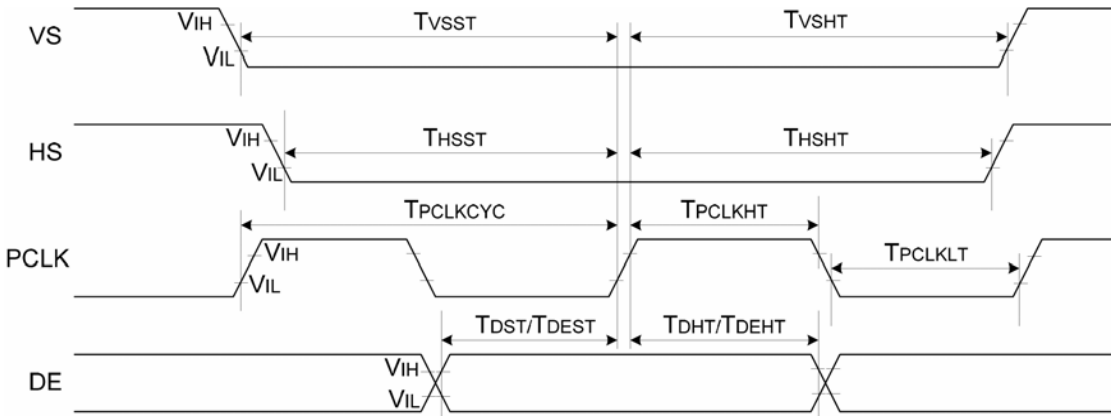


Table 15.3.3 RGB Interface Charateristics

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
PCLK	TPCLKCYC	TPCLK Cycle Time	66		ns	
	TPCLKLT	Pixel Low Pulse Width	15	-	ns	
	TPCLKHT	Pixel High Pulse Width	15	-	ns	
VS	TVSST	Vertical Sync.setup time	15	-	ns	
	TVSHT	Vertical Sync.hold time	15	-	ns	
HS	THSST	Horizontal Sync.setup time	15	-	ns	
	THSHT	Horizontal Sync.hold time	15	-	ns	
DE	TDEST	Data Enable Setup Time	15	-	ns	
	TDEHT	Data Enable Hold Time	15	-	ns	
D[17:0]	TDST	Data Setup Time	15	-	ns	
	TDHT	Data Hold Time	15	-	ns	

16. Revision History

Date	Revision	Page	Description
2018/07/12	V1.0	All	First Release
2018/11/15	V1.1	All	