DESCRIPTION

The PT6891 is a single-chip CMOS OLED driver for O/PLED (organic/polymer light emitting diode) passive dot matrix graphic display systems. The PT6891 consists of 96 cathodes (commons) and 128 anodes (segments).

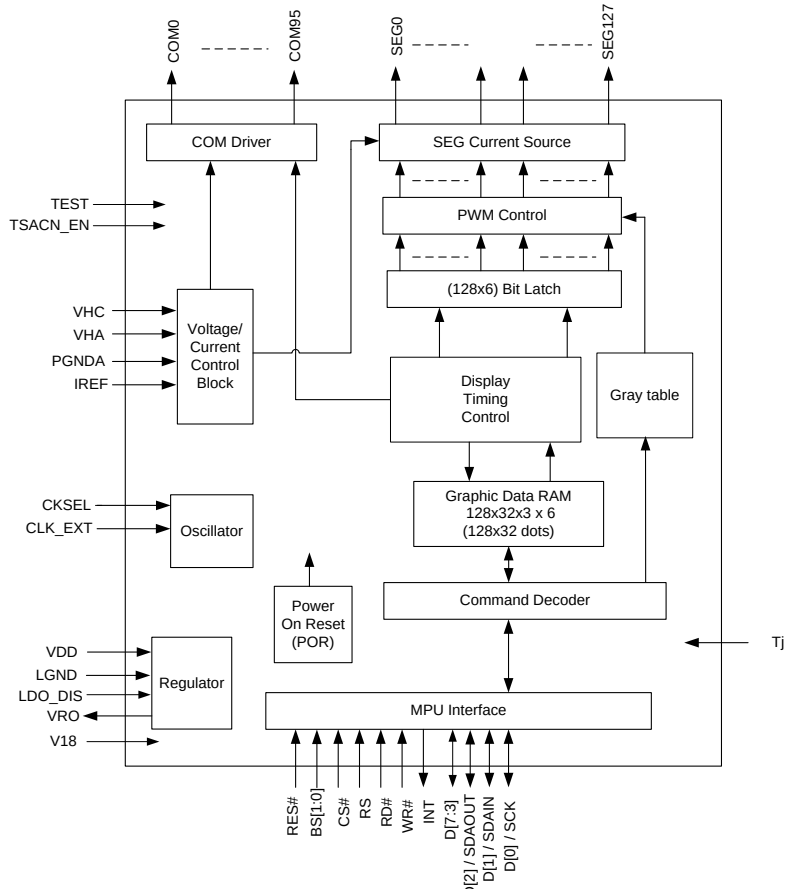
The PT6891 displays data directly from its internal 128x32x3x6 (128x32 RGB dots) GD-RAM (Graphic Data RAM) or 128x96x6 (128x32 Mono dots) GD-RAM (Graphic Data RAM). Data/Commands are sent from the general MCU through parallel interface or serial interface.

The PT6891 reduces the number of external components by including a brightness control function and an on-chip oscillator.

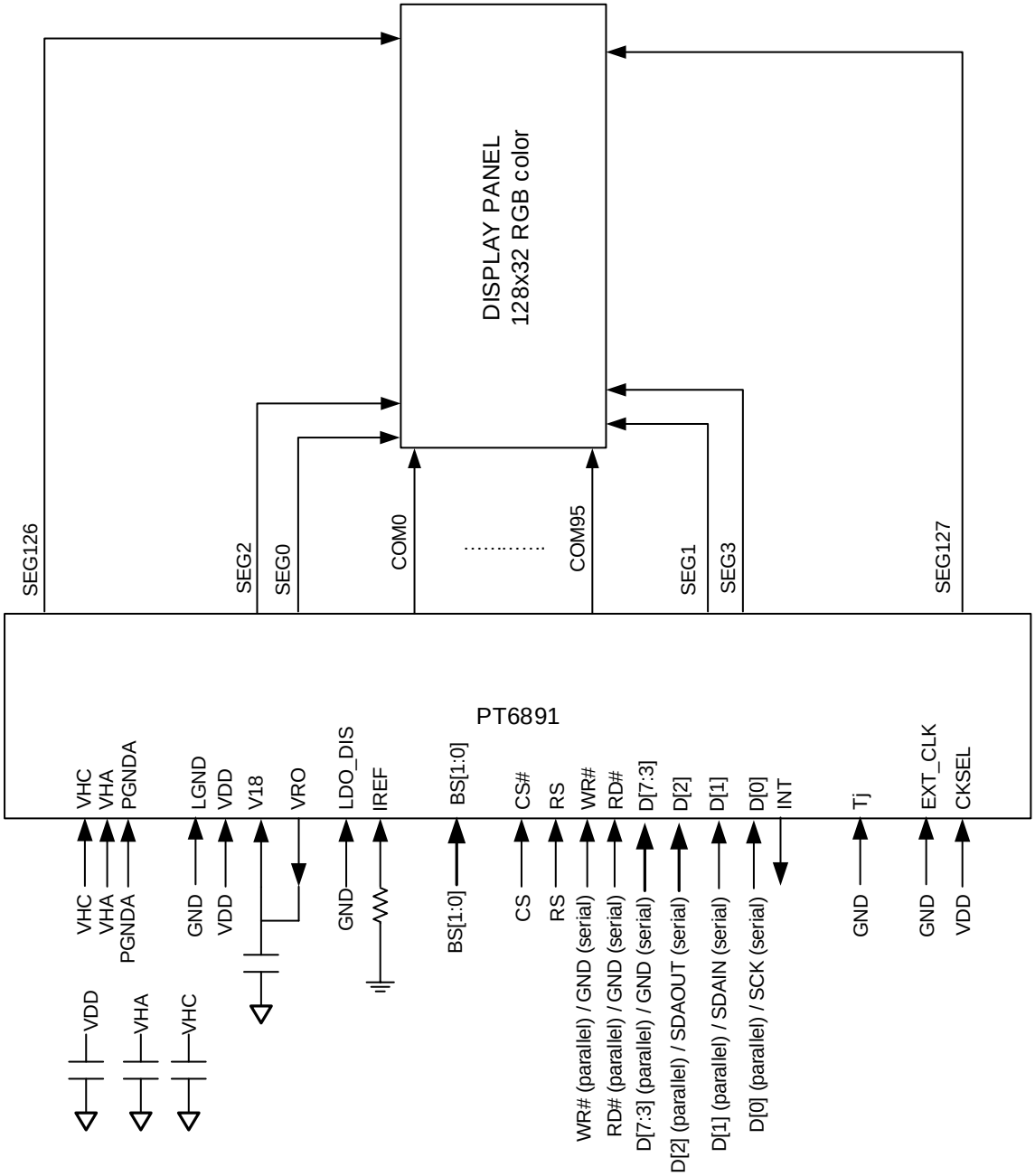
FEATURES

- Supports max. 128 x 32 RGB dot matrix panel
- Supports max. 128 x 96 Mono dot matrix panel
- Power supply to logic system: 1.65V~3.6V
- Power supply to OLED system: 8.0V~18V
- Segment output typical current : 250μA;maximum current: 300μA
- Brightness control
- Program gamma table
- Programmable frame rate
- Crosstalk compensation
- Interface
  Parallel interface: 8080-series command (8 bits) / data (8 bits)
  Serial interface: 3 wire SPI interface / 4 wire SPI interface / I^2C interface
- Embedded 128x32x3x6 (128x32 RGB dots) SRAM for image buffer
- COG or Gold Bump dice are available

BLOCK DIAGRAM



APPLICATION EXAMPLE



Note:

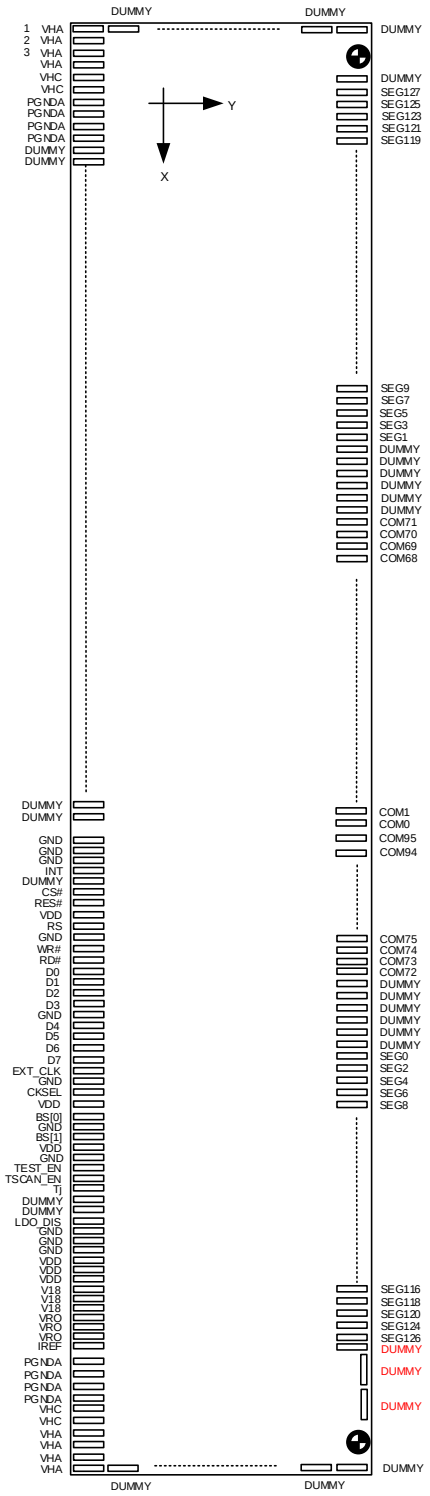
1. In serial interface, D[7:3], WR# and RD# are connected to ground or VDD.
2. Capacitance 0.1uF ~ 10uF

CONTENTS

1.ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6891	COG	-

2. PIN CONFIGURATION



3. PIN DESCRIPTION

I=Input, O=Output, IO=Bi-directional (input/output), P=Power pin, A=Analog pin

Pin Name	Pin Type	Description
CLK_EXT	I	When internal oscillator is disabled (LOW in CKSEL pin), the pin is the input pin for external clock source. When internal oscillator is enabled (HIGH in CKSEL pin), this pin is not used and should be connected to ground.
CKSEL	I	This pin is internal clock enable. When this pin is pulled HIGH, the internal oscillator is enabled. When this pin is pulled LOW, the internal oscillator is disabled
INT	O	INT signal that is used to synchronize MCU.
RES#	I	This pin is low-active reset input. When the pin is LOW, the chip is reset. When chip is reset, oscillator is enabled, anode driver outputs are LOW and all control registers are set to default values, and the memory content would not be reset.
BS[1:0]	I	This pin is MCU interface selection input. When BS[1:0] is "00", SPI (4-wire) interface be selected. When BS[1:0] is "01", SPI (3-wire) interface be selected. When BS[1:0] is "10", I^2C interface be selected. When BS[1:0] is "11", Parallel(8080) interface be selected.
CS#	I	This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled LOW.
RS	I	This pin is Data/Command control pin. When the pin is pulled LOW, the data at D[7:0] will be treated as a command. When the pin is pulled HIGH, the data at D[7:0] is treated as a parameter. For detail relationship of MCU interface signals, please refer to the Timing Characteristics Diagrams.
WR#	I	This pin is write control of MCU interface. Data write operation is performed when this pin is pulled LOW and the CS# is LOW. When SPI mode is used, WR# must be connected to VDD or GND.
RD#	I	This pin is read control of MCU interface. When this pin is pulled LOW and the CS# is LOW, Data read operation is performed. When SPI mode is used, RD# must be connected to VDD or GND.
D[7:0]	IO	These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When SPI mode is selected, D[2] will be the serial data output (SDO), D[1] will be the serial data input (SDI) and D[0] will be the serial clock input (SCK). When SPI mode is used, D[7] ~ D[3] must be connected to VDD or GND. When I2C mode is selected, D[2] will be the serial data output (SDAOUT), D[1] will be the serial data input (SDAIN) and D[0] will be the serial clock input (SCK). When serial mode is used, D[7] ~ D[3] must be connected to VDD or GND.
SEG[127:0]	O	These pins are anode outputs.
COM[95:0]	O	These pins are cathode outputs.
TEST_EN	I(PL)	When this pin is LOW, the chip would function normally. When this pin is HIGH, the chip is in test mode for scan-chain test and MBIST. In normal mode. This pin could be left open.
TSCAN_EN	I(PL)	When this pin is LOW, the chip would function normally. This pin is used in scan-test mode. In normal mode, it can be left open.
LDO_DIS	I(PL)	When this pin is connected to GND, the embedded regulator (3.3V to 1.8V) is enabled. When this pin is connected to VDD, the regulator is disabled.
VRO	P	This pin is regulator voltage output pin. When LDO_DIS is GND, VRO output 1.8V.
IREF	A	This is reference current pin. A resistor (typical 100KΩ) connected between this pin and ground determines the reference current for anode driver. When register "IRE"=1, IREF

Pin Name	Pin Type	Description
		pin will be used.
V18	P	This is 1.8V power input pin for core logic circuit. If regulator is enabled (GND in LDO_DIS pin), this pin connected to VRO pin. If regulator is disabled (VDD in LDO_DIS pin), this pin is connected to external 1.8V power.
VDD	P	This is Logic power input.
GND	P	This is ground pin for power domain (VDD, V18).
VHA	P	This is the most positive voltage supply pin of the chip to drive anode. It is supplied externally.
VHC	P	This is the most positive voltage supply pin of the chip to drive cathode. It is supplied externally.
PGNDA	P	It is ground pin for power domain (VHA, VHC).

4. FUNCTION BLOCK DESCRIPTION

4.1 COMMAND DECODER AND COMMAND INTERFACE

The command decoder decodes the command/data sent by MPU. Data is interpreted based upon the input of the RS pin. Whenever RS been pulled to logic “LOW”, the input D[7:0] would be interpreted as a command.

4.2 MPU INTERFACE

Function / PIN	BS[1:0]	CS#	RS	WR#	RD#	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
SPI(4wire)	00	CS#	RS	Tie VDD / Tie GND							SDO(OUT)	SDI(IN)	SCK
SPI(3wire)	01	CS#	Tie VDD / Tie GND								SDO(OUT)	SDI(IN)	SCK
I^2C	10	Tie VDD / Tie GND	SA0	SA1	SA2	Tie VDD / Tie GND					SDA(OUT)	SDA(IN)	SCK
Parallel(8080)/Write	11	CS#	RS	WR#	VDD	D[7:0]							
Parallel(8080)/Read	11	CS#	RS	VDD	RD#	D[7:0]							

MPU PARALLEL 8080-SERIES INTERFACE
The Parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, RS and CS#. A rising edge of RD# serves as a data read signal. A rising edge of WR# serves as a data write signal.
When RS is LOW, D[7:0] should be treated as a command. When RS is HIGH, the D[7:0] should be treated as data.

MPU SERIAL PERIPHERAL INTERFACE(SPI-4wire)
The serial peripheral interface consists of serial clock (SCK), serial input data SDI(IN), serial output data SDO(OUT), RS and CS#. SDI is shifted into an 8-bit shift register on every rising edge of SCL in the order of b7, b6, …, b0.
When RS is LOW, “b7~b0” should be treated as a command. When RS is HIGH, “b7~b0” should be treated as data.

MPU SERIAL PERIPHERAL INTERFACE(SPI-3wire)
The serial peripheral interface consists of serial clock (SCK), serial input data SDI(IN), serial output data SDO(OUT), and CS#. SDI is shifted into an 9-bit shift register on every rising edge of SCL in the order of b8, b7, b6, …, b0.
When “b8” is LOW, “b7~b0” should be treated as a command. When “b8” is HIGH, “b7~b0” should be treated as data.

MPU I^2C INTERFACE
The I^2C interface consists of serial clock (SCK), serial input data (SDAIN), and serial output data (SDAOUT). SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of b7, b6, …, b0. “RD#,WR#,RS” is I^2C slave address A2.A1.A0.So I^2C slave address is (60h~67h).

4.3 OSCILLATOR CIRCUIT

The below is an On-Chip LOW power RC oscillator circuitry. The oscillator generates the system clock for the chip.

The oscillator is not affected by RES# pin or software reset command.
“OSC TRIMING COMMAND” can be adjusted OSC frequency.

4.4 VOLTAGE / CURRENT CONTROL BLOCK

This block is used to divide the incoming power sources into the different levels of internal use voltage and current. VHA, VHC, and VDD are external power supplies.

4.5 GRAPHIC DATA RAM

The Graphic Data RAM (128x3x32x6/ 128x96x6, 15.48KB) is used as a graphic buffer that could be loaded 128x32 mono-dots image.

4.6 SEG(SEGMENT) CURRENT SOURCE

SEGMENT(anode) current source drives deliver 128 current sources to drive OLED panel. It uses current source to drive the anode Cell where the driving current can be adjusted by brightness controller.

4.7 COM(COMMON) DRIVER

COMMON(cathode) gate drives deliver 96 channels to drive OLED panel.

The common voltage is generated by embedded high-voltage regulator whose output level is controlled by 3-bit control register (DAC[2:0]). If the high-voltage regulator is disabled, an external power supply is needed.

5.COMMAND TABLE

Command	Byte	D7	D6	D5	D4	D3	D2	D1	D0	Description	Default	Response	
												Scan	No scan
Software Reset	1st	1	0	1	0	0	1	0	1	Reset chip to initial condition	-	Real-time	
Standby	1st	0	1	0	0	1	0	0	1	Enter Standby mode.	-	Next Frame	Next HSYNC
Wake-up	1st	1	0	1	0	1	0	1	0	Exit Standby mode.	◎	-	
INT Setting	1st	0	1	0	0	0	0	1	INT	INT=1 Enable	0h	Next Frame	Next HSYNC
Clock Divider	1st	0	1	0	0	0	1	DIV[1:0]		T_{PWMCLK} = 1 X T_{OSC}(DIV=00) T_{PWMCLK} = 2 X T_{OSC}(DIV=01) T_{PWMCLK} = 4 X T_{OSC}(DIV=10) T_{PWMCLK} = 8 X T_{OSC}(DIV=11)	0h	Real-time	
OSC Trimming	1st	0	1	0	0	1	1	0	0	OSC trimming	8h	Real-time	
	2nd	*	*	*	*	TRIM[3:0]							
Color Mode	1st	0	0	1	1	0	0	CM[1:0]		CM=00 (RGB: 666; 262K colors) CM=01 (RGB: 565; 65K colors) CM=10 (Mono; 64 gray) CM=11 (Mono; 2 gray)	0h	Next frame	Next HSYNC
Green Gamma Table	1st	0	0	1	0	1	0	0	0	G Gamma table setting		Next frame	Next HSYNC
	2nd	D[7:0]Note											
Blue Gamma Table	1st	0	0	1	0	1	0	0	1	B Gamma table setting		Next frame	Next HSYNC
	2nd	D[7:0]Note											
Red Gamma Table	1st	0	0	1	0	1	0	1	0	R Gamma table setting		Next frame	Next HSYNC
	2nd	D[7:0]Note											
Gamma Table Update	1st	0	0	1	0	1	0	1	1	Gamma table update		Next frame	Next HSYNC
Row Address Setting	1st	1	0	0	0	0	0	0	0	Start of row address for 128x32-dot image	00h	Real-time	
	2nd	*	RA[6:0]										
Column Address Setting	1st	1	0	0	0	0	0	0	1	Start of column address for 128x32-dot image	00h	Real-time	
	2nd	*	CA[6:0]										
Return Length Setting	1st	1	0	0	0	0	0	1	0	Length of pixels to Return	7Fh	Real-time	
	2nd	*	RL[6:0]										
Display Data Write	1st	1	0	0	0	0	0	1	1	To Write graphic data	-	Real-time	
Display Data Write	2nd	Write Data D[7:0]								Write Data	-	Real-time	
Display Data Read	1st	1	0	0	0	0	1	0	0	To Read graphic data	-	Real-time	
Display Data Read	2nd	Read Data D[7:0]								Read Data	-	Real-time	
Display ON/OFF	1st	0	1	0	1	1	0	B1	B0	Display ON/OFF setting	B0=0 B1=0	Next frame	Next HSYNC
Vertical and Horizontal Mirror	1st	0	1	1	0	1	0	H	V	Rotate display image V=1, Vertical mirroring H=1, Horizontal mirroring	H=0 V=0	Next frame	Next HSYNC
Graphic Acceleration Enable	1st	0	1	1	1	0	0	0	GE	Graphic Acceleration enable	0h	Next frame	Next HSYNC

Command	Byte	D7	D6	D5	D4	D3	D2	D1	D0	Description	Default	Response	
												Scan	No scan
Graphic Acceleration Mode	1st	0	1	1	1	0	0	1	0	Graphic Acceleration Setting GA[2:0] = 000: Horizontal Scroll 001: Vertical Scroll 010: Horizontal and Vertical Scroll 011: Fade Out 100: Blinking 101: Zoom In 110~111: No active GH=0, Left- Horizontal Scroll GH=1, Right- Horizontal Scroll GV=0, Top- Vertical Scroll GV=1, Bottom- Vertical Scroll	0h	Next frame	Next HSYNC
	2nd	*	*	*	GH	GV	GA[2:0]						
Acceleration Frame Setting	1st	0	1	1	1	0	0	1	1	Set time interval for each step GA_FN[7:0] : N frames	0h	Next frame	Next HSYNC
	2nd	GA_FN[7:0]											
Acceleration Start/End Row	1st	0	1	1	1	0	1	0	0	Graphic Acceleration Setting	GA_SR =0h GA_ER =1Fh	Next frame	Next HSYNC
	2nd	*	GA_SR[6:0]										
	3rd	*	GA_ER[6:0]										
Black-White Inversion	1st	0	1	1	1	1	0	0	BW	Black-white inverse	0h	Next frame	Next HSYNC
Overlap Mode	1st	1	0	1	1	0	0	0	OM	OM=0, low-overlap mode OM=1, high-overlap mode	0h	Next frame	Next HSYNC
SEG Output Type	1st	1	0	1	1	0	0	1	SQ	SEG0~SEG159 output type SQ=0: (COM_{3n}, COM_{3n+1}, COM_{3n+2}) is RGB SQ=1: (COM_{3n}, COM_{3n+1}, COM_{3n+2}) is BGR	0h	Next frame	Next HSYNC
SEG EVEN/ODD Swap	1st	1	0	1	1	0	1	0	0	SEG EVEN/ODD swap	0h	Next frame	Next HSYNC
	2nd	*	*	*	*	*	*	*	SE				
Voltage/ Current Control	1st	1	0	1	1	0	1	0	1	"if CE = 0; COM voltage by pin""VHC"" if CE = 1; COM voltage by DAC setting. COM voltage= 0.72 ~ 0.86 (VHA)" if IRE=1, to use external referenct current.	CE=0 IRE=0 DAC =5h	Real-time	
	2nd	CE	IRE	*	*	*	DAC[2:0]						
COMP_BRI	1st	1	0	1	1	0	1	1	1	Set Brightness decrease table		Real-time	
	2nd	D[7:0]Note											
Brightness	1st	1	0	1	1	1	0	0	0	Control segment output current BRR[6:0]: R-Brightness BRG[6:0]: G-Brightness BRB[6:0]: B-Brightness	7Fh	Next frame	Next HSYNC
	2nd	*	BRR[6:0]										
	3rd	*	BRG[6:0]								7Fh	Next frame	Next HSYNC
	4th	*	BRB[6:0]								7Fh	Next frame	Next HSYNC
Compensation Threshold	1st	1	0	1	1	1	0	1	0	Set threshold of compensation	-	Next Frame	Next HSYNC
	2nd	TH[7:0]											
Compensation	1st	1	0	1	1	1	0	1	1	Set pulse threshold of	42h	Next	Next

Command	Byte	D7	D6	D5	D4	D3	D2	D1	D0	Description	Default	Response	
												Scan	No scan
Pulse Threshold	2nd	CPT[7: 0]								compensation		Frame	HSYNC
PWD Enable	1st	1	0	1	1	0	1	1	0	Set PWM decrease enable	0h	Next Frame	Next HSYNC
	2nd	*	*	*	*	PE4	PE3	PE2	PE1				
PWD_Table	1st	1	0	1	1	1	0	0	1	Set PWM decrease table	-	Next Frame	Next HSYNC
	2nd	PWD[7:0]											
Cathode Scan Direction	1st	1	0	1	1	1	1	0	CD	CD: COM Scan direction	0h	Next Frame	Next HSYNC
Anode Trimming	1st	1	0	1	1	1	1	1	0	Anode Current Trimming	8h	Real-time	
	2nd	*	*	*	*	AT[3:0]							
Pre-Charge Period	1st	1	1	0	0	1	0	0	0	Pre-charge period PR[3:0]: pre-charge	Ah	Next frame	Next HSYNC
	2nd	*	*	*	*	PR[3:0]							
Pre-Charge Current	1st	1	1	0	1	0	0	0	0	Pre-charge Current PC[1:0]: pre-charge current	3h	Next frame	Next HSYNC
	2nd	*	*	*	*	*	*	PC[1:0]					
All-zero Blank Mode	1st	1	1	0	0	1	1	0	ZB	ZB=1, enable	0	Next frame	Next HSYNC
COM Pulse Width	1st	1	1	0	1	1	0	0	0	COM pulse period	06h	Next Frame	Next HSYNC
	2nd	COM_W[7:0]											
	3rd	*	*	*	*	*	*	*	[8]				
COM Number	1st	1	1	1	0	0	0	0	0	Number of Common	1Fh	Next frame	Next HSYNC
	2nd	*	COM_N[6:0]										
Display Row Setting	1st	1	1	1	0	0	0	0	1	Display row address	00h	Next frame	Next HSYNC
	2nd	*	DR[6:0]										
Display Column Setting	1st	1	1	1	0	0	0	1	0	Display column address	00h	Next frame	Next HSYNC
	2nd	*	DC[6:0]										
Common Delay Mode	1st	1	1	1	0	0	0	1	1	To set odd Common driver output delay time when low-overlap mode is selected	00h	Next frame	Next HSYNC
	2nd	*	*	*	*	*	*	D1	D0				
Blank Period	1st	1	1	1	0	0	1	0	1	Black / Blank period	Ah	Next frame	Next HSYNC
	2nd	Black[2:0]			Blank[4:0]								
Dummy Scan	1st	1	1	1	0	0	1	1	DS	Dummy scan enable	0h	Next frame	Next HSYNC
TESTMOD Enable	1st	1	1	0	0	0	1	0	0	TSTMOD enable TM=0 disable TM=1 enable	0h	Real-time	
	2nd	0	1	0	1	0	1	0	1				
	3rd	1	0	1	0	1	0	1	0				
	4th	0	0	0	0	0	0	0	TM				
Driver Output Test Mode	1st	1	1	0	0	0	0	0	0	To control driver output for testing	00h	Real-time	
	2nd	T7	T6	T5	T4	T3	T2	T1	T0				
Test RGB data	1st	1	1	0	0	0	0	0	1	Reserved for testing	00h	Real-time	
	2nd	TD[7:0]											
Clock Output Test Mode	1st	1	1	0	0	0	1	0	1	Reserved for testing CO: Enable output	00h	Real-time	
	2nd	0	0	0	0	0	0	0	CO				
Parameter Read	1st	1	1	0	0	1	1	1	0	Parameter read	-	Real-time	
	2nd	Read Data											
Read Scan Com Order	1st	1	1	0	0	1	1	1	1	Parameter scan com order	-	Real-time	
	2nd	Read Data											

Notes:

1. *=Don't Care

2 "Regulator OFF"

6. COMMAND DESCRIPTION

6.1 SOFT RESET COMMAND

Byte information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Software Reset	1st	1	0	0	1	0	1	0	0	1	0	1	Soft Reset

This command reset all logic circuit. Memory content would not be changed.

6.2 STANDBY COMMAND

Byte information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Standby	1st	1	0	0	0	1	0	0	1	0	0	1	Enter standby mode

6.3 WAKE-UP COMMAND

Byte information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Wake-up	1st	1	0	0	1	0	1	0	1	0	1	0	Exit standby mode

The sequence of actions after entering standby mode is: SEG=ALL Low, COM=ALL High → Oscillator disabled.

After MCU issued Standby command, the Standby command will take effect in the next frame. Before the chip enter standby mode, the chip would not accept any other command.

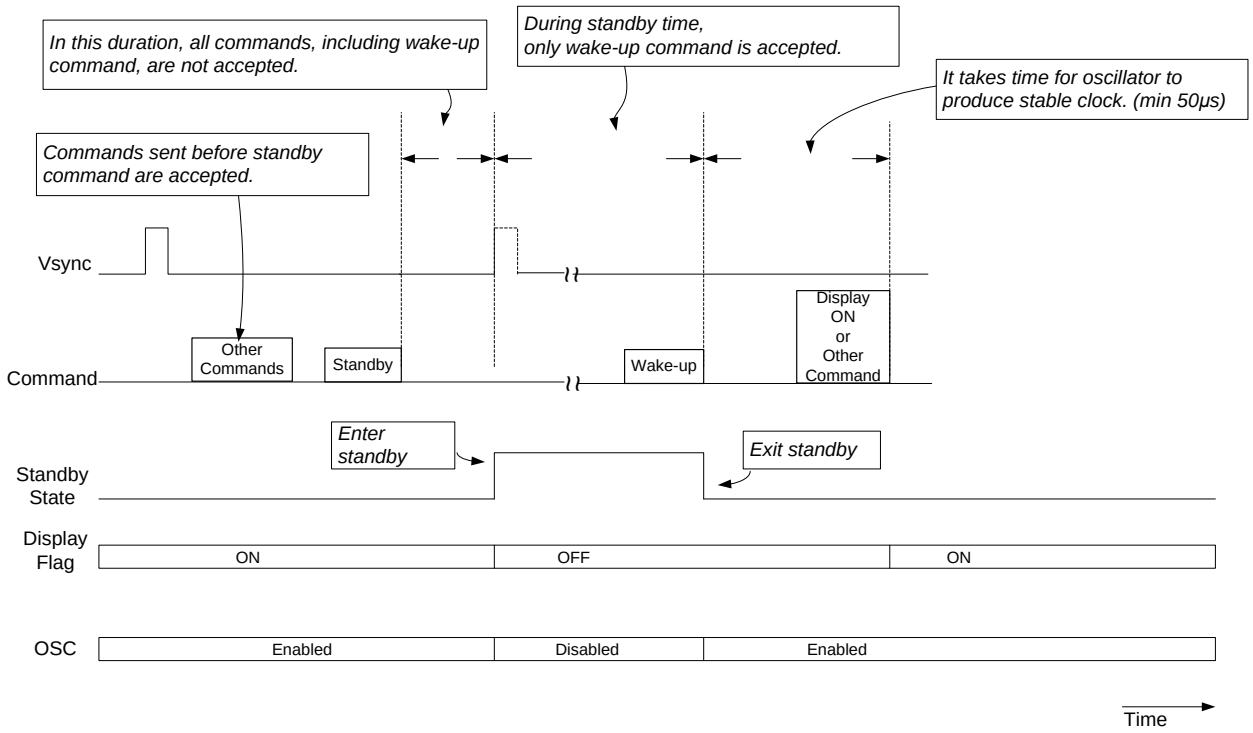
When entering standby mode, the chip will be switched to display off mode (Type_1 OFF) automatically. After wake-up, display state would stay at “Type_1 OFF” mode.

The content of graphic RAM and control registers remain.

In standby mode, only the wake-up command is acceptable. When the chip exits standby mode, it take about 30μs for the internal oscillator to produce stable clock signal. The MCU must wait 50μs to send another command otherwise the command would be decoded with error.

In standby mode, low of RES# cannot reset the chip.

The following figure illustrates the standby and wakeup.



6.4 INT PIN ENABLE COMMAND (DEFAULT VALUE=0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
INT Setting	1st	1	0	0	0	1	0	0	0	0	1	INT	INT=1 Enable INT=0, INT pin output stuck at LOW

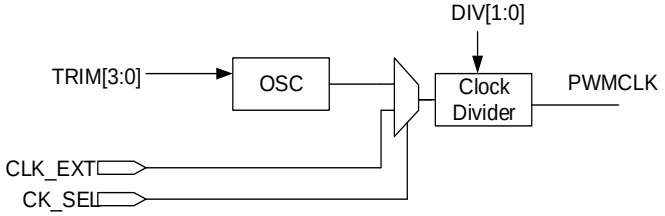
This command enables or disables the INT pin. When INT pin is disabled, the pin output is stuck at low. The INT is a frame synchronized signal, and appears at the first line of every frame.

The duty of INT is one line time set by “COM Pulse Width”.

6.5 CLOCK DIVIDER COMMAND (DEFAULT VALUE=0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
INT Setting	1st	1	0	0	0	1	0	0	0	1	DIV[1:0]		T_{PWMCLK} = 1 X T_{OSC}(DIV=00) T_{PWMCLK} = 2 X T_{OSC}(DIV=01) T_{PWMCLK} = 4 X T_{OSC}(DIV=10) T_{PWMCLK} = 8 X T_{OSC}(DIV=11)

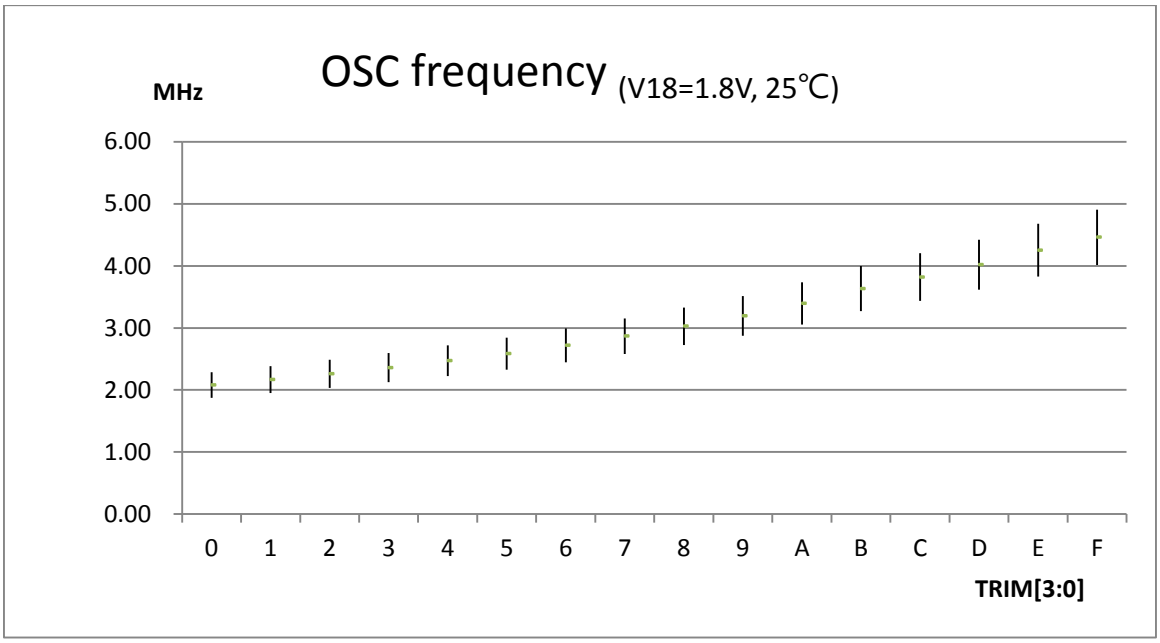
This command is setting PWMCLK frequency. PWMCLK period (T_{PWMCLK}) is selected by DIV[1:0].Exmaple : When command is setting(DIV=00),the Clock (PWMCLK) period is 1 X T_{OSC}, T_{OSC} =1/ F_{OSC}.



6.6 OSC TRIMMING COMMAND (DEFAULT VALUE=8H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
OSC	1st	1	0	0	0	1	0	0	1	1	0	0	
Trimming	2nd	1	0	1	*	*	*	*	TRIM[3:0]				

This command can be adjusted OSC frequency.



6.7 COLOR MODE COMMAND (DEFAULT VALUE=0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Color Mode	1st	1	0	0	0	0	1	1	0	0	CM[1:0]		Display Color mode CM=00 (RGB: 666; 262K colors) CM=01 (RGB:565; 65K colors) CM=10 (Mono; 64 gray) CM=11 (Mono; 2 gray)

This command set the Color mode.
For CM=00 (RGB: 666; 262K colors) mode is selected, and 1 pixel consists of 18 bits. To support max. 128 x 32 RGB dot matrix panel.
For CM=01 (RGB: 565; 65K colors) mode is selected, and 1 pixel consists of 16 bits. To support max. 128 x 32 RGB dot matrix panel.
For CM=10, (Mono mode; 64 Gray) mode is selected, and 1 pixel consists of 6 bits. To support max. 128 x 96 Mono dot matrix panel.
For CM=11, (Mono mode; 2 Gray) mode is selected, and 1 pixel consists of 1 bits. To support max. 128 x 96 Mono dot matrix panel.
If “Color mode command” be change, the parameters will be set to default value, “COM_N[6:0] “, “DR[6:0]”, “GA_SR[6:0]”, ”GA_ER[6:0]”.

6.8 GAMMA TABLE COMMAND

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Green Gamma Table	1st	1	0	0	0	0	1	0	1	0	0	0	G Gamma table setting
	2nd	1	0	1	D[7:0]Note								
	Nth	1	0	1	D[7:0]Note								
Blue Gamma Table	1st	1	0	0	0	0	1	0	1	0	0	1	B Gamma table setting
	2nd	1	0	1	D[7:0]Note								
	Nth	1	0	1	D[7:0]Note								
Red Gamma Table	1st	1	0	0	0	0	1	0	1	0	1	0	R Gamma table setting
	2nd	1	0	1	D[7:0]Note								
	Nth	1	0	1	D[7:0]Note								
Gamma Table Update	1st	1	0	0	0	0	1	0	1	0	1	1	Gamma table update

Note: D[7:0]=to access data by MCU Bus Mode.

When the Color mode is “10” (Mono; 64 gray) or “11” (Mono; 2 gray), the chip only used R Gamma table setting.

DEFAULT VALUES OF GAMMA LEVELS

For G Gamma table (colors mode-RGB666), B Gamma table (colors mode-RGB666), R Gamma table (colors mode-RGB666), G Gamma table (colors mode-RGB565), Mono mode (64 Gray)

Gamma Table No.	Default Value	Gamma Table No.	Default Value
Level_1	0X01	Level_33	0X21
Level_2	0X02	Level_34	0X22
Level_3	0X03	Level_35	0X23
Level_4	0X04	Level_36	0X24
Level_5	0X05	Level_37	0X25
Level_6	0X06	Level_38	0X26
Level_7	0X07	Level_39	0X27
Level_8	0X08	Level_40	0X28
Level_9	0X09	Level_41	0X29
Level_10	0X0A	Level_42	0X2A
Level_11	0X0B	Level_43	0X2B
Level_12	0X0C	Level_44	0X2C
Level_13	0X0D	Level_45	0X2D
Level_14	0X0E	Level_46	0X2E
Level_15	0X0F	Level_47	0X2F
Level_16	0X10	Level_48	0X30
Level_17	0X11	Level_49	0X31
Level_18	0X12	Level_50	0X32
Level_19	0X13	Level_51	0X33
Level_20	0X14	Level_52	0X34
Level_21	0X15	Level_53	0X35
Level_22	0X16	Level_54	0X36
Level_23	0X17	Level_55	0X37
Level_24	0X18	Level_56	0X38
Level_25	0X19	Level_57	0X39
Level_26	0X1A	Level_58	0X3A
Level_27	0X1B	Level_59	0X3B
Level_28	0X1C	Level_60	0X3C
Level_29	0X1D	Level_61	0X3D
Level_30	0X1E	Level_62	0X3E
Level_31	0X1F	Level_63	0X3F
Level_32	0X20		

For B Gamma table (colors mode-RGB565) as same as B Gamma table (colors mode-RGB666), R Gamma table (colors mode-RGB565) as same as R Gamma table (colors mode-RGB666)

Gamma Table No.	Default Value
Level_2	0X02
Level_4	0X04
Level_6	0X06
Level_8	0X08
Level_10	0X0A
Level_12	0X0C
Level_14	0X0E
Level_16	0X10
Level_18	0X12
Level_20	0X14
Level_22	0X16
Level_24	0X18
Level_26	0X1A
Level_28	0X1C
Level_30	0X1E
Level_32	0X20
Level_34	0X22
Level_36	0X24
Level_38	0X26
Level_40	0X28
Level_42	0X2A
Level_44	0X2C
Level_46	0X2E
Level_48	0X30
Level_50	0X32
Level_52	0X34
Level_54	0X36
Level_56	0X38
Level_58	0X3A
Level_60	0X3C
Level_62	0X3E

For Mono mode -- R Gamma table (2 Gray):

Gamma Level No.	Default Value
Level_1	0X01

This command is used to configure the Gamma table. By this table, the pixel data are mapped to corresponding width pulses of segment drivers' output. The range of pulse width is 1 to 256 PWMCLK. The written Gamma table data must be monotonically increased. If the written Gamma table values do not increase monotonically, the setting is not valid and discarded.

The new set table takes effect at the start of next frame.
The "Common Pulse Width" has higher priority than "Gamma-level". If Gamma-level ≥ com_pulse_width, the segment PWM output width (of Gamma-level) would be equal to "COM Pulse Width – Blank Period".

The required number of bytes following the command is 2, for mono mode(2 gray).
The required number of bytes following the command is 63, for G Gamma table (colors mode-RGB666), B Gamma table (colors mode-RGB666), R Gamma table (colors mode-RGB666), G Gamma table (colors mode-RGB565), Mono mode (64 Gray), B Gamma table (colors mode-RGB565), R Gamma table (colors mode-RGB565).

Before next "CS#=L", "RS=H", and "rising WR#" appear, if the sent number of bytes exceeds the range of requirement, the excess data is discarded.

When "CS#=L", "RS=H", and "rising WR#" appear, if the number of bytes is less than the required number then the data is not accepted.

After right number of data is received, the new table data would be loaded on next frame.

D7	D6	D5	D4	D3	D2	D1	D0	Function
Gamma_data[7:0]								8 bits bus / gamma data Serial interface(D7~D0)

There are 256 levels for segment driver's output pulse (1~256 PWMCLK):

L7	L6	L5	L4	L3	L2	L1	L0	Segment Pulse Duration
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	127
1	1	1	1	1	1	1	1	256

Please refer to "SEG /COM waveform".
While MCU configuring Gamma table, the CS# can either go high after command-writing or parameter-writing (Figure a), or stay low during all the command time (Figure b).

While MCU configuring Gamma table, if the number of parameter bytes sent by the MCU are not enough, the all data are discarded, Figure c.

Example for Mono mode(2 Gray) table and MCU bus mode is '11' is as the following figures:

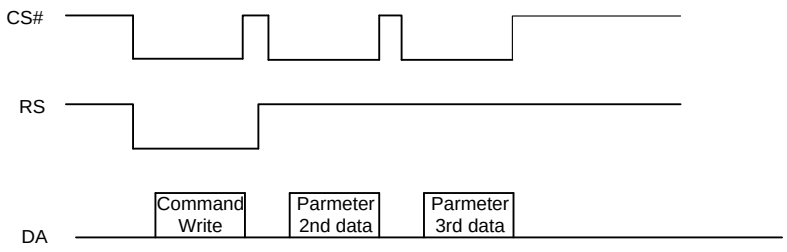


Figure a. CS# can go high after a command-writing/parameter-writing.

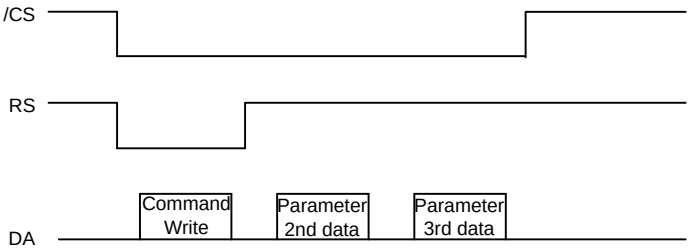
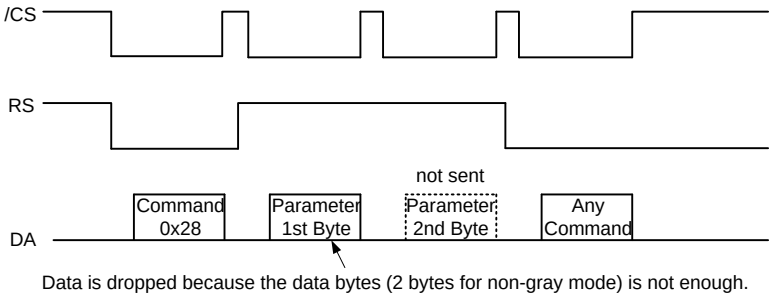
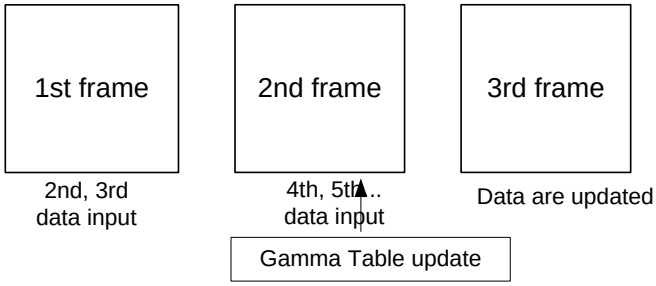


Figure b. CS# can stay low.



c. Failure example of Mono (2Gray) Gamma-level

The chip responds to new settings at the beginning of a new frame after "Gamma Table update" command are sent. The behavior is illustrated by the following figure:



6.9 ROW ADDRESS SETTING CMMAND (DEFAULT VALUE=00H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Row Address Setting	1st	1	0	0	1	0	0	0	0	0	0	0	Set the Row address start of the image.
	2nd	1	0	1	*	RA[6:0]							

"Row address" can be the value of 0 to 31 for color mode.
"Row address" can be the value of 0 to 95 for mono mode.

6.10 COLUMN ADDRESS SETTING COMMAND (DEFAULT VALUE=00H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Column Address Setting	1st	1	0	0	1	0	0	0	0	0	0	1	Set the column address of the image.
	2nd	1	0	1	*	CA[6:0]							

"Column address" can be the value of 0 to 127 for color mode and mono mode(64-Gray).
"Column address" can be the value of 0, 8, 16…, 120 for mono mode(2-Gray).

6.11 RETURN LENGTH SETTING COMMAND (DEFAULT VALUE=7FH)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Return Length Setting	1st	1	0	0	1	0	0	0	0	0	1	0	Return Length setting
	2nd	1	0	1	*	RL[6:0]							

These commands are for MCU to read/write image to graphic data RAM (GDRAM).

The image that MCU can write/read is a 128x32 RGB-pixel image. The "row address" and "column address" define the start pixel position of image where the MCU would read/write image data. The "return length" defines the number of pixels in a line that MCU could read/write.

"Return Length" can be the value of 0 to 127 for color mode and mono mode(64-Gray).
"Return Length" can be the value of 0, 8, 16…, 120 for mono mode(2-Gray).

6.12 DISPLAY DATA WRITE/READ COMMAND

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Display Data Write	1st	1	0	0	1	0	0	0	0	0	1	1	Display Data Write
Display Data Write	2nd	1	0	1	Write Data D[7:0]								Write graphic data to RAM
Display Data Read	1st	1	0	0	1	0	0	0	0	1	0	0	Display Data Read
Display Data Read	2nd	0	1	1	Read Data D[7:0]								Read graphic data from the RAM.

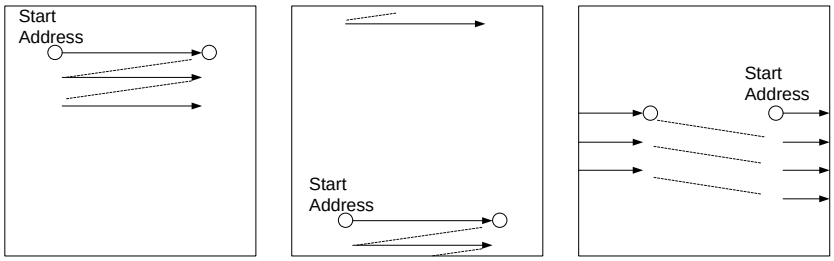
Graphic RAM has 128x32 pixels (18 bits/1 pixel) for color mode(RGB666).
Graphic RAM has 128x32 pixels (16 bits/1 pixel) for color mode(RGB565).
Graphic RAM has 128x96 pixels (6 bits/1 pixel) for mono mode(64 gray).
Graphic RAM has 128x96 pixels (1 bit/1 pixel) for mono mode(2 gray).

When MCU reads or writes pixel(color mode(RGB666)=3 bytes) in normal mode, the address pointer would increase 1 automatically.
When MCU reads or writes pixel(color mode(RGB565)=2 bytes) in normal mode, the address pointer would increase 1 automatically.
When MCU reads or writes pixel(mono mode(64 gray)= 1 byte) in normal mode, the address pointer would increase 1 automatically.
When MCU reads or writes pixel(mono mode(2 gray)= 1 byte) in normal mode, the address pointer would increase 8 automatically.

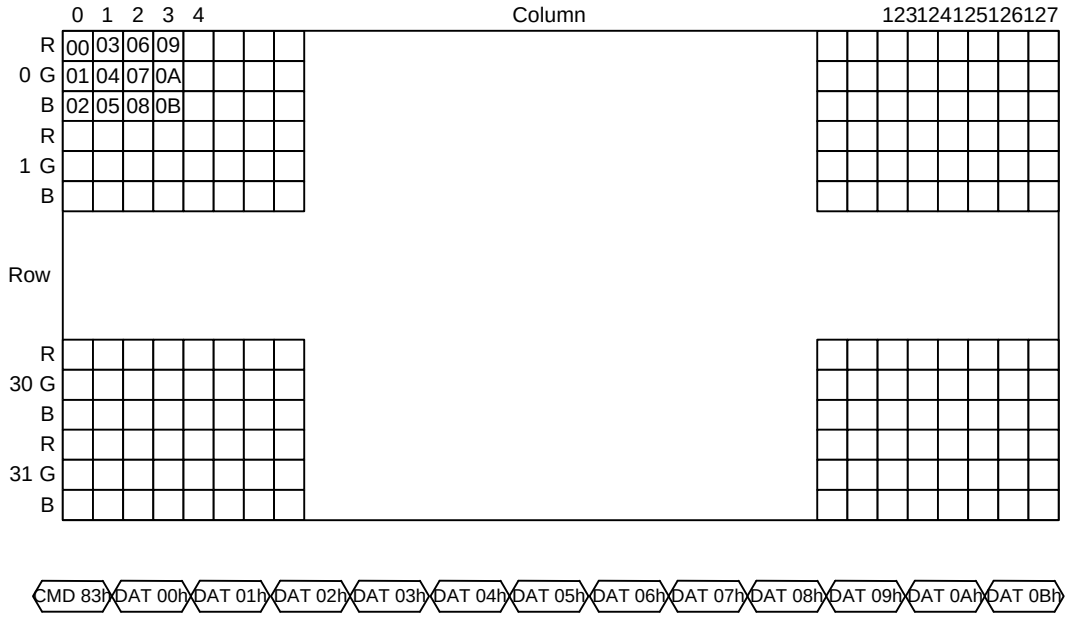
This RAM data Read/Write in RGB / Mono mode.

	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]/SDA	D[0]/SCK	Function
1st	*	*	R[5:0]						8 bits bus/color mode(RGB666) Serial interface(D7~D0)/color mode(262k colors)
2nd	*	*	G[5:0]						
3rd	*	*	B[5:0]						
1st	R[4:0]					G[5:3]			8 bits bus/color mode(RGB565) Serial interface(D7~D0)/color mode (262k colors)
2nd	G[2:0]		B[4:0]						
1st	*	*	DATA[5:0]						8 bits bus/mono mode(64 Gray)
1st	P7	P6	P5	P4	P3	P2	P1	P0	8 bits bus/mono mode(2 Gray)

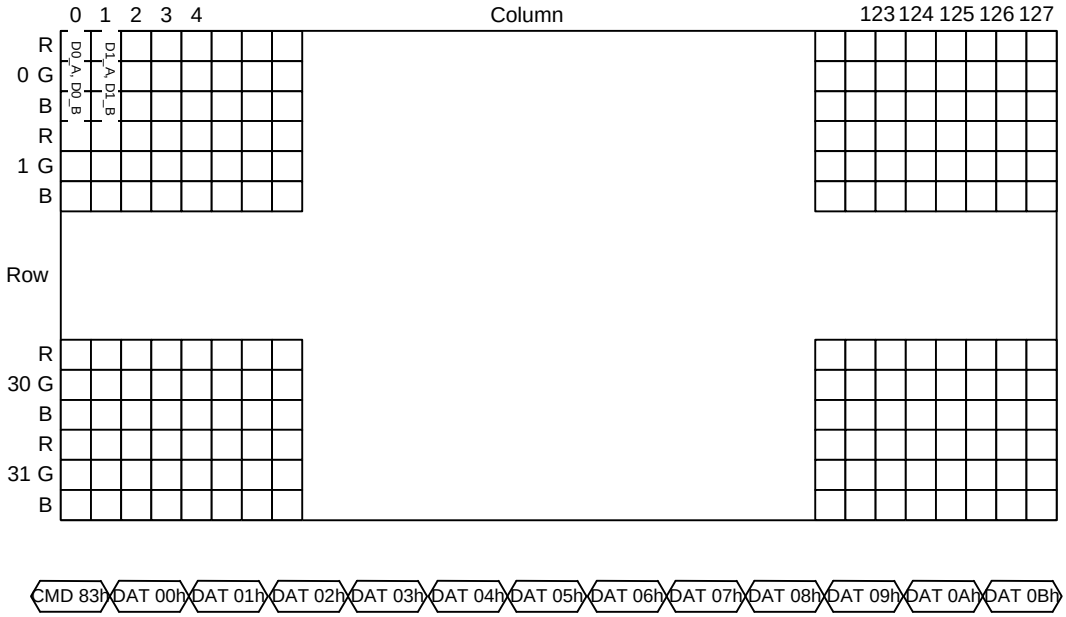
If the pixels of a line travel across the line boundary, the pixel position return to the beginning of the line and continue to traverse the line till the number of pixels satisfy. Then, the pixel position goes to the “column start” of the next line. The following 3 figures illustrate the behavior.



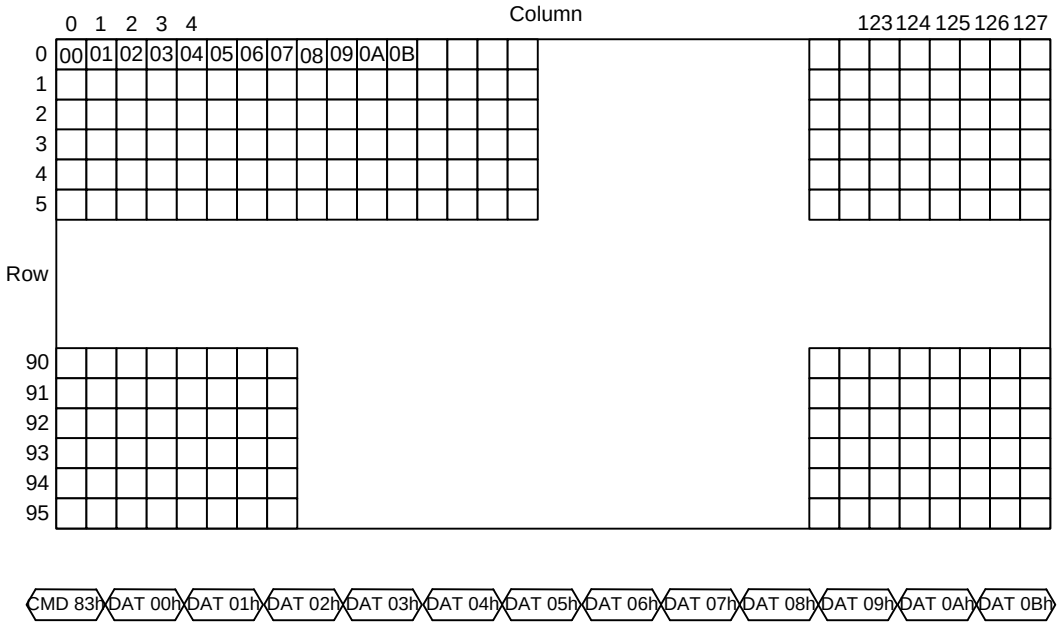
Example: for color mode(RGB666), write data: 00h, 01h, …, 0Bh



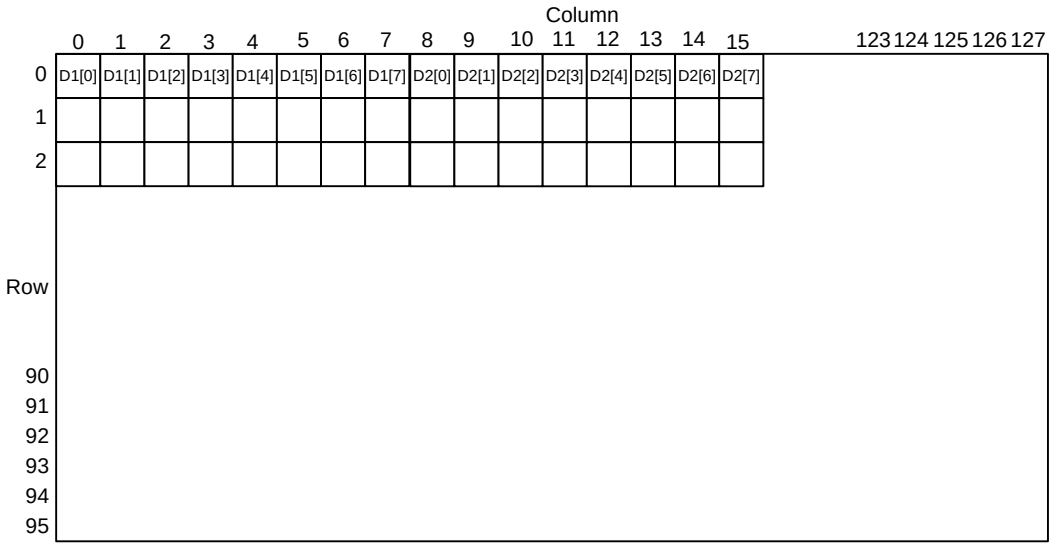
Example: for color mode(RGB565), write data: D0_A, D0_B, …, D4_A, D4_Bh
RGB565(R[4:0], G[5:0], B[4:0]) be transferred to RGB666(R[4:0],1'b0, G[5:0], B[4:0], 1'b0).

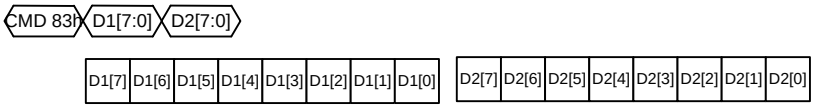


Example: mono mode(64 gray), write data: 00h, 01h, …, 0Bh



Example: mono mode(2 gray), write data: D1, D2





6.13 DISPLAY ON/OFF COMMAND (DEFAULT VALUE=0H)

Byte information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Display ON/OFF	1st	1	0	0	0	1	0	1	1	0	B1	B0	(B1, B0)= 00: Type_1 OFF 01: Type_2 OFF 10: All ON 11: Normally display

This command sets the display ON/OFF behavior.

(B1, B0)	Function
"00" (Type_1 OFF)	All segment outputs are low, All common outputs are high.
"01" (Type_2 OFF)	All segment outputs are low All common scan normally.
"10" (ALL ON),	All segment outputs are high All common scan normally.
"11" (Normally Display)	The chip scans normally.

6.14 VERTICAL AND HORIZONTAL MIRROR COMMAND (DEFAULT VALUE=0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Vertical and Horizontal Mirror	1st	1	0	0	0	1	1	0	1	0	H	V	Rotate display image V=1, Vertical mirroring H=1, Horizontal mirroring

This command is vertical / horizontal mirroring for display image data.

6.15 GRAPHIC ACCELERATION ENABLE COMMAND (DEFAULT VALUE=0H)

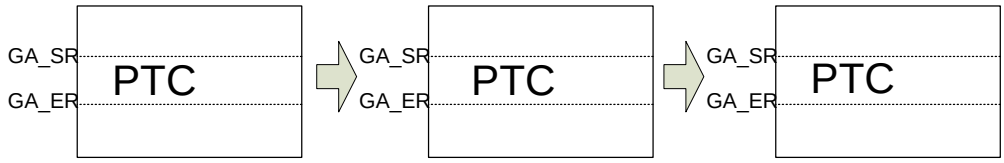
Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Graphic Acceleration Enable	1st	1	0	0	0	1	1	1	0	0	0	GE	GE=1, Graphic Acceleration enable

6.16 GRAPHIC ACCELERATION MODE COMMAND (DEFAULT VALUE=0H)

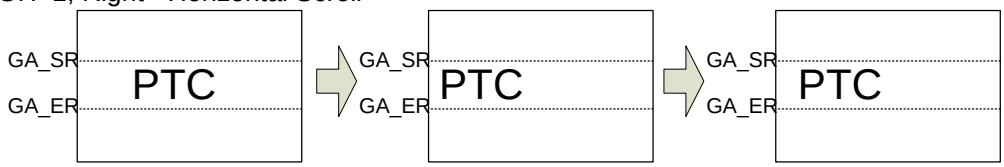
Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Graphic Acceleration Mode	1st	1	0	0	0	1	1	1	0	0	1	0	Graphic Acceleration Setting GA[2:0] = 000: Horizontal Scroll 001: Vertical Scroll 010: Horizontal and Vertical Scroll 011: Fade Out 100: Blinking 101: Zoom In 110~111: No active
	2nd	1	0	1	*	*	*	GH	GV	GA[2:0]			

GA[2:0]=000 : Horizontal Scroll. For the continuous horizontal scroll function, the display scroll one column at each GA_FN frames.

GH=0, Left - Horizontal Scroll

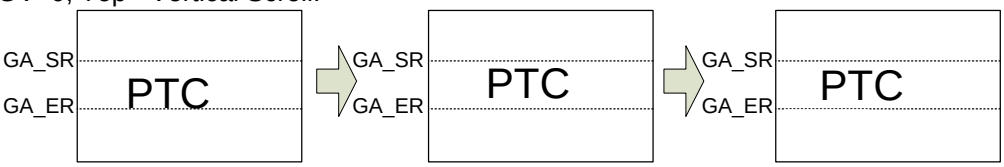


GH=1, Right - Horizontal Scroll

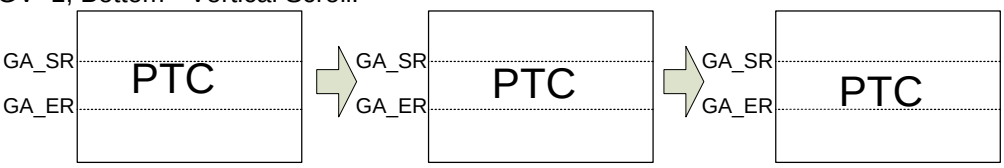


GA[2:0]=001 : Vertical Scroll. For the continuous Vertical scroll function, the display scroll one row at each GA_FN frames.

GV=0, Top - Vertical Scroll.

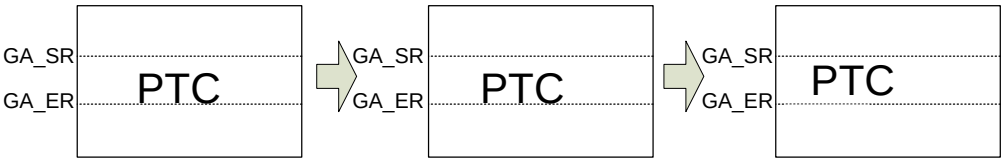


GV=1, Bottom - Vertical Scroll.

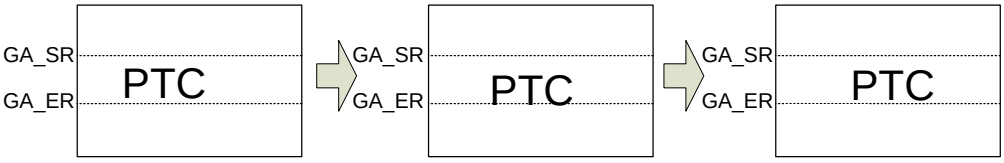


GA[2:0]=010 : Horizontal and Vertical Scroll. For the continuous Horizontal and Vertical scroll function, the display scroll one row and column at each GA_FN frames.
GH=0, Left - Horizontal Scroll. GH=1, Right - Horizontal Scroll.
GV=0, Top - Vertical Scroll. GV=1, Bottom - Vertical Scroll.

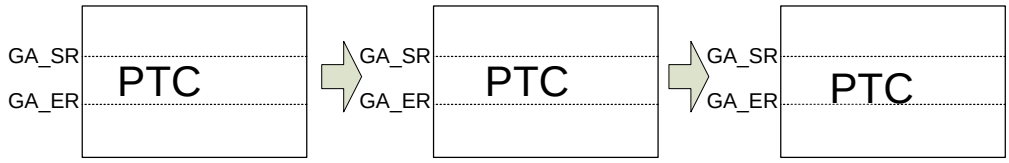
GV=0, GH=0



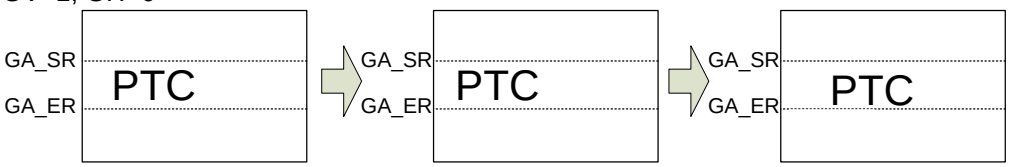
GV=1, GH=1



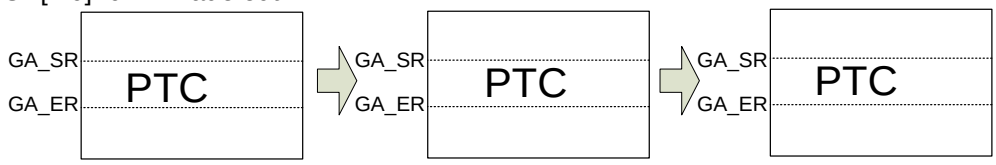
GV=0, GH=1



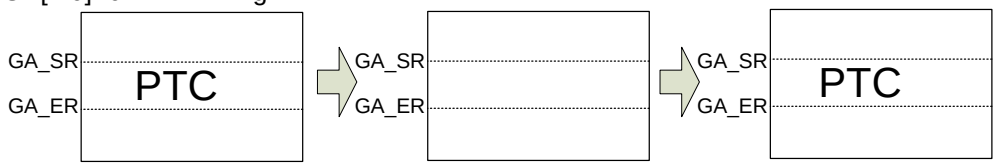
GV=1, GH=0



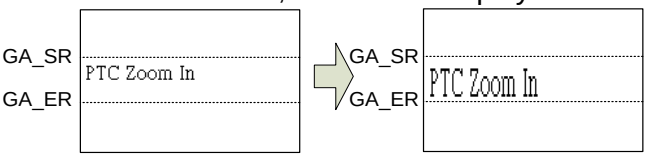
GA[2:0]=011 : Fade out.



GA[2:0]=011 : Blinking.



Under Zoom in mode, one row of display contents is expanded into two rows on the display.



6.17 ACCELERATION FRAME SETTING COMMAND (DEFAULT VALUE=0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Acceleration Frame setting	1st	1	0	0	0	1	1	1	0	0	1	1	Set time interval for each step GA_FN[7:0] : N+1 frames
	2nd	1	0	1	GA_FN[7:0]								

6.18 ACCELERATION START/END ROW SETTING COMMAND (DEFAULT VALUE GA_SR=0H / GA_ER=1FH)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Acceleration Start / End Row	1st	1	0	0	0	1	1	1	0	1	0	0	Set start/end row for graphic acceleration mode GA_SR[6:0] : Start row GA_ER[6:0] : End row
	2nd	1	0	1	*	GA_SR[6:0]							
	3rd	1	0	1	*	GA_ER[6:0]							

The command be must condition,"GA_SR[6:0] <= GA_ER[6:0]".

6.19 BLACK-WHITE INVERSION COMMAND (DEFAULT VALUE=0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Black-White Inversion	1st	1	0	0	0	1	1	1	1	0	0	Y	Y=0, Normal Y=1, black-white inversion

When this command sets Y=1, the pixel will be black-white inverted. The inverted pixel data is 1's complement of original pixel data.

6.20 OVERLAP MODE COMMAND (DEFAULT VALUE = 0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Overlap	1st	1	0	0	1	0	1	1	0	0	0	OM	

This command sets the type of cathode output.

Setting	Type
M=1	High-overlap
M=0	Low-overlap

Please refer to "SEG / COM waveform" for timing diagram.

6.21 SEGMENT OUTPUT TYPE COMMAND (DEFAULT VALUE=0H)

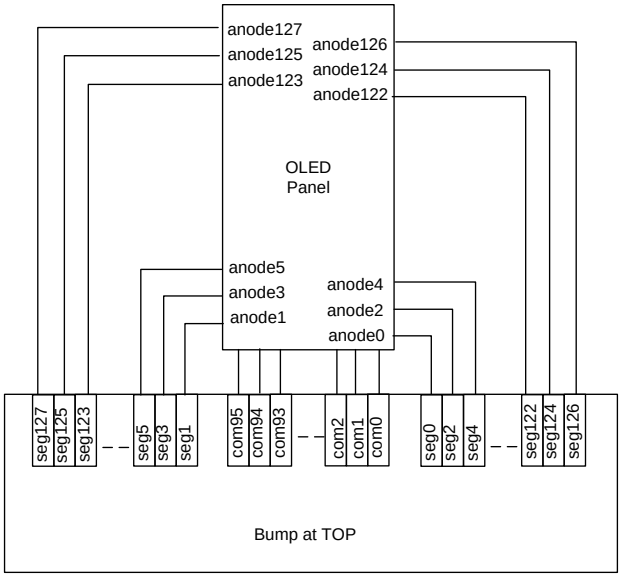
Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
SEG Output Type	1st	1	0	0	1	0	1	1	0	0	1	SQ	SEG0~SEG127 output type SQ=0: (COM_{3n}, COM_{3n+1}, COM_{3n+2}) is RGB SQ=1: (COM_{3n}, COM_{3n+1}, COM_{3n+2}) is BGR

This command sets the type of Segment output.
For SQ=0, the color type of (COM_{3n}, COM_{3n+1}, COM_{3n+2}) is "RGB"
For SQ=1, the color type of (COM_{3n}, COM_{3n+1}, COM_{3n+2}) is "BGR".
For Mono_mode, SEG Output Type is invalid.

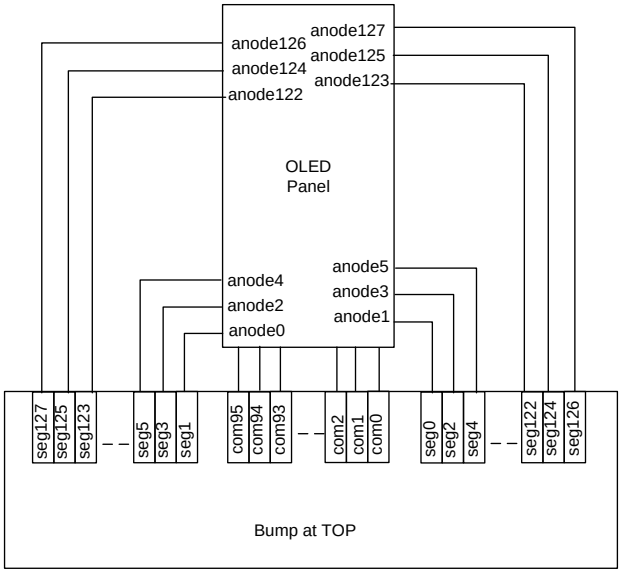
6.22 SEG EVEN/ODD SWAP COMMAND (DEFAULT VALUE=0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
SEG EVEN/ODD Swap	1st	1	0	0	1	0	1	1	0	1	0	0	SE=1, EVEN / ODD pin swap.
	2nd	1	0	1	*	*	*	*	*	*	*	SE	

When SE=0,



When SE=1,



6.23 VOLTAGE/ CURRENT CONTROL COMMAND (DEFAULT VALUE CE= 0H, IRE=0H, DAC=5H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Voltage/ Current Control	1st	1	0	0	1	0	1	1	0	1	0	1	If CE = 0; COM voltage by pin "VHC" If CE = 1; COM voltage by DAC setting. COM voltage= 0.72 ~ 0.86 (VHA)" IRE
	2nd	1	0	1	CE	IRE	*	*	*	DAC[2:0]			

The common voltage is generated by embedded high-voltage regulator (DAC) whose output level is controlled by 3-bit control register (DAC[2:0]).
During blank period, the output voltage of anode and cathode are the same. If register CE = 0, the voltage is provided by external supplier; If CE = 1, the voltage provided by embedded high-voltage regulator whose voltage is controlled by this register.

DAC[2:0]	Common Voltage
0	0.72 x VHA
1	0.74 x VHA
:	:
5	0.82 x VHA
6	0.84 x VHA
7	0.86 x VHA

If IRE = 1, the current of anodes provided by external current source pin(IREF) whose reference current is controlled by this register.

6.24 SET BRIGHTNESS DECREASE COMMAND (DEFAULT VALUE=00H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
COMP_BRI	1st	1	0	0	1	0	1	1	0	1	1	1	Set Brightness decrease table PE4 is enable
	2nd	1	0	1	*	BR1[2:0]			*	BR0[2:0]			
	3rd	1	0	1	*	BR3[2:0]			*	BR2[2:0]			
	Nth	1	0	1	*	….			*	….			

This command set brightness decrease table for compensation, When PE4 is enable. BR0 is brightness decrease of com0. BR1 is brightness decrease of com1, … and BR95 is brightness decrease of com95.

6.25 BRIGHTNESS COMMAND (DEFAULT VALUE=7FH)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Brightness	1st	1	0	0	1	0	1	1	1	0	0	0	set segment output current BRR[6:0]: R-Brightness BRG[6:0]: G-Brightness BRB[6:0]: B-Brightness
	2nd	1	0	1	*	BRR[6:0]							
	3rd	1	0	1	*	BRG[6:0]							
	4th	1	0	1	*	BRB[6:0]							

This command set the segment output current. The larger current makes higher brightness of panel.
In mono-mode, The brightness is only using BRR[6:0].

6.26 COMPENSATION THRESHOLD COMMAND

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Compensation Threshold	1st	1	0	0	1	0	1	1	1	0	1	0	Set threshold of compensation
	2nd	1	0	1	TH1[7:0]								
	3rd	1	0	1	TH2[7:0]								
	4th	1	0	1	TH3[7:0]								
	5th	1	0	1	TH4[7:0]								

Default Values of Threshold of compensation:

Threshold No.	Default Value
TH1[7:0]	50
TH2[7:0]	100
TH3[7:0]	125
TH4[7:0]	128

TH1~TH4 value be must condition, “0 < TH1 < TH2 < TH3 < TH4 <= 128”.

6.27 COMPENSATION PULSE THRESHOLD COMMAND (DEFAULT VALUE = 42H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Compensation Pulse Threshold	1st	1	0	0	1	0	1	1	1	0	1	1	Set pulse threshold of compensation
	2nd	1	0	1	CPT[7:0]								

The command is setting pulse threshold for compensation. If PWM pulse is smaller than this threshold, the PWM pulse will be not compensation of “PWM decrease table” when the PE3 of “PWM Decrease Enable” is enable.

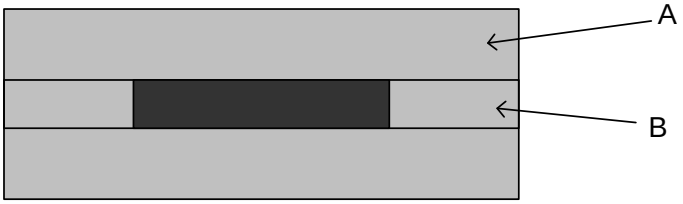
6.28 PWM DECREASE ENABLE COMMAND (DEFAULT PE3, PE2, PE1, PE0 =0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Compensation Enable	1st	1	0	0	1	0	1	1	0	1	1	0	Set PWM decrease enable
	1	0	1	1	*	*	*	*	PE4	PE3	PE2	PE1	

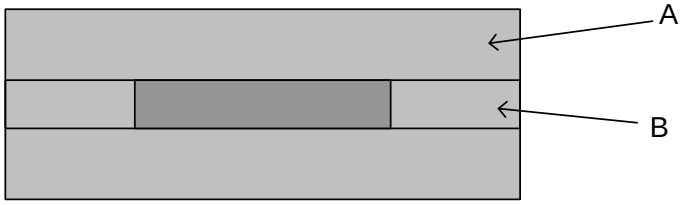
The command is setting PWM decrease enable for crosstalk issue. The case1 pattern is black-bar on the line. The case2 pattern is gray-bar on the line. The line B will be compensation.

PE1 is “1”, this is enable case1 compensation by PWD_table.
PE2 is “1”, this is enable case2 compensation by PWD_table.
PE3 is “1”, this is enable of pulse threshold compensation.
PE4 is “1”, this is enable of brightness compensation.

Case 1



Case 2



6.29 PWM DECREASE TABLE COMMAND

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
PWD_Table	1st	1	0	0	1	0	1	1	1	0	0	1	Set PWM decrease table
	2nd	0	1	1	PWD_1[3:0]				PWD_0[3:0]				
	3rd	0	1	1	PWD_3[3:0]				PWD_2[3:0]				
	4th	0	1	1	*				PWD_4[3:0]				

Default Values of PWD table:

Gray Level Counter	Threshold No.	Default Value	Decrease Pulse Width
0~H1	PWD_0[3:0]	0000	0 PWMCLK
(TH1+1)~H2	PWD_1[3:0]	0001	1 PWMCLK
(TH2+1)~H3	PWD_2[3:0]	0010	2 PWMCLK
(TH3+1)~H4	PWD_3[3:0]	0011	3 PWMCLK
(TH4+1)~28	PWD_4[3:0]	0100	4 PWMCLK

PWD table decrease pulse width= PWD_N x PWMCLK.

6.30 CATHODE SCAN DIRECTION COMMAND (DEFAULT VALUE = 0H)

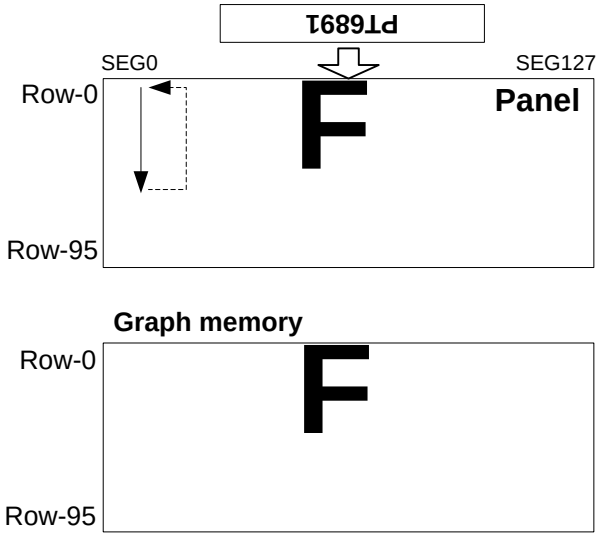
Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Cathode Scan Direction	1st	1	0	0	1	0	1	1	1	1	0	CD	CD: COM Scan direction

This command set the cathode scan mode.

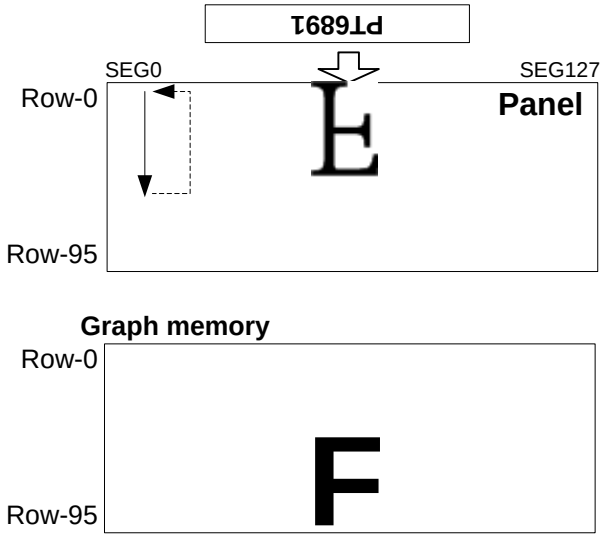
CD (Scan Direction)	Description
0	From the COM0 to COMn
1	From the COMn to COM0

IN MONO_MODE:

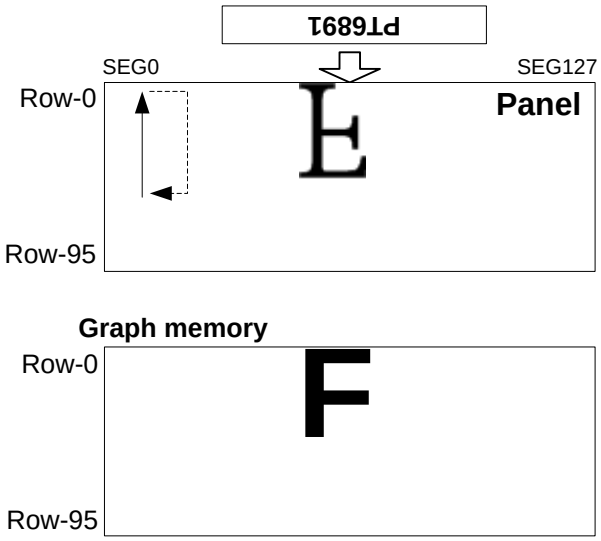
CD = 0, V = 0, H = 0



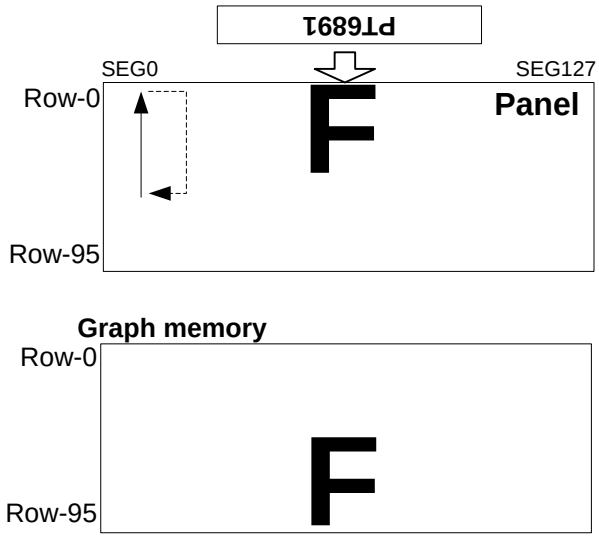
CD = 0, V = 1, H = 0



CD = 1, V = 0, H = 0

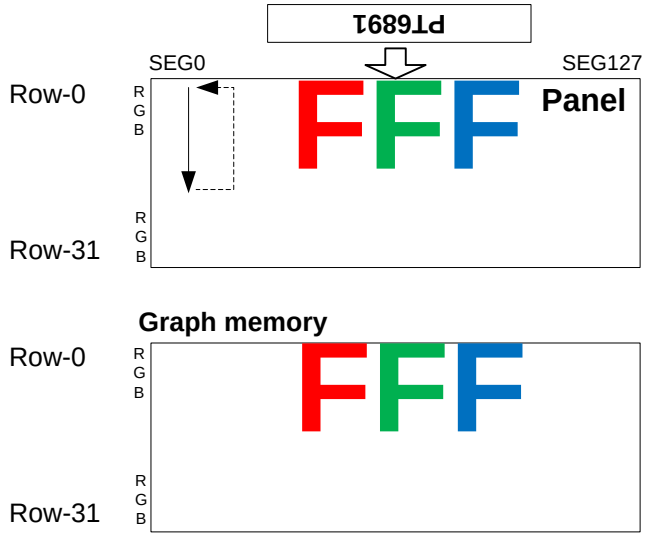


CD = 1, V = 1, H = 0

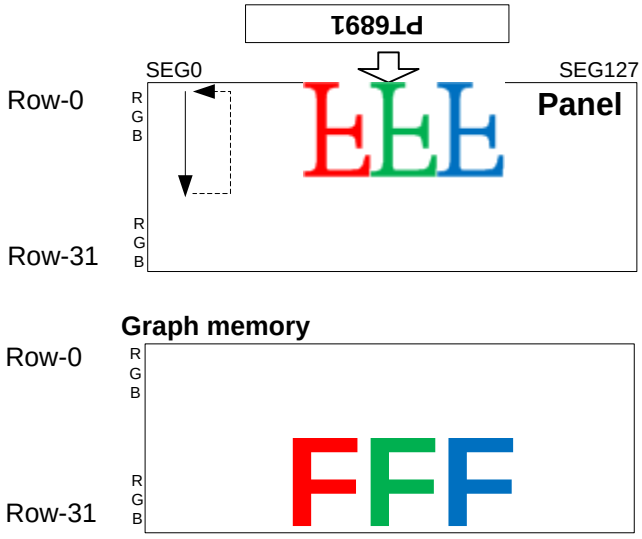


IN COLOR_MODE:

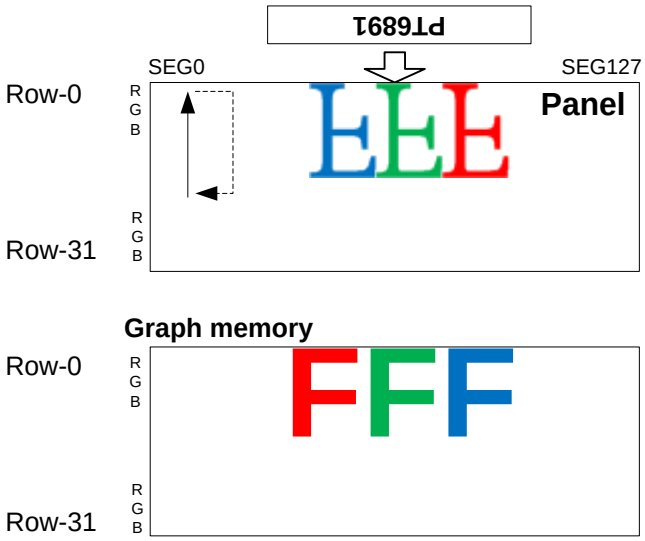
CD = 0, V = 0, H = 0



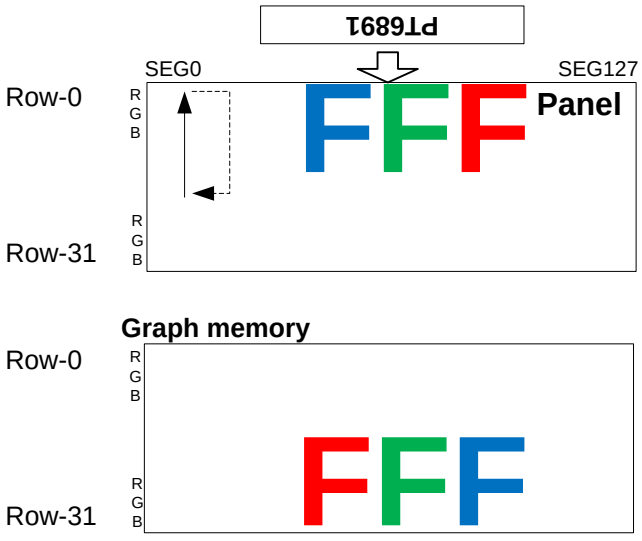
CD = 0, V = 1, H = 0



CD = 1, V = 0, H = 0



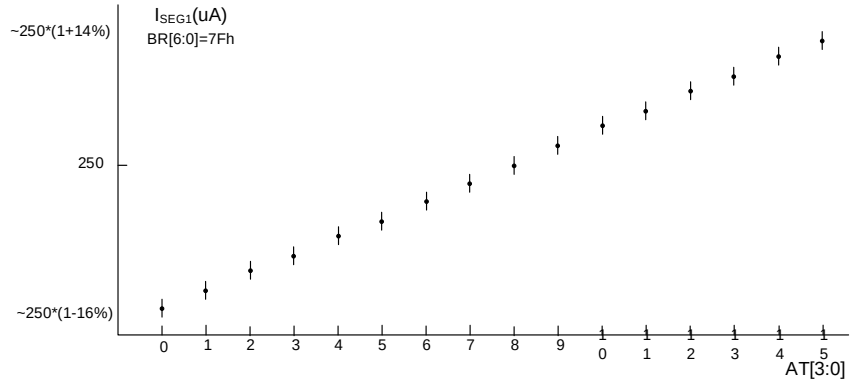
CD = 1, V = 1, H = 0



6.31 ANODE TRIMMING COMMAND (DEFAULT VALUE = 8H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Anode Trimming	1st	1	0	0	1	0	1	1	1	1	1	0	Anode Current Trimming
	2nd	1	0	1	*	*	*	*	AT[3:0]				

This command set trimming current of anode.



6.32 PRE-CHARGE PERIOD COMMAND (DEFAULT=AH)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Pre-charge Period	1st	1	0	0	1	1	0	0	1	0	0	0	Pre-charge period
	2nd	1	0	1	*	*	*	*	PR[3:0]				

This command sets the duration of pre-charge time (0~15 x 4 PWMCLK).
PR[3:0] : pre-charge time, default “Ah”. Please refer to “SEG /COM waveform”.

6.33 PRE-CHARGE CURRENT COMMAND (DEFAULT VALUE=3H)

Byte Information		RDB	WRB	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Pre-charge Current	1st	1	0	0	1	1	0	1	0	0	0	0	Pre-charge current select
	2nd	1	0	1	*	*	*	*	*	*	PC[1:0]		

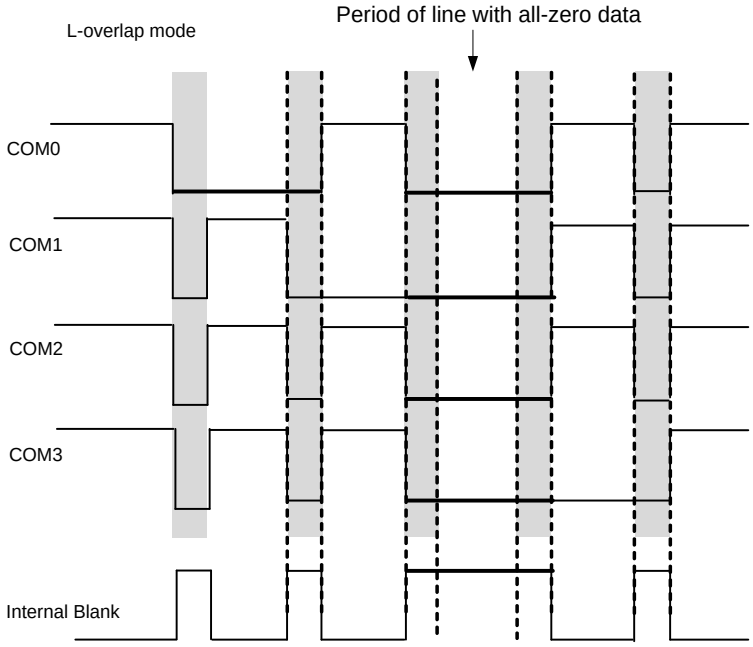
This command set the pre-charge current to be below table.

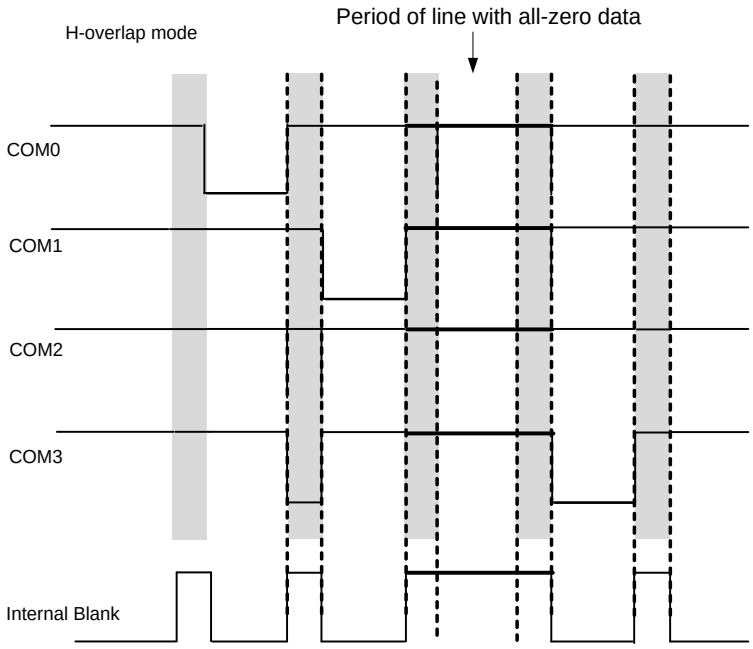
PC	Pre-Charge Current	I_{seg7F} = 250μA
“11”	(I_{seg7F} X 2) (μA)	(250 X 2) =500 (μA)
“10”	(I_{seg3F} X 2) (μA)	(125 X 2) =250 (μA)
“01”	(I_{seg1F} X 2) (μA)	(62.5 X 2) =125 (μA)
“00”	(I_{seg0F} X 2) (μA)	(31.25 X 2) =62.5 (μA)

6.34 ALL-ZERO BLANK MODE COMMAND (DEFAULT VALUE = 0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
All-zero Blank Mode	1st	1	0	0	1	1	0	0	1	1	0	ZB	ZB=1, enable

While enabling this mode (ZB = 1), there is no scan (blank) for the line with all-zero data.





6.35 COM PULSE WIDTH COMMAND (DEFAULT VALUE=06H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
COM Pulse Width	1st	1	0	0	1	1	0	1	1	0	0	0	Determine COM pulse width
	2nd	1	0	1	COM_W[7:0]								
	3rd	1	0	1	*	*	*	*	*	*	*	[8]	

This command sets the low-active duration of all common driver outputs. The minimum pulse duration is 65 PWMCLK and the maximum duration is 576 PWMCLK.

If Gray-level ≥ com_pulse_width, the segment PWM output width (of Gamma-level) would be equal to “COM Pulse Width – Blank Period”.

COM_W[8:0]									COM pulse width period
0	0	0	0	0	0	0	0	0	65 PWMCLK
0	0	0	0	0	0	0	0	1	66 PWMCLK
0	0	0	0	0	0	0	1	0	67 PWMCLK
0	0	0	0	0	0	0	1	1	68 PWMCLK
:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	0	575 PWMCLK
1	1	1	1	1	1	1	1	1	576 PWMCLK

Please refer to “SEG /COM waveform”.

6.36 COM NUMBER COMMAND (DEFAULT VALUE=1FH)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
COM Number	1st	1	0	0	1	1	1	0	0	0	0	0	Setting Row numbers
	2nd	1	0	1	*	COM_N[6:0]							

The “COM Number” set the lines number to be displayed.

The “COM number” value of 0 to 31 map to 1 ~ 32 rows that is displayed to panel for color-mode
The “COM number” value of 0 to 95 map to 1 ~ 96 rows that is displayed to panel for Mono-mode.

6.37 DISPLAY ROW START COMMAND (DEFAULT VALUE=00H)

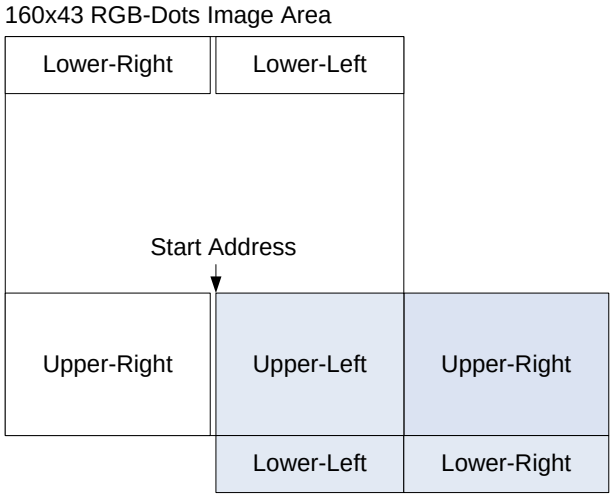
Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Display Row Start	1st	1	0	0	1	1	1	0	0	0	0	1	Start of row address for display
	2nd	1	0	1	*	DR[6:0]							

“Display Row start” can be the value of 0 to 31 for color mode.
“Display Row start” can be the value of 0 to 95 for mono mode.

6.38 DISPLAY COLUMN START COMMAND (DEFAULT VALUE=00H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Display Column Start	1st	1	0	0	1	1	1	0	0	0	1	0	Start of column address for display
	2nd	1	0	1	*	DC[6:0]							

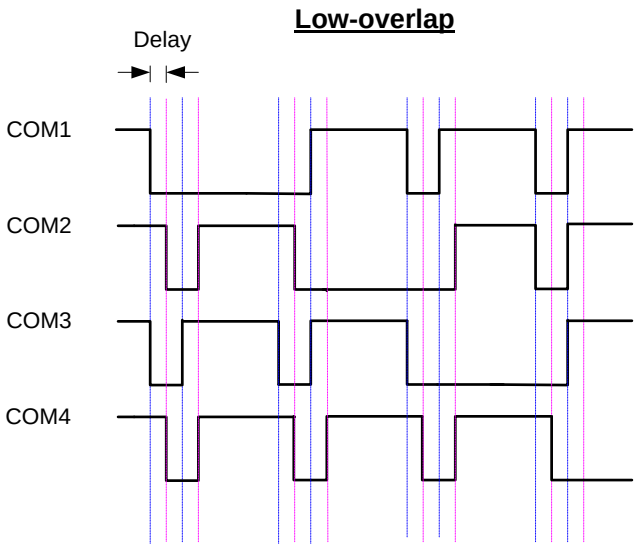
The “Display Row Start” and “Display Column Start” set the start position of pixel to be displayed.
“Display Column start” can be the value of 0 to 127.



6.39 COM OUTPUT DELAY MODE COMMAND (DEFAULT VALUE = 0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
COM Output	1st	1	0	0	1	1	1	0	0	0	1	1	To set delay between odd and even bits of cathode driver
Delay Mode	2nd	1	0	1	*	*	*	*	*	*	D1	D0	

When Low-overlap mode is selected, this command could set the delay time of even common output relative to odd common outputs.



(D1, D0)	Delay Time (T_{PWMCLK} X 4)
‘00’	0
‘01’	1
‘10’	2
‘11’	3

6.40 BLACK / BLANK PERIOD COMMAND (DEFAULT VALUE=AH)

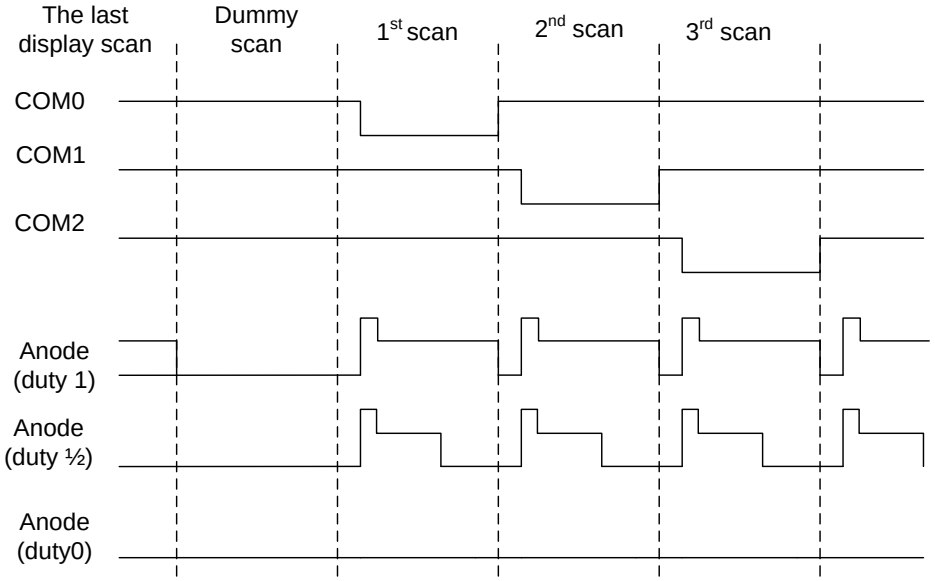
Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Blank Period	1st	1	0	0	1	1	1	0	0	1	0	1	Black / Blank period
	2nd	1	0	1	Black[2:0]			Blank[4:0]					

This command sets the black (Black) duration (0~7 x 4 PWMCLK) of all segment driver outputs.
This command sets the blank (Blank) duration (4~31 x 4 PWMCLK) of all common driver outputs. When “Blank” is setting less than 4, it is invalid command.
Please refer to “SEG /COM waveform”.

6.41 DUMMY SCAN COMMAND (DEFAULT VALUE=0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Dummy Scan	1st	1	0	0	1	1	1	0	0	1	1	DS	DS=1, dummy scan be enable

There is an additional dummy scan followed by a frame of display scan. In the period of dummy scanning, all commons output HIGH and all anodes output LOW.



6.42 TESTMOD ENABLE COMMAND

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
TESTMOD Enable	1st	1	0	0	1	1	0	0	0	1	0	0	TSTMOD enable TM=0 disable TM=1 enable
	2nd	1	0	1	0	1	0	1	0	1	0	1	
	3rd	1	0	1	1	0	1	0	1	0	1	0	
	4th	1	0	1	0	0	0	0	0	0	0	TM	

If “TM” be setting from “1” to “0”, the parameters will be set to default value, “T[7:0] “, “TEST_RGB[7:0]”, “CO”.

6.43 DRIVER OUTPUT TEST MODE COMMAND (DEFAULT VALUE=0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Driver Output Test Mode	1st	1	0	0	1	1	0	0	0	0	0	0	TSTMOD(TM=1) must be enable
Mode	2nd	1	0	1	T7	T6	T5	T4	T3	T2	T1	T0	

This command configures the segment drivers' outputs and common drivers' outputs for test purpose.
For (T2, T1, T0)="000", Normal mode.

For (T2, T1, T0)="001", all segment outputs and common outputs are LOW.

For (T2, T1, T0)="010", all segment outputs and common outputs are HIGH. Please PR[3:0] be set to "0h", before this command be setting.

For (T2, T1, T0)="011", all segment drivers are High-impedance, and common drivers scan normally for cathode testing.

For (T2, T1, T0)="100", all segment drivers are High-impedance, and common drivers are controlled by MCU via serial interface. In '100' mode, the MCU interface is switched to serial mode automatically.

For (T2, T1, T0)="101", segment drivers and common drivers are controlled by MCU via serial interface. In '101' mode, the MCU interface is switched to serial mode automatically.

For (T2, T1, T0)="110", segment drivers and common drivers are controlled by MCU via serial interface; the segments always output pre-charge current. In '110' mode, the MCU interface is switched to serial mode automatically.

For (T2, T1, T0)="111", segment drivers, and the bias circuit are disabled; common drivers is all High (H-overlap) or Low(L-overlap).

The following table is summary of (T2, T1, T0):

(T2, T1, T0)	Segment Driver	Common Driver	Bias Circuit
"000"	Normally scan	Normally scan	Enabled
"001"	All Low	All Low	Enabled
"010"	All High	All High	Enabled
"011"	High-Impedance	Normally scan	Disabled
"100"	High-Impedance	MCU serial input	Enabled
"101"	MCU serial input	MCU serial input	Enabled
"110"	MCU serial input	MCU serial input	Enabled
"111"	High-Impedance	all High(H-overlap) or all Low(L-overlap)	Disabled

If T7=1, all segment drivers are disabled.

T7	Segment Driver
0	Normal
1	High-impedance

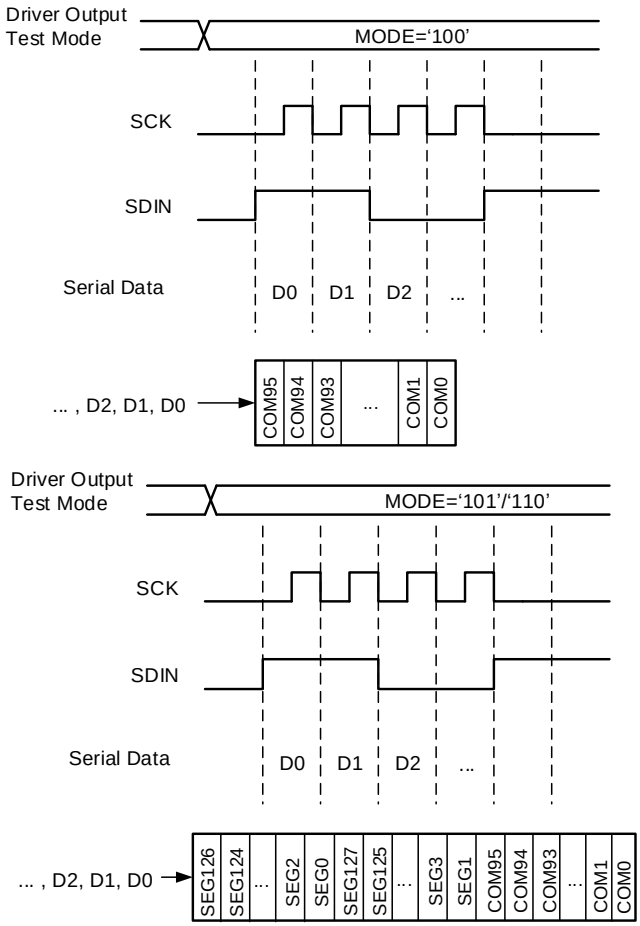
If T6=1, all common drivers are disabled.

T6	Common Driver
0	Normal
1	all High(H-overlap) or all Low(L-overlap)

If T5=1, the bias circuit is disabled.

T5	Bias Circuit
0	Enabled
1	Disabled

The input timing for Mode='100', '101' and '110' are specified by following figures(D[1] will force SDIN, D[0] will force to SCK) :



If T3=1, Graphic Data RAM out will be "TESTRGB data" replace.
If T4=1, D7-D0, INT will be setting to output mode and value is bit0 of "TESTRGB data".

6.44 TEST RGB DATA (DEFAULT VALUE=0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Test RGB data	1st	1	0	0	1	1	0	0	0	0	0	1	TSTMOD(TM=1) must be enable.
	2nd	1	0	1	D[7:0]								Reserved for testing

If T4=1, D[7:0], INT is value for test output pads.

6.45 CLOCK OUTPUT TEST MODE (DEFAULT VALUE=0H)

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Clock Output Test Mode	1st	1	0	0	1	1	0	0	0	1	0	1	TSTMOD(TM=1) must be enable.
	2nd	1	0	1	0	0	0	0	0	0	0	CO	Reserved for testing

If CO=1, the INT pin could output clock signal.

When CO=1, the output clock signal could be OSC clock signal Divide 2 (If F_{OSC} =3.3MHz, measure F_{INT} = 3.3MHz / 2 = 1.65MHz).

6.46 PARAMETER READ TEST MODE

Byte Information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Parameter Read	1st	1	0	0	1	1	0	0	1	1	1	0	
	2nd	0	1	1	Read Data								Read parameter data.
	Nrd	0	1	1	Read Data								

This command configures the parameter data outputs for test purpose.

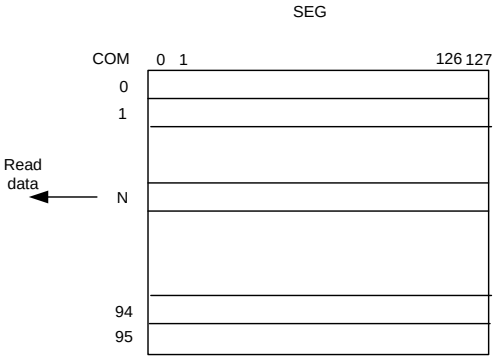
Read Byte	Register
0	INT
1	DIV[1:0]
2	TRIM[3:0]
3	CM
4	RA[7:0]
5	CA[7:0]
6	RL[7:0]
7	B1,B0
8	H,V
9	GE
10	GA[2:0]
11	GA_FN[7:0]
12	GA_SR[7:0]
13	GA_ER[7:0]
14	BW
15	OM
16	SQ
17	SE
18	CE, IRE,3'b0,DAC[2:0]
19	BRR[6:0]
20	BRG[6:0]
21	BRB[6:0]
22	TH1[7:0]
23	TH2[7:0]
24	TH3[7:0]
25	TH4[7:0]
26	CPT[7:0]
27	PE4,PE3, PE2, PE1
28	PWD_1[3:0],PWD0[3:0]

Read Byte	Register
29	PWD_3[3:0],PWD2[3:0]
30	4'b0,PWD4[3:0]
31	CD
32	AT[3:0]
33	PR[3:0]
34	PC[1:0]
35	ZB
36	COM_W[7:0]
37	COM_W[8]
38	COM_N[7:0]
39	DR[7:0]
40	DC[7:0]
41	D1,D0
42	Black[2:0],Blank[4:0]
43	DS
44	TM
45	TD[7:0]
46	TEST_RGB[7:0]
47	CO
48	1'b0,BR1[2:0],1'b0,BR0[2:0]
:	1'b0,BR3[2:0],1'b0,BR2[2:0]
94	:
95	1'b0,BR95[2:0],1'b0,BR94[2:0]
96	Green_LEVEL1[7:0]
:	Green_LEVEL2[7:0]
156	:
157	Green_LEVEL62[7:0]
158	Green_LEVEL63[7:0]
159	Blue_LEVEL1[7:0]
:	Blue_LEVEL2[7:0]
219	:
220	Blue_LEVEL62[7:0]
221	Blue_LEVEL63[7:0]
222	Red_LEVEL1[7:0]
:	Red_LEVEL2[7:0]
282	:
283	Red_LEVEL62[7:0]
284	Red_LEVEL63[7:0]

6.47 READ SCAN COM ORDER

Byte information		RD#	WR#	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
Read Scan	1st	1	0	0	1	1	0	0	1	1	1	1	
Com Order	2nd	0	1	1	Read Data								

This command is reading scan com order number. The read data is 0~95, when color mode (COM_N=31) or mono mode (COM_N=95).



7. ABSOLUTE MAXIMUM RATING

(Unless otherwise stated, Ta=25℃)

Parameter	Symbol	Min.	Max.	Unit
Supply voltage	V_{HA}	-0.3	+24	V
Supply voltage	V_{DD}	-0.3	+6.0	V
I/O pin voltage	V_X	-0.3	V_{DD}+0.3	V
Junction temperature	Tj	-40	+85	℃
Storage temperature	Tstg	-40	+150	℃
Electrostatic discharge	V_{ESD}	See note 2	-2000 ~ +2000	V
		See note 3	-200 ~ + 200	
		See note 4	100	mA

Notes:

1. Voltage or temperature beyond the maximum ratings might cause damages to the device. Functional operation should be restricted within the limits
   the Electrical Characteristics tables and Pin Description. Unless further specified, Voltage Referenced to V_{SS}, V_{DD}=3 to 3.6V, T_A=25℃)
2. Human Body Model: According to the standard of EIA/JESD22-A114-B
3. Machine Model: According to the standard of EIA/JESD22-A115-A
4. According to the standard of EIA/JESD78

8. DC CHARACTERISTICS

(Unless further specified, Voltage Referenced to V_{SS}, V_{DD}=1.65 to 3.6V, Tj= -40~85 ℃)

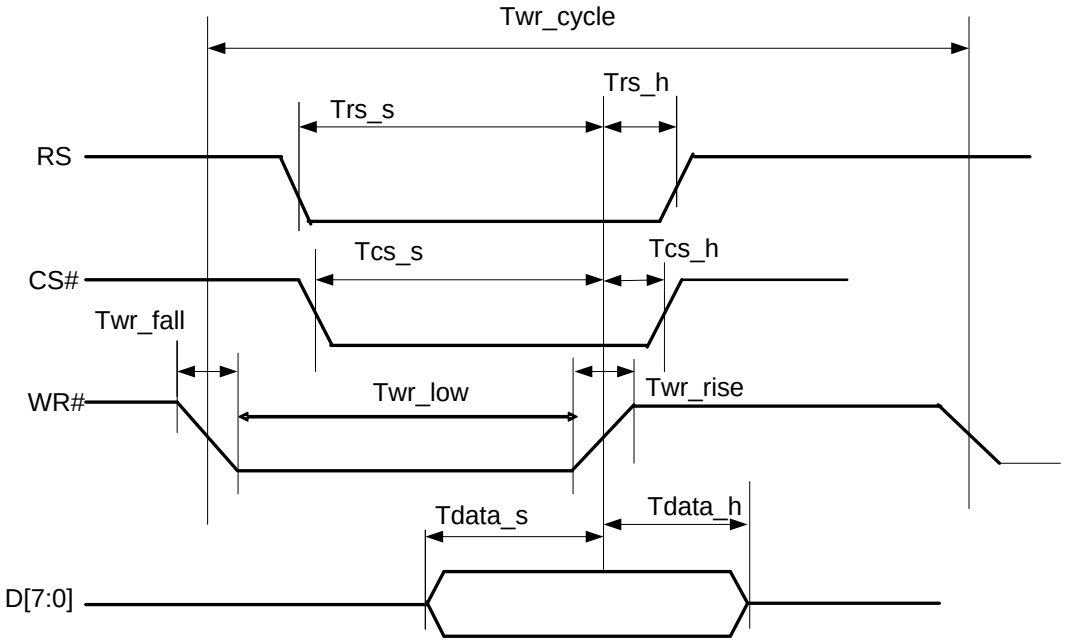
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating voltage	V_{HA}		8	-	18	V
Logic supply voltage	V_{DD}		1.65	3.3	3.6	V
HIGH logic output level	V_{OH}	Iout=-1mA, (see note 1)	0.9xV_{DD}	-	-	V
LOW logic output level	V_{OL}	Iout=1mA, (see note 1)	-	-	0.1xV_{DD}	V
HIGH logic input level	V_{IH}	(see note 2)	0.8xV_{DD}	-	V_{DD}	V
LOW logic input level	V_{IL}	(see note 2)	0	-	0.2xV_{DD}	V
Input leakage current of logic input (@3.3V)	I_{IH}	(see note 3)	-	-	1	μA
Input leakage current of logic input (@0V)	I_{IL}	(see note 3)	-	-	1	μA
Input leakage current of logic input (@3.3V)	I_{IH_PD}	TEST_EN, TSCAN_EN, LDO_DIS	-	-	50	μA
Regulator output voltage	V_{RO}	V_{DD}=2.4~3.6V , Force VRO, I_L=-5mA (current loading)	1.65	1.8	2.22	V
V18 Input voltage	V18	VRO to V18 no connect. Force V18, check Logical function	1.62	1.8	2.22	V
Oscillation frequency	F_{OSC}	V_{18}=1.8V; VDD=3.3V, test mode, Tj=25℃ F_{OSC} = F_{INT} x 2 measure “INT”	2.7	3.0	3.3	MHz
VHA-Standby current (DAC disable, LDO enable)	$I_{HA0\_LDO-STBY}$	VDD=3.3V, VHA=14V, VHC= 14V; HV-DAC off (CE =0) V18= LV-LDO; LDO_DIS=0V CKSEL=3.3V, CLK_EXT=0V; No Loading; At standby mode and Tj=25℃,measure VHA	-	1	5	μA
VHA-Standby current (DAC, LDO enable)	$I_{HA1\_LDO-STBY}$	VDD=3.3V, VHA=14V, VHC= HV-DAC; HV-DAC on (CE =1) V18= LV-LDO; LDO_DIS=0V CKSEL=3.3V, CLK_EXT=0V; No Loading; At standby mode and Tj=25℃,measure VHA	-	-	70	μA
VDD-Standby current (DAC, LDO enable)	$I_{DD\_LDO-STBY}$	VDD=3.3V, VHA=14V, VHC= HV-DAC; HV-DAC on (CE =1) , DAC = 5h V18= LV-LDO; LDO_DIS=0V CKSEL=3.3V, CLK_EXT=0V; No Loading; At standby mode and Tj=25℃,measure VDD	-	34	60	uA
VDD-Standby current (LDO disable)	$I_{DD\_LDODIS-STBY}$	VDD=1.8V, VHA=14V, V18= 1.8V; LDO_DIS=pull-hi(MCU) CKSEL=1.8V, CLK_EXT=0V; No Loading; At standby mode and Tj=25℃,measure VDD	-	-	3	uA
V18-Standby current (LDO disable)	$I_{18\_LDODIS-STBY}$	VDD=1.8V; VHA=14V, V18= 1.8V; LDO_DIS=pull-hi(MCU) CKSEL=1.8V, CLK_EXT=0V; No Loading; At standby mode and Tj=25℃,measure V18	-	-	12	uA

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
VHA-Operating current	IHA	VDD=3.3V, V18=1.8V, VHA=14V, VHC=14V DISPLAY ON/OFF (B1=1,B0=0) Maximum Brightness, No Loading		-	-	560	μA
VHA-Operating current (HV-DAC enable)	IHA1	VDD=3.3V, V18=1.8V, VHA=14V, CE=1 DISPLAY ON/OFF (B1=1,B0=0) Maximum Brightness, No Loading		-	-	850	μA
VDD-Operating current (VRO to V18 is no connecting)	IDD	VDD=3.3V, V18=1.8V, VHA=14V; No Loading		-	28	38	μA
V18-Operating current (VRO to V18 is no connecting)	I18	VDD =3.3V, V18=1.8V, VHA =14V ; No Loading		-	1.5	2	mA
Segment current	I_{SEG1}	V_{DD}=3.3V V_{HA}=14V, Vo=11V Tj= 25 ℃	BR[6:0]=7Fh	-	250	300	μA
			BR[6:0]=3Fh	-	-	-	
			BR[6:0]=2Fh	-	-	-	
			BR[6:0]=1Fh	-	-	-	
			BR[6:0]=0Fh	-	-	-	
			BR[6:0]=00h	-	-	-	
Pre_charge current	I_{PRE}	V_{DD}=3.3V, V_{HA}=14V,Vo=11V PC=0, BR[6:0]=7Fh, PC[1:0]=11 Measure SEG0, SEG1, SEG126,SEG127		-	-	-	μA
Segment current uniformity	Dev	V_{HA}=14V, Vo=11V BR[6:0]=7Fh Measure SEG[0:127], I_{MAX}=Max(I_{SEG}[0:127]) I_{MIN} =Min(I_{SEG}[0:127]) I_{AVG}=AVG(I_{SEG}[0:127]) Dev=(I_{MAX}-I_{MIN})/I_{AVG}		-	-	5	%
Adjacent pin output current uniformity	Adj_{DEV}	V_{HA}=14V, Vo=11V BR[6:0]=7Fh Measure SEG[0:127] SEG_EVEN[0:63]=SEG[0], SEG[2], …,SEG[126] SEG_ODD[0:63]=SEG[1], SEG[3], …,SEG[127] Adj_{DEV_EVEN}=Abs($I_{SEG\_EVEN[n]}$-$I_{SEG\_EVEN\ [n+1]}$) / [($I_{SEG\_EVEN\ [n]}$+$I_{SEG\_EVEN\ [n+1]}$)/2] Adj_{DEV_ODD}=Abs($I_{SEG\_ODD\ [n]}$-$I_{SEG\_ODD\ [n+1]}$) / [($I_{SEG\_ODD[n]}$+$I_{SEG\_ODD\ [n+1]}$)/2]		-	-	2	%
Segment current variation dependence with Vo	I_{VAR}	V_{HA}=14V, BR[6:0]=7Fh force SEG, Vo=(6V~11V)		-	-	0.4	%/V
Segment low-level output voltage	V_{OSL}	V_{HA}=16V, Force Iout= 1mA		-	-	0.5	V
Common low-level sink voltage	V_{COML}	VHA=16V, Force Iout= 30mA, Tj=25 ℃		-	1.05	1.8	V

Notes:
1. Application to the following pins: INT, D0~D7
2. Application to the following pins: CLK_EXT, CKSEL, BS[1:0], WR#, RD#, CS#, RS, D0~D7, RES#, LDO_DIS, TEST_EN, TSCAN_EN,
3. Application to the following pins: CLK_EXT, BS[1:0], WR#, RD#, CS#, RS, D0~D7, RES#

9.AC CHARACTERISTICS

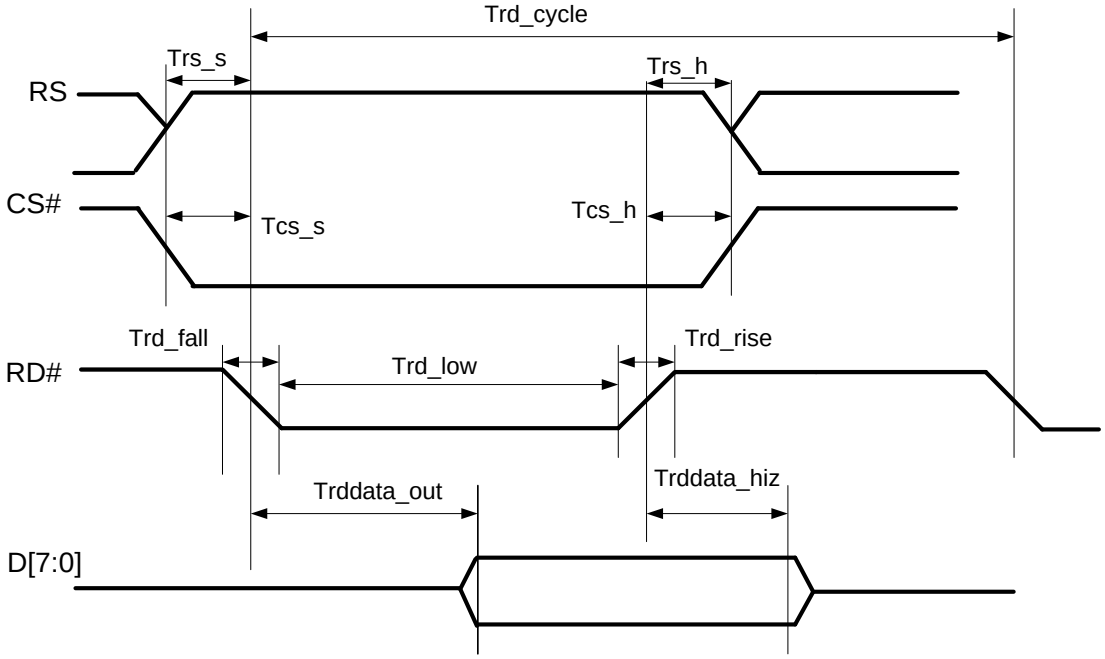
9.1 WRITE CHARACTERISTICS FOR THE 8080 SERIES MPU



(Unless further specified, Voltage Referenced to V_{SS}, V_{DD}=1.65 to 3.6V, Tj= -40~85 ℃)

Item	Description	Min.	Typ.	Max.	Units
Twr_cycle	-	500	-	-	ns
Twr_rise / Twr_fall	-	-	-	15/15	ns
Twr_low	-	100	-	-	ns
Trs_s / Trs_h	RS setup & hold time	100/5	-	-	ns
Tcs_s / Tcs_h	CS# setup & hold time	100/0	-	-	ns
Tdata_s / Tdata_h	Data setup & hold time	100/5	-	-	ns

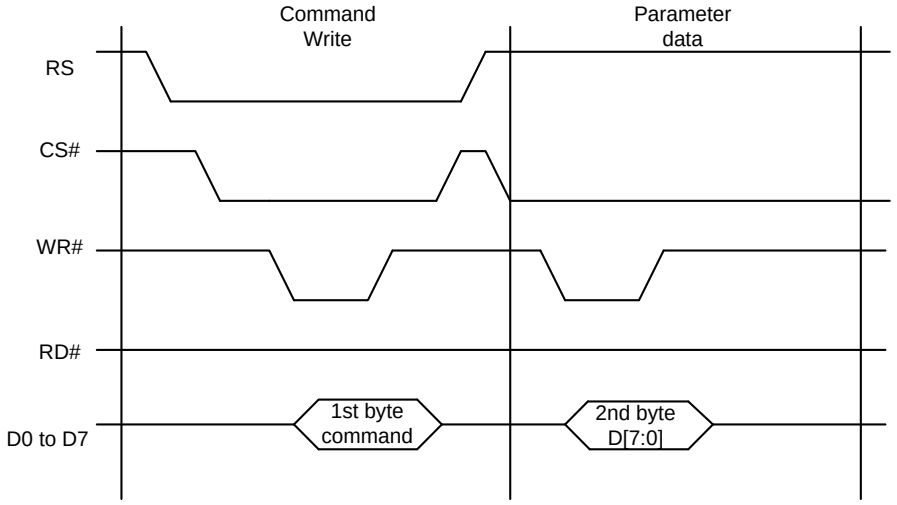
9.2 READ CHARACTERISTICS FOR THE 8080 SERIES MPU



(Unless further specified, Voltage Referenced to V_{SS}, V_{DD}=1.65 to 3.6V, Tj= -40~85 ℃)

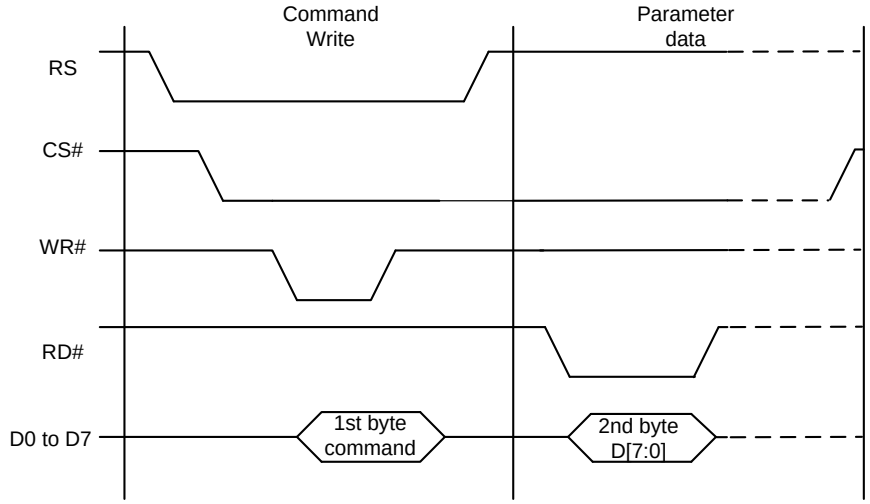
Item	Description	Min.	Typ.	Max.	Units
Trd_cycle	-	500	-	-	ns
Trd_rise / Trd_fall	-	-	-	15/15	ns
Trd_low	-	230	-	-	ns
Trs_s / Trs_h	RS setup & hold time	100/5	-	-	ns
Tcs_s / Tcs_h	CS# setup & hold time	100/0	-	-	ns
Trddata_out	Data out from RD# falling edge	-	-	220	ns
Trddata_hiz	Data Hiz from RD# rising edge	3	-	100	ns

9.3 WRITE COMMAND TIMING WHEN RS=0, PARAMETER/WRITE DATA TIMING WHEN RS=1 FOR THE 8080 SERIES MPU



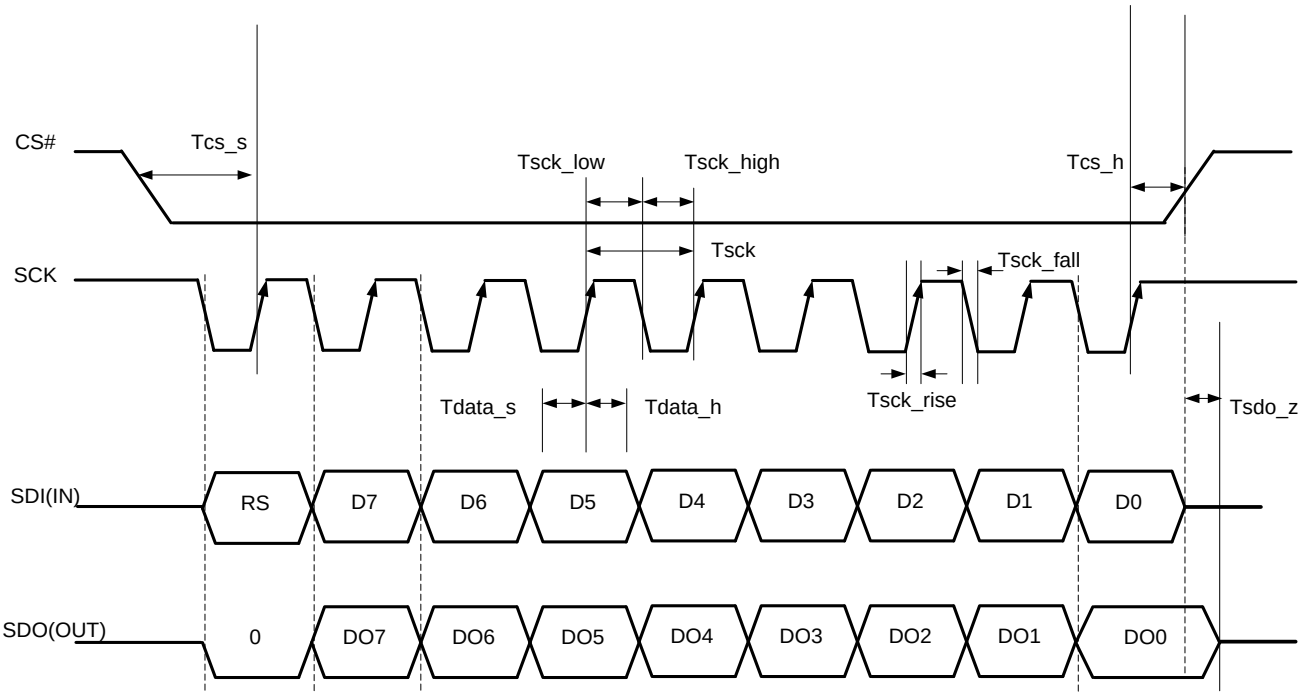
Note: D[7:0]: to access data by MCU Bus Mode.

9.4 READ COMMAND TIMING WHEN RS=0, READ DATA TIMING WHEN RS=1 FOR THE 8080 SERIES MPU



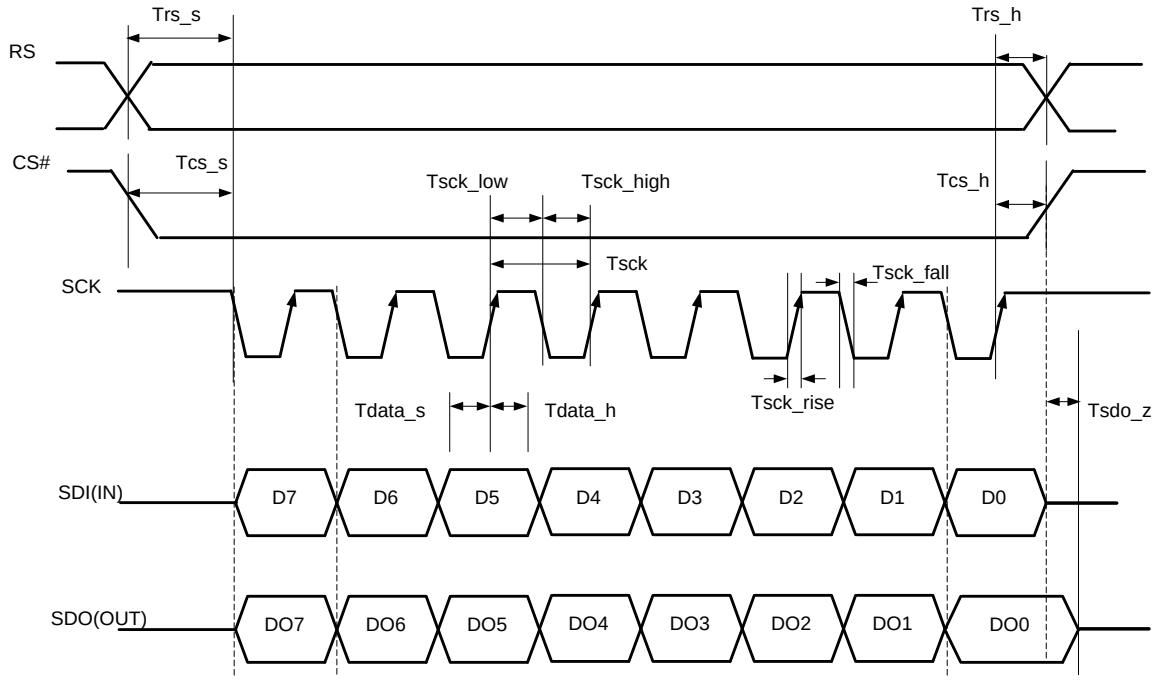
Note: D[7:0]: to access data by MCU Bus Mode.

9.5 SERIAL PERIPHERAL INTERFACE (SPI-3WIRE) CHARACTERISTICS

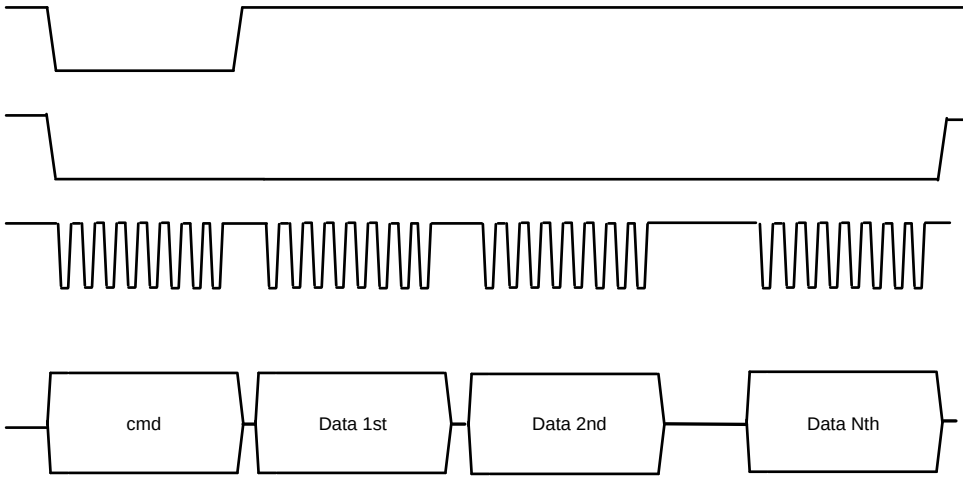


RS=0, D7~D0 should be treated as a command. RS=1, D7~D0 should be treated as data.

9.6 SERIAL PERIPHERAL INTERFACE (SPI-4WIRE) CHARACTERISTICS

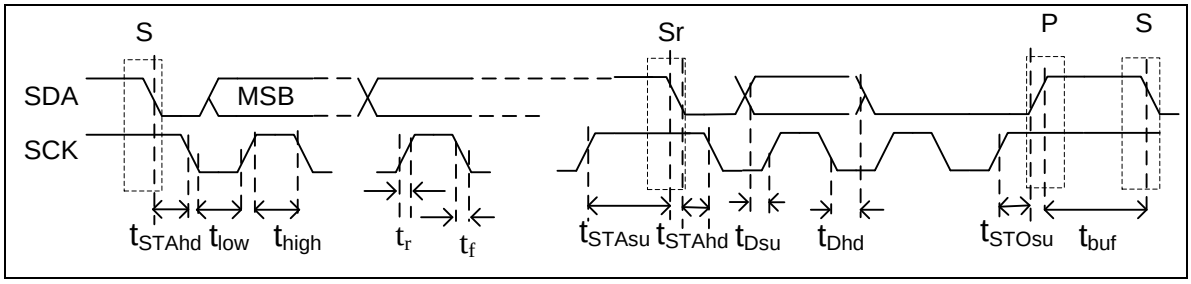


9.7 SERIAL PERIPHERAL INTERFACE



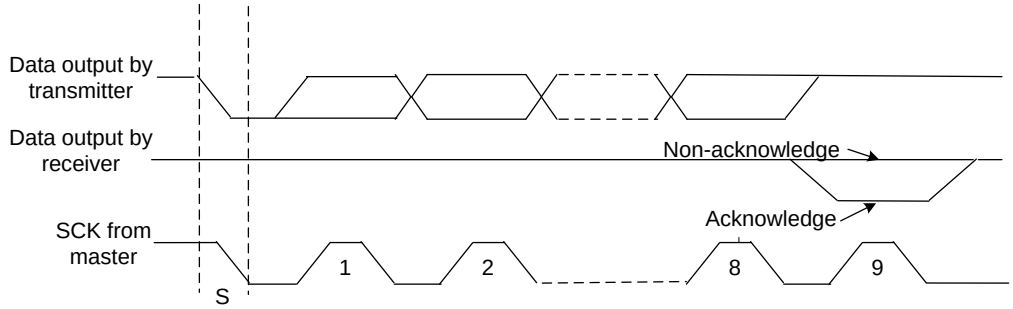
Item	Description	Min.	Typ.	Max.	Units
Tsck	Clock cycle time	40	50	-	ns
Trs_s / Trs_h	RS setup & hold time	20/20	-	-	ns
Tcs_s / Tcs_h	CS# setup & hold time	20/20	-	-	ns
Tdata_s / Tdata_h	Data setup & hold time	20/20	-	-	ns
Tsck_low / Tsck_high	-	20/20	-	-	ns
Tsck_rsie / Tsck_fall	-	-	-	15/15	ns
Tsdo_z	SDO output hi-Z	-	-	20	ns

9.8 I²C WAVEFORM

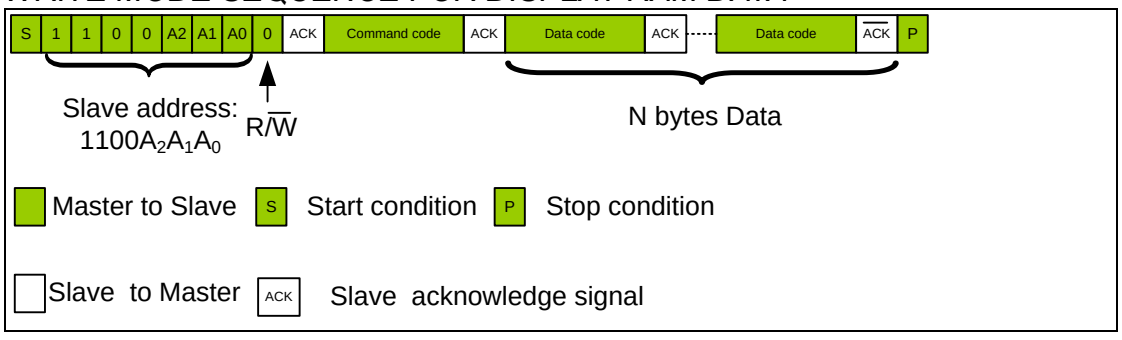


Item	Description	Min.	Typ.	Max.	Units
t_{SCL}	Clock cycle time	2.5	-	-	us
t_{low}	High pulse width for SCK	0.6			us
t_{high}	Low pulse width for SCK	0.6			us
t_{STAhd}	Start condition Hold Time	0.6	-	-	us
t_{Dhd}	Data Hold Time (for t_{HD} "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300			ns
t_{Dsu}	Data Setup Time	100	-	-	ns
t_{STAsu}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{STOsu}	Stop condition Setup Time	0.6	-	-	us
t_r / t_f	Rise/fall Time for data and clock pin	-	-	40/40	ns
tbuf	Idle Time before a new transmission can start	1.3			us

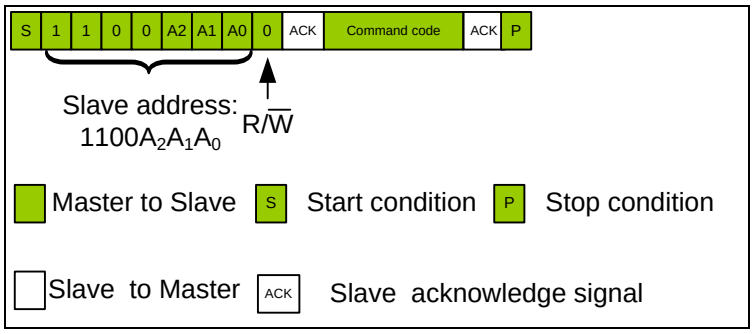
DEFINITION OF THE ACKNOWLEDGEMENT CONDITION



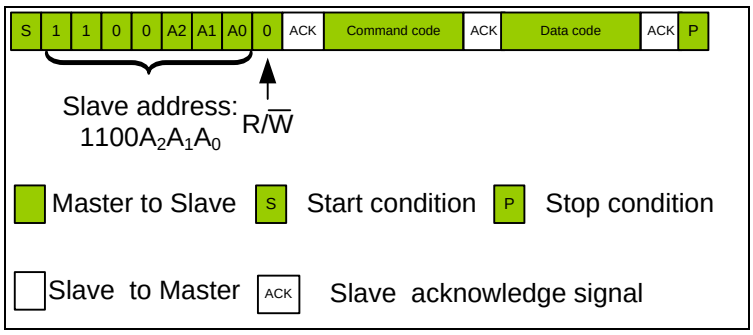
WRITE MODE SEQUENCE FOR DISPLAY RAM DATA



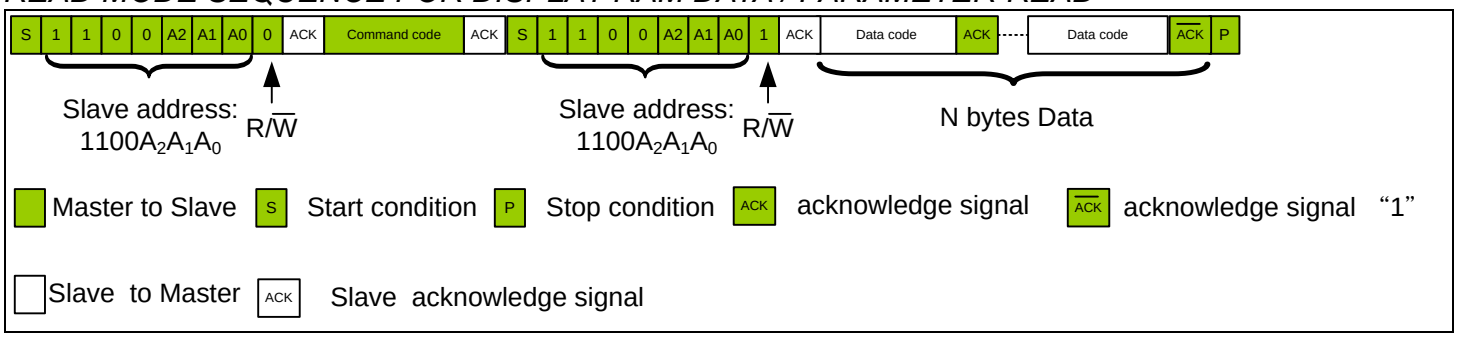
WRITE MODE ONE BYTE COMMAND



WRITE MODE TWO BYTE COMMAND

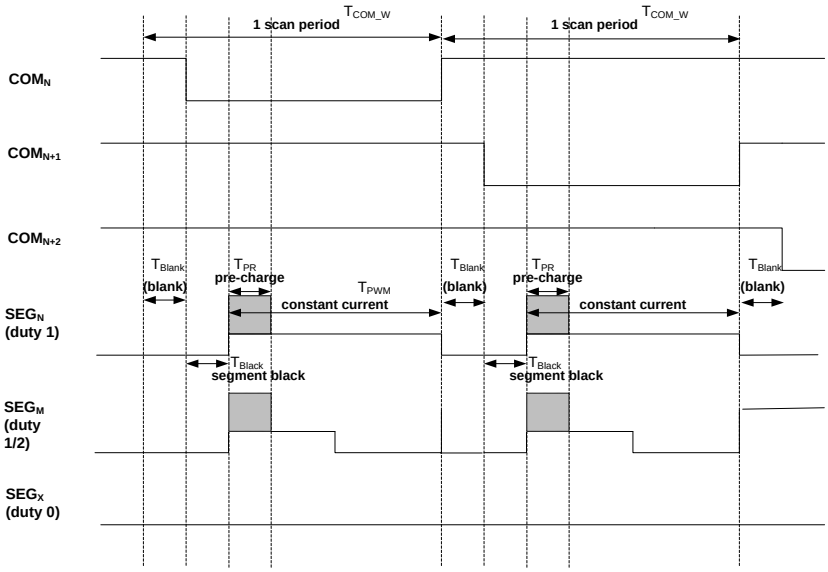


READ MODE SEQUENCE FOR DISPLAY RAM DATA / PARAMETER-READ

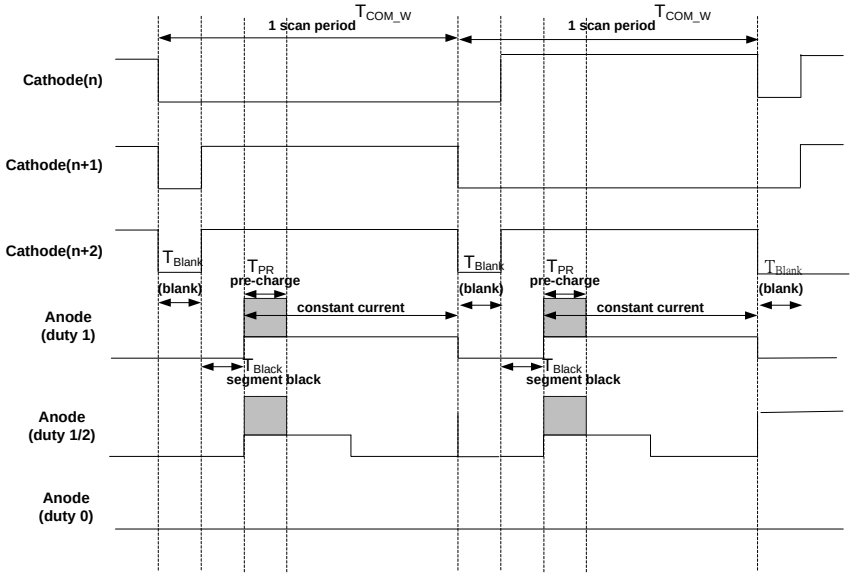


9.9 SEG / COM WAVEFORM

H-OVERLAP WAVEFORM

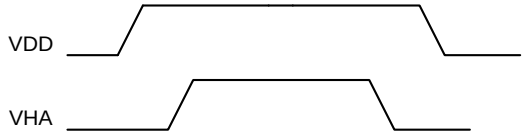


L-OVERLAP WAVEFORM

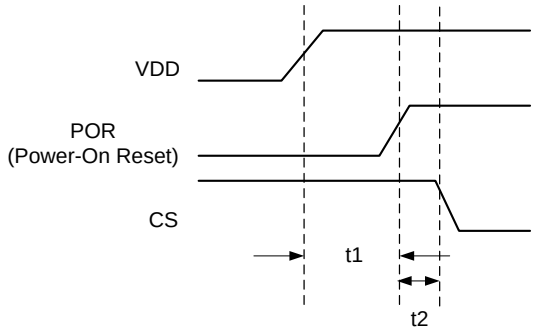


Item	Description	Min.	Typ.	Max.	Units
T_{COM_W}	One COM Pulse Period	64	-	575	PWMCLK
T_{Blank}	Blank Period	4		31	PWMCLK X 4
T_{Black}	Black Period	0		7	PWMCLK X 4
T_{PR}	Pre-Charge Period	0	-	15	PWMCLK X 4
T_{PWM}	PWM Active Period for Gamma Table	1	-	256	PWMCLK
T_{FRAME}(color mode)	COM Number by One Color Frame	1	-	43	T_{COM_W} X 3
T_{FRAME}(Mono mode)	COM Number by One Mono Frame	1	-	96	T_{COM_W}
$T_{FRAME+DUMMY}$	One Frame with Dummy Scan	$T_{FRAME} + T_{COM\_W}$			

9.10 VDD AND VHA POWER SEQUENCE TIMING



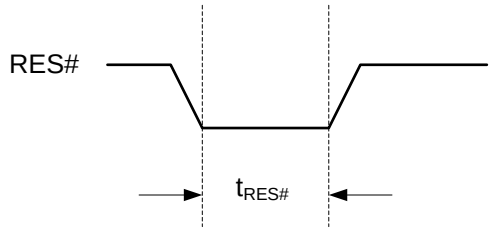
9.11 POWER-ON AND RESET TIMING



Item	Unit (µs)
t1	600
t2	100

9.12 MINIMUM LOW-ACTIVE PULSE WIDTH REQUIRED FOR RES# PIN

Minimum Pulse Width for RES# Pin	Min.	Description
$t_{RES\#}$	T_{OSC} * 40	$t_{RES\#}$ ➔ Valid RES# signal



Note: In standby mode, low of RES# cannot reset the chip.

9.13 STANDBY ABOUT DISABLE-MODE ON ANALOG BLOCKS

Description	LDO_DIS pin	Standby command	OSC	POR	VRO	BIAS	HV DAC	Condition
Normal 1 (VRO ON)	GND	Disabled	ON	ON	ON	ON	ON	VDD =2.4~3.6V V18 = VRO
Standby 1 (VRO ON)	GND	Enabled	OFF	ON	ON	OFF	OFF	VDD =2.4~3.6V V18 = VRO
Normal 2 (VRO OFF)	VDD	Disabled	ON	ON	OFF	ON	ON	VDD =1.65~3.6V V18 = 1.65~1.98V
Standby 2 (VRO OFF)	VDD	Enabled	OFF	ON	OFF	OFF	OFF	VDD=1.65~3.6V V18 = 1.65~1.98V

Note: “VRO” shows 1.8V regulator output

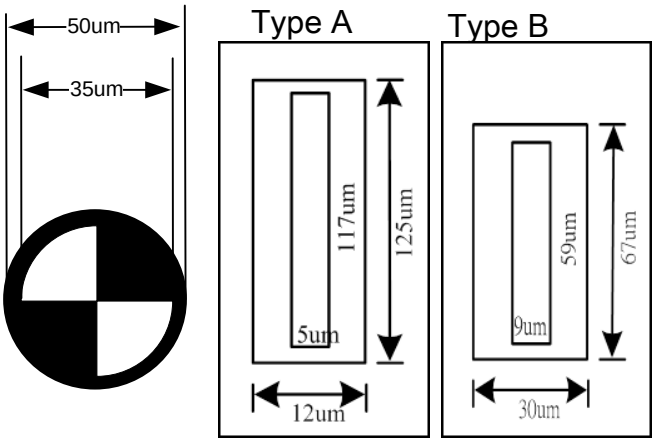
10. PAD CONFIGURATION

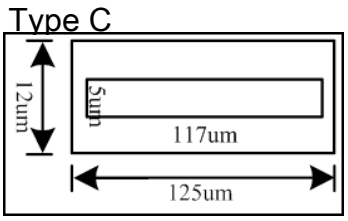
Die size: 7015.5 μm x 1161 μm (excluding scribe line width: 80um)

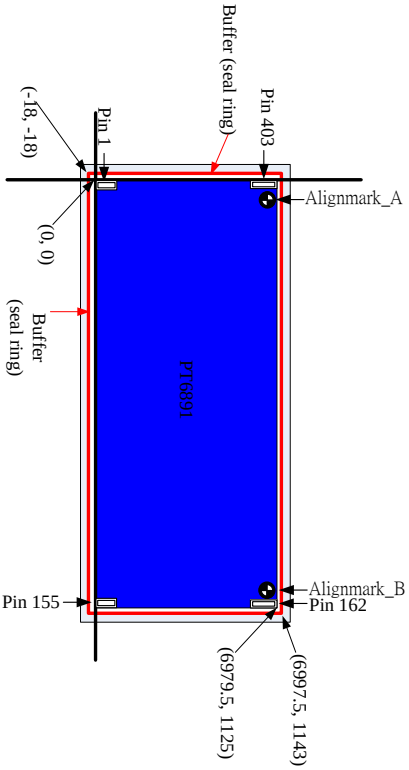
Chip thickness: 250 ±15 μm

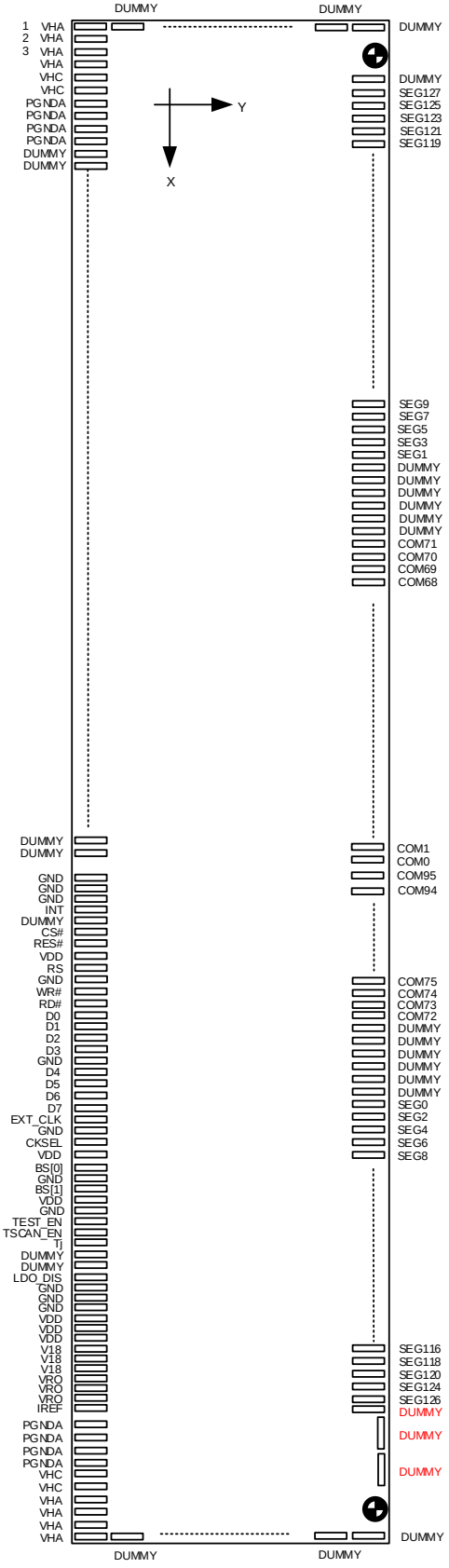
Bump height = 9 ± 3 μm ; Bump hardness = 65 ± 15

Alignment Size:









11. PAD LOCATION

No.	Side	Name	Location		Bump Type
			X[μm]	X[μm]	
1	***Bottom***	VHA	18	36.9	TYPE B
2		VHA	63	36.9	TYPE B
3		VHA	108	36.9	TYPE B
4		VHA	153	36.9	TYPE B
5		VHC	198	36.9	TYPE B
6		VHC	243	36.9	TYPE B
7		PGNDA	288	36.9	TYPE B
8		PGNDA	333	36.9	TYPE B
9		PGNDA	378	36.9	TYPE B
10		PGNDA	423	36.9	TYPE B
11		DUMMY	468	36.9	TYPE B
12		DUMMY	513	36.9	TYPE B
13		DUMMY	558	36.9	TYPE B
14		DUMMY	603	36.9	TYPE B
15		DUMMY	648	36.9	TYPE B
16		DUMMY	693	36.9	TYPE B
17		DUMMY	738	36.9	TYPE B
18		DUMMY	783	36.9	TYPE B
19		DUMMY	828	36.9	TYPE B
20		DUMMY	873	36.9	TYPE B
21		DUMMY	918	36.9	TYPE B
22		DUMMY	963	36.9	TYPE B
23		DUMMY	1008	36.9	TYPE B
24		DUMMY	1053	36.9	TYPE B
25		DUMMY	1098	36.9	TYPE B
26		DUMMY	1143	36.9	TYPE B
27		DUMMY	1188	36.9	TYPE B
28		DUMMY	1233	36.9	TYPE B
29		DUMMY	1278	36.9	TYPE B
30		DUMMY	1323	36.9	TYPE B
31		DUMMY	1368	36.9	TYPE B
32		DUMMY	1413	36.9	TYPE B
33		DUMMY	1458	36.9	TYPE B
34		DUMMY	1503	36.9	TYPE B
35		DUMMY	1548	36.9	TYPE B
36		DUMMY	1593	36.9	TYPE B
37		DUMMY	1638	36.9	TYPE B
38		DUMMY	1683	36.9	TYPE B
39		DUMMY	1728	36.9	TYPE B
40		DUMMY	1773	36.9	TYPE B
41		DUMMY	1818	36.9	TYPE B
42		DUMMY	1863	36.9	TYPE B
43		DUMMY	1908	36.9	TYPE B
44		DUMMY	1953	36.9	TYPE B
45		DUMMY	1998	36.9	TYPE B
46		DUMMY	2043	36.9	TYPE B
47		DUMMY	2088	36.9	TYPE B
48		DUMMY	2133	36.9	TYPE B

No.	Side	Name	Location		Bump Type
			X[μm]	X[μm]	
49		DUMMY	2178	36.9	TYPE B
50		DUMMY	2223	36.9	TYPE B
51		DUMMY	2268	36.9	TYPE B
52		DUMMY	2313	36.9	TYPE B
53		DUMMY	2358	36.9	TYPE B
54		DUMMY	2403	36.9	TYPE B
55		DUMMY	2448	36.9	TYPE B
56		DUMMY	2493	36.9	TYPE B
57		DUMMY	2538	36.9	TYPE B
58		DUMMY	2583	36.9	TYPE B
59		DUMMY	2628	36.9	TYPE B
60		DUMMY	2673	36.9	TYPE B
61		DUMMY	2718	36.9	TYPE B
62		DUMMY	2763	36.9	TYPE B
63		DUMMY	2808	36.9	TYPE B
64		DUMMY	2853	36.9	TYPE B
65		DUMMY	2898	36.9	TYPE B
66		DUMMY	2943	36.9	TYPE B
67		DUMMY	2988	36.9	TYPE B
68		DUMMY	3033	36.9	TYPE B
69		DUMMY	3078	36.9	TYPE B
70		DUMMY	3123	36.9	TYPE B
71		DUMMY	3168	36.9	TYPE B
72		DUMMY	3213	36.9	TYPE B
73		DUMMY	3258	36.9	TYPE B
74		DUMMY	3303	36.9	TYPE B
75		DUMMY	3348	36.9	TYPE B
76		DUMMY	3393	36.9	TYPE B
77		DUMMY	3438	36.9	TYPE B
78		DUMMY	3483	36.9	TYPE B
79		DUMMY	3528	36.9	TYPE B
80		DUMMY	3573	36.9	TYPE B
81		DUMMY	3618	36.9	TYPE B
82		DUMMY	3663	36.9	TYPE B
83		DUMMY	3708	36.9	TYPE B
84		DUMMY	3753	36.9	TYPE B
85		DUMMY	3798	36.9	TYPE B
86		DUMMY	3843	36.9	TYPE B
87		DUMMY	3888	36.9	TYPE B
88		DUMMY	3933	36.9	TYPE B
89		DUMMY	3978	36.9	TYPE B
90		DUMMY	4023	36.9	TYPE B
91		DUMMY	4068	36.9	TYPE B
92		DUMMY	4113	36.9	TYPE B
93		DUMMY	4158	36.9	TYPE B
94		DUMMY	4203	36.9	TYPE B
95		DUMMY	4248	36.9	TYPE B
96		DUMMY	4293	36.9	TYPE B
97		GND	4338	36.9	TYPE B
98		GND	4383	36.9	TYPE B
99		GND	4428	36.9	TYPE B

No.	Side	Name	Location		Bump Type
			X[μm]	X[μm]	
100		INT	4486.5	36.9	TYPE B
101		DUMMY	4531.5	36.9	TYPE B
102		CS#	4576.5	36.9	TYPE B
103		RES#	4621.5	36.9	TYPE B
104		VDD	4666.5	36.9	TYPE B
105		RS	4711.5	36.9	TYPE B
106		GND	4756.5	36.9	TYPE B
107		WR#	4801.5	36.9	TYPE B
108		RD#	4846.5	36.9	TYPE B
109		D[0]	4891.5	36.9	TYPE B
110		D[1]	4936.5	36.9	TYPE B
111		D[2]	4981.5	36.9	TYPE B
112		D[3]	5026.5	36.9	TYPE B
113		GND	5071.5	36.9	TYPE B
114		D[4]	5116.5	36.9	TYPE B
115		D[5]	5161.5	36.9	TYPE B
116		D[6]	5206.5	36.9	TYPE B
117		D[7]	5251.5	36.9	TYPE B
118		EXT_CLK	5296.5	36.9	TYPE B
119		GND	5341.5	36.9	TYPE B
120		CKSEL	5386.5	36.9	TYPE B
121		VDD	5431.5	36.9	TYPE B
122		BS[0]	5476.5	36.9	TYPE B
123		GND	5521.5	36.9	TYPE B
124		BS[1]	5566.5	36.9	TYPE B
125		VDD	5611.5	36.9	TYPE B
126		GND	5656.5	36.9	TYPE B
127		TEST_EN	5701.5	36.9	TYPE B
128		TSCAN_EN	5746.5	36.9	TYPE B
129		TJ	5791.5	36.9	TYPE B
130		DUMMY	5836.5	36.9	TYPE B
131		DUMMY	5881.5	36.9	TYPE B
132		LDO_DIS	5926.5	36.9	TYPE B
133		GND	5971.5	36.9	TYPE B
134		GND	6016.5	36.9	TYPE B
135		GND	6061.5	36.9	TYPE B
136		VDD	6106.5	36.9	TYPE B
137		VDD	6151.5	36.9	TYPE B
138		VDD	6196.5	36.9	TYPE B
139		V18	6241.5	36.9	TYPE B
140		V18	6286.5	36.9	TYPE B
141		V18	6331.5	36.9	TYPE B
142		VRO	6376.5	36.9	TYPE B
143		VRO	6421.5	36.9	TYPE B
144		VRO	6466.5	36.9	TYPE B
145		I_{REF}	6511.5	36.9	TYPE B
146		PGNDA	6556.5	36.9	TYPE B
147		PGNDA	6601.5	36.9	TYPE B
148		PGNDA	6646.5	36.9	TYPE B
149		PGNDA	6691.5	36.9	TYPE B

No.	Side	Name	Location		Bump Type
			X[μm]	X[μm]	
150		VHC	6736.5	36.9	TYPE B
151		VHC	6781.5	36.9	TYPE B
152		VHA	6826.5	36.9	TYPE B
153		VHA	6871.5	36.9	TYPE B
154		VHA	6916.5	36.9	TYPE B
155		VHA	6961.5	36.9	TYPE B
156	Right	DUMMY	6970.5	216.9	TYPE A
157		DUMMY	6970.5	357.3	TYPE A
158		DUMMY	6970.5	497.7	TYPE A
159		DUMMY	6970.5	638.1	TYPE A
160		DUMMY	6970.5	778.5	TYPE A
161		DUMMY	6970.5	918.9	TYPE A
162	Top	DUMMY	6970.5	1059.3	TYPE A
		Alignmark_B	6896.7	1099.8	
163		DUMMY	6784.2	1116	TYPE C
164		DUMMY	6643.8	1116	TYPE C
165		DUMMY	6547.5	1059.3	TYPE A
166		SEG[126]	6520.5	1059.3	TYPE A
167		SEG[124]	6493.5	1059.3	TYPE A
168		SEG[122]	6466.5	1059.3	TYPE A
169		SEG[120]	6439.5	1059.3	TYPE A
170		SEG[118]	6412.5	1059.3	TYPE A
171		SEG[116]	6385.5	1059.3	TYPE A
172		SEG[114]	6358.5	1059.3	TYPE A
173		SEG[112]	6331.5	1059.3	TYPE A
174		SEG[110]	6304.5	1059.3	TYPE A
175		SEG[108]	6277.5	1059.3	TYPE A
176		SEG[106]	6250.5	1059.3	TYPE A
177		SEG[104]	6223.5	1059.3	TYPE A
178		SEG[102]	6196.5	1059.3	TYPE A
179		SEG[100]	6169.5	1059.3	TYPE A
180		SEG[98]	6142.5	1059.3	TYPE A
181		SEG[96]	6115.5	1059.3	TYPE A
182		SEG[94]	6088.5	1059.3	TYPE A
183		SEG[92]	6061.5	1059.3	TYPE A
184		SEG[90]	6034.5	1059.3	TYPE A
185		SEG[88]	6007.5	1059.3	TYPE A
186		SEG[86]	5980.5	1059.3	TYPE A
187		SEG[84]	5953.5	1059.3	TYPE A
188		SEG[82]	5926.5	1059.3	TYPE A
189		SEG[80]	5899.5	1059.3	TYPE A
190		SEG[78]	5872.5	1059.3	TYPE A
191		SEG[76]	5845.5	1059.3	TYPE A
192		SEG[74]	5818.5	1059.3	TYPE A
193		SEG[72]	5791.5	1059.3	TYPE A
194		SEG[70]	5764.5	1059.3	TYPE A
195		SEG[68]	5737.5	1059.3	TYPE A
196		SEG[66]	5710.5	1059.3	TYPE A
197		SEG[64]	5683.5	1059.3	TYPE A
198		SEG[62]	5656.5	1059.3	TYPE A
199		SEG[60]	5629.5	1059.3	TYPE A

No.	Side	Name	Location		Bump Type
			X[μm]	X[μm]	
200		SEG[58]	5602.5	1059.3	TYPE A
201		SEG[56]	5575.5	1059.3	TYPE A
202		SEG[54]	5548.5	1059.3	TYPE A
203		SEG[52]	5521.5	1059.3	TYPE A
204		SEG[50]	5494.5	1059.3	TYPE A
205		SEG[48]	5467.5	1059.3	TYPE A
206		SEG[46]	5440.5	1059.3	TYPE A
207		SEG[44]	5413.5	1059.3	TYPE A
208		SEG[42]	5386.5	1059.3	TYPE A
209		SEG[40]	5359.5	1059.3	TYPE A
210		SEG[38]	5332.5	1059.3	TYPE A
211		SEG[36]	5305.5	1059.3	TYPE A
212		SEG[34]	5278.5	1059.3	TYPE A
213		SEG[32]	5251.5	1059.3	TYPE A
214		SEG[30]	5224.5	1059.3	TYPE A
215		SEG[28]	5197.5	1059.3	TYPE A
216		SEG[26]	5170.5	1059.3	TYPE A
217		SEG[24]	5143.5	1059.3	TYPE A
218		SEG[22]	5116.5	1059.3	TYPE A
219		SEG[20]	5089.5	1059.3	TYPE A
220		SEG[18]	5062.5	1059.3	TYPE A
221		SEG[16]	5035.5	1059.3	TYPE A
222		SEG[14]	5008.5	1059.3	TYPE A
223		SEG[12]	4981.5	1059.3	TYPE A
224		SEG[10]	4954.5	1059.3	TYPE A
225		SEG[8]	4927.5	1059.3	TYPE A
226		SEG[6]	4900.5	1059.3	TYPE A
227		SEG[4]	4873.5	10 59.3	TYPE A
228		SEG[2]	4846.5	1059.3	TYPE A
229		SEG[0]	4819.5	1059.3	TYPE A
230		DUMMY	4792.5	1059.3	TYPE A
231		DUMMY	4765.5	1059.3	TYPE A
232		DUMMY	4738.5	1059.3	TYPE A
233		DUMMY	4711.5	1059.3	TYPE A
234		DUMMY	4684.5	1059.3	TYPE A
235		DUMMY	4657.5	1059.3	TYPE A
236		COM[72]	4630.5	1059.3	TYPE A
237		COM[73]	4603.5	1059.3	TYPE A
238		COM[74]	4576.5	1059.3	TYPE A
239		COM[75]	4549.5	1059.3	TYPE A
240		COM[76]	4522.5	1059.3	TYPE A
241		COM[77]	4495.5	1059.3	TYPE A
242		COM[78]	4468.5	1059.3	TYPE A
243		COM[79]	4441.5	1059.3	TYPE A
244		COM[80]	4414.5	1059.3	TYPE A
245		COM[81]	4387.5	1059.3	TYPE A
246		COM[82]	4360.5	1059.3	TYPE A
247		COM[83]	4333.5	1059.3	TYPE A
248		COM[84]	4306.5	1059.3	TYPE A
249		COM[85]	4279.5	1059.3	TYPE A
250		COM[86]	4252.5	1059.3	TYPE A

No.	Side	Name	Location		Bump Type
			X[μm]	X[μm]	
251		COM[87]	4225.5	1059.3	TYPE A
252		COM[88]	4198.5	1059.3	TYPE A
253		COM[89]	4171.5	1059.3	TYPE A
254		COM[90]	4144.5	1059.3	TYPE A
255		COM[92]	4117.5	1059.3	TYPE A
256		COM[91]	4090.5	1059.3	TYPE A
257		COM[93]	4063.5	1059.3	TYPE A
258		COM[94]	4036.5	1059.3	TYPE A
259		COM[95]	4009.5	1059.3	TYPE A
260		COM[0]	3982.5	1059.3	TYPE A
261		COM[1]	3955.5	1059.3	TYPE A
262		COM[2]	3928.5	1059.3	TYPE A
263		COM[3]	3901.5	1059.3	TYPE A
264		COM[4]	3874.5	1059.3	TYPE A
265		COM[5]	3847.5	1059.3	TYPE A
266		COM[6]	3820.5	1059.3	TYPE A
267		COM[7]	3793.5	1059.3	TYPE A
268		COM[8]	3766.5	1059.3	TYPE A
269		COM[9]	3739.5	1059.3	TYPE A
270		COM[10]	3712.5	1059.3	TYPE A
271		COM[11]	3685.5	1059.3	TYPE A
272		COM[12]	3658.5	1059.3	TYPE A
273		COM[13]	3631.5	1059.3	TYPE A
274		COM[14]	3604.5	1059.3	TYPE A
275		COM[15]	3577.5	1059.3	TYPE A
276		COM[16]	3550.5	1059.3	TYPE A
277		COM[17]	3523.5	1059.3	TYPE A
278		COM[18]	3496.5	1059.3	TYPE A
279		COM[19]	3469.5	1059.3	TYPE A
280		COM[20]	3442.5	1059.3	TYPE A
281		COM[21]	3415.5	1059.3	TYPE A
282		COM[22]	3388.5	1059.3	TYPE A
283		COM[23]	3361.5	1059.3	TYPE A
284		COM[24]	3334.5	1059.3	TYPE A
285		COM[25]	3307.5	1059.3	TYPE A
286		COM[26]	3280.5	1059.3	TYPE A
287		COM[27]	3253.5	1059.3	TYPE A
288		COM[28]	3226.5	1059.3	TYPE A
289		COM[29]	3199.5	1059.3	TYPE A
290		COM[30]	3172.5	1059.3	TYPE A
291		COM[31]	3145.5	1059.3	TYPE A
292		COM[32]	3118.5	1059.3	TYPE A
293		COM[33]	3091.5	1059.3	TYPE A
294		COM[34]	3064.5	1059.3	TYPE A
295		COM[35]	3037.5	1059.3	TYPE A
296		COM[36]	3010.5	1059.3	TYPE A
297		COM[37]	2983.5	1059.3	TYPE A
298		COM[38]	2956.5	1059.3	TYPE A
299		COM[39]	2929.5	1059.3	TYPE A
300		COM[40]	2902.5	1059.3	TYPE A
301		COM[41]	2875.5	1059.3	TYPE A

No.	Side	Name	Location		Bump Type
			X[μm]	X[μm]	
302		COM[42]	2848.5	1059.3	TYPE A
303		COM[43]	2821.5	1059.3	TYPE A
304		COM[44]	2794.5	1059.3	TYPE A
305		COM[45]	2767.5	1059.3	TYPE A
306		COM[46]	2740.5	1059.3	TYPE A
307		COM[47]	2713.5	1059.3	TYPE A
308		COM[48]	2686.5	1059.3	TYPE A
309		COM[49]	2659.5	1059.3	TYPE A
310		COM[50]	2632.5	1059.3	TYPE A
311		COM[51]	2605.5	1059.3	TYPE A
312		COM[52]	2578.5	1059.3	TYPE A
313		COM[53]	2551.5	1059.3	TYPE A
314		COM[54]	2524.5	1059.3	TYPE A
315		COM[55]	2497.5	1059.3	TYPE A
316		COM[56]	2470.5	1059.3	TYPE A
317		COM[57]	2443.5	1059.3	TYPE A
318		COM[58]	2416.5	1059.3	TYPE A
319		COM[59]	2389.5	1059.3	TYPE A
320		COM[60]	2362.5	1059.3	TYPE A
321		COM[61]	2335.5	1059.3	TYPE A
322		COM[62]	2308.5	1059.3	TYPE A
323		COM[63]	2281.5	1059.3	TYPE A
324		COM[64]	2254.5	1059.3	TYPE A
325		COM[65]	2227.5	1059.3	TYPE A
326		COM[66]	2200.5	1059.3	TYPE A
327		COM[67]	2146.5	1059.3	TYPE A
328		COM[68]	2173.5	1059.3	TYPE A
329		COM[69]	2119.5	1059.3	TYPE A
330		COM[70]	2092.5	1059.3	TYPE A
331		COM[71]	2065.5	1059.3	TYPE A
332		DUMMY	2038.5	1059.3	TYPE A
333		DUMMY	2011.5	1059.3	TYPE A
334		DUMMY	1984.5	1059.3	TYPE A
335		DUMMY	1957.5	1059.3	TYPE A
336		DUMMY	1930.5	1059.3	TYPE A
337		DUMMY	1903.5	1059.3	TYPE A
338		SEG[1]	1876.5	1059.3	TYPE A
339		SEG[3]	1849.5	1059.3	TYPE A
340		SEG[5]	1822.5	1059.3	TYPE A
341		SEG[7]	1795.5	1059.3	TYPE A
342		SEG[9]	1768.5	1059.3	TYPE A
343		SEG[11]	1741.5	1059.3	TYPE A
344		SEG[13]	1714.5	1059.3	TYPE A
345		SEG[15]	1687.5	1059.3	TYPE A
346		SEG[17]	1660.5	1059.3	TYPE A
347		SEG[19]	1633.5	1059.3	TYPE A
348		SEG[21]	1606.5	1059.3	TYPE A
349		SEG[23]	1579.5	1059.3	TYPE A
350		SEG[25]	1552.5	1059.3	TYPE A
351		SEG[27]	1525.5	1059.3	TYPE A
352		SEG[29]	1498.5	1059.3	TYPE A

No.	Side	Name	Location		Bump Type
			X[μm]	X[μm]	
353		SEG[31]	1471.5	1059.3	TYPE A
354		SEG[33]	1444.5	1059.3	TYPE A
355		SEG[35]	1417.5	1059.3	TYPE A
356		SEG[37]	1390.5	1059.3	TYPE A
357		SEG[39]	1363.5	1059.3	TYPE A
358		SEG[41]	1336.5	1059.3	TYPE A
359		SEG[43]	1309.5	1059.3	TYPE A
360		SEG[45]	1282.5	1059.3	TYPE A
361		SEG[47]	1255.5	1059.3	TYPE A
362		SEG[49]	1228.5	1059.3	TYPE A
363		SEG[51]	1201.5	1059.3	TYPE A
364		SEG[53]	1174.5	1059.3	TYPE A
365		SEG[55]	1147.5	1059.3	TYPE A
366		SEG[57]	1120.5	1059.3	TYPE A
367		SEG[59]	1093.5	1059.3	TYPE A
368		SEG[61]	1066.5	1059.3	TYPE A
369		SEG[63]	1039.5	1059.3	TYPE A
370		SEG[65]	1012.5	1059.3	TYPE A
371		SEG[67]	985.5	1059.3	TYPE A
372		SEG[69]	958.5	1059.3	TYPE A
373		SEG[71]	931.5	1059.3	TYPE A
374		SEG[73]	904.5	1059.3	TYPE A
375		SEG[75]	877.5	1059.3	TYPE A
376		SEG[77]	850.5	1059.3	TYPE A
377		SEG[79]	823.5	1059.3	TYPE A
378		SEG[81]	796.5	1059.3	TYPE A
379		SEG[83]	769.5	1059.3	TYPE A
380		SEG[85]	742.5	1059.3	TYPE A
381		SEG[87]	715.5	1059.3	TYPE A
382		SEG[89]	688.5	1059.3	TYPE A
383		SEG[91]	661.5	1059.3	TYPE A
384		SEG[93]	634.5	1059.3	TYPE A
385		SEG[95]	607.5	1059.3	TYPE A
386		SEG[97]	580.5	1059.3	TYPE A
387		SEG[99]	553.5	1059.3	TYPE A
388		SEG[101]	526.5	1059.3	TYPE A
389		SEG[103]	499.5	1059.3	TYPE A
390		SEG[105]	472.5	1059.3	TYPE A
391		SEG[107]	445.5	1059.3	TYPE A
392		SEG[109]	418.5	1059.3	TYPE A
393		SEG[111]	391.5	1059.3	TYPE A
394		SEG[113]	364.5	1059.3	TYPE A
395		SEG[115]	337.5	1059.3	TYPE A
396		SEG[117]	310.5	1059.3	TYPE A
397		SEG[119]	283.5	1059.3	TYPE A
398		SEG[121]	256.5	1059.3	TYPE A
399		SEG[123]	229.5	1059.3	TYPE A
400		SEG[125]	202.5	1059.3	TYPE A
401		SEG[127]	175.5	1059.3	TYPE A
402		DUMMY	148.5	1059.3	TYPE A
		Alignmark_A	82.8	1099.8	

No.	Side	Name	Location		Bump Type
			X[µm]	X[µm]	
403		DUMMY	9	1059.3	TYPE A
404		DUMMY	9	918.9	TYPE A
405		DUMMY	9	778.5	TYPE A
406		DUMMY	9	638.1	TYPE A
407		DUMMY	9	497.7	TYPE A
408		DUMMY	9	357.3	TYPE A
409		DUMMY	9	216.9	TYPE A

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