SH8601A

480RGBx480 / 16.7M color
AMOLED Display Driver IC

Datasheet

User Command Set

Preliminary Version 0.0

December, 2019

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Version History

December, 2019

Ver.	Date	Page	Description of Changes
Ver0.0	October. 2019		Initial Draft

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1 General description

1.1 Introduction

This IC is used for driving a 480RGBx480 LTPS AMOLED for a wearable or mobile application. It supports a low voltage operation and single chip solution including 240 Source channels. All circuits are designed suitable for AMOLED display panel. For high-speed data transfer, the data for display and command are received via MIPI DSI with 1-lane. Also SH8601A supports MIPI DBI Type-B and Type-C interface. IC is connected to the Application Processor(AP) directly and stores display data into internal display GRAM which is sent from the AP. IC generates AMOLED driving signals by itself and stored display data can be performed with minimal power consumption. Also integrated Source driver, Panel Gate controller, GRAM, Power generation circuit, Voltage Regulator and Timing controller so on. The initialization settings can be partially or fully stored in the non-volatile memory(OTP) and these settings are loaded at the starting stagey of display. This IC provides a high-performance and higher display quality using minimum number of external components for lower power consumption and saving design cost and space.

- MIPI: Mobile Industry Processor Interface
- DSI: Display Serial Interface
- DBI: Display Bus Interface

1.2 Ordering information

- Product Code: SH8601A
- Package: COF

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1.3 Features

Features	Description	
Device Type	LTPS AMOLED Driver IC	
Display Resolution	Max. 480 RGB (H) x 480 (V)	
	Support 1:6 MUX and 1:12 MUX Operation	
	4 Line Horizontal x 2 Line Vertical Control Step	
Color Depth	16M Colors	
Display Type	Panel Type	AMOLED – Rigid & Flexible
	Pixel Arrangement	Real RGB, Delta RGB
	Source Output	240CH with MUX
	GOA for Gate Output	GOAR[22:1], GOAL[22:1].
	Support P-MOS Type Panel	
Interface	High Speed Interface	MIPI (DSI), Data 1 Lane, Clock 1 Lane
	D-PHY Version	v1.0
	DSI Version	v1.02
	Polarity Inversion of MIPI Pins	
	Support Command Mode	
	MIPI DBI Type-B (MPU 8-bit) and Type-C (3/4-wire mode), Quad-SPI	
Internal Graphics RAM	480x480x24bits = 5,529,600bits	
Display Features	RGB separated gamma	
	ACL, HBM	
	Image Enhancement Functions : CRP, Hue, Saturation, Brightness, CE with Skin Tone, Gamut Expansion, Sunlight Readability Enhancement	
One Time Programmable Device (OTP)	Program Voltage Supply	Only External Mode
	Size	16K x 8bit (3times Re-writable)
	Built-in	Gamma, Chip ID, MCS register
On-chip Functions	Internal DC/DC Voltage Converter	
	Timing Generator	
	Adjustable Gamma Curves (Separated R/G/B)	
External Supply Voltages	Interface Power	VDDI = 1.8 V (1.65 V to 3.3 V)
	Analog Power	VCI = 2.8 V (2.7 V to 3.6 V)
Internal Drive Supply Voltages	AVDD	4.6V to 7.0V
	VLOUT2	4.6V to 14.0V
	VLOUT3	-14.0V to -4.6V
	VGH	5.0V to 10.0V
	VGL	-10.0V to -5.0V

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	UELVDD	3.0V to 5.0V
	UELVSS	-4.0V to -0V
	VINT	-6.0V to -0.2V
	VREGOUT	2.0V to 6.5V
	VGS	0.0V to 3.3V
COF Package		
Operating Temperature	-40 °C to + 85 °C	
Storage Temperature	-55 °C to + 125 °C	

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1.4 PAD Description

1.4.1 Power Supply Part

Table 1 PADs for Power Supply

Symbol	I/O	Item	Function Description	Condition
VDDI	P	Voltage Range	Typ. = 1.80V (Min. = 1.65V, Max. = 3.3V)	
		Unused	Required	
		Component	Capacitor	
		Description	Power supply for I/O block provided from outside VDDI < 0.05V (When power is turned off)	
VCI	P	Voltage Range	Typ. = 2.8V (Min. = 2.70V, Max. = 3.60V)	
		Unused	Required	
		Component	Capacitor	
		Description	Power Supply for Analog Circuits VCI < 0.05V (When power is turned off)	
VOTP	P	Voltage Range	Typ. = 6.0V (Min. = 5.8V, Max. = 6.2V)	
		Unused	Open	
		Description	External Voltage Input for OTP Data Program	
VSSI	P	Description	GND for I/O Block provided from outside (VSSI = 0V)	
VSS	P	Description	GND for Logic Block (VSS = 0V)	
VSSM	P	Description	GND for Memory Block (VSSM = 0V)	
VSS_MIPI	P	Description	GND for MIPI DSI receiver (VSS_MIPI = 0V)	
VSSA	P	Description	GND for Analog circuits (VSSA = 0V)	
VSSC	P	Description	GND for DCDC block (VSSC = 0V)	

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1.4.2 Analog Part

Table 2 PADs for Analog Power

Symbol	I/O	Item	Function Description	Condition
AVDD	O	Voltage Range	Min. = 4.6V Max. = 7.0V	AVDD-VREGOUT = Min.0.5V
		Component	Capacitor	
		Description	Power supply for Source Driver and Booster	
C11P C11N	O	Voltage Range	Min. = 0.0V Max. = 7.0V	
		Unused	Open	
		Component	Capacitor	
		Description	Charge-pumping capacitor.	
C12P C12N	O	Voltage Range	Min. = 0.0V Max. = 7.0V	
		Unused	Open	
		Component	Capacitor	
		Description	Charge-pumping capacitor.	
VLOUT2	O	Voltage Range	Min. = AVDD Max. = AVDD x 2	VLOUT2-VGH = Min.2.0V
		Component	Capacitor	
		Description	Power Supply for VGH	
C21P C21N	O	Voltage Range	Min. = 0.0V Max. = AVDD x 2	
		Unused	Open	
		Component	Capacitor	
		Description	Charge-pumping capacitor	
VLOUT3	O	Voltage Range	Min. = -AVDD x 2 Max. = -AVDD	|VLOUT3-VGL| = Min. 2.0V
		Component	Capacitor	
		Description	Power Supply for VGL	
C31P C31N	O	Voltage Range	Min. = -AVDD Max. = AVDD	
		Unused	Open	
		Component	Capacitor	
		Description	Charge-pumping capacitor	
C32P C32N	O	Voltage Range	Min. = -AVDD x 2 Max. = -AVDD	
		Unused	Open	

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Symbol	I/O	Item	Function Description	Condition
		Component	Capacitor	
		Description	Charge-pumping capacitor	
VREGOUT	O	Voltage Range	Min. = 2.0V Max. = 6.5V	lower than AVDD – 0.5V
		Unused	Required	
		Component	Capacitor(optional)	
		Description	Reference High Voltage Output for Grayscale Voltage Generator.	
VGS	O	Voltage Range	Min. = 0.0V Max. = 3.3V	
		Unused	Required	
		Component	Capacitor(optional)	
		Description	Reference Low Voltage Output for Grayscale Voltage Generator.	
VGH	O	Voltage Range	Min. = 5.0V Max. = 10.0V	–
		Unused	Required	
		Component	Capacitor	
		Description	Reference High Voltage Output for Gate Driver.	
VGL	O	Voltage Range	Min. = -10.0V Max. = -5.0V	–
		Unused	Required	
		Component	Capacitor	
		Description	Reference Low Voltage Output for Gate Driver	
VINT	O	Voltage Range	Min. = -6.0V Max. = -0.2V	
		Unused	Required	
		Component	Capacitor	
		Description	Reference Voltage Output for Pixel Initialization	
UELVDD	O	Voltage Range	Min. = 3.0V Max. = 5.0V	
		Unused	Required	
		Component	Capacitor	
		Description	Panel Positive Power in AOD Mode	
UELVSS	O	Voltage Range	Min. = -4.0V Max. = -0.0V	
		Unused	Required	
		Component	Capacitor	
		Description	Panel Negative Power in AOD Mode	

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1.4.3 Logic Part

Table 3 PADs for Logic Interface

Symbol	I/O	Item	Function Description	Condition
CKP/CKN	I	Voltage Range	Min. = -50mV Max. = 1.30V	
		Unused	Fix to VSS_MIPI.	
		Description	Differential Clock Input Pins These pins always receive high speed clock when MIPI activates in high speed data transmission mode.	
D0P/D0N	I/O	Voltage Range	Min. = -50mV Max. = 1.30V	
		Unused	Fix to VSS_MIPI.	
		Description	Differential Data Input/Output Pins When forward link activates, these pins receive data from host. When reverse link activates, these pins transmit data to host.	
S<240:1>	O	Voltage Range	Min. = 0.0V Max. = 6.5V	
		Unused	Open	
		Description	Source Driver Output Pins	
GOAR<22:1>	O	Voltage Range	Min. = -10.0V Max. = 10.0V	
		Unused	Open	
		Description	This pin used to panel control.	
GOAL<22:1>	O	Voltage Range	Min. = -10.0V Max. = 10.0V	
		Unused	Open	
		Description	This pin used to panel control.	
IM[2:0]	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VDDI or VSSI	
		Description	This pin used to interface mode control.	
RESX	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Required	
		Description	This signal is used to reset the device and must be applied to initialize the chip properly. Active Low	
CSX	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VDDI	

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Symbol	I/O	Item	Function Description	Condition
		Description	Chip Select Signal in MIPI DBI Type-B(MPU) and Type-C(SPI) Active Low	
DCX	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VDDI or VSSI	
		Description	Data is selected if DCX is high in MIPI DBI Type-B(MPU) and Type-C(SPI). Otherwise command is selected.	
SCL_WRX	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VDDI or VSSI	
		Description	Synchronous Clock Signal in MIPI DBI Type-B(MPU) and Type-C(SPI)	
SDI_RDX	I/O	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VDDI or VSSI	
		Description	Serial Data Input in MIPI DBI Type-C(SPI) Synchronous Clock Signal in MIPI DBI Type-B(MPU) Please reference to 4.1 Interface Type Selection	
SDO_SDI1	I/O	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VDDI or VSSI	
		Description	Serial Data Output in MIPI DBI Type-C(SPI) Data Input Signal at Dual Input Mode Please reference to 4.1 Interface Type Selection	
SDI2	I/O	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VDDI or VSSI	
		Description	Serial Data Input in Quad-SPI Please reference to 4.1 Interface Type Selection	
SDI3	I/O	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Fix to VDDI or VSSI	
		Description	Serial Data Input in Quad-SPI Please reference to 4.1 Interface Type Selection	
PSWAP	I	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Required	
		Description	These pins control polarity of MIPI Lane. 1 : P→P, N→N 0 : P→N, N→P	
DB[7:0]	I	Voltage Range	Min. = VSSI	

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Symbol	I/O	Item	Function Description	Condition
			Max. = VDDI	
		Unused	Fix to VSSI or VDDI	
		Description	Data Input MIPI DBI Type-B If not used, this pad should be connected to VDDI or VSSI.	
ERR_FG	O	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Open	
		Description	Purpose on Test for MIPI Status	
TE	O	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Open	
		Description	Monitor Pin of TE (Tearing Effect) Logic Signal When this pad is not activated, this signal stays low.	
EL_CTRL	O	Voltage Range	Min. = VSSI Max. = VDDI	
		Unused	Necessary	
		Description	PMIC Control Signal	

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2 Electrical Characteristics

2.1 Absolute Maximum Ratings

It defines the maximum operating conditions. The reliability of IC is not guaranteed if used in the conditions beyond the limits and it may lead to malfunction.

Table 4 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage for I/O Block	VDDI-VSS	– 0.3 to + 3.6	V
Supply Voltage for Step-up Circuit	VCI-VSS	– 0.3 to + 4.0	V
AMOLED Supply Voltage Range	AVDD-VSS	– 0.3 to + 8.4	V
	VSS-VINT	– 0.3 to + 6.6	V
	VLOUT2-VSS	– 0.3 to + 15.0	V
	VSS-VLOUT3	– 0.3 to + 15.0	V
	VGH-VSS	– 0.3 to + 11	V
	VSS-VGL	– 0.3 to + 11	V
	UELVDD – VSS	– 0.3 to + 5.5	V
	VSS- UELVSS	– 0.3 to + 4.4	V
	|VLOUT2-VLOUT3|	– 0.3 to + 26	V
Supply Voltage for OTP	VOTP-VSS	– 0.3 to + 6.2	V
Input Voltage Range	V_{in}	– 0.3 to VDDI + 0.3	V
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Conditions outside the range listed in the above table may cause permanent damage to the device, may not be recovered. It is strongly recommended to use the IC within the limits of its electrical characteristics during normal operation. Absolute voltages are referenced to ground. The functional operation of the device is not implied for these conditions.

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2.2 DC Electrical Characteristics

2.2.1 DC Characteristics for Power Supply

Table 5 DC Characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Application Pin	Unit	Note
			Min.	Typ.	Max.			
Power supply voltage	VDDI		1.65	1.8	3.3	VDDI	V	
	VCI		2.7	2.8	3.6	VCI		
	VOTP			6.0		VOTP		

NOTE: TA = – 40 to 85 °C

2.2.2 DC Characteristics for Generated Voltage

Table 6 DC Characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit	Note
			Min.	Typ.	Max.		
Operation voltage	VREGOUT	VREGOUT < AVDD – 0.5 V	2.0	–	6.5	V	
	VGS		0	–	3.3		
	VINT	VINT > VLOUT3 + 2.0V	-6.0	–	– 0.2		
	VGH	VGH < VLOUT2 – 2.0V	5.0	–	10.0		
	VGL	VGL > VLOUT3 + 2.0V	–10.0	–	–5.0		
	AVDD	VCI x 2, VCI x 3	4.6	–	7.0		
	VLOUT2	|VLOUT2-VLOUT3| < 25 V	4.6	–	14		
	VLOUT3		–14	–	–4.6		

NOTE: TA = – 40 to 85 °C

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2.2.3 DC Characteristics for Interface

Table 7 DC Characteristic for Interface Signals

Parameter	Symbol	Condition	Specification			Pin	Unit
			Min.	Typ.	Max.		
Logic high level input voltage	VIH_IO1	–	0.8 × VDDI	–	VDDI	RESX	V
Logic low level input voltage	VIL_IO1	–	0.0	–	0.2 × VDDI		
Logic high level output voltage	VOH_IO1	IOUT = – 1 mA	0.8 × VDDI	–	VDDI	TE	
Logic low level output voltage	VOL_IO1	IOUT = + 1 mA	0.0	–	0.2 × VDDI		
Input high level leakage current	IIH	VIN = VDDI	–	–	1	RESX	μA
Input low level leakage current	IIL	VIN = VSS	– 1	–	–		

NOTE: TA = – 40 to 85 °C

2.2.4 Power Consumption

Table 8 Power Consumption

Parameter	Symbol	Condition	Specification			Unit	Note
			Min.	Typ.	Max.		
Operating current (DSI, dynamic display)	$IVDDI_{op}$	Frame frequency = 60 Hz No load SR_SET = 5'b10110 SPR Function OFF	–	–	2.805	mA	(NOTE)
	$IVCI_{op}$		–	–	5.5		
Sleep current	$IVDDI_{LP}$	LP11 mode	–	–	850	uA	
	$IVCI_{LP}$		–	–	50		
	$IVDDI_{ULPS}$	ULPS mode	–	–	833	uA	
	$IVCI_{ULPS}$		–	–	50		
Deep standby current	$IVDDI_{DSLP}$		–	–	4	uA	
	$IVCI_{DSLP}$		–	–	2		

NOTE: The table above shows only driver IC's power consumption. (MIPI I/F @0.5Gbps, white pattern).
VCI = 2.8V, VDDI = 1.8V, TA = 25 °C.

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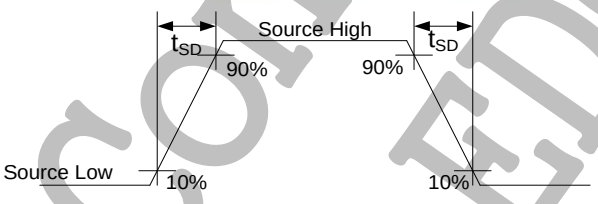
2.2.5 DC Characteristics for Internal Circuits

Table 9 DC Characteristics for Internal Circuits

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating frequency	$F_{oscTA25}$	TA = 25 °C	21.34	22	22.66	MHz	
Voltage efficiency of Step-up output	VLOUT2	I_VLOUT2 = -0.5mA, TA = 25 °C	90	–	–	%	
	VLOUT3	I_VLOUT3 = +0.5mA, TA = 25 °C	90	–	–		
Panel driving voltage	VGH	I_VGH = -0.5mA, TA = 25 °C	Target - 0.1	Target	–	V	
	VGL	I_VGL = +0.5mA, TA = 25 °C	Target - 0.1	Target	–		
	VINT	I_VINT = +0.5mA, TA = 25 °C	Target - 0.1	Target	–		
Output on resistance of Gate driver	Ron_{vgh}	VGH = 6.6 V VGL = – 8.0 V	–	–	2	kΩ	
	Ron_{vgl}		–	–	2		
Delay, Source driver	t_{SD}	AVDD = 5.6 V VREGOUT = 5.0 V VGS = 2.0 V SR_SET = 5'b10110	–	–	1.8	μs	(1)
Source output voltage deviation: mean value (channel to channel)	Δ_{Vo}	VSS + 1.0V < Vso < AVDD – 1.0 V	–	–	± 5	mV	(2)

NOTE: TA = – 40 to 85 °C Unless Otherwise Specified

1. Measurement condition (Delay Measurement of Source Driver), EDS load (0.1k,100pF)



2. SR_SET=5b'10110, Offset cancellation condition=ON

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2.2.6 DC Characteristics for Reset

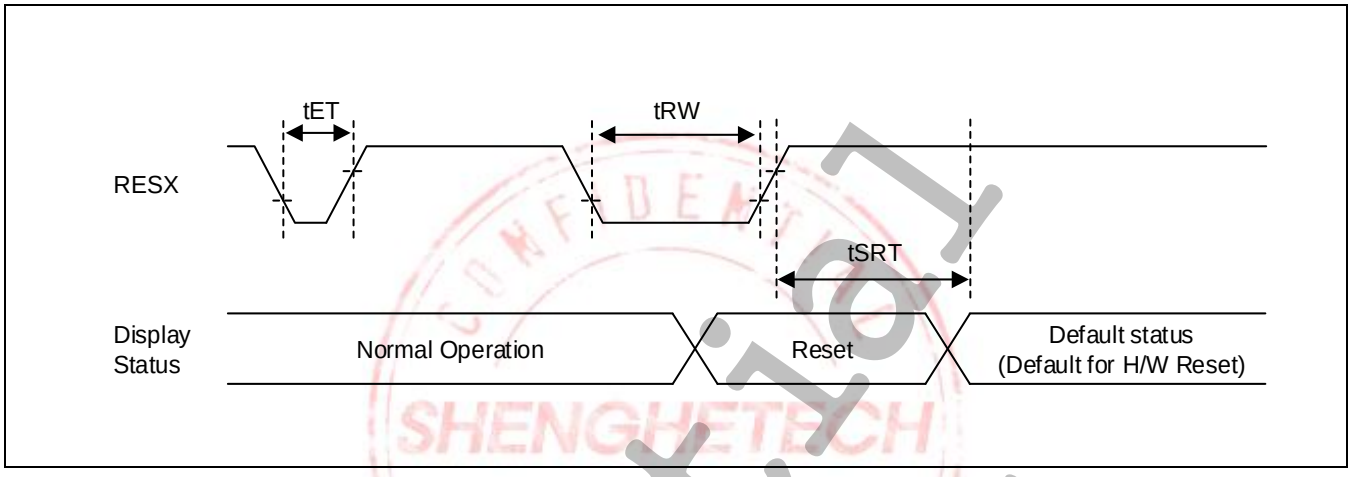

Figure 1 Reset Input Timing

Table 10 Reset Input Timing

Parameter	Symbol	Pad	Min.	Typ.	Max.	Unit	Note
Reset low pulse width	tRW	RESX	10	–	–	μs	–
Secure reset completion time	tSRT	RESX	–	–	5	ms	Reset during Sleep In mode
		RESX	–	–	150		Reset during Sleep Out mode
Reset un-reacted pulse width	tET	RESX			5	μs	–

NOTE:

1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

Table 11 RESX Pulse

RESX Pulse	Action
Shorter than 5 μs	Reset rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset start

2. During the reset period, the display will be blanked (The display is entering blanking sequence, for which the maximum time is 150ms, when Reset starts in Sleep Out-mode. The display remains in the blank state in Sleep In-mode) and then return to Default condition for H/W reset.
3. During Reset Completion Time, ID bytes (or similar) value in OTP will be latched to the internal register during this period. This loading is done every time when there is H/W reset complete time (tSRT) within 5ms after a rising edge of RESX.

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2.3 AC Characteristics

2.3.1 MIPI DBI Type-C – Option1 (SPI 3 Wire)

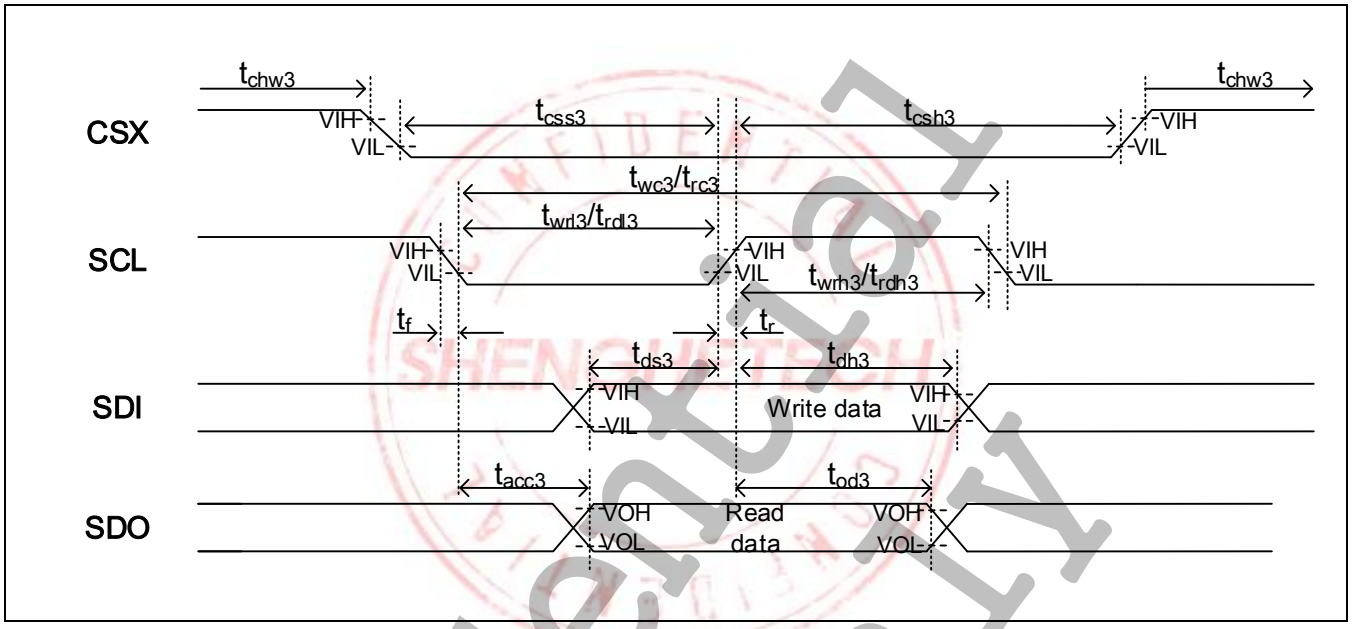

Figure 2 3 Wire 9bit Serial Interface Characteristics

Table 12 AC Characteristics of MIPI DBI Type-C – Option1 (SPI 3 Wire)

Characteristic	Symbol		Specification		Unit
			Min.	Max.	
Chip select setup time	CSX	t_{css3}	40	–	ns
Chip select hold time		t_{csh3}	40	–	ns
Chip select “High” pulse width		t_{chw3}	50	–	ns
Write cycle time	SCL (Write)	t_{wc3}	65	–	ns
SCL “High” period (Write)		t_{wrh3}	25	–	ns
SCL “Low” period (Write)		t_{wrl3}	25	–	ns
Read cycle time	SCL (Read)	t_{rc3}	100	–	ns
SCL “High” period (Read)		t_{rdh3}	50	–	ns
SCL “Low” period (Read)		t_{rdl3}	50	–	ns
Data setup time	SDI	t_{ds3}	15	–	ns
Data hold time		t_{dh3}	15	–	ns
Access time	SDO	t_{acc3}	5	15	ns
Output disable time		t_{od3}	20	–	ns
Rise/Fall time	-	t_r/t_f	–	1	ns

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2.3.2 MIPI DBI Type-C – Option3 (SPI 4 Wire)

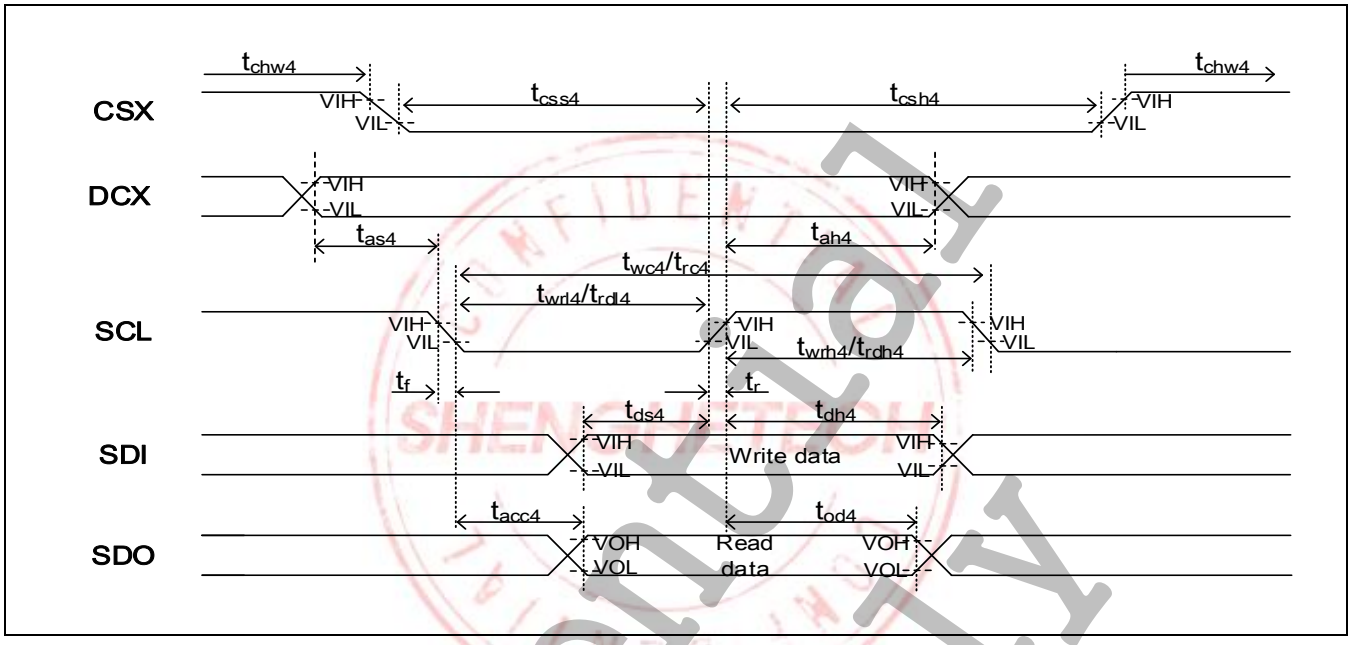

Figure 3 4 Wire 8bit Serial Interface Characteristics

Table 13 AC Characteristics of MIPI DBI Type-C – Option3 (SPI 4 Wire)

Characteristic	Symbol		Specification		Unit
			Min.	Max.	
Chip select setup time	CSX	t_{css4}	40	–	ns
Chip select hold time		t_{csh4}	40	–	ns
Chip select “High” pulse width		t_{chw4}	50	–	ns
Address setup time	DCX	t_{as4}	10	–	ns
Address hold time(Write/Read)		t_{ah4}	20	–	ns
Write cycle time	SCL (Write)	t_{wc4}	50	–	ns
SCL “High” period (Write)		t_{wrh4}	25	–	ns
SCL “Low” period (Write)		t_{wrl4}	25	–	ns
Read cycle time	SCL (Read)	t_{rc4}	100	–	ns
SCL “High” period (Read)		t_{rdh4}	50	–	ns
SCL “Low” period (Read)		t_{rdl4}	50	–	ns
Data setup time	SDI	t_{ds4}	15	–	ns
Data hold time		t_{dh4}	15	–	ns
Access time	SDO	t_{acc4}	5	–	ns
Output disable time		t_{od4}	20	–	ns
Rise/Fall time	-	t_r/t_f	–	1	ns

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2.3.3 Quad SPI

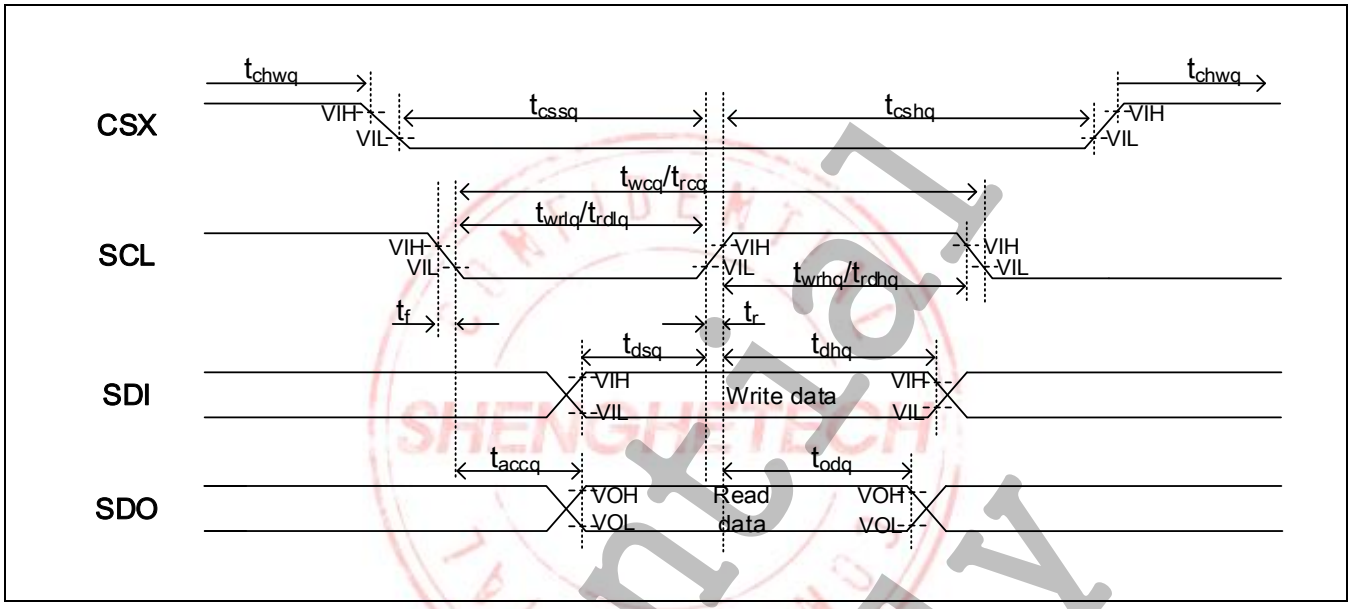

Figure 4 Quad Serial Interface Characteristics

Table 14 AC Characteristics of Quad SPI

Characteristic	Symbol		Specification		Unit
			Min.	Max.	
Chip select setup time	CSX	t_{cssq}	40	–	ns
Chip select hold time		t_{cshq}	40	–	ns
Chip select “High” pulse width		t_{chwq}	50	–	ns
Write cycle time	SCL (Write)	t_{wcq}	50	–	ns
SCL “High” period (Write)		t_{wrhq}	25	–	ns
SCL “Low” period (Write)		t_{wrlq}	25	–	ns
Read cycle time	SCL (Read)	t_{rcq}	100	–	ns
SCL “High” period (Read)		t_{rdhq}	50	–	ns
SCL “Low” period (Read)		t_{rdlq}	50	–	ns
Data setup time	SDI	t_{dsq}	15	–	ns
Data hold time		t_{dhq}	15	–	ns
Access time	SDO	t_{accq}	5	–	ns
Output disable time		t_{odq}	20	–	ns
Rise/Fall time	-	t_r/t_f	–	1	ns

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2.3.4 MIPI DBI Type-B (MPU 8bit)

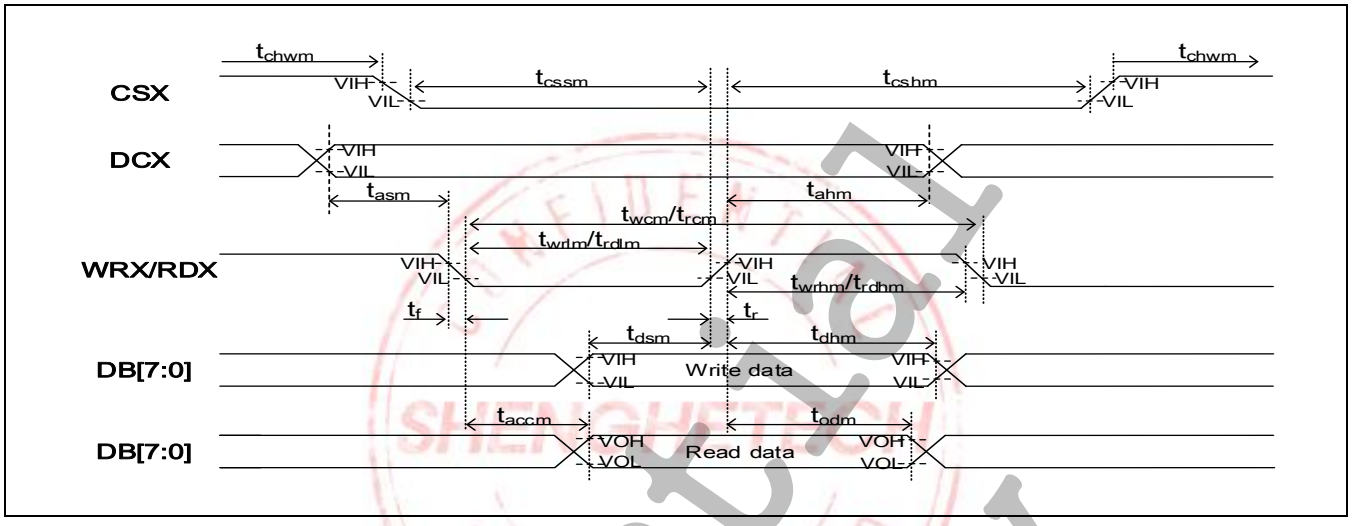

Figure 5 MPU Interface Characteristics

Table 15 AC Characteristics of MPU

Characteristic	Symbol		Specification		Unit
			Min.	Max.	
Chip select setup time	CSX	t_{cssm}	40	–	ns
Chip select hold time		t_{cshm}	40	–	ns
Chip select “High” pulse width		t_{chwm}	50	–	ns
Address setup time	DCX	t_{asm}	10	–	ns
Address hold time(Write/Read)		t_{ahm}	20	–	ns
Write cycle time	WRX (Write)	t_{wcm}	50	–	ns
WRX “High” period (Write)		t_{wrhm}	25	–	ns
WRX “Low” period (Write)		t_{wrlm}	25	–	ns
Read cycle time (Register Read)	RDX (Register Read)	t_{rcm}	100	–	ns
RDX “High” period (Register Read)		t_{rdhm}	50	–	ns
RDX “Low” period (Register Read)		t_{rdlm}	50	–	ns
Read cycle time (Memory Read)	RDX (Memory Read)	t_{rcm}	200	–	ns
RDX “High” period (Memory Read)		t_{rdhm}	10	–	ns
RDX “Low” period (Memory Read)		t_{rdlm}	10	–	ns
Data setup time	DB[7:0]	t_{dsm}	15	–	ns
Data hold time		t_{dhm}	15	–	ns
Access time	DB[7:0]	t_{accm}	5	–	ns
Output disable time		t_{odm}	20	–	ns
Rise/Fall time	-	t_r/t_f	–	1	ns

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2.4 MIPI Characteristics

2.4.1 DC Characteristics for MIPI DSI

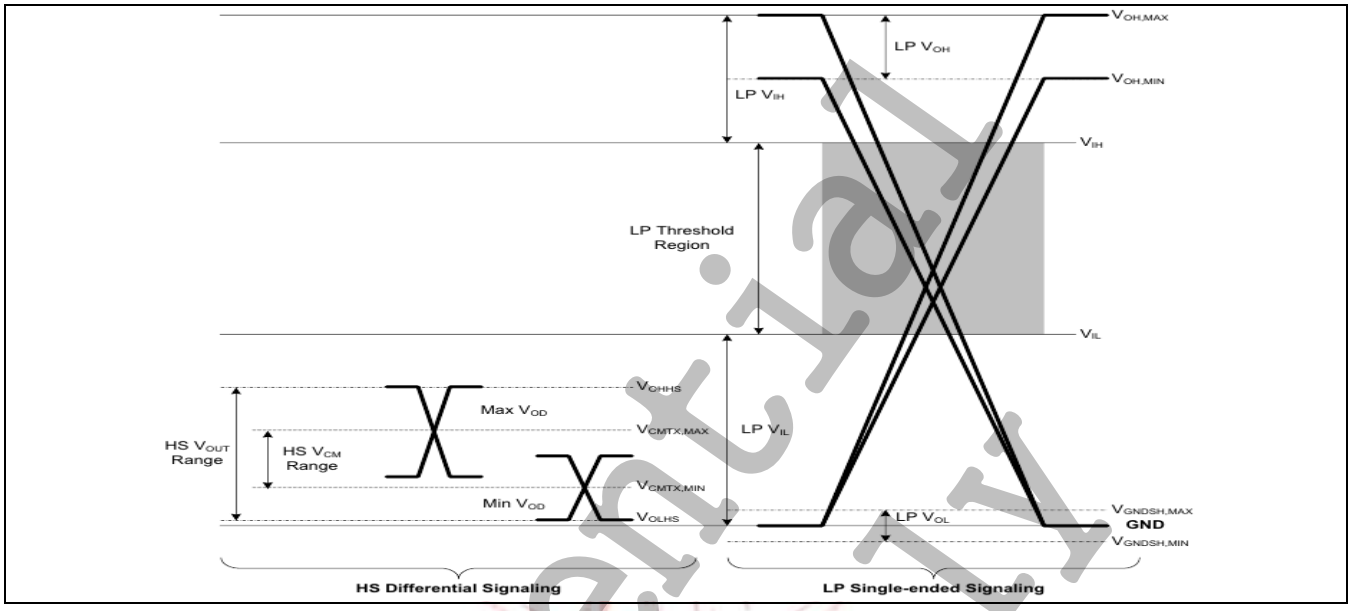

Figure 6 MIPI D-PHY Signaling Levels

Table 16 MIPI DSI DC Characteristic

Item		Symbol	Min.	Typ.	Max.	Unit	Note
HS_RX	Differential input high threshold	V_{IDTH}	–	–	70	mV	3
	Differential input low threshold	V_{IDTL}	– 70	–	–		3
	Single-ended input high voltage	V_{IHHS}	–	–	460		
	Single-ended input low voltage	V_{ILHS}	– 40	–	–		
	Single-ended threshold for HS termination enable	$V_{TERM-EN}$	–	–	450		
	Common-mode voltage HS receive mode	$V_{CMRX\ (DC)}$	70	–	330		1
	Differential input impedance	Z_{ID}	80	100	125	Ω	2
LP_RX	Logic0 voltage not in ULP State	V_{IL}	–	–	550	mV	
	Logic1 input voltage	V_{IH}	880	–	–		
	I/O leakage current	I_{LEAK}	-10	–	10	uA	
LP_TX	Thevenin output low level	V_{OL}	– 50	–	50	mV	
	Thevenin output high level	V_{OH}	1.1	–	1.3	V	
	Output impedance of LP transmitter	Z_{OLP}	110	–	–	Ω	2

NOTE:

1. $V_{CMRX(DC}$ (DC) = (V_{DP}+V_{DN})/2
2. COG resistance is excluded (contact resistance and ITO wiring resistance). The values are tentative.
3. Minimum ±110mV HS differential swing is required for display data transfer.

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2.4.2 MIPI Line Contention Detection

The Low-Power receiver and a separate contention detector shall be used in a bi-directional data Lane to monitor the line voltage on each low-power signal. The low-power receiver shall be used to detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than V_{IL}. The contention detector shall be used to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than V_{IHCD}. An LP low fault shall not be detected when the pin voltage is less than V_{ILCD}.

The LP-CD threshold voltages (V_{ILCD} and V_{IHCD}) are shown along with the normal signaling voltages as below. After contention has been detected, the protocol shall take proper measures to resolve the situation.

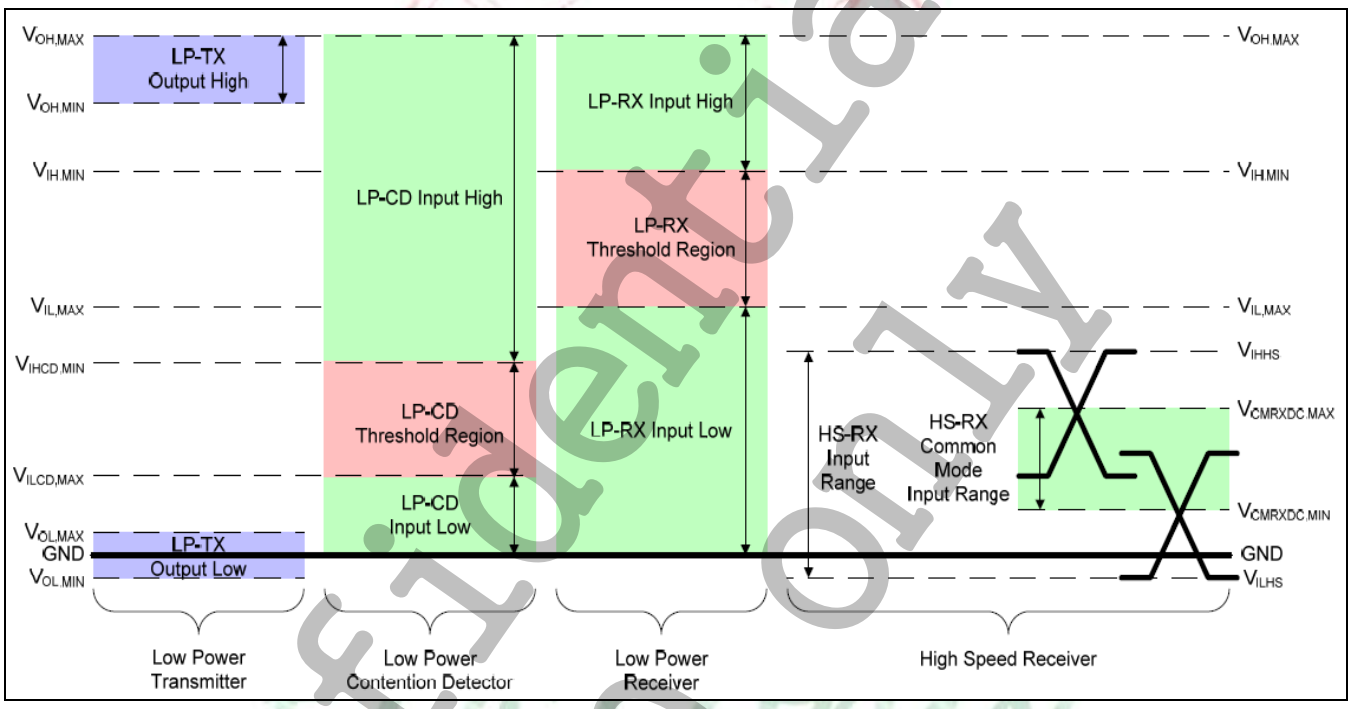

Figure 7 Signaling and Contention Voltage Levels

Table 17 MIPI Contention Detector (LP-CD) DC Characteristic

Item		Symbol	Min.	Typ.	Max.	Unit	Note
CD_RX	Logic0 contention threshold	V_{ILCD}	–	–	200	mV	
	Logic1 contention threshold	V_{IHCD}	450	–	–		

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2.4.3 MIPI DSI High-Speed RX Clock and Data-Clock Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in following figure. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

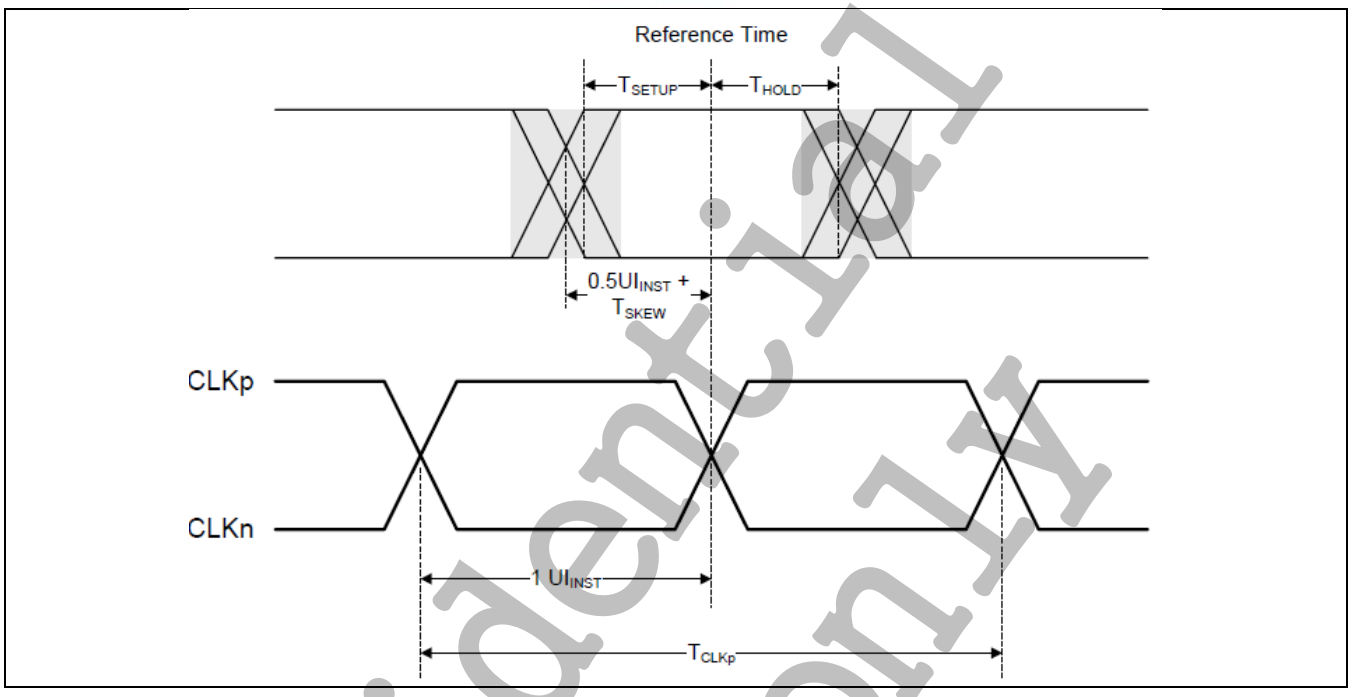

Figure 8 Data to Clock Timing Definitions

Table 18 Data to Clock Signal Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
DSI Data Transfer Rate	T_{DSIR}		80		500	Mbps	
Data to Clock Skew	$T_{SKEW[TX]}$		-0.15		0.15	UI_{INST}	3
Data to Clock Setup time	T_{SETUP}		0.15	–	–	UI_{INST}	1,2
Data to Clock Hold time	T_{HOLD}		0.15	–	–	UI_{INST}	1,2,4
UI instantaneous	UI_{INST}		2	–	12.5	ns	

NOTE:

1. Min. $T_{SETUP[Rx]}$/$T_{HOLD[Rx]}$ time is 0.15UI. (May change depends on DSI transfer rate)
2. $T_{SETUP[Rx]}$ and $T_{HOLD[Rx]}$ are measured without HS-TX jitter and FPC circuit.
3. Total silicon and package delay budget of 0.3* UI_{INST}.
4. Total setup and hold window for receiver of 0.3* UI_{INST}.

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2.4.4 High Speed Clock and Data Timing

Below Figure shows the sequence of the high speed data transmission.

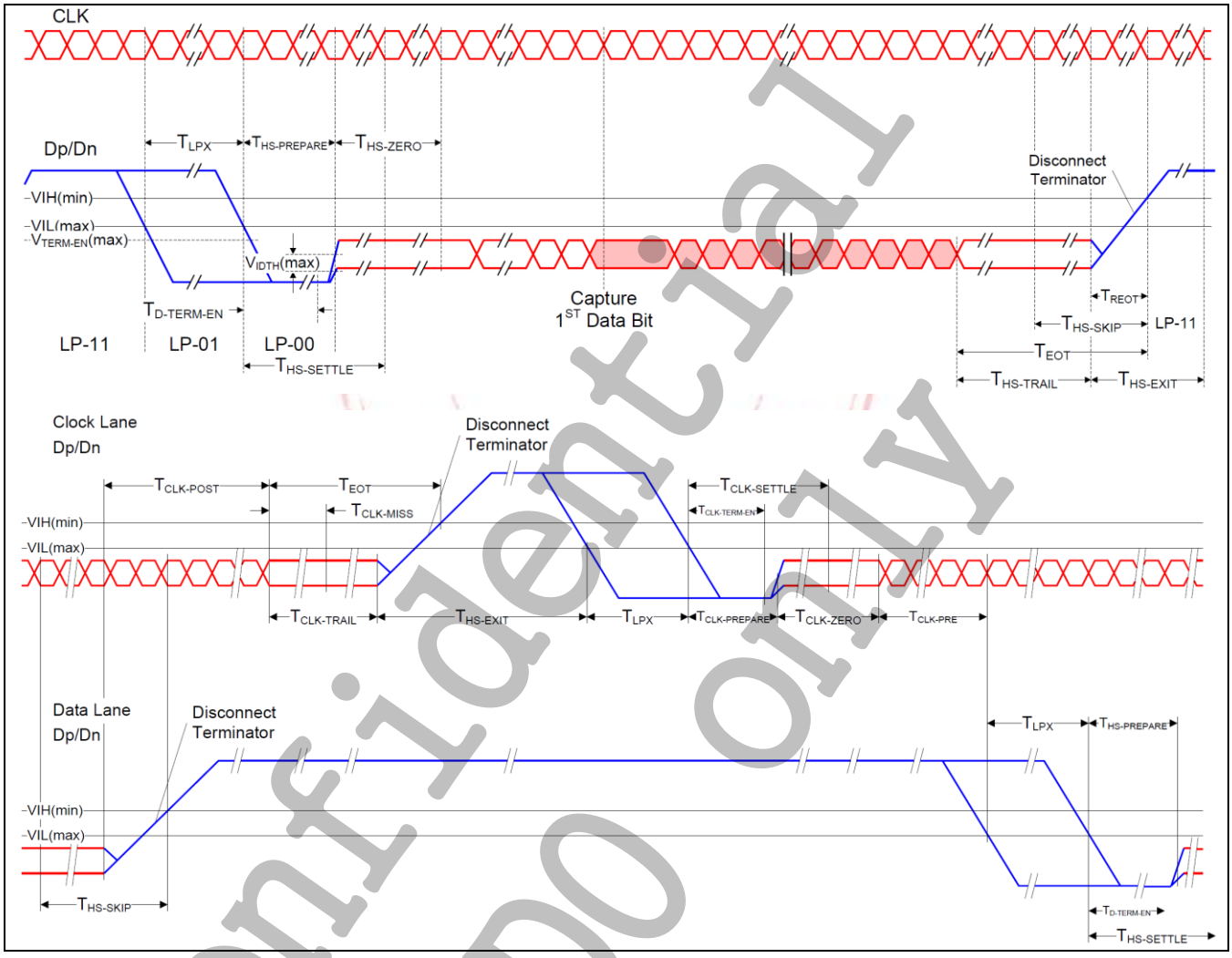

Figure 9 High Speed Clock and Data timing

The values in the following table require a clock tolerance no worse than ± 10 % for implementation.

Table 19 Global Operation Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Unit	Note
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-Rx.	–	–	60	ns	(1) (6)
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52 × UI	–	–		(5)

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Symbol	Description	Min.	Typ.	Max.	Unit	Note
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	–	–	UI	
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	–	95	ns	
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$.	95	–	300		(6)
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	–	38		
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	–	–		(5)
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	–	–		
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	–	35 ns + 4 × UI	–	(6)
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst.	–	–	105 ns + n × 12 × UI	–	(3) (5)
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	–	–	ns	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4 × UI	–	85 ns + 6 × UI		(5)
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10 × UI	–	–		
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$.	85 ns + 6 × UI	–	145 ns + 10 × UI		(6)
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	–	55 ns + 4 × UI		
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max (n × 8 × UI, 60 ns + n × 4 × UI)	–	–		(2) (3) (5)

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Symbol	Description	Min.	Typ.	Max.	Unit	Note
T_{LPX}	Transmitted length of any Low-Power state period	–	56.6	–	ns	(4) (5)
Ratio T_{LPX}	Ratio of T_{LPX}(MASTER)/ T_{LPX}(SLAVE) between Master and Slave side	2/3	–	3/2	–	
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	$5 \times T_{LPX}$			ns	(5)
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	$4 \times T_{LPX}$				
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}	–	$2 \times T_{LPX}$		
T_{WAKEUP}	Time that a transmitter drivers a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	(5)

NOTE:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. If a > b then Max. (a, b) = a, otherwise Max. (a, b) = b
3. Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode
4. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
5. Transmitter-specific parameter
6. Receiver-specific parameter

2.4.5 MIPI Receiver Initialization

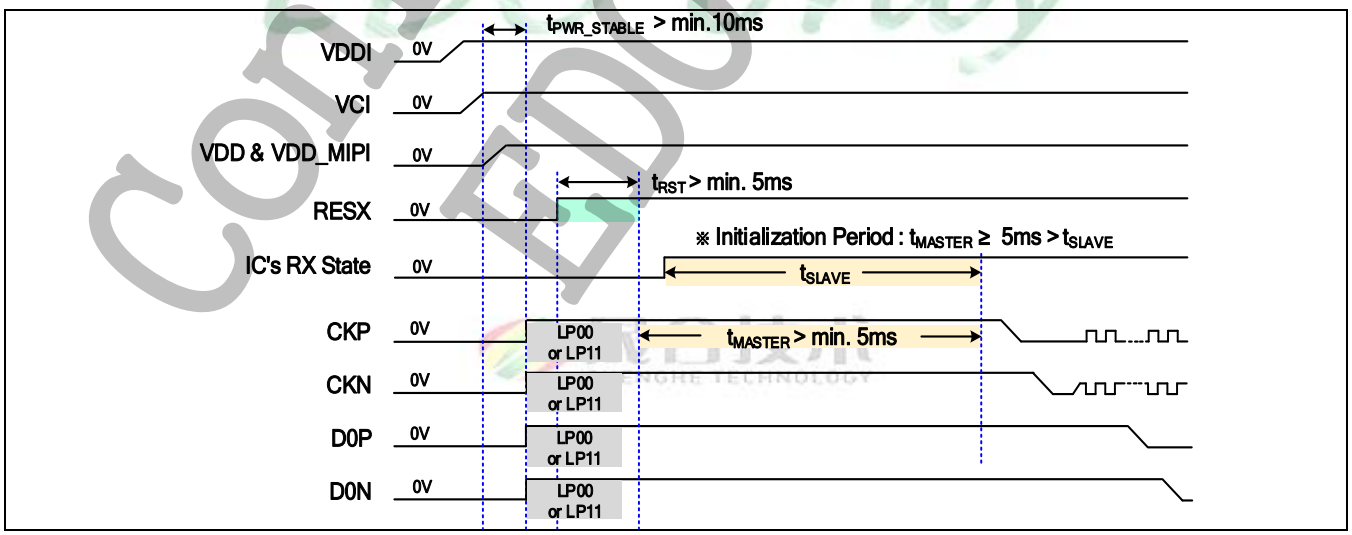

Figure 10 MIPI lanes Status when Reset Operation & Initialization Time

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3 Functional Description

3.1 Tearing Effect Information

The Tearing Effect output line supplies a Panel synchronization signal to the external AP. This signal can be enabled or disabled by the TE control commands. SH8601A has two TE functions. One is controlled by UCS command and the other is controlled by MCS command. The MCS TE function is superior to the UCS TE function.

3.1.1 Tearing Effect Control

TE signal is controlled by TEM (35h) and TESCAN (44h) commands. In TE Mode 1 (UCS TEON and TEM=0), the Tearing Effect output signal is generated by V-Sync information or by the only one H-Sync information designated by TESCAN. In TE Mode 2(UCS TEON and TEM=1), the Tearing Effect output signal consists of V-Sync & H-Sync information.

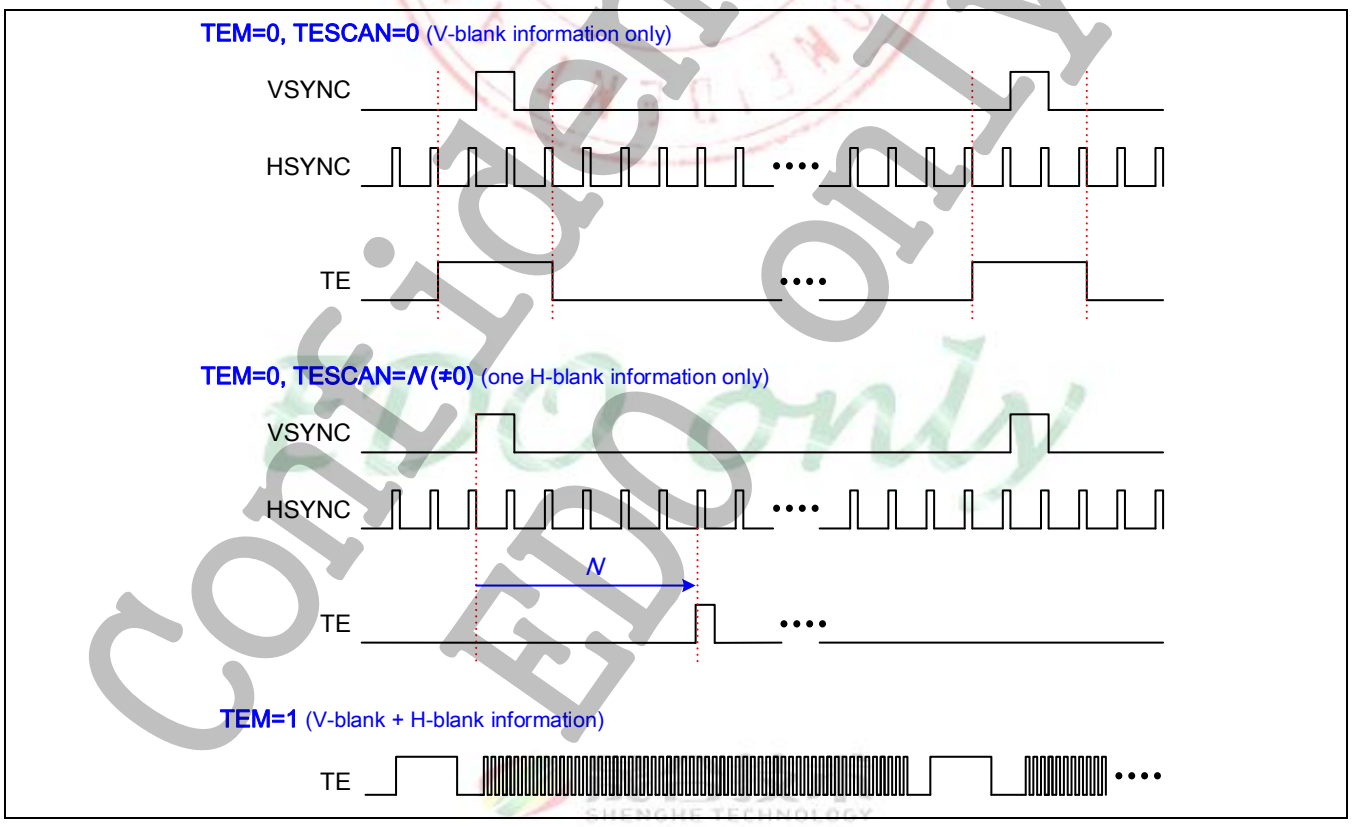

Figure 11 Tearing Effect Line Modes – by UCS

NOTE: During sleep in mode, the Tearing Effect output pin is active low.

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3.1.2 Tearing Effect Line Timings

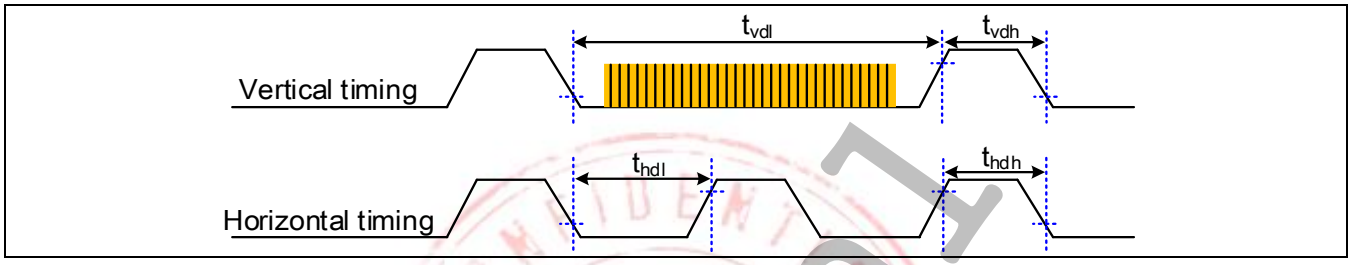

Figure 12 Tearing Effect Line Timings

Table 20 AC Characteristics of Tearing Effect Signal

Parameter	Symbol	Specification			Unit	Description
		Min.	Typ.	Max.		
Vertical timing low duration	tvdl	–	480	–	Line	Note2
Vertical timing high duration	tvdh	–	16	–	Line	Note2
Horizontal timing low duration	thdl	–	480	–	Pixel	Note2
Horizontal timing high duration	thdh	–	32	–	Pixel	Note2
Rise time	tr	–	–	15	ns	Note1
Fall time	tf	–	–	15	ns	

NOTE:

1. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15 ns.
2. Condition : Resolution 480x480, HACTIVE = 480 pixels, HBP = 16 pixels, HFP = 16 pixels, VACTIVE = 480 lines, VBP = 8lines, VFP = 8lines.

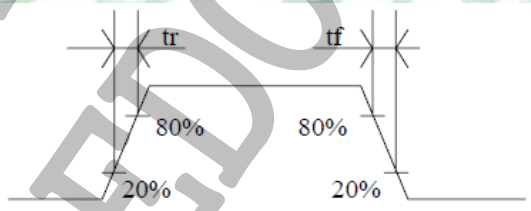

Figure 13 Rise and Fall Times

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3.2 Sleep Out Command and Self-Diagnostic Functions

3.2.1 Register Loading Detection

Sleep out command is a trigger for an internal function of the display module which indicates, if the display module loading function of factory default values from OTP to registers of the display controller is working properly.

There are compared factory values of the OTP and register values of the display controller by the display controller (1st step: Compares register and OTP) values, 2nd step: Loads OTP value to register. If those both values (OTP and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command "Read Display Self-Diagnostic Result (0FH)" (= RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following.

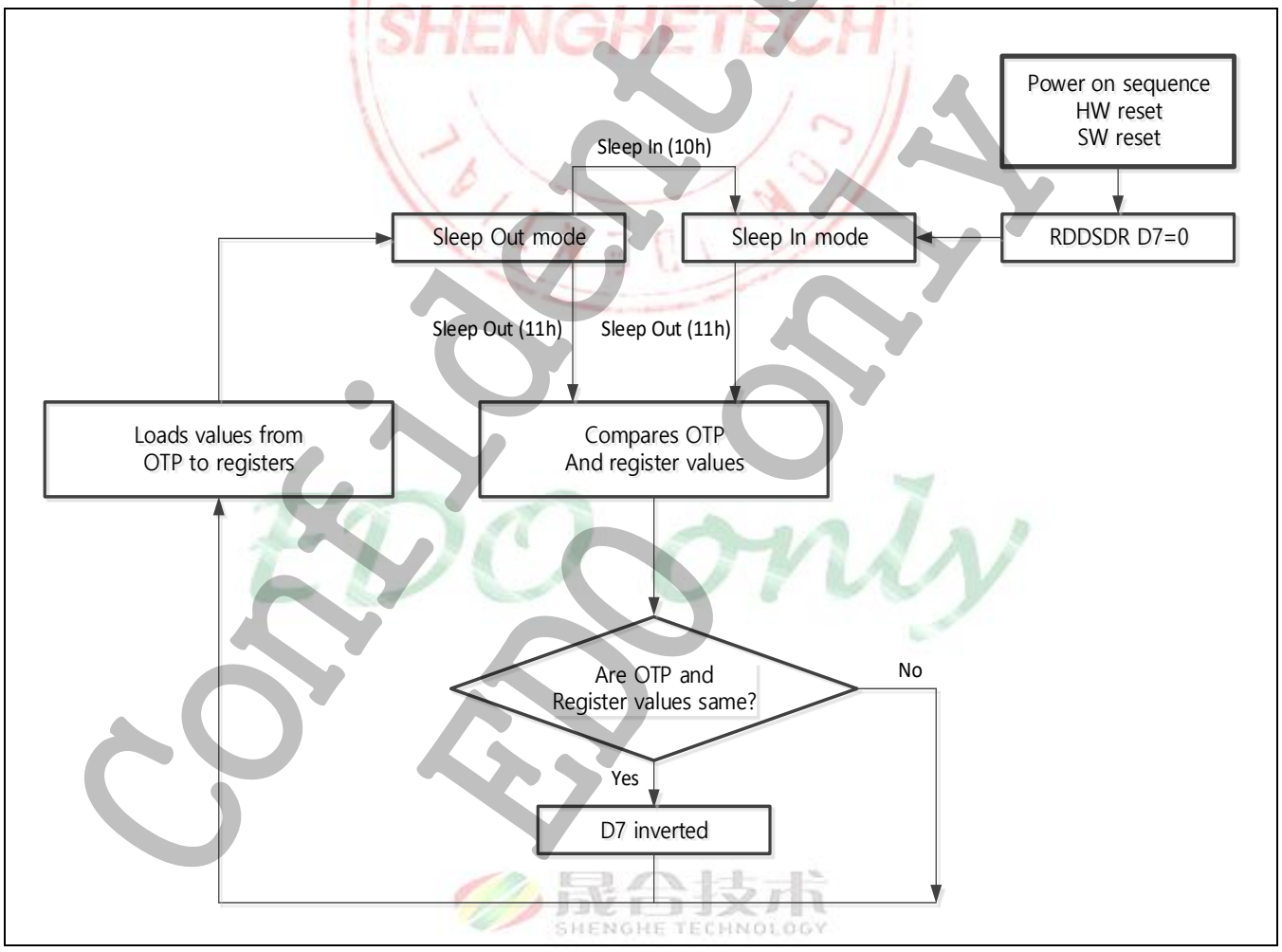

Figure 14 Flow Chart of Register Loading Detection

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3.2.2 Functionality Detection

Sleep out command is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (=the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. Step up circuit voltage levels, timings, etc.). If functionality requirement is met, there is inverted (=Increased by 1) a bit, which defined in command "Read Display Self-Diagnostic Result (0FH)" (= RDDSDR) (the used bit of this command is D6). If functionality requirement is not met, this bit (D6) is not inverted (= Not increased by 1)

The flow chart for this internal function is following:

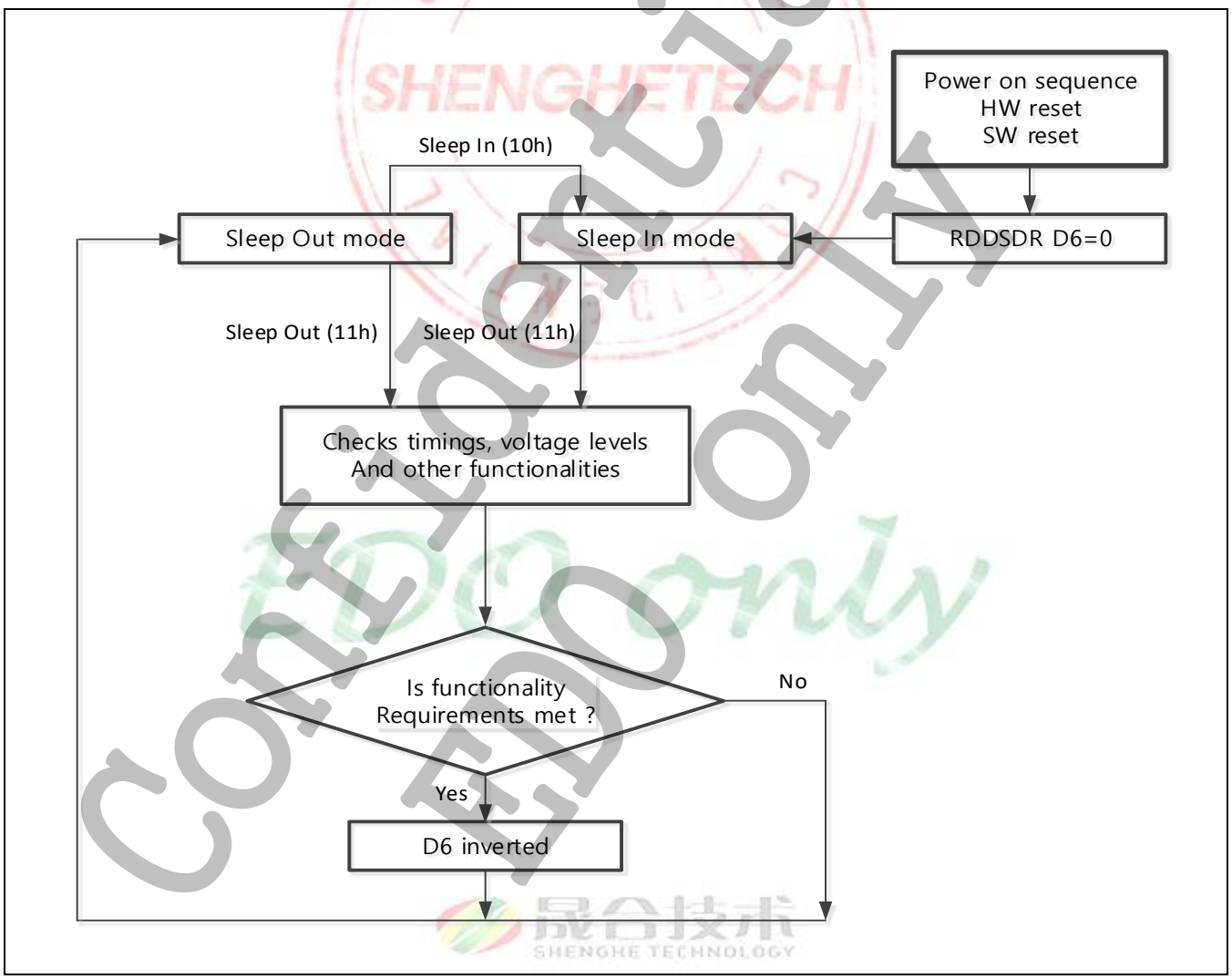

Figure 15 Flow Chart of Functionality Detection

NOTE: There is needed 150ms after sleep out command, when there is changing from Sleep in mode to sleep out mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise there is 10ms delay for D6's value when Sleep out command is sent in Sleep out mode.

3.3 Power

3.3.1 Power On/Off Sequence

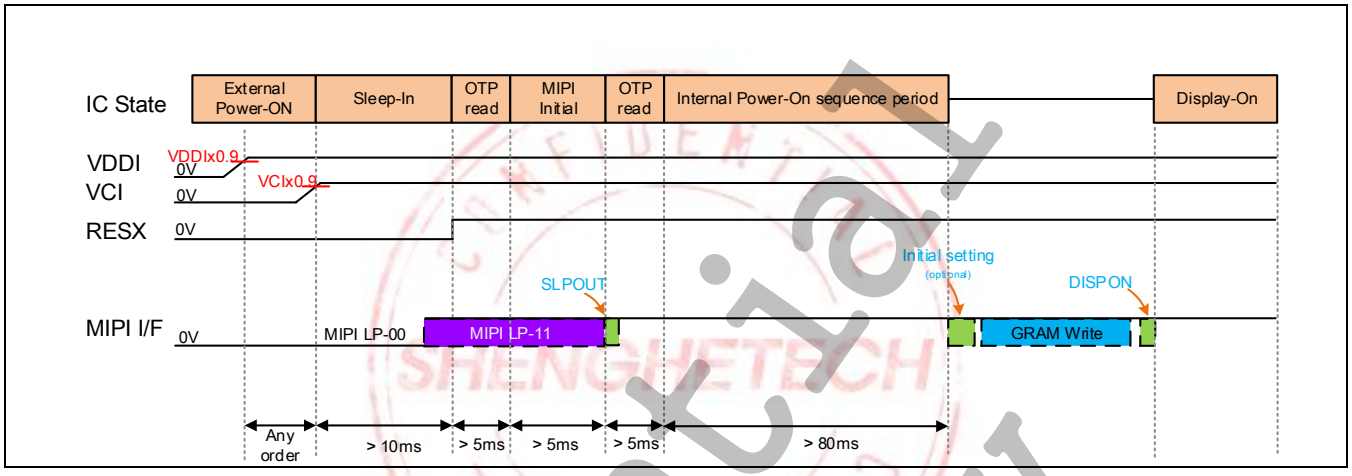

Figure 16 Power-On Sequence

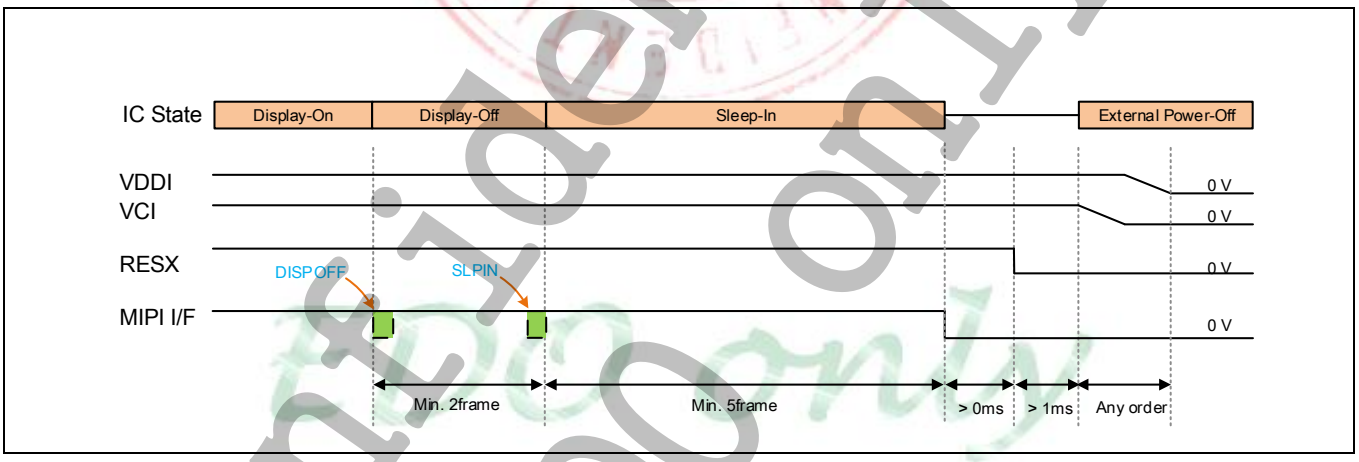

Figure 17 Power-Off Sequence

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3.3.1.1 Power On to Display On / Display Off to Power Off Sequence

The power on to display-on sequence & display-off to power-off sequence are illustrated in the following figures.

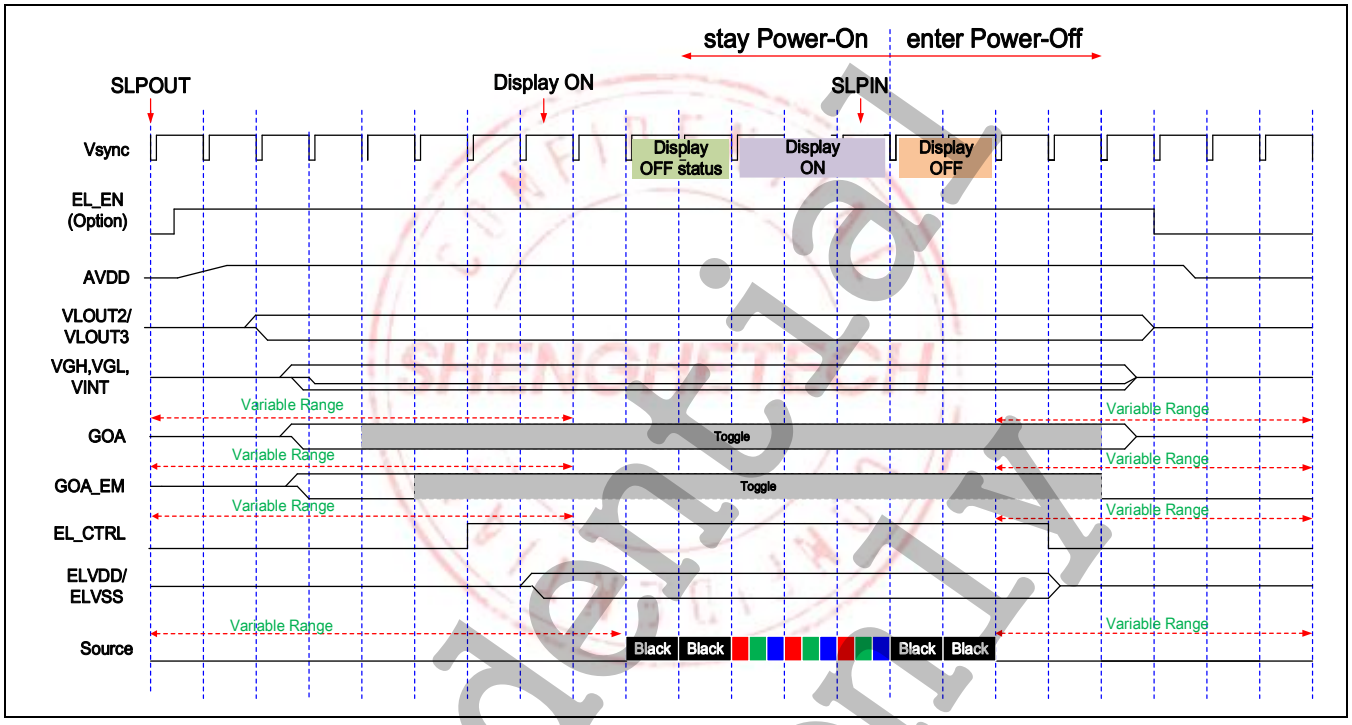

Figure 18 Power-On to Display-On & Display-Off to Power-Off Sequence

3.3.1.2 Power Ramp Up/Down

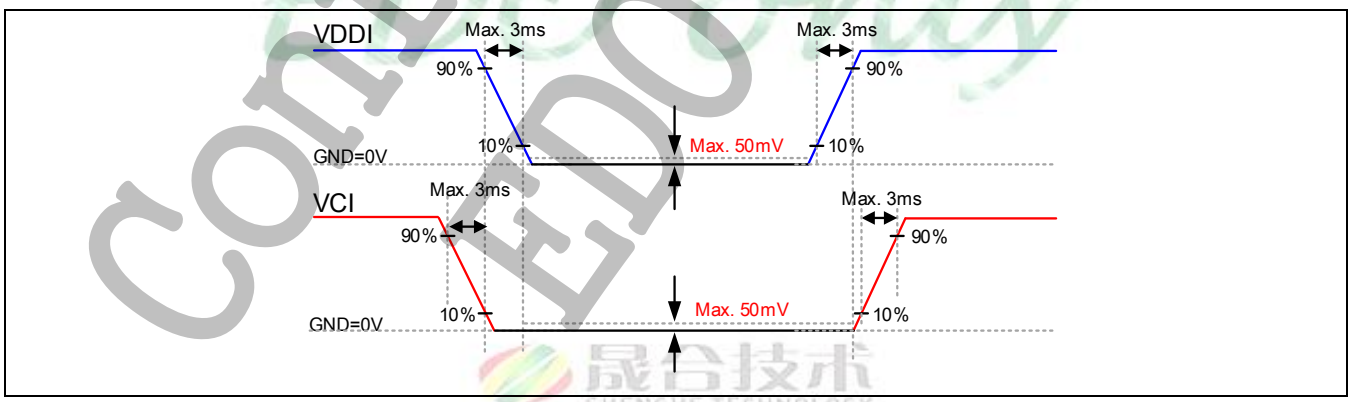

Figure 19 Power Ramp Up/Down

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3.3.2 Power Levels

SH8601A supports 4 types of power-consumption modes. Each mode is described as follows:

1. Normal Mode On (full display), Sleep Out.
   In this mode, the display is able to show maximum 16,777,216 colors.

2. Sleep In Mode.
   In this mode, the booster, internal oscillator and panel driver circuit are stopped.

3. DSTB Mode.
   In this mode, the booster, internal oscillator and panel driver circuit are stopped.
   Interface and registers are not working.

4. Power off Mode.
   In this mode, VCI and VDDI are removed.

NOTE:

1. Transitions between modes 1-2 are controllable by register control.
2. Mode 3 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by Hardware reset only(RESX=Low)
3. Mode 4 is entered only when both Power supplies are removed.

3.3.3 Discharge Status of Power Block and I/O PADs

Table 21 Discharge Status of Power Block and I/O PADs

Power	After H/W or S/W Reset Sleep In Mode	Deep Standby Mode	Abrupt Power Off
VDD	VDD	GND	GND
VDD_MIPI	VDD_MIPI	GND	GND
AVDD	GND	GND	GND
VLOUT2	GND	GND	GND
VLOUT3	GND	GND	GND
VGH	GND	GND	GND
VGL	GND	GND	GND
VREGOUT	GND	GND	GND
VGS	GND	GND	GND
VREF	GND	GND	GND
VINT	GND	GND	GND
SOURCE	Floating	Floating	Floating
GOA	GND	Floating	User defined NOTE

NOTE:

1. Refer to “GOACLK_CTL(B5h)” Description
2. When IC enters to Deep standby mode & Abrupt power off, please set MIPI Pin(=D0P/N & CKP/N) state to GND.

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3.3.4 Deep Standby Flow

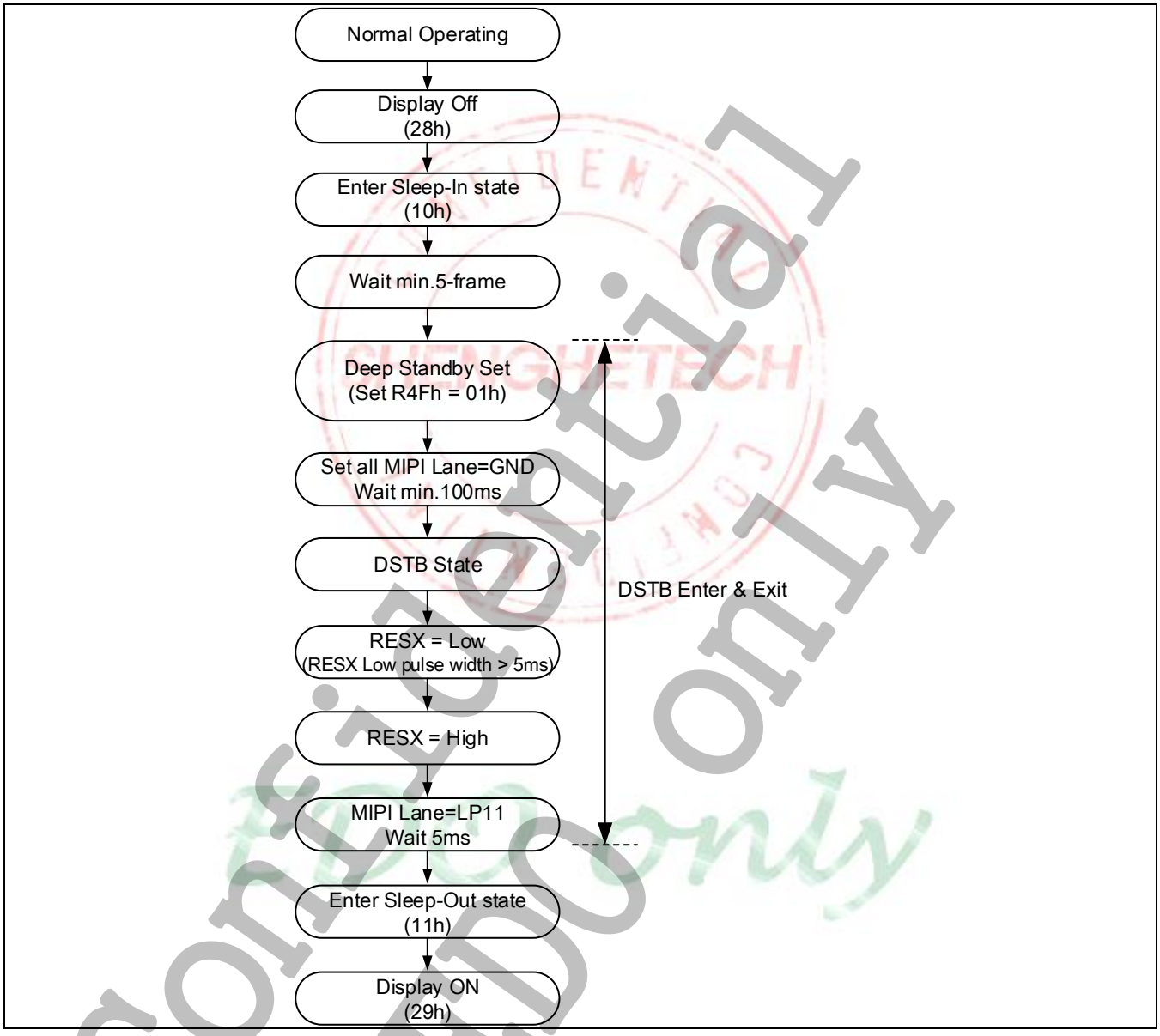

Figure 20 Flow Chart of Deep Standby Mode

NOTE: For MIPI IF, If DSTB mode is used, please set CKP/N, D0P/N state to GND after executing DSTB command.

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3.3.5 Sleep In/Out Flow

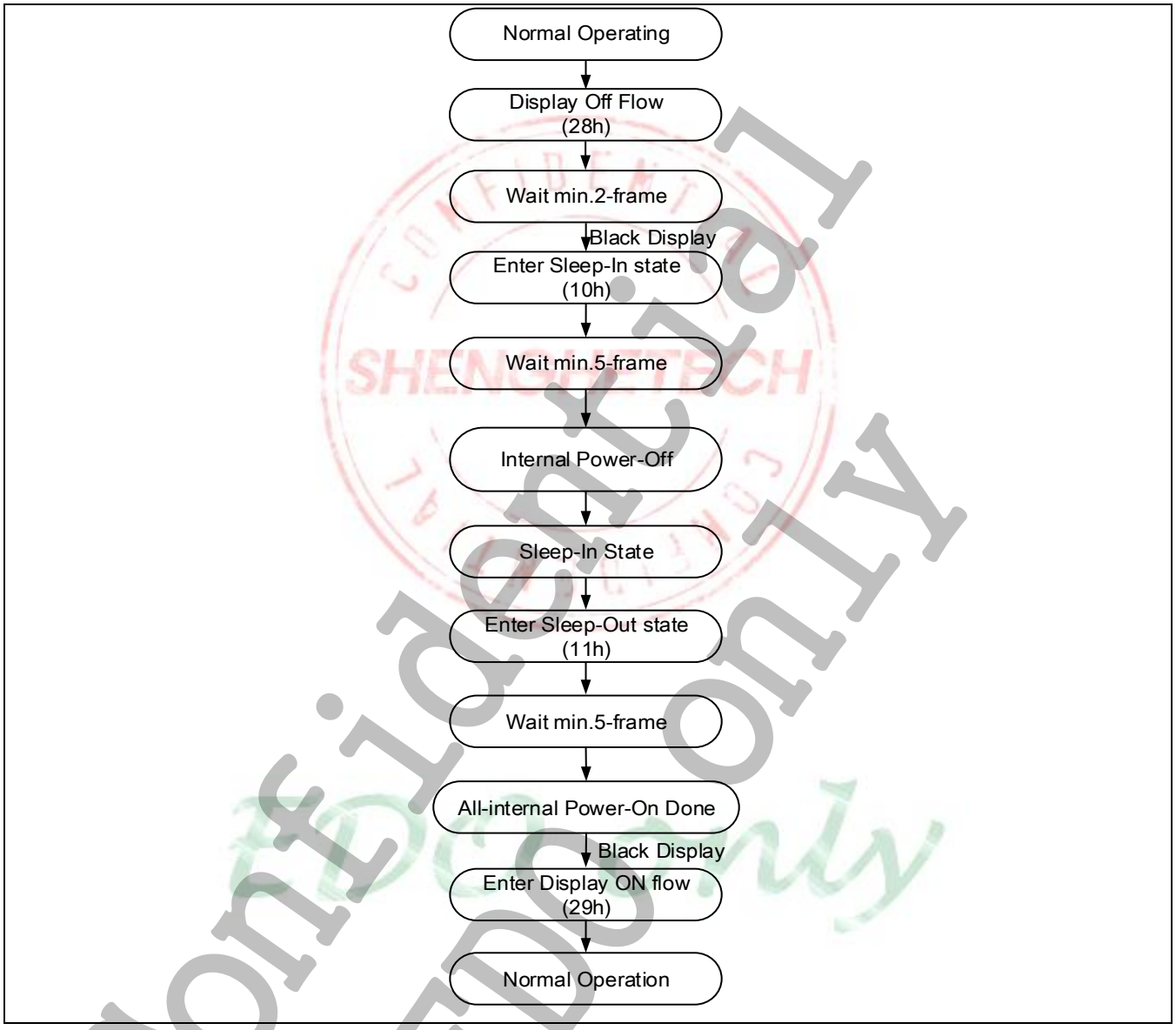

Figure 21 Flow chart of Sleep-In & Sleep-Out Mode

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3.4 Operation Sequence

3.4.1 Display Operating Sequence

The below chart is one of the reference for display operation.

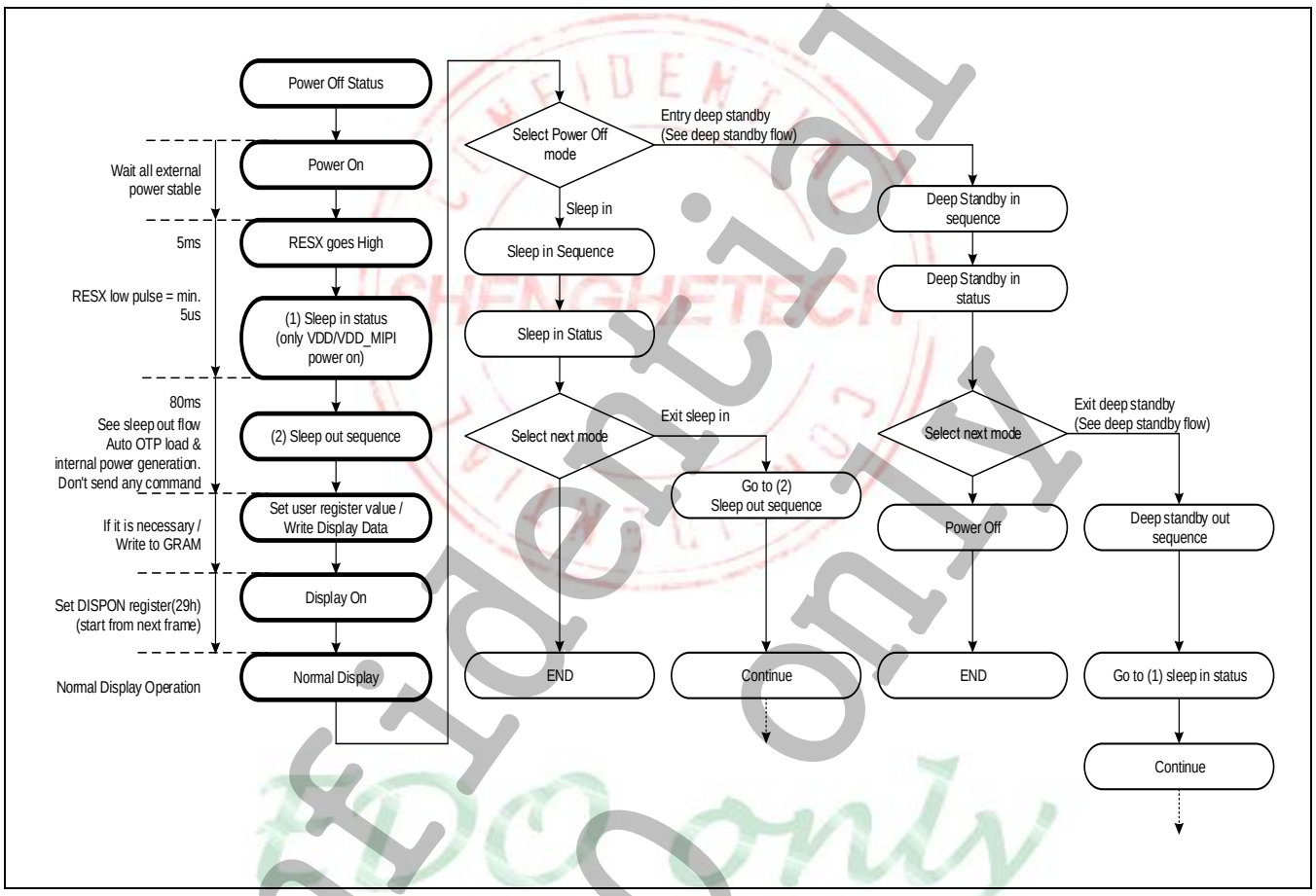

Figure 22 Flow Chart of Display Operation

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3.5 Reset

3.5.1 Register Value

Table 22 The Default Value of the Register – User Command Set

Item	After Power On	After Hardware Reset	After Software Reset
SWRESET(01h)	Off	Off	Off
RDDIDIF(04h)	OTP value	OTP value	OTP value
RDNUMED(05h)	00h	00h	00h
RDDPM(0Ah)	08h	08h	08h
RDDMADCTL(0Bh)	00h	00h	00h
RDDCOLMOD(0Ch)	77h	77h	77h
RDDIM(0Dh)	00h	00h	00h
RDDSM(0Eh)	00h	00h	00h
RDDSDR(0Fh)	00h	00h	00h
SLPIN(10h) / SLPOUT(11h)	SLPIN	SLPIN	SLPIN
PTLON(12h)	Off	Off	Off
NORON(13h)	On	On	On
INVOFF(20h) / INVON(21h)	Off / Off	Off / Off	Off / Off
ALLOFF(22h) / ALLON(23h)	Off / Off	Off / Off	Off / Off
DISPOFF(28h) / DISPON(29h)	Off / Off	Off / Off	Off / Off
CASET(2Ah) : SC/EC	0000h/01DFh	0000h/01DFh	0000h/01DFh
PASET(2Bh) : SP/EP	0000h/01DFh	0000h/01DFh	0000h/01DFh
RAMWR(2Ch)	Contents of memory is set randomly	Contents of memory is set randomly	Contents of memory is set randomly
PTLAR(30h) : PSR / PER	0000h / 01DFh	0000h / 01DFh	0000h / 01DFh
PTLAC(31h) : PSC / PEC	0000h / 01DFh	0000h / 01DFh	0000h / 01DFh
TEOFF(34h) / TEON(35h)	Off / Off	Off / Off	Off / Off
Tearing Line Mode (35h)	00h	00h	00h
MADCTL (36h)	00h	00h	00h
IDMOFF(38h) / IDMON(39h)	Off / Off	Off / Off	Off / Off
COLMOD(3Ah)	77h	77h	77h
RAMWRC(3Ch)	Contents of memory is set randomly	Contents of memory is set randomly	Contents of memory is set randomly
TESCAN(44h) / RDSCL(45h)	0000h / 0000h	0000h / 0000h	0000h / 0000h
SPIRDON(46h) / SPIRDOFF(47h)	Off / Off	Off / Off	Off / Off
AOD_WRDISBV(4Ah)	00FFh	00FFh	00FFh
AOD_RDDISBV(4Bh)	00FFh	00FFh	00FFh
Deep Standby Control(4Fh)	Off	Off	Off
WRDISBV(51h)	00FFh	00FFh	00FFh
RDDISBV(52h)	00FFh	00FFh	00FFh

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Item	After Power On	After Hardware Reset	After Software Reset
WRCTRLD1(53h)	28h	28h	28h
RDCTRLD1(54h)	28h	28h	28h
WRCTRLD2(55h)	00h	00h	00h
RDCTRLD2(56h)	00h	00h	00h
WR_CE(58h)	00h	00h	00h
RD_CE(59h)	00h	00h	00h
HBM_WRDISBV(63h)	00FFh	00FFh	00FFh
HBM_RDDISBV(64h)	00FFh	00FFh	00FFh
HBMCTRL(66h)	10h	10h	10h
RDDDBS(A1h)	(OTP values)	(OTP values)	(OTP values)
RDDDBC(A8h)	(OTP values)	(OTP values)	(OTP values)
RDFCS(AAh)	00h	00h	00h
RDCCS(AFh)	00h	00h	00h
SPI_MODE(C4h)	00h	00h	00h
RDID1(DAh)	(OTP values)	(OTP values)	(OTP values)
RDID2(DBh)	(OTP values)	(OTP values)	(OTP values)
RDID3(DCh)	(OTP values)	(OTP values)	(OTP values)

NOTE: There will be no abnormal visible effects on the display when S/W or H/W Reset is applied. Internal PoR (Power-on Reset) circuit generates a reset signal within 1ms after VDDI and VCI rise up to 90% of their typical value. It is necessary to wait 5msec after Power-on reset before sending commands. this is to allow time for OTP loading.

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3.6 Modules Input/output/Bi-direction (I/O) PADs

3.6.1 Output or Bi-directional (I/O) PADs

Table 23 Reset States of Output and Bi-direction PADs

Output or Bi-directional PADs	When RESX is Low	After Power On	After Hardware Reset	After Software Reset
D0P	High-Z	High-Z	High-Z	High-Z
D0N	High-Z	High-Z	High-Z	High-Z
SDI_RDX	High-Z	High-Z	High-Z	High-Z
SDO_SDI1	Low	Low	Low	Low
SDI2	Low	Low	Low	Low
SDI3	Low	Low	Low	Low
DB[7:0]	Low	Low	Low	Low
ERR_FG	Low	Low	Low	Low
EL_CTRL	Low	Low	Low	Low
TE	Low	Low	Low	Low

NOTE: There will be no output from TE during power on/off sequence, hardware reset and software reset

3.6.2 Input PADs

Table 24 Reset States of Input PADs

Input PADs	When RESX is Low	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	–	See Section	Input valid	Input valid	Input valid	See Section
CKP	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input invalid
CKN	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input invalid
CSX	High	High	High	High	High	High
DCX	High	High	High	High	High	High
SCL_WRX	High	High	High	High	High	High

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3.7 OTP (One-Time Programmable Memory) Control

3.7.1 Structure of OTP

SH8601A has three separated independent OTP area
For Module control of manufacturer. It has 3 register sectors and Manufacturer can write each sector at a time.
User must follow a recommended OTP Program sequence of IC manufacturer's given.

3.7.2 OTP Control Function

Refer the command description for OTP Control (0xD0).

3.7.3 OTP Program Sequence

To program registers, refer following program sequence.

- pre-register setting
- supply VOTP power=6.0V(Typ.)
- set OTP program command bit in 0xD0
  - Set MCS_PROG_EN=1 and wait more than 560msec

    Note: *waiting time is considered at 22MHz OSC clock cycle. Please contact SHT for how long your system needed the waiting time.*
- reset OTP program command bit MCS_PROG_EN=0
- remove VOTP power
- Check programming error: after programming SH8601A checks program error by comparing OTP cell data and mapped register values. Do read CFh 3rd para and follow below instruction.

  CFh 3rd para PRE_ERR_0=0 & PRE_ERR_1=0 → OTP writing is success
  CFh 3rd para PRE_ERR_0=0 & PRE_ERR_1=1 → need OTP rewriting
  CFh 3rd para PRE_ERR_0=1 → OTP rewriting is impossible(No more use IC)

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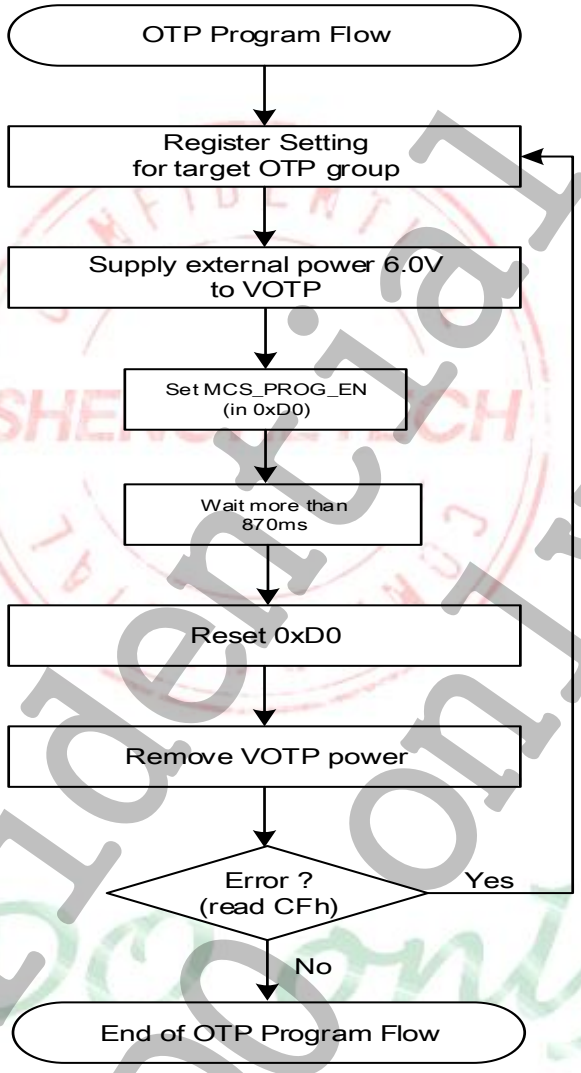

Figure 23 OTP Program Flow

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4 Interface

Terminology used in this section

- Mobile Industry Processor Interface(MIPI): MIPI Alliance has defined DBI, DSI, and D-PHY
- Display Bus Interface(DBI): Type-B 8-bit / Type-C Option1 SPI3W/ Option3 SPI4W
- Dual mode in SPI3W and SPI4W (register option)
- Quad SPI: Quad serial interface
- DSI: Display serial interface. DSI is usually called as MIPI
- D-PHY: Physical layer

4.1 Interface Type Selection

Interface type is decided by input IM[2:0].

Table 25 Interface Type Selection

IM[2:0]	Command Interface	Display Data Interface
000	SPI 3-wire / MIPI	SPI 3-wire / MIPI
001	SPI 4-wire / MIPI	SPI 4-wire / MIPI
010	Quad SPI / MIPI	Quad SPI / MIPI
011, 100	MPU 8-bit	MPU 8-bit
101	SPI 3-wire	SPI 3-wire
110	SPI 4-wire	SPI 4-wire
111	MIPI	MIPI

In-Out pad mapping for each interface mode is shown below.

MPU I/F

Table 26 MPU Interface PAD Assignment

PAD name	IO	DBI Type-B (80-series 8bit MPU)		
		Signal Name	IO	Description
CSX	I	CSX	I	Chip selection, Active Low
SCL_WRX	I	WRX	I	Write clock, Rising edge
DCX	I	DCX	I	0:Command, 1:Data
SDI_RDX	IO	RDX	I	Read clock, Falling edge
DB[7:0]	IO	DB	IO	Bi-direction data bus

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SPI 3-Wire

Table 27 SPI 3-Wire PAD Assignment

PAD name	IO	DBI Type-C – SPI 3-wire			DBI Type-C – SPI 3-wire Dual		
		Signal Name	IO	Description	Signal name	IO	Description
CSX	I	CSX	I	Chip selection, Active Low	CSX	I	Chip selection, Active Low
SCL_WRX	I	SCL	I	SPI clock, Rising edge	SCL	I	SPI clock, Rising edge
SDI_RDX	IO	SDA	IO	Serial Data in-out or	SDIO	IO	Serial Data in 0, Data out
		SDI	I	Serial Data input			
SDO_SDI1	IO	SDO	O	Serial Data output	SDI1	I	Serial Data in 1

SPI 4-Wire

Table 28 SPI 4-Wire PAD Assignment

PAD name	IO	DBI Type-C – SPI 4-wire			DBI Type-C – SPI 4-wire Dual		
		Signal Name	IO	Description	Signal name	IO	Description
CSX	I	CSX	I	Chip selection, Active Low	CSX	I	Chip selection, Active Low
SCL_WRX	I	SCL	I	SPI clock, Rising edge	SCL	I	SPI clock, Rising edge
DCX	I	DCX	I	0:Command, 1:Data	DCX	I	0:Command, 1:Data
SDI_RDX	IO	SDA	IO	Serial Data in-out or	SDIO	IO	Serial Data in 0, Data out
		SDI	I	Serial Data input			
SDO_SDI1	IO	SDO	O	Serial Data output	SDI1	I	Serial Data in 1

QUAD SPI

Table 29 Quad SPI PAD Assignment

PAD name	IO	DBI Type-B (80-series 8bit MPU)		
		Signal Name	IO	Description
CSX	I	CSX	I	Chip selection, Active Low
SCL_WRX	I	SCL	I	Serial clock, Rising edge
SDI_RDX	IO	SDIO	IO	Serial Data in 0, Data out
SDO_SDI1	IO	SDI1	I	Serial Data input 1
SDI2	IO	SDI2	I	Serial Data input 2
SDI3	IO	SDI3	I	Serial Data input 3

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4.2 MIPI DBI Type-B and Type-C Interface Configuration

SH8601A driver IC supports parallel interface DBI Type-B. 8bits data transmitted from Host to SH8601A driver IC. And supports serial interface DBI Type-C (Option1 and Option3). 8/9bits data transmitted from Host to SH8601A driver IC. It is possible to suspend data transfer if the Chip select(CSX) and clock signal (WRX or SCL) are held in their current state until data transfer can resume. Host can read SH8601A register value from DB[7:0] or SDIA(or SDO) output. Also SH8601A can support Quad SPI mode.

4.3 MIPI DBI Interface Data Transfer Ignore and Pause

SH8601A stores the command/parameters into the register file. The command and parameters transferred from Host Application processor (AP) to SH8601A are stored in the register file of SH8601A before transmission break occurred. e.g.) such as CSX to “High” during data transmission. If transmission break is occurred before the last parameter is transmitted, only the last transmitted parameters are stored. If a new command is transferred before the last parameter is done, SH8601A begins to store a new parameter. And previous left parameters are ignored even they are resent. SH8601A does not support data transmission pause operation during Write/Read sequence.

4.4 MIPI DBI Type-B (MPU 8bit) Interface

In MIPI DBI Type-B interface, SH8601A supports 8-bit interface mode. Register write-read timing diagram is shown below. Using this mode, user also can send RGB image data with command 0x2C and 0x3C.

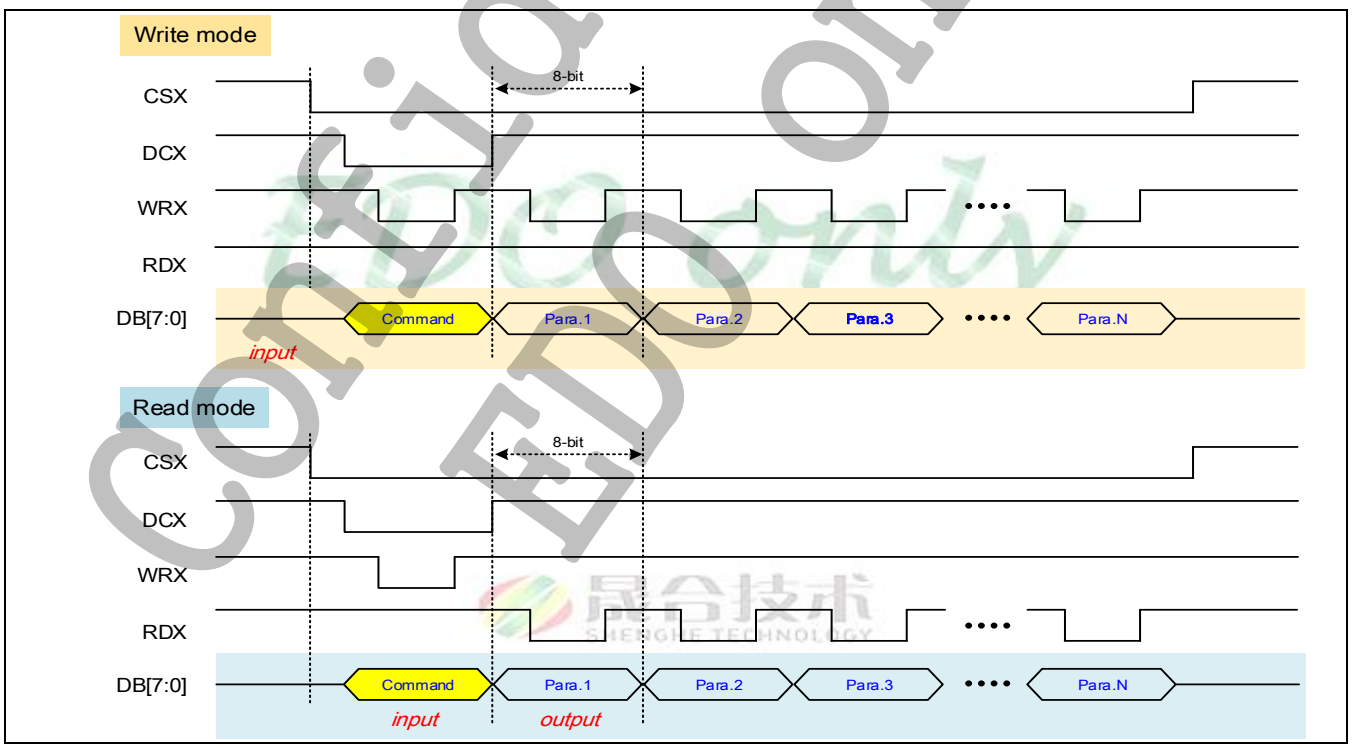

Figure 24 MPU 8-bit Interface Protocol – Register Read and Write

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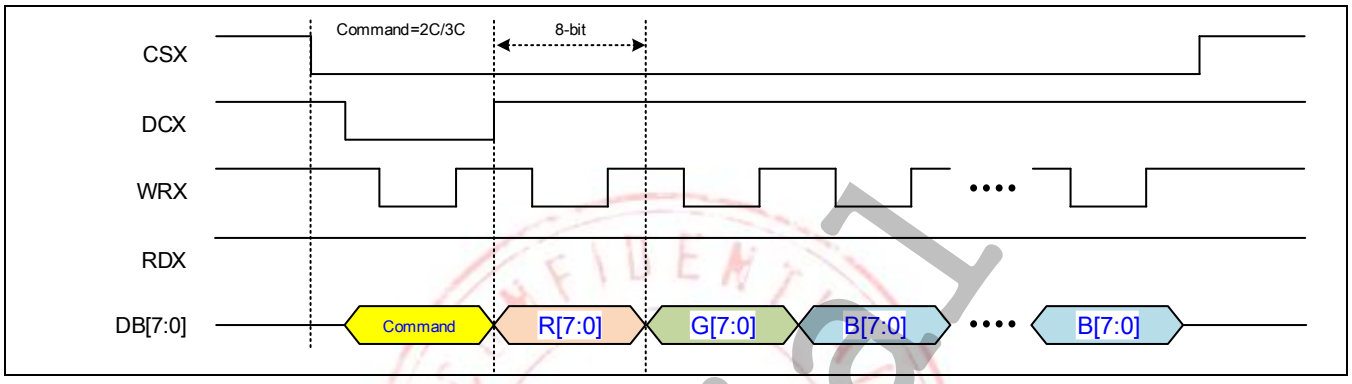

Figure 25 MPU 8-bit Interface – Pixel Interface

4.5 MIPI DBI Type-C (3-Wire 9-Bit) Interface

This serial interface is MIPI DBI Type-C (3-wire 9-bit) bi-directional interface for communication between the Host Application Processor (AP) and the SH8601A. CSX, SCL, SDIO (or SDI, SDO) are used for interface with AP only, so it can be stopped when communication is not necessary. In read protocol, SDIO or SDI+SDO condition is decided by register SDIO_MODE setting in command SPI_MODE(C4h). UCS read is divided into 8 bit para mode and 24 bit para mode. MCS read is the same as the 24 bit para mode of UCS, but SPI READ should be set to '1' with the command SPI_RDON (47h). SPI_READ must be reset to '0' with the command SPI_RDOFF (46h).

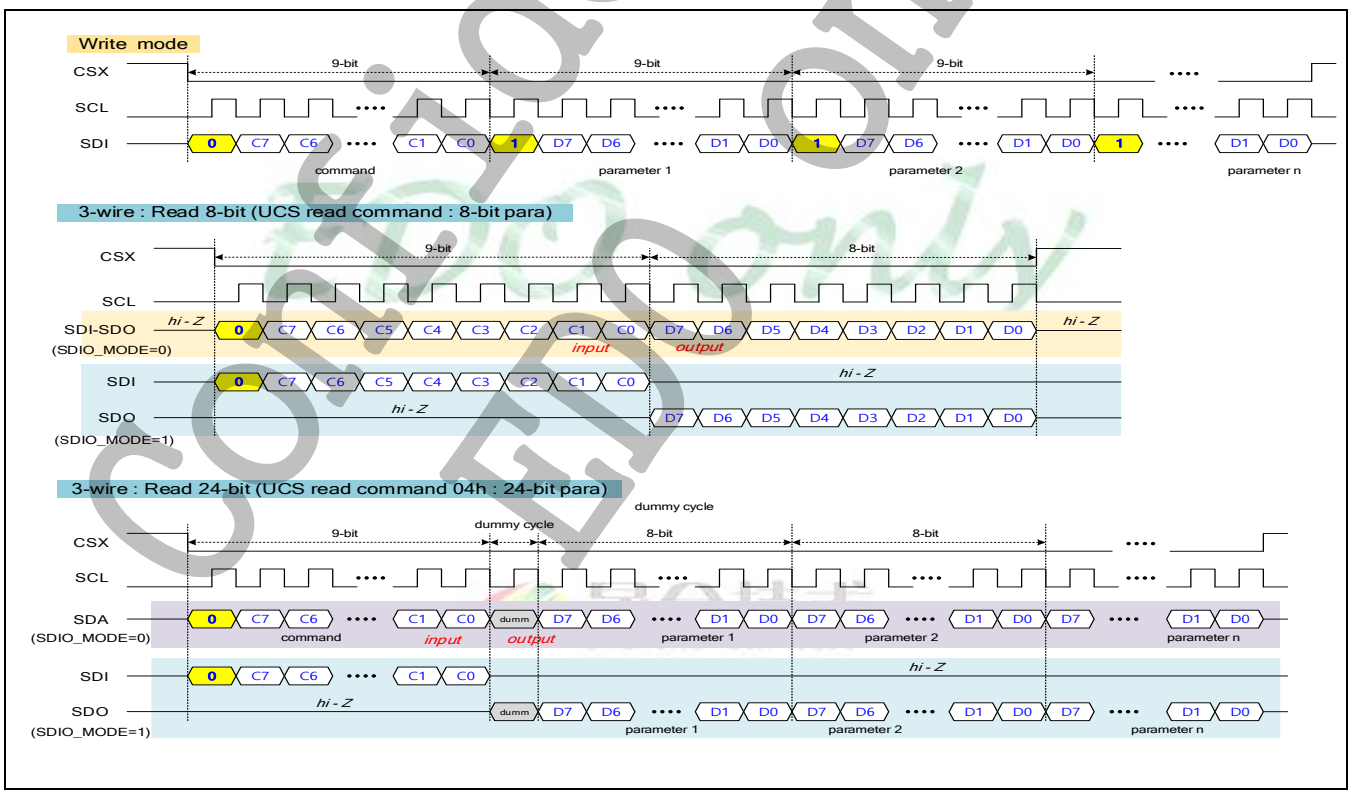

Figure 26 MIPI DBI Type-C Interface – Register Write and Read

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4.6 MIPI DBI Type-C (4-Wire 8-Bit) Interface

This serial interface is MIPI DBI Type-C (4-wire 8-bit) bi-directional interface for communication between the Host Application Processor (AP) and the SH8601A. CSX, DCX, SCL, SDIO (or SDI, SDO) are used for interface with AP only, so it can be stopped when communication is not necessary. In read protocol, SDIO or SDI+SDO condition is decided by register SDIO_MODE setting in command SPI_MODE(C4h). UCS read is divided into 8 bit para mode and 24 bit para mode. MCS read is the same as the 24 bit para mode of UCS, but SPI READ should be set to '1' with the command SPI_RDON (47h). SPI_READ must be reset to '0' with the command SPI_RDOFF (46h).

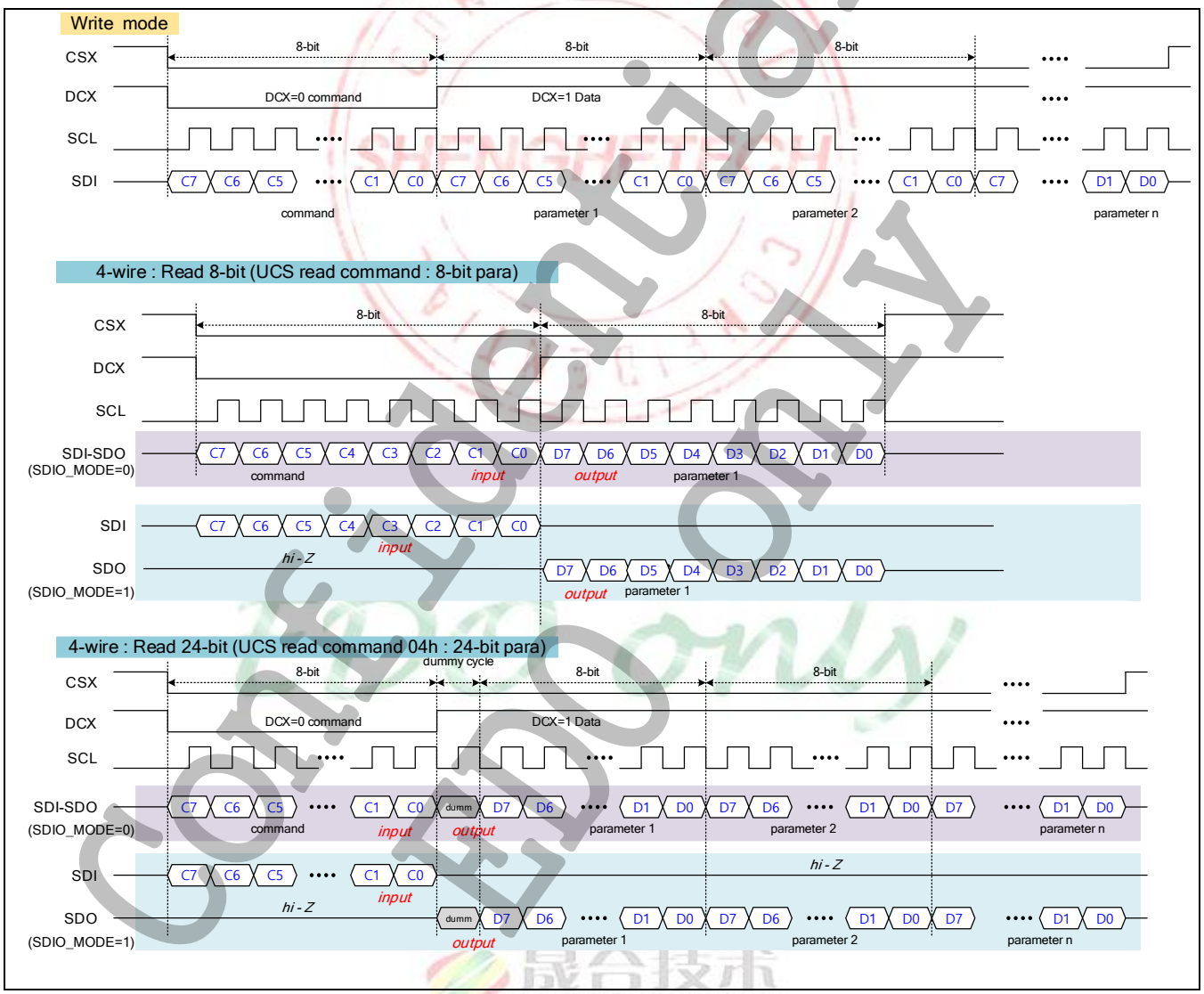

Figure 27 MIPI DBI Type-C (4-Wire 8-Bit) Interface Protocol – Register Write and Read

4.7 Dual SPI Interface

This interface is optional for SPI 3-wire and SPI 4- wire to send RGB image data. All of RGB image transfer formats are explained below. Transfer types 1P/1T 1 line, 1P/1T 2 line, and 2P/3T 2 line are selected by register

SPI_MODE(C4h).

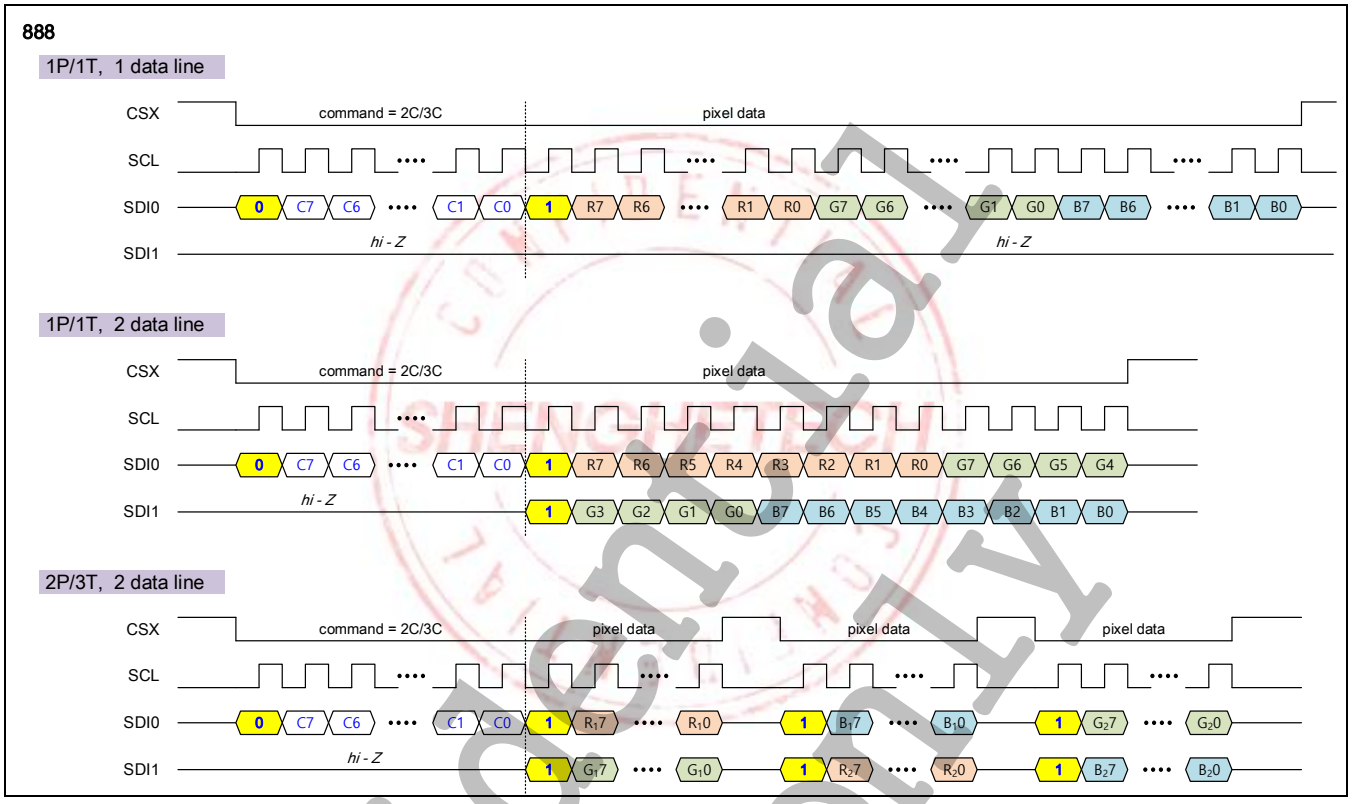

Figure 28 SPI 3-Wire 888 Pixel Format

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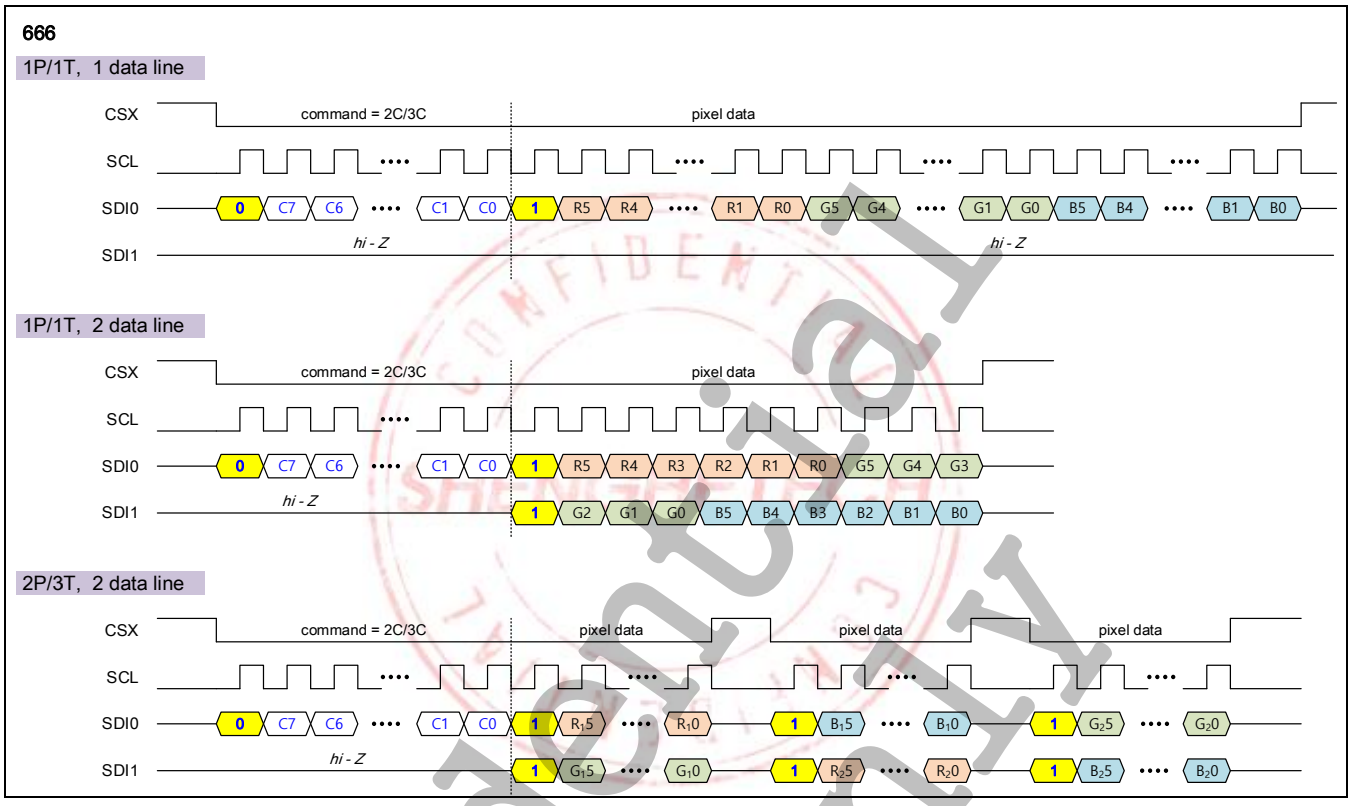

Figure 29 SPI 3-Wire 666 Pixel Format

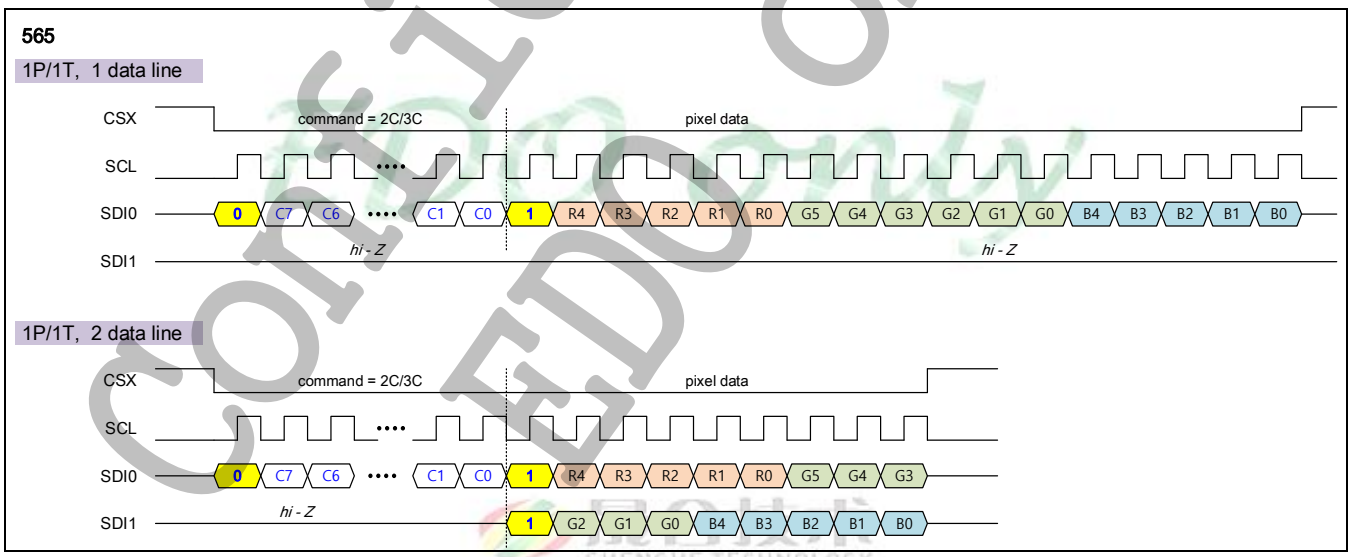

Figure 30 SPI 3-Wire 565 Pixel Format

888

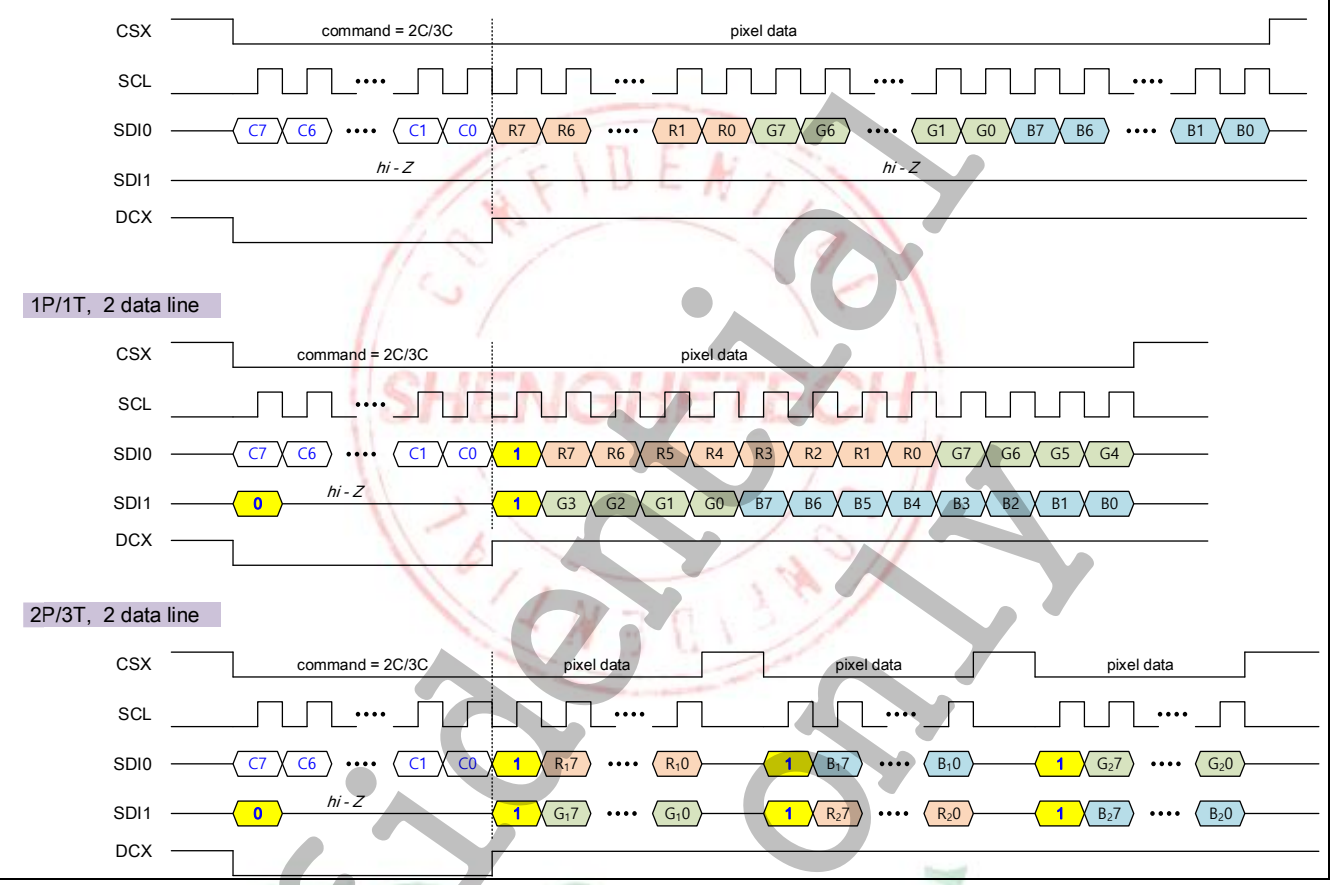

Figure 31 SPI 4-Wire 888 Pixel Format

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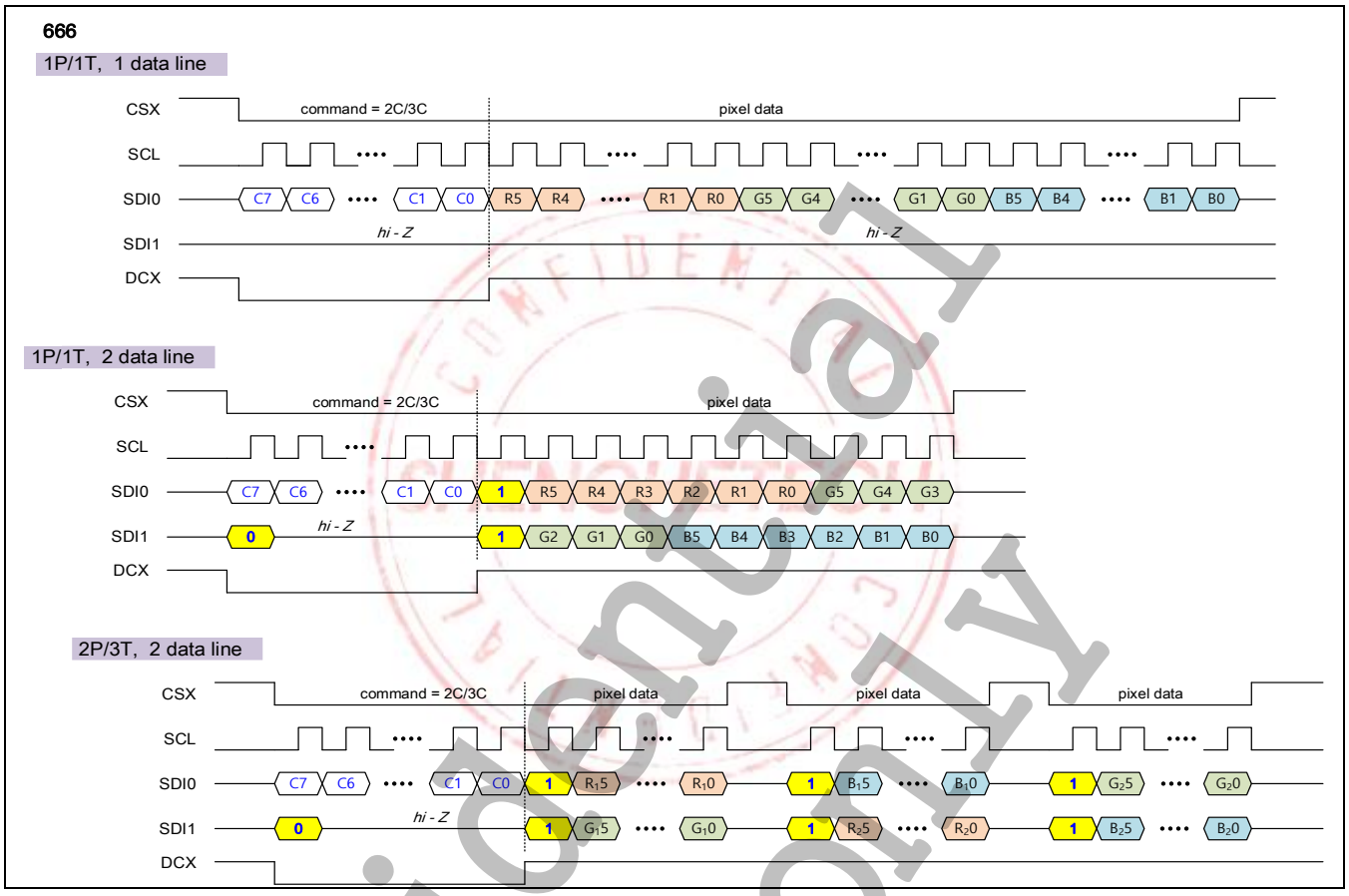

Figure 32 SPI 4-Wire 666 Pixel Format

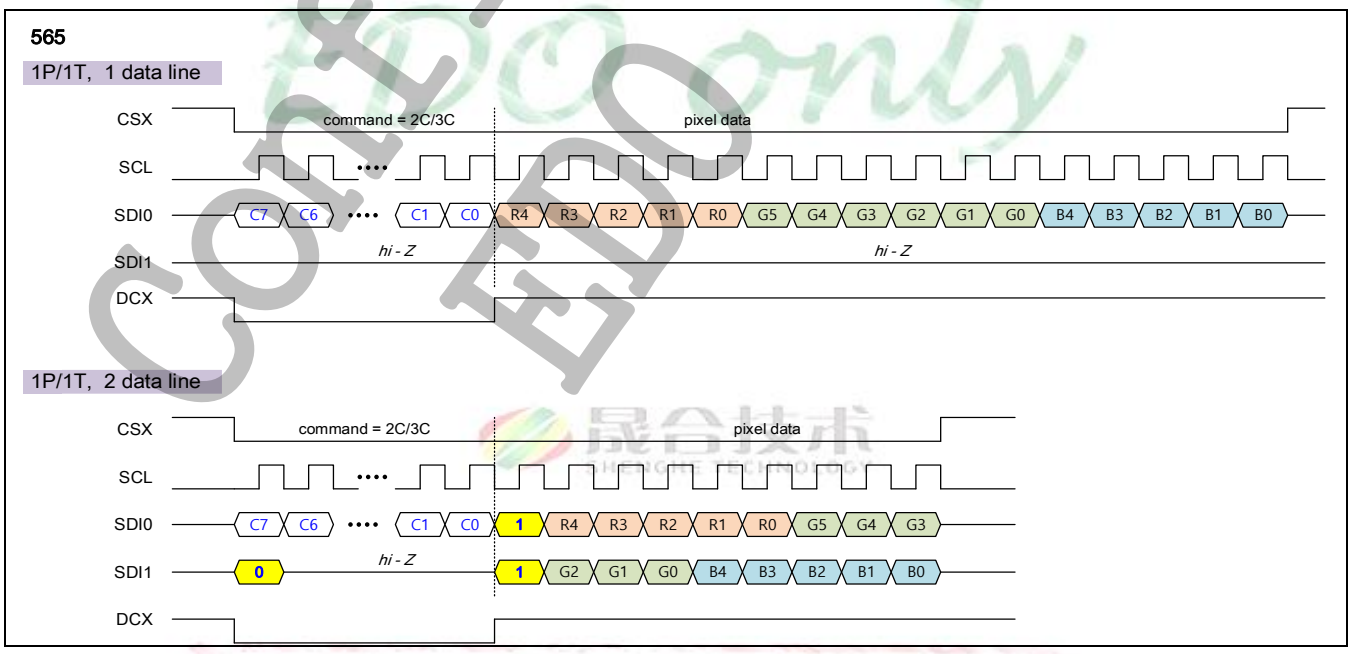

Figure 33 SPI 4-Wire 565 Pixel Format

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4.8 Quad SPI Interface

In addition to MIPI DBI Type-C interface, SH8601A supports Quad-SPI interface. Register read, write interface and RGB pixel interface timing diagrams are shown below. 1-wire or 4-wire option is selected by register SPI_MODE(C4h).

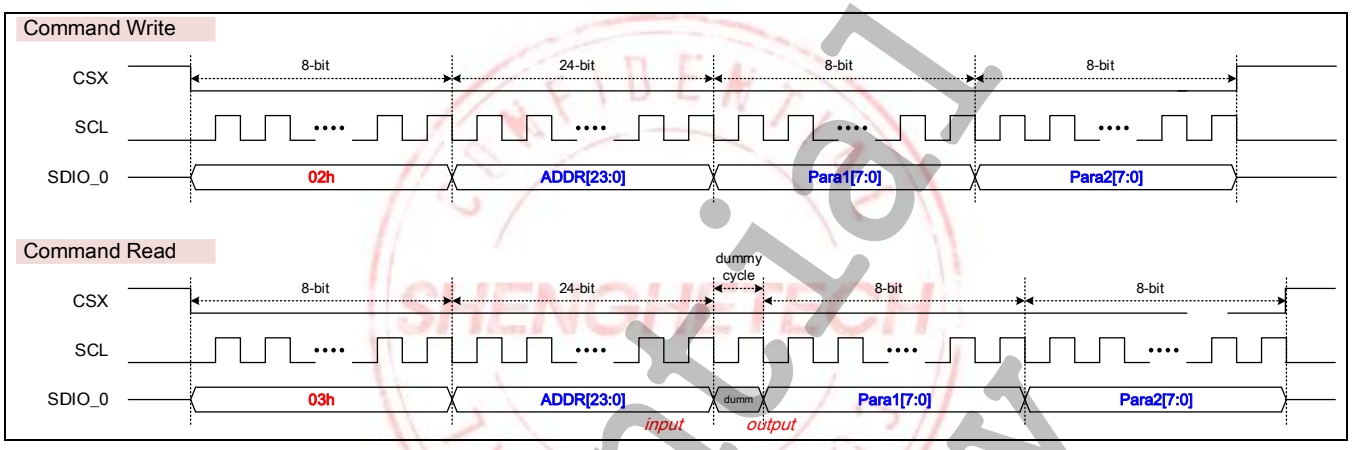

Figure 34 Quad SPI Interface Protocol – Register Read and Write

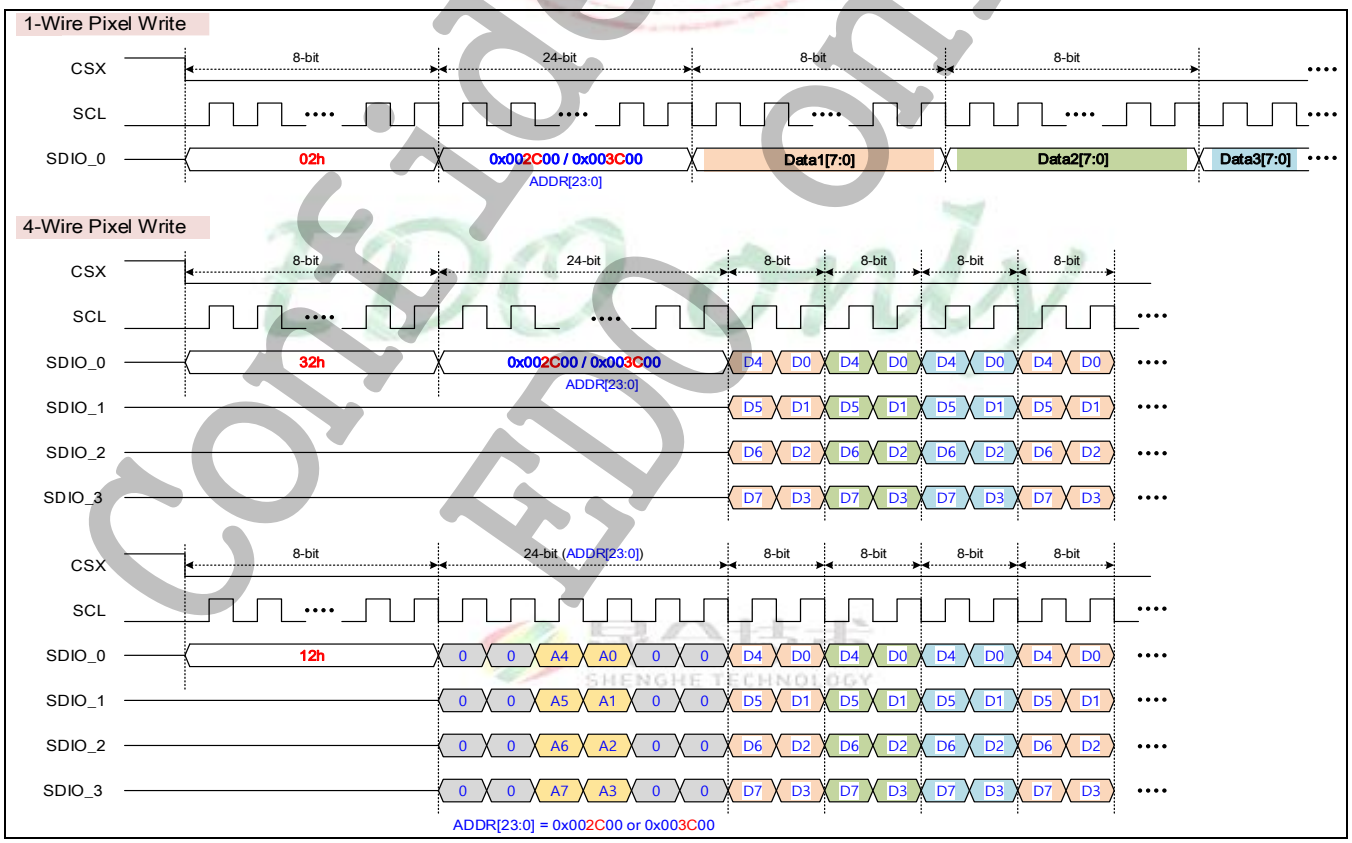

Figure 35 Quad SPI Interface Protocol – Pixel Interface

4.9 Pixel Format for SPI/MPU Interface

SH8601A supports various pixel formats through SPI/MPU interface. Target pixel format is decided by IFPF in COLMOD(0x3A). For 111, 332, and 256-gray pixel formats, SPI/MPU transfer RGB image data using register write command (0x2C or 0x3C), not RGB image interface. 8-bit data format for this interface is shown below. Quad SPI support only 24-bit color format.

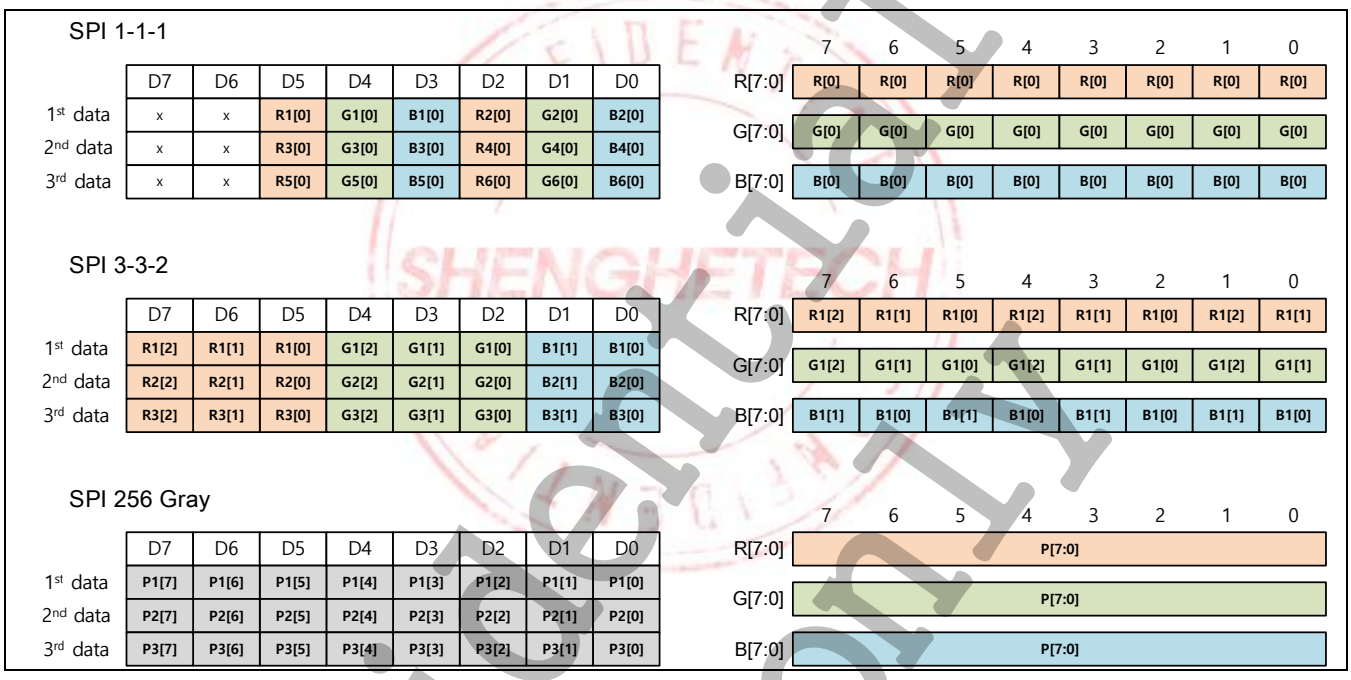

Figure 36 RGB Pixel Format

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4.10 MIPI DSI

MIPI (Mobile Industry Processor Interface) DSI (Display Serial Interface) standard defines protocols between a Host (Application Processor) and Client peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards. It builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-2 and DCS standards. Figure58 shows a simplified DSI interface configuration. From a conceptual viewpoint, a DSI-compliant interface performs the same functions as interfaces based on DBI-2 and DPI-2 standards or similar parallel display interfaces. It sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals. From a system or software point of view, the serialization and deserialization operations should be transparent. The most visible, and unavoidable, consequence of transformation to serial data and back to parallel is increased latency for transactions that require a response from the peripheral. For example, reading a pixel from the frame buffer on a display module has a higher latency using DSI than DBI. Another fundamental difference is the host processor's inability during a read transaction to throttle the rate, or size, of returned data.

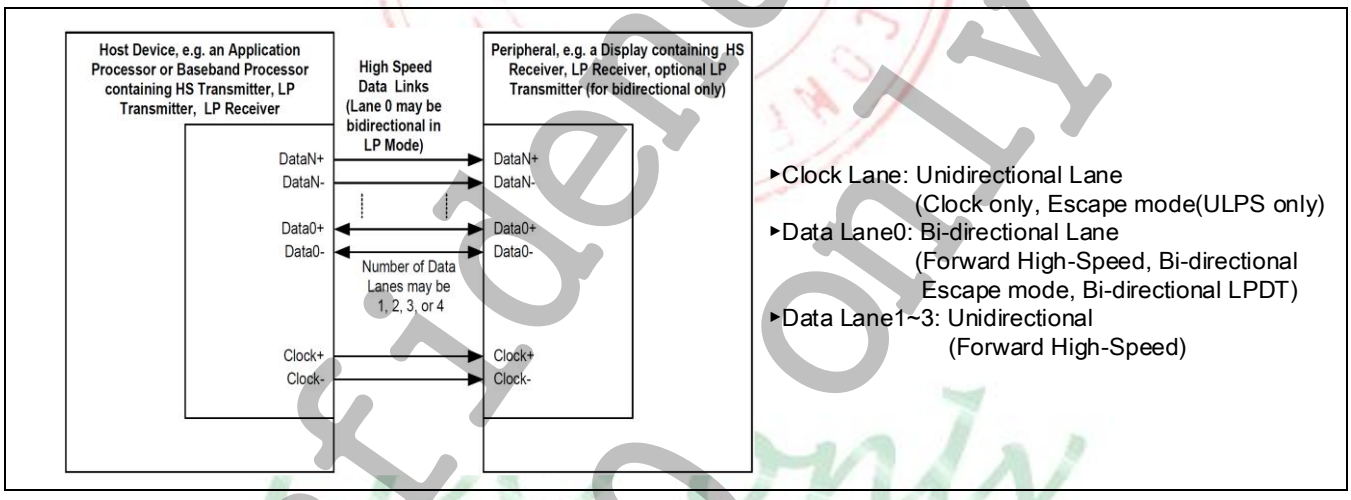

Figure 37 DSI Tx and Rx Interface Configuration

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4.10.1 DSI Feature

- Support One Data lane and Clock lane.
- High speed(HS) transmissions(uni-direction) and Low Power(LP) transmission(bi-direction)
- Clock lane supports ULPS mode
- Support Command and Video mode
- Support Tearing effect (TE) signal
- Diagnostic function - Checksum and ECC error
- Functionality supported by Escape mode
- Packet-Based Protocol

	MIPI Alliance Specification for D-PHY	MIPI Alliance Specification for DSI
Version	1.0	1.02
Date	Sep 22, 2009	Oct 20, 2010

4.10.2 DSI Layer Definitions

A conceptual view of DSI organizes the interface into several functional layers. A description of the layers follows and is also shown in Figure 25 and it consists of 4 types such as Application Layer, Low level protocol Layer, Lane management Layer and PHY Layer.

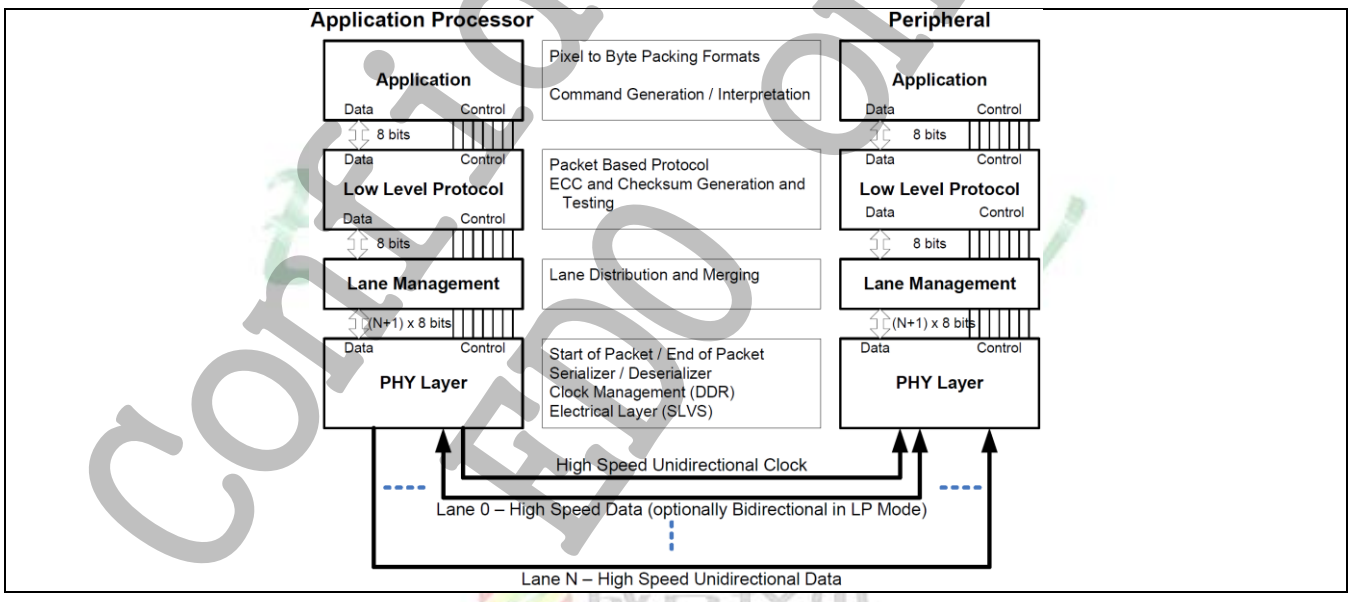

Figure 38 MIPI DSI Layers

4.10.3 Command and Video Mode

DSI-compliant peripherals support either of two basic modes of operation, Command mode and Video mode. The mode used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other

applications. Typically, a peripheral is capable of Command mode operation or Video mode operation. Some Video mode display modules also include a simplified form of Command mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

4.10.4 DSI Physical Layer (D-PHY)

The D-PHY provides a synchronous connection between master and slave. A practical PHY configuration consists of a clock signal and one or more data signals. The clock signal is unidirectional, originating at the master and terminating at the slave. The data signals can be either unidirectional or bi-directional, depending on the selected options. For half-duplex operation, the reverse direction bandwidth is one-fourth of the forward direction bandwidth. Token passing is used to control the communication direction of the link.

4.10.4.1 Lane State Definition

Display module uses data and clock lane differential pairs for DSI. Both differential lane pairs can be driven Low Power(LP) mode or High Speed(HS) mode. The State Codes of the High Speed(HS) mode and Low Power(LP) mode lane pair are defined Table 27. All LP state periods shall be at least T_{LPX} in duration. State transitions shall be smooth and exclude glitch effects. A clock signal can be reconstructed by exclusive-ORing the Dp and Dn Lines.

Table 30 MIPI Lane State Description

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

NOTE:

1. During High-Speed transmission the Low-Power Receivers observe LP-00 on the Lines.
2. If LP-11 occurs during Escape mode the Lane returns to Stop state (Control Mode LP-11)

4.10.4.2 Global Operation Flow Diagram

Below figure shows the operational flow diagram for a Data Lane Mode. Within both Tx and Rx four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround and Initialization.

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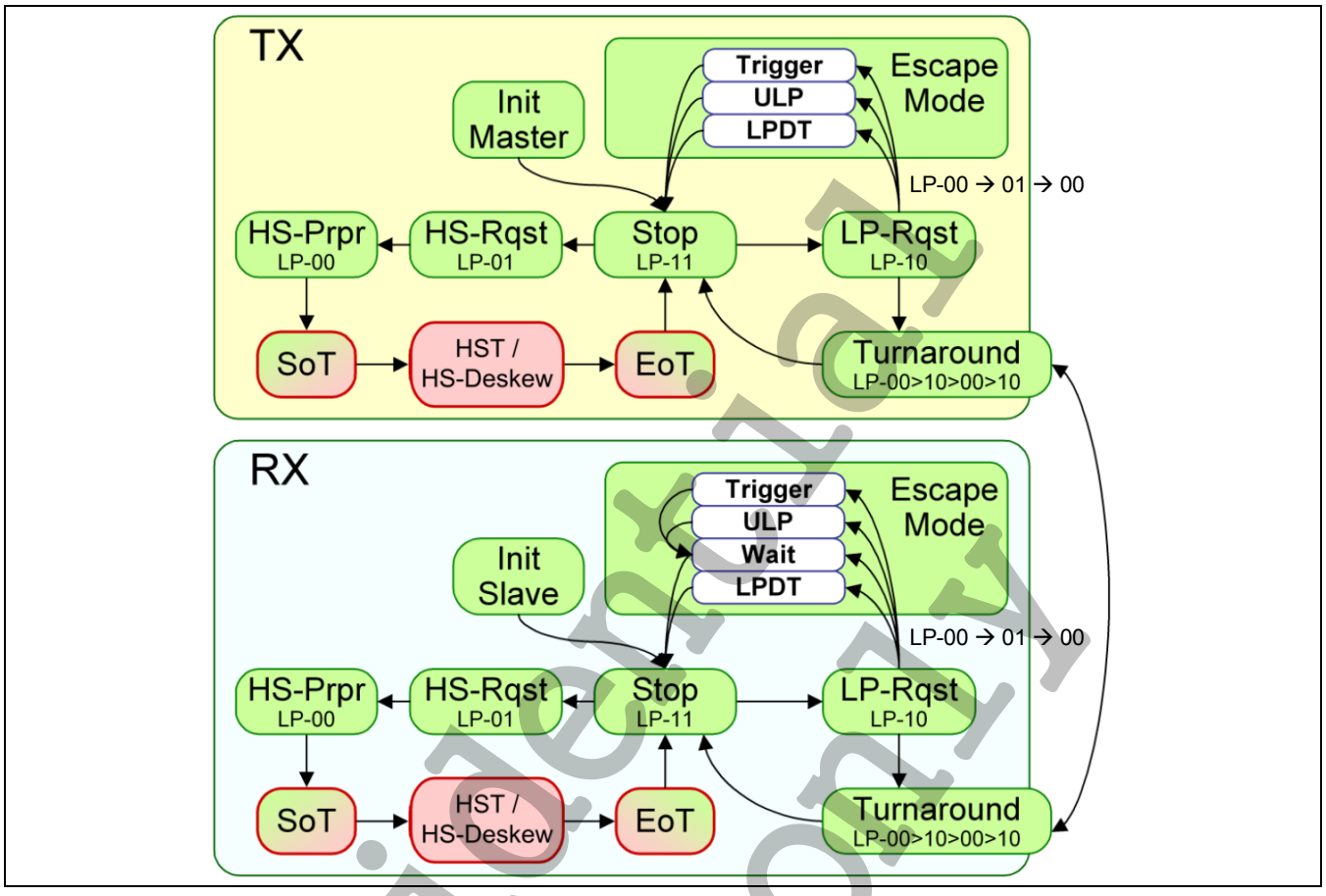

Figure 39 MIPI PHY Data Lane Mode State Diagram

4.10.4.3 Clock Lane Mode State Diagram

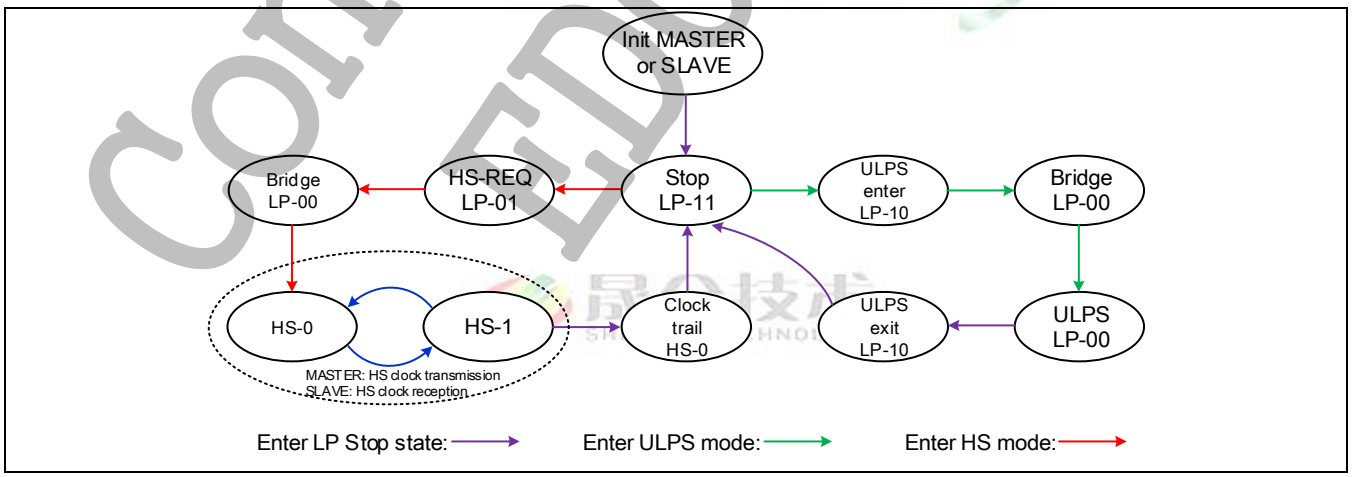

Figure 40 Clock Lane Module State Diagram

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4.10.4.3.1 Clock Lane Switching

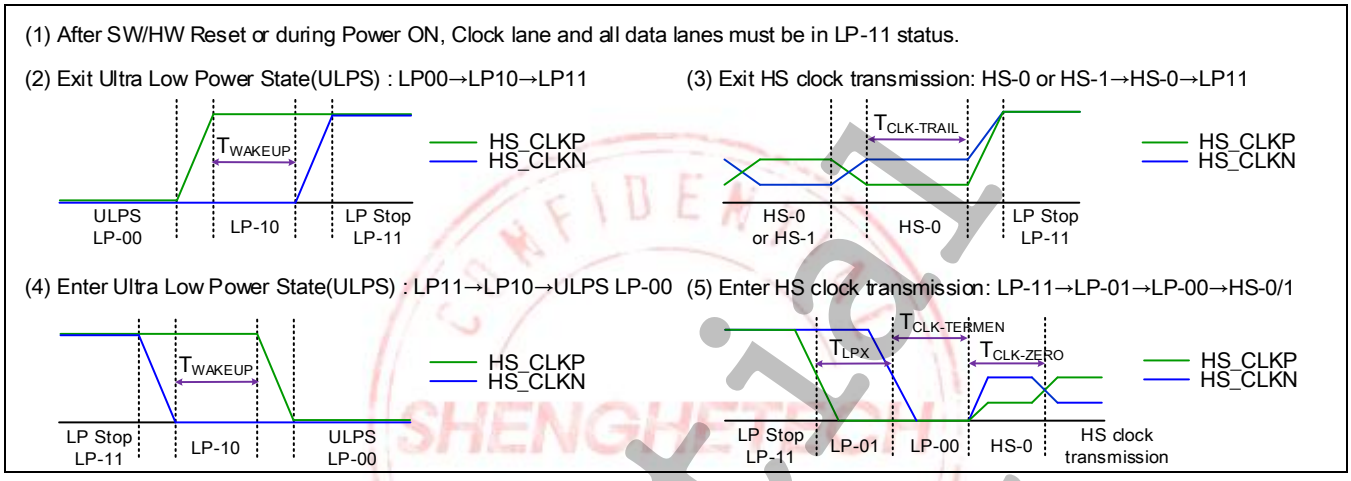

Figure 41 Clock Lane Switching State Diagram

4.10.4.4 HS (High Speed) Data Transmission Burst

The *Figure 42* shows the sequence of events during the transmission of a Data Burst. Transmission can be started and ended independently for any Lane by the protocol. However, for most applications the Lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per Lane.

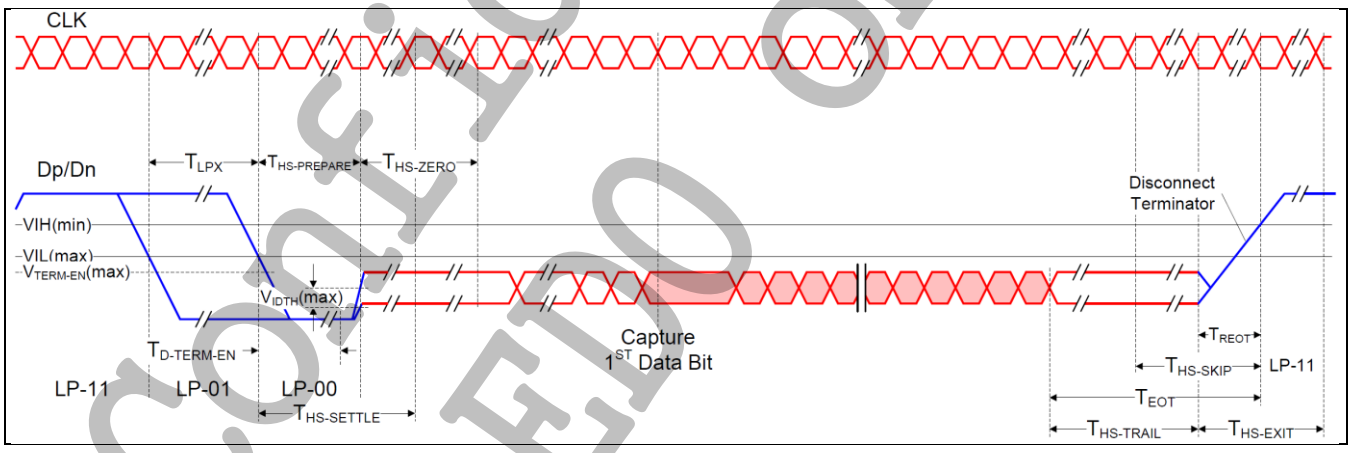

Figure 42 High-Speed Data Transmission in Bursts

4.10.4.5 High Speed Clock Transmission

The *Figure 43* shows the sequence of the high speed clock transmission. In high speed mode the clock lane provides a low-swing differential DDR clock signal from Master to Slave for high speed data transmission.

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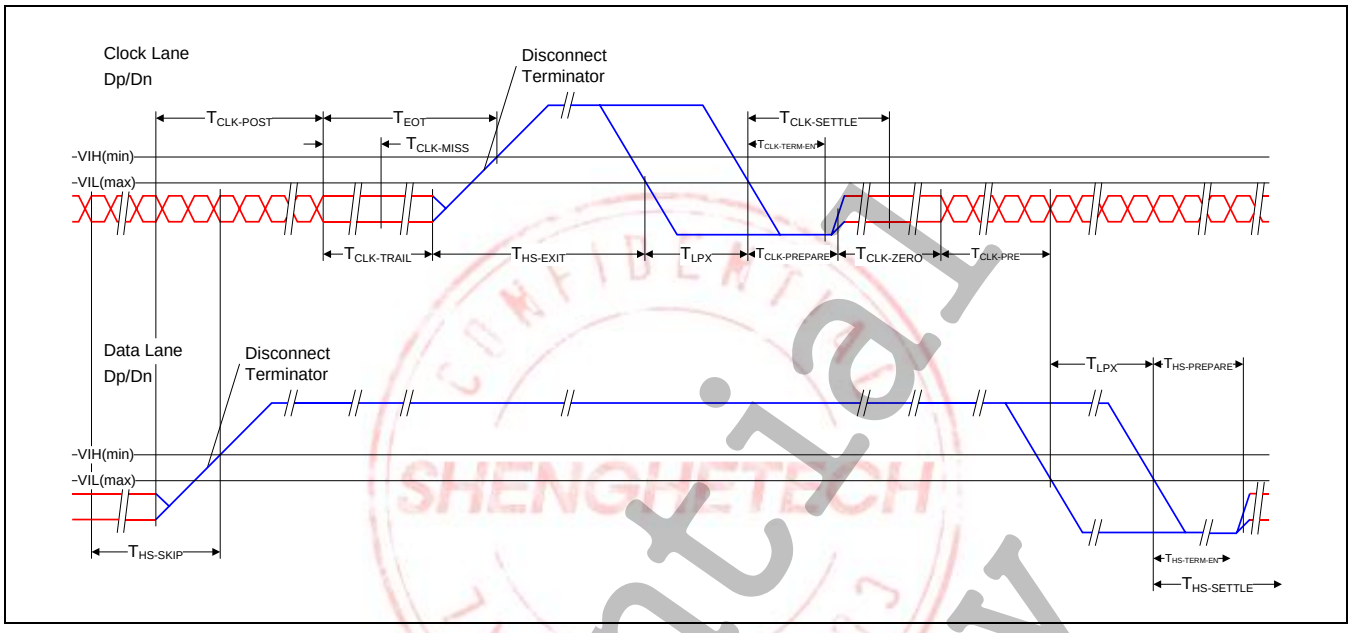

Figure 43 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

4.10.4.6 Bi-Directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. Master and Slave side shall not be changed by Turnaround. Link Turnaround shall be handled completely in Control mode. The low power clock timing for both sides of the Link does not have to be the same, but may differ. However, the ratio between the Low Power State Periods, T_{LPX} is constrained to ensure proper Turnaround behavior. The T_{LPX} (master)/T_{LPX} (slave) shall be between 2/3 (0.667) and 3/2 (1.50). The handshake process for BTA allows only limited mismatch of Escape Mode clock frequencies between a host processor and a peripheral.

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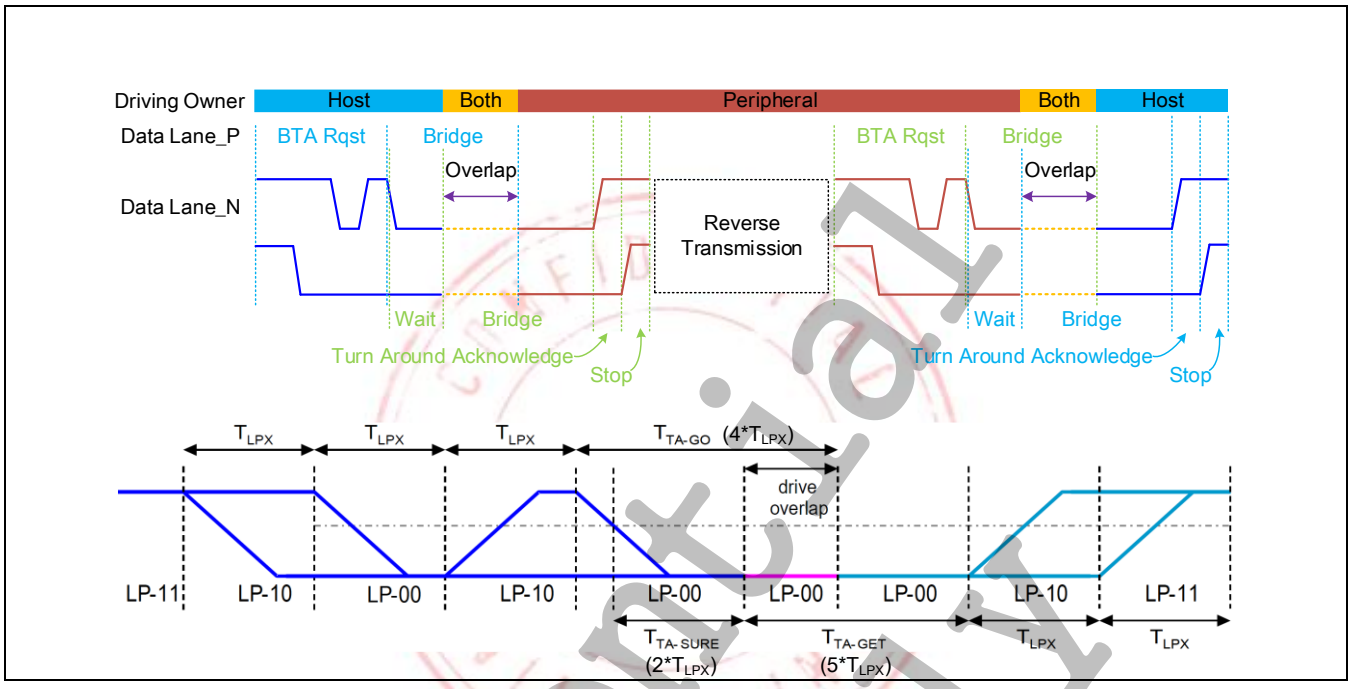

Figure 44 Bus Turn Around procedure

Figure 45 shows an example of BTA operations. The SLAVE get the lane controllability by BTA procedure to send the acknowledge packet on the successful data reception if there is no Error and send the acknowledge with error packet on the data reception if Error is occurred.

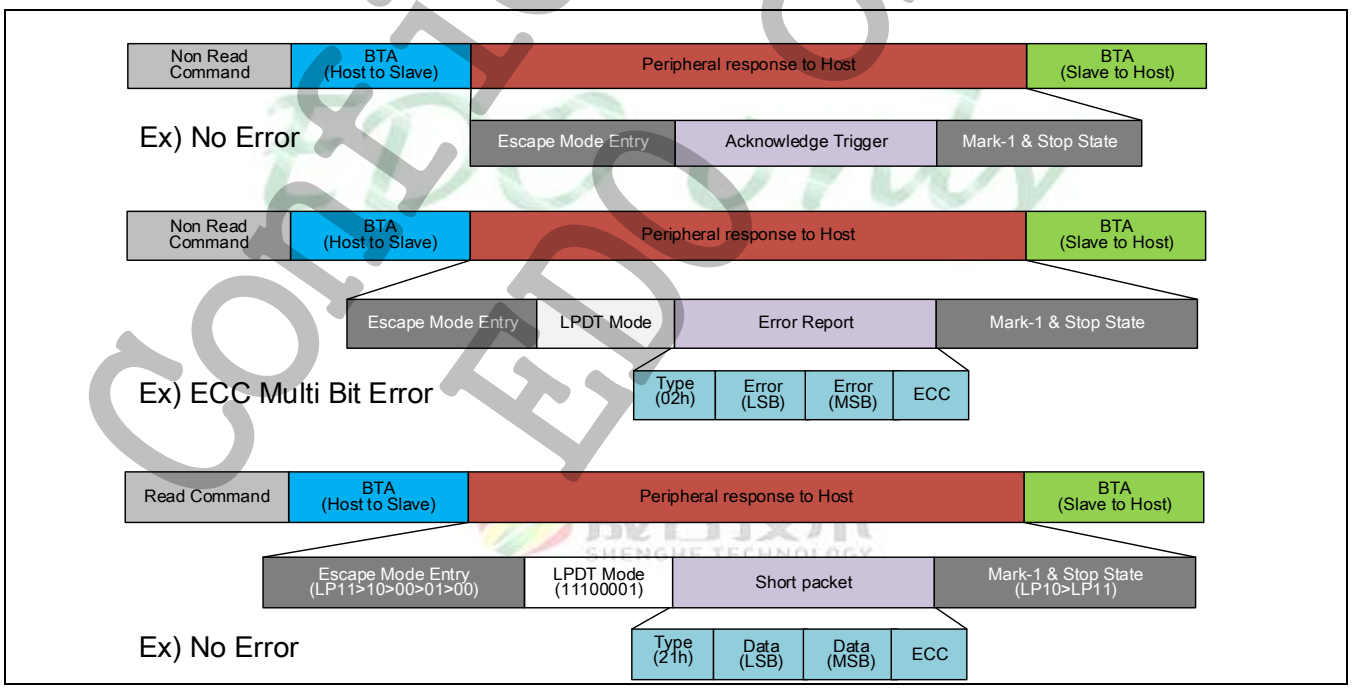

Figure 45 BTA Operation – No Error/Error after Non-Read Command

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4.10.4.7 Escape Mode

Escape Mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and is optional in the Reverse direction. If supported, Escape mode does not have to include all available features. A Data Lane shall enter Escape Mode via an Escape Mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape Mode in Space state (LP-00). If an LP-10 is detected after the first Bridge state or an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape Mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state. Once Escape Mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. Below table lists all currently available Escape Mode commands and actions. All unassigned commands are reserved for future expansion.

Table 31 MIPI Escape Mode Entry Code

Escape Mode Action	Command Type	Entry Command Pattern (First Bit Transmitted to Last Bit Transmitted)	SH8601A	
			LP-Rx	LP-Tx
Low-power data transmission	mode	11100001 (87h)	O	O
Ultra-low power state	mode	00011110 (78h)	O	–
Undefined-1	mode	10011111 (F9h)	–	–
Undefined-2	mode	11011110 (7Bh)	–	–
Reset-trigger (Remote Application)	Trigger	01100010 (46h)	O	–
TE trigger	Trigger	01011101 (BAh)	–	O
Unknown-4 (Acknowledge trigger)	Trigger	00100001 (84h)	–	O
Unknown-5	Trigger	10100000 (05h)	–	–

The complete Escape mode action for a Trigger-Reset command is shown as follows. It shows the sequence of the low power data transmission.

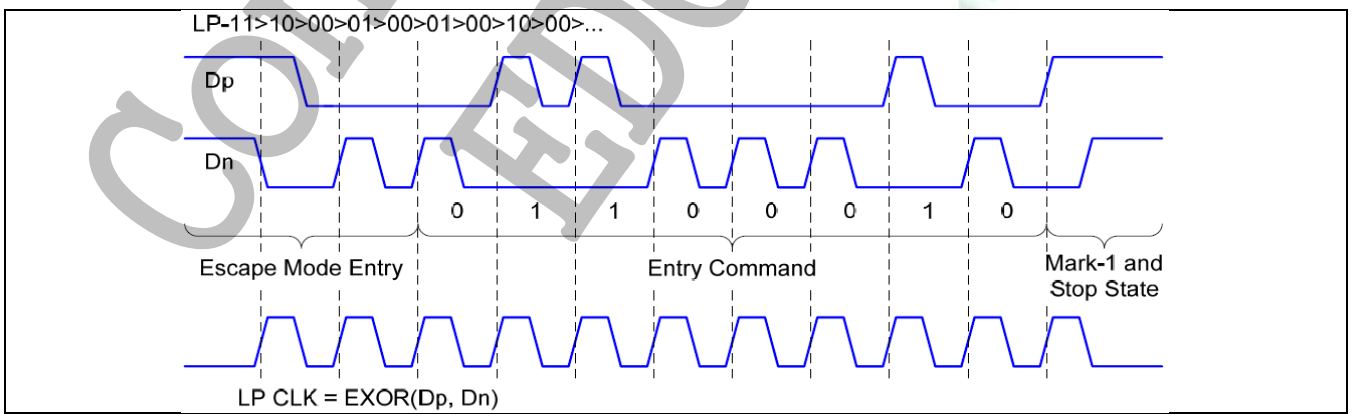

Figure 46 Trigger-Reset Command in Escape Mode

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4.10.4.7.1 Escape mode Low-Power Data Lane Operation

If the Escape Mode Entry procedure is followed-up by the Entry Command for Low-Power Data Transmission (LPDT), Data can be communicated by the protocol at low speed, while the Lane remains in Low-Power mode. The PHY in Escape mode shall apply Spaced-One-Hot bit encoding for asynchronous communication. Therefore, operation of a Data Lane in this mode does not depend on the Clock Lane.

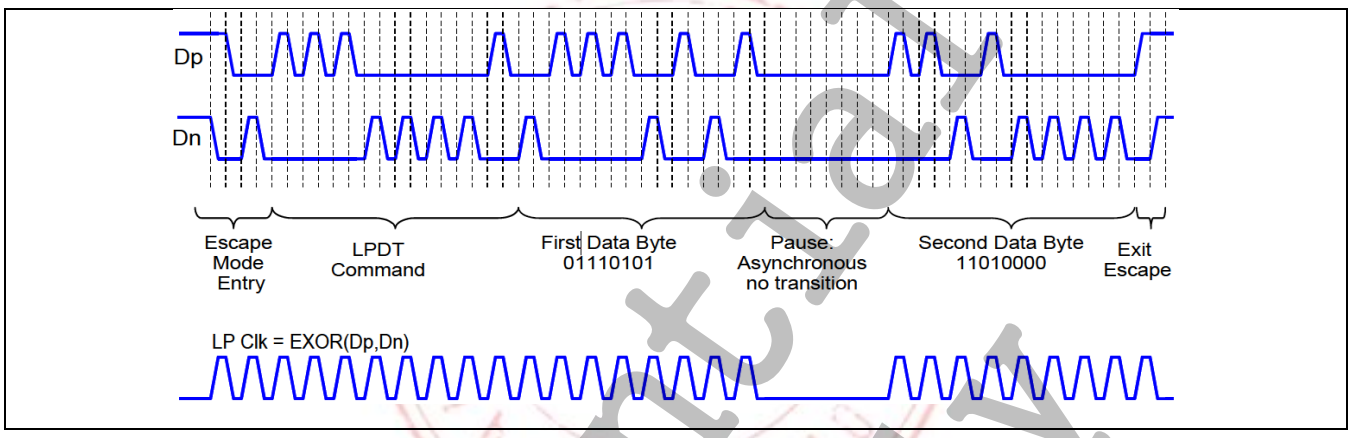

Figure 47 Data Byte Low-Power Data Transmission

4.10.4.7.2 Remote Application Reset

Remote Application Reset Command is used in case of transmission from the host processor to the peripheral. If the Entry Command Pattern matches the Remote Application Reset Command a Trigger is flagged to the protocol at the peripheral side via the logical PPI. The host processor can send software reset trigger by Remote Application Reset Packet.

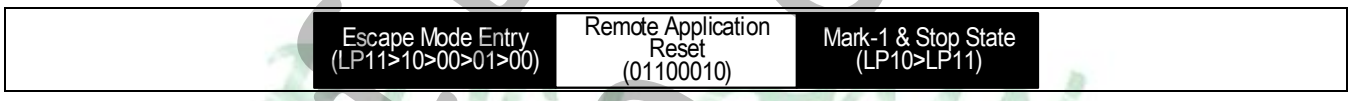

Figure 48 Remote Application Reset

4.10.4.7.3 TE Signaling in DSI

A Command Mode display module has its own timings controller and local frame buffer for display refresh. In some cases, the host processor needs to be notified of timing events on the display module, e.g. the start of vertical blanking or similar timing information. In a traditional parallel-bus interface like DBI-2, a dedicated signal wire labeled TE (Tearing Effect) is provided to convey such timing information to the host processor. In a DSI system, the same information, with reasonably low latency, shall be transmitted from the display module to the host processor when requested, using the bi-directional Data Lane. The PHY for DSI has no inherent interrupt capability from peripheral to host processor so the host processor shall give bus ownership to the peripheral for extended periods, as it does not know when the peripheral will send the TE message. Since the timing of a TE event is, by definition, unknown to the host processor, the host processor shall give bus possession to the display module and then wait up to one video frame period for the TE response. During this time, the host processor cannot send new commands, or request to the display module, because it does not have bus possession. The TE Signaling function is enabled and disabled by three DCS commands to the display module's controller: set_tear_on, set_tear_off. After sending set_tear_on to enable this function, the host processor ends the transmission with BTA asserted, giving bus possession to the display module. Since the display module's DSI protocol layer does not interpret DCS commands, but only passes them through to the display controller, it responds with normal Acknowledge and returns bus possession to the host processor. In this state, the display module cannot report TE events to the host processor since it does not have bus possession. To enable TE

Reporting, the host processor shall give bus possession to the display module without an accompanying DSI command transmission after TE Signaling has been enabled. This is accomplished by the host processor's protocol logic asserting (internal) Bus Turn-Around signal to its PHY functional block. The PHY layer will then initiate a Bus Turn-Around sequence in LP mode which gives bus possession to the display module. This Trigger Message is reserved by DSI for TE signaling only and shall not be used for any other purpose in a DSI-compliant interface.

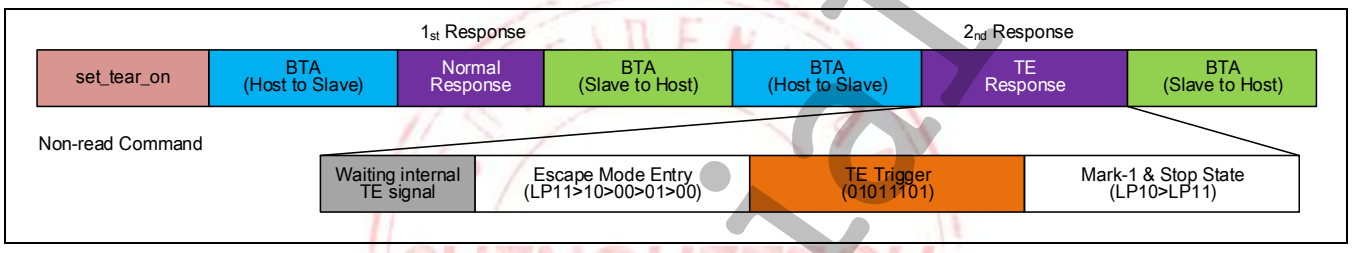

Figure 49 BTA Mode-TE Signaling

4.10.5 MIPI DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted in the Protocol layer to packets. The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY. Packets are serialized by the PHY and sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. If there are multiple Lanes, the Lane Management layer distributes bytes to separate PHYs, one PHY per Lane. Packet protocol and formats are independent of the number of Lanes used.

4.10.5.1 Multiple Packets per Transmission

The MIPI CORE of SH8601A supports four data transmission defined in MIPI DSI specification. And in order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp packet can be enabled or disabled with register.

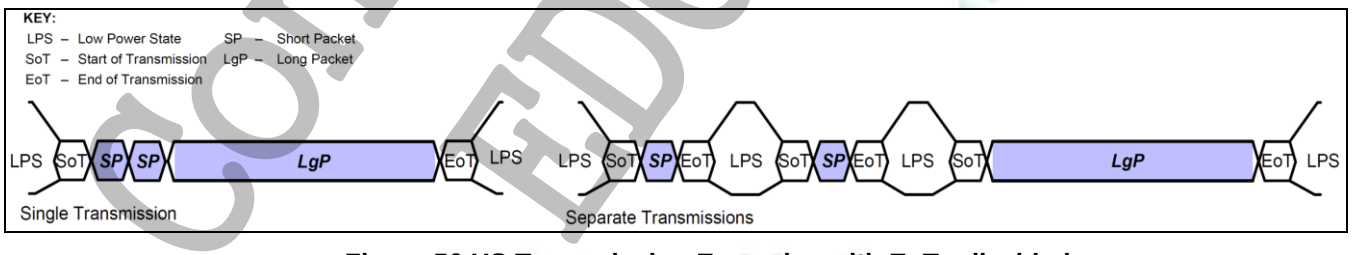

Figure 50 HS Transmission Examples with EoTp disabled

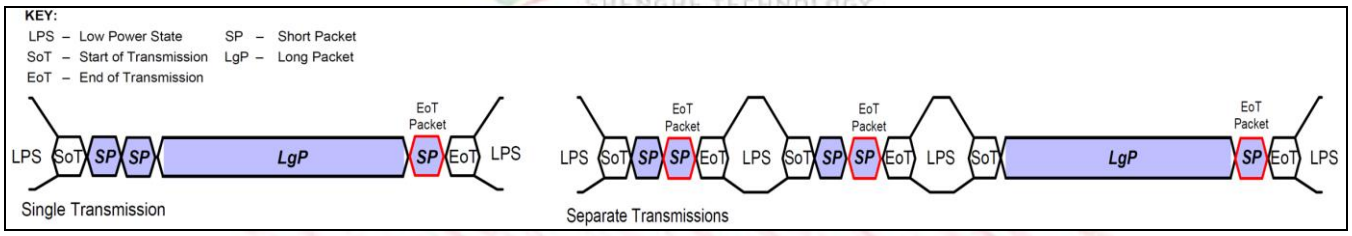

Figure 51 HS Transmission Examples with EoTp enabled

4.10.5.2 Endian Policy

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. *Figure 52* shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

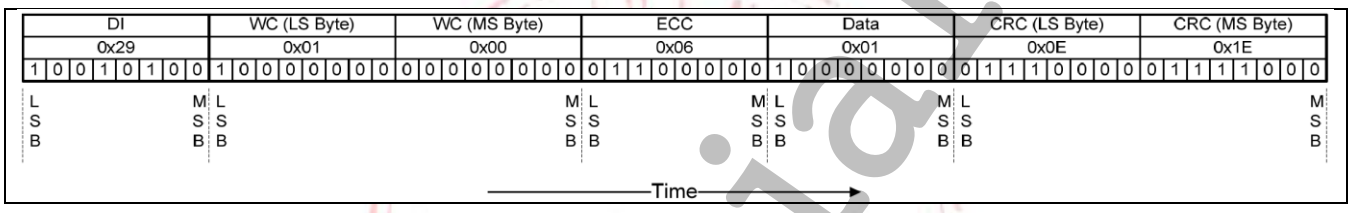

Figure 52 Endian Example (Long Packet)

4.10.5.3 General Packet Structure

Two packet structures are defined for low-level protocol communication: Long packets and Short packets. For both packet structures, the Data Identifier is always the first byte of the packet.

4.10.5.3.1 Long Packet Format

Figure 44 shows the structure of the Long packet. A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length. In the Long Packet, Packet Footer is added after Packet Data. Packet footer includes CRC calculated from Packet Data as checksum.

The Checksum (2 bytes) shall be realized as a 16bit CRC (Packet Data): Polynomial = $X^{16} + X^{12} + X^5 + X^0$

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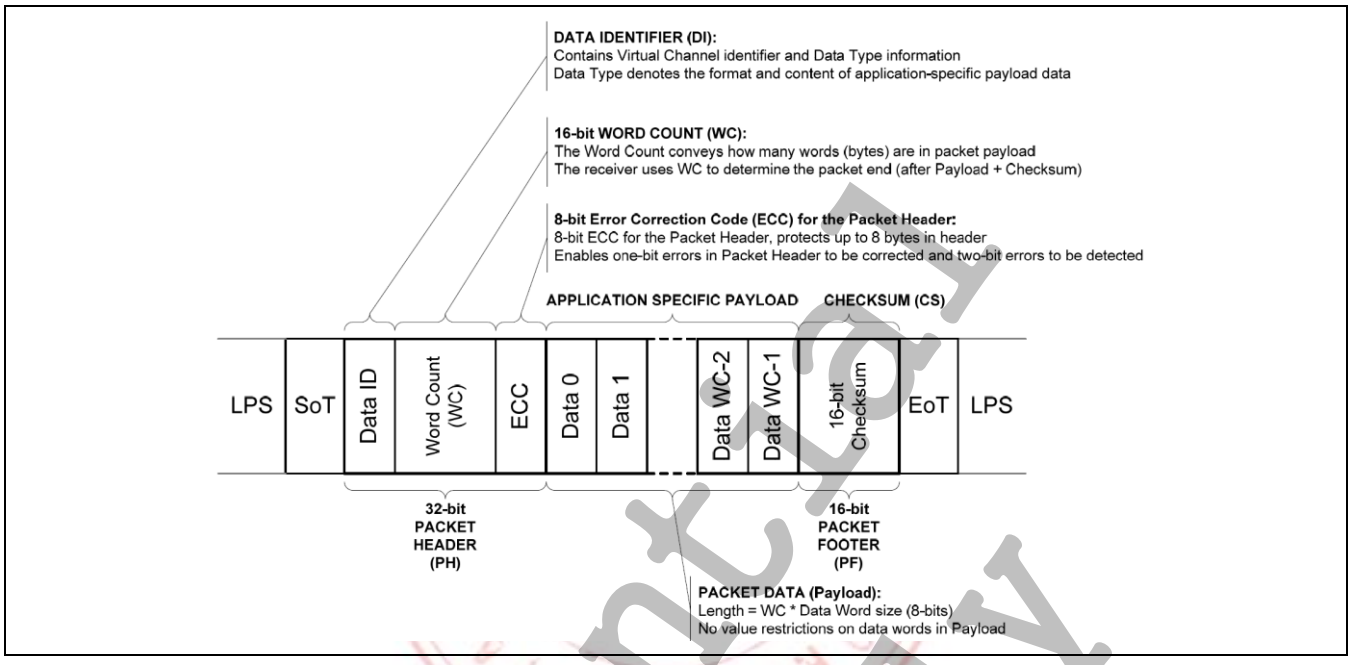

Figure 53 Long Packet Structure

4.10.5.3.2 Short Packet Structure

Figure 75 shows the structure of the Short packet. A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC. a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

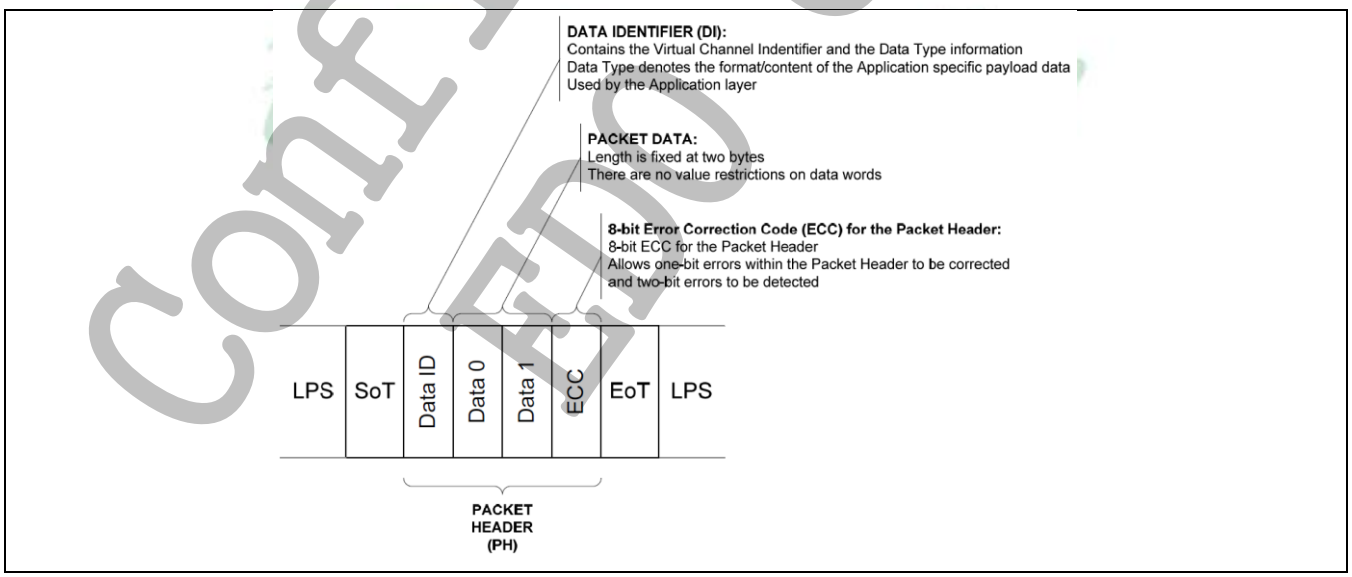

Figure 54 Short Packet Structure

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4.10.5.4 Common Packet Element

Long and Short packets have several common elements.

4.10.5.4.1 Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte. Figure 45 shows the composition of the Data Identifier (DI) byte.

DI[7:6] - These two bits identify the data as directed to one of four virtual channels.

DI[5:0] - These six bits specify the Data Type.

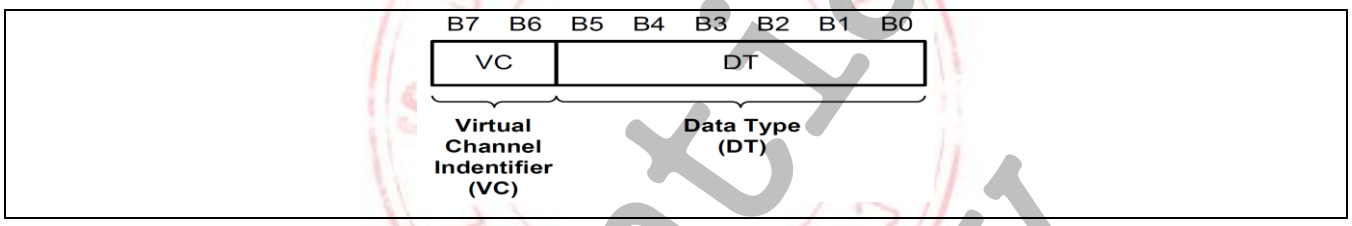

Figure 55 Data Identifier Byte

4.10.5.4.1.1 Virtual Channel Identifier – VC field DI[7:6]

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals.

4.10.5.4.1.2 Data Type Field – DT[5:0]

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start/end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet. When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

4.10.5.4.2 Error Correction Code

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications. ECC is generated from the twenty-four data bits within the Packet Header as illustrated in Figure 46.

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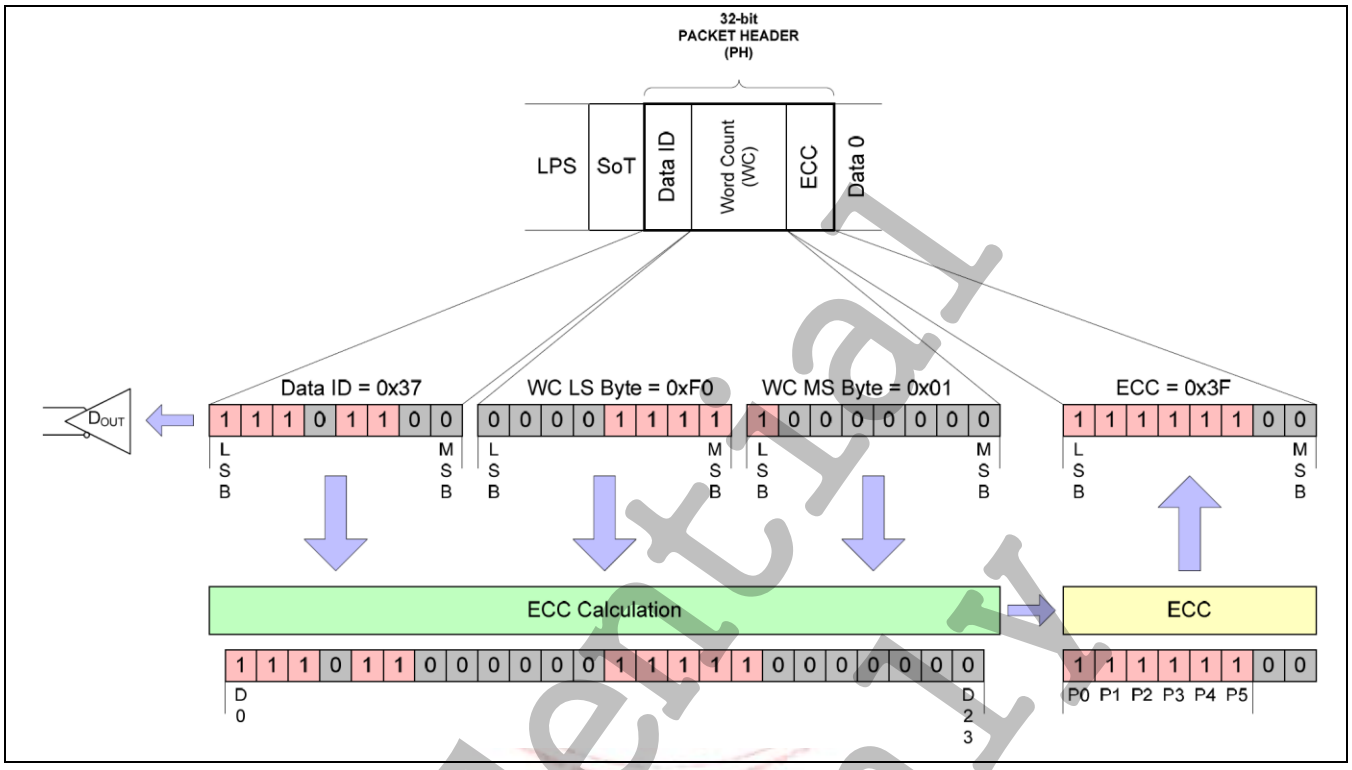

Figure 56 24bit ECC generation on TX side

P7=0
P6=0
P5=D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
P4=D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
P3=D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
P2=D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
P1=D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
P0=D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

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4.10.5.5 Processor to Peripheral Direction (Processor – Sourced) Packet Data Type

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 28.

Table 32 Data Types for Processor-Sourced Packets

Data Type		Description	Packet Size
(Hex)	(Binary)		
01h	00 0001	Sync event, V sync start	Short
11h	01 0001	Sync event, V sync end	Short
21h	10 0001	Sync event, H sync start	Short
31h	11 0001	Sync event, H sync end	Short
08h	00 1000	End of transmission packet	Short
02h	00 0010	Color mode (CM) off command	Short
12h	01 0010	Color mode (CM) on command	Short
22h	10 0010	reserved	Short
32h	11 0010	reserved	Short
03h	00 0011	reserved	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	reserved	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS WRITE, no parameters	Short
15h	01 0101	DCS WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set maximum return packet size	Short
09h	00 1001	Null packet, no data	Long
19h	01 1001	Blanking packet, no data	Long
29h	10 1001	Generic long write	Long
39h	11 1001	DCS long write/write_LUT command packet	Long
0Eh	00_1110	Packet pixel stream, 16-bit RGB 565 format	Long
1Eh	01_1110	Packet pixel stream, 18-bit RGB 666 format	Long
2Eh	10_1110	Packet pixel stream, 18-bit RGB Loosely 666 format	Long
3Eh	11 1110	Packed pixel stream, 24-bit RGB, 888 format	Long
x0h&Fh	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	–

NOTE: Unspecified codes are reserved.

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4.10.5.6 Peripheral to Processor Direction (Processor – Sourced) Packet Data Type

Table 29 presents the complete set of peripheral to processor data types.

Table 33 Data Types for Peripheral-Sourced Packets

Data Type		Description	Packet Size
(Hex)	(Binary)		
00h – 01h	00 000x	Reserved	Short
02h	00 0010	Acknowledge with error report	Short
03h – 07h	00 0011 – 00 0111	Reserved	–
08h	00 1000	End of transmission packet	Short
09h – 10h	00 1001 – 01 0000	Reserved	–
11h	01 0001	Generic Short READ response, 1 byte returned	Short
12h	01 0010	Generic Short READ response, 2 bytes returned	Short
13h – 18h	01 0011 – 01 1000	Reserved	–
1Ah	01 1010	Generic long READ response	Long
1Bh	01 1011	Reserved	–
1Ch	01 1100	DCS long READ response	Long
1Dh – 20h	01 1101 – 10 0000	Reserved	–
21h	10 0001	DCS Short READ response, 1 byte returned	Short
22h	10 0010	DCS Short READ response, 2 bytes returned	Short
23h – 3Fh	10 0011 – 11 1111	Reserved	–

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4.10.5.7 Color Format

There are several data packet structure for pixel data transmission, 16-bit (5-6-5) format, two 18-bit (6-6-6) formats, 24-bit format (8-8-8) and the data packet structures.

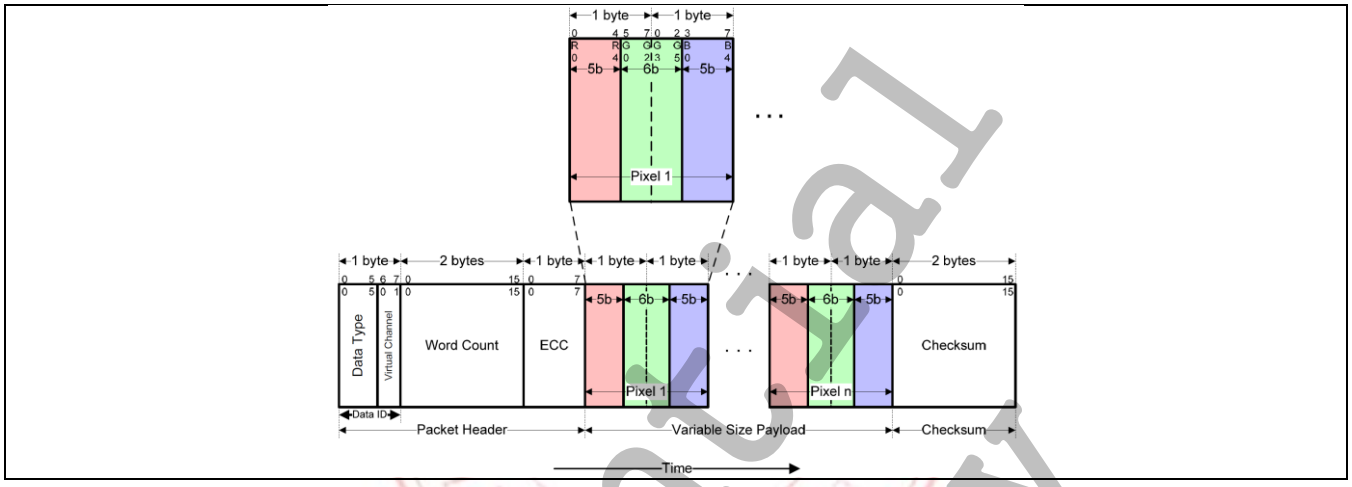

Figure 57 16-bit per Pixel - RGB Color Format, Long Packet

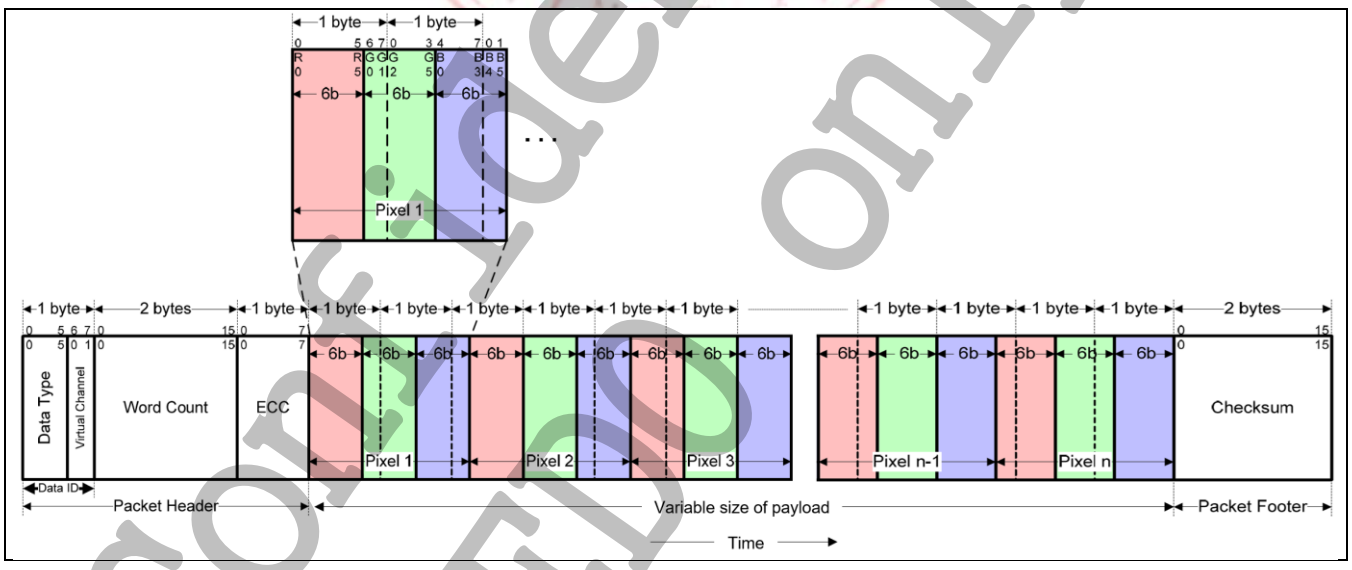

Figure 58 18-bit per Pixel (Packed) - RGB Color Format, Long Packet

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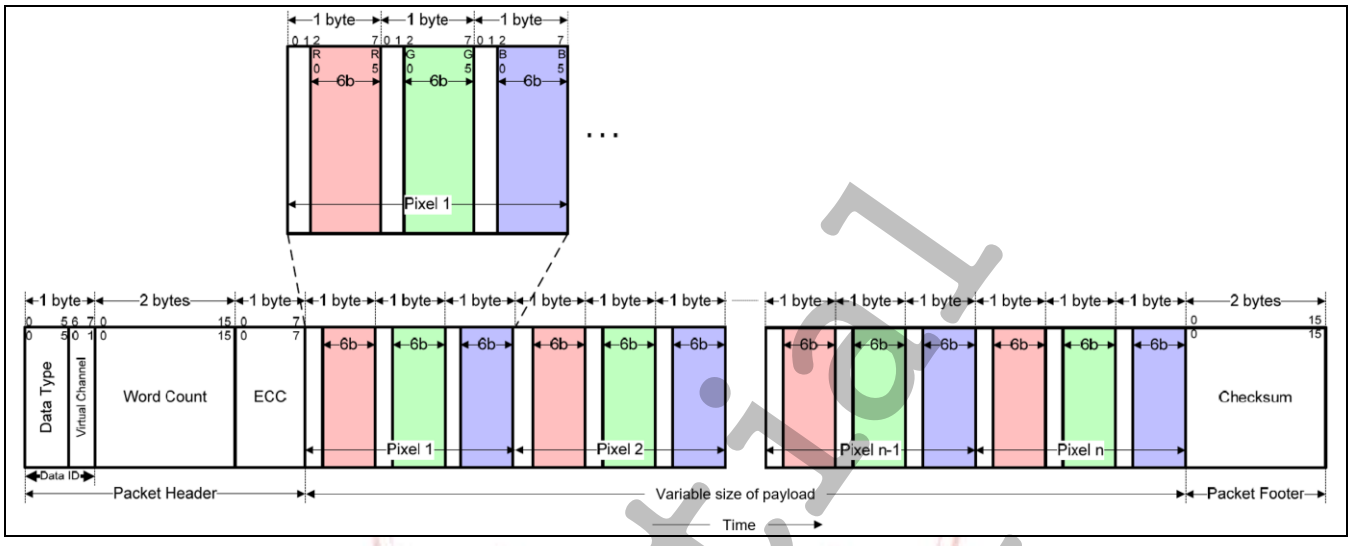

Figure 59 18-bit per Pixel(Loosely Packed) - RGB Color Format, Long Packet

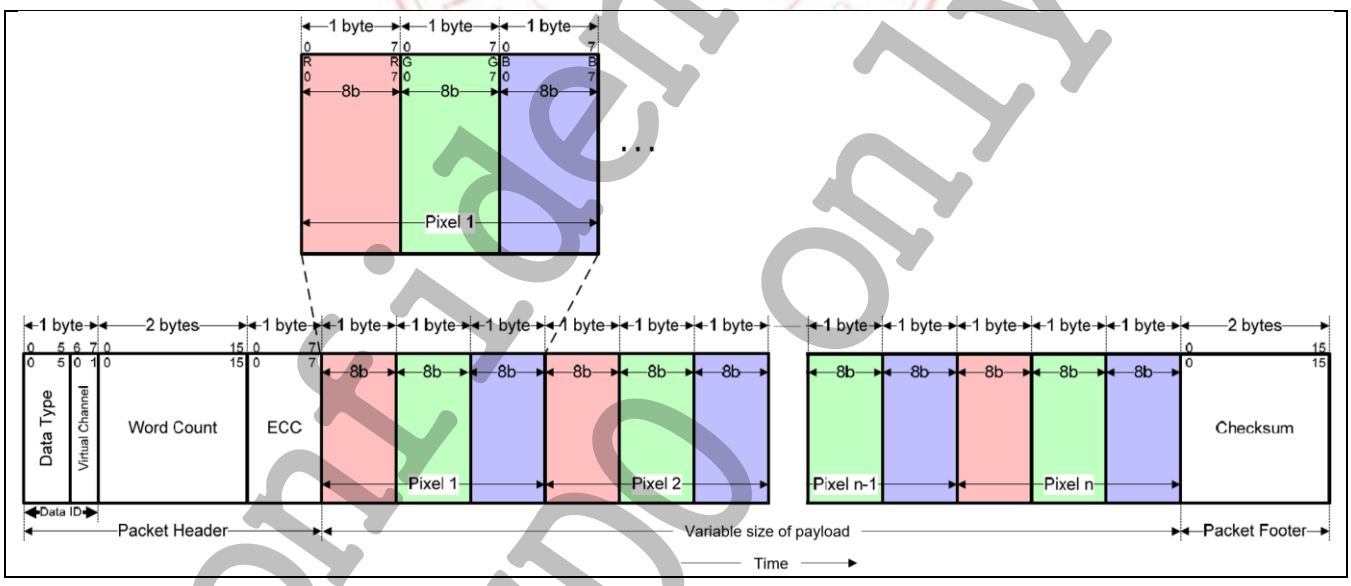

Figure 60 24-bit per Pixel RGB Color Format, Long Packet

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4.10.5.8 Error Report Packet

An error report is a Short packet comprised of two bytes following the DI byte, with an ECC byte following the Error Report bytes. By convention, detection and reporting of each error type is signified by setting the corresponding bit to “1”.

Table 34 Error Report Bit Definitions

Bit	Description
0	SoT error
1	SoT sync error
2	EoT sync error
3	Escape Mode Entry command error
4	Low-power transmit sync error
5	HS receive timeout error (Timeout error)
6	False control error
7	Contention detection error
8	ECC error, single-bit (Detected and corrected)
9	ECC error, multi-bit (Detected, not corrected)
10	Checksum error (Long packet only)
11	DSI data type not recognized
12	DSI VC ID invalid
13	Invalid transmission length
14	Reserved
15	DSI protocol violation

4.10.5.9 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral’s timing requirements dictate which format is appropriate. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

• Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

• Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.

• Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

4.10.5.9.1 Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods

are defined using packets transmitting both start and end of sync pulses.

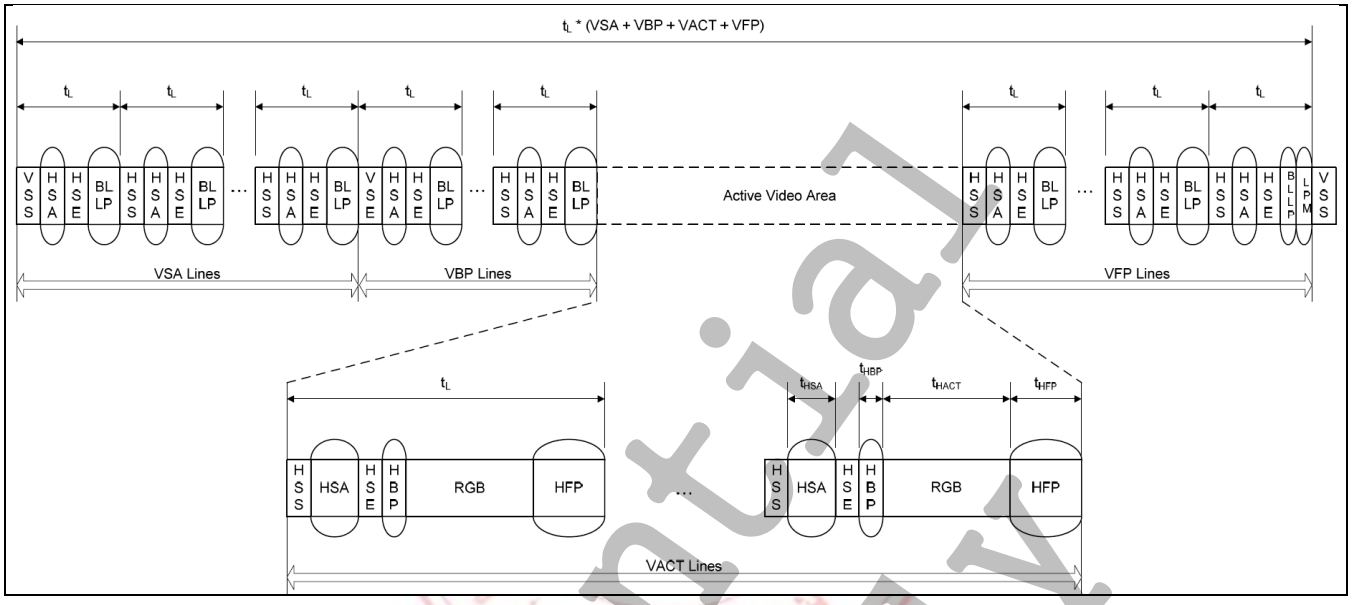

Figure 61 Non-Burst Transmission with Sync Start and End

4.10.5.9.2 Non-Burst Mode with Sync Events

This mode is a simplification of the format described in section 8.11.2. Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2.

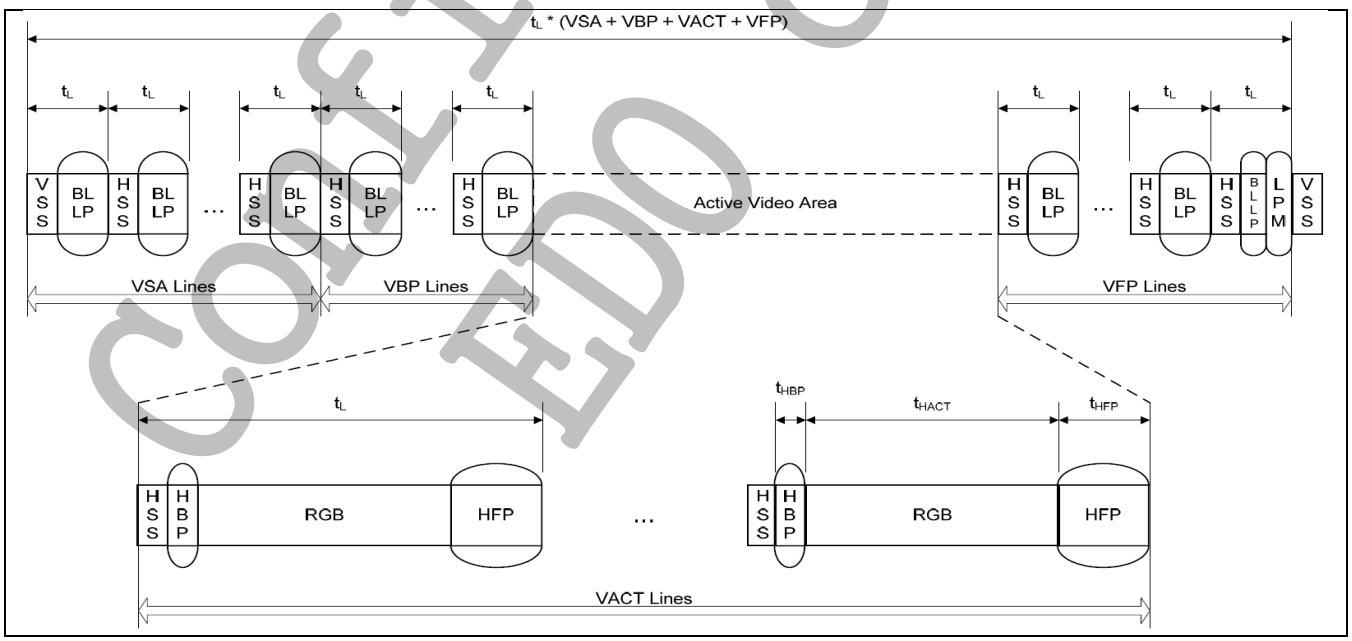

Figure 62 Non-Burst Transmission with Sync Events

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4.10.5.9.3 Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction.

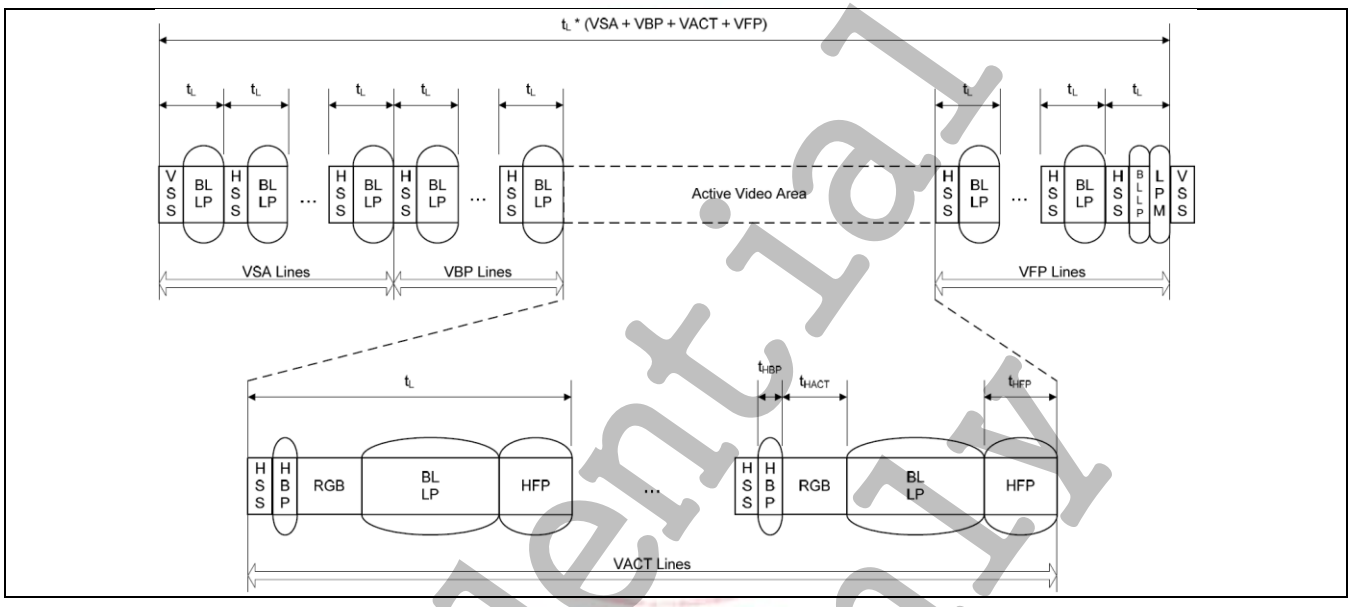

Figure 63 Burst Transmission

4.10.6 MIPI Interface Timing on Video Mode

SH8601A video mode operates as RGB interface.

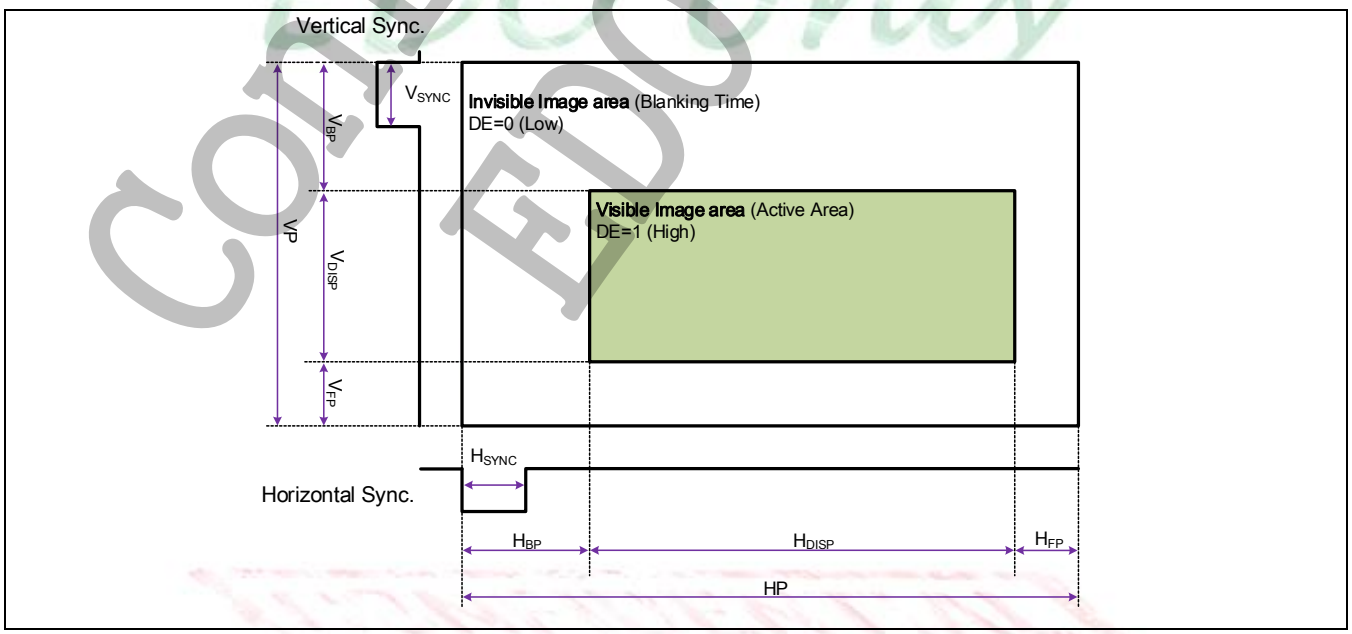

Figure 64 Display Timing (Video Mode)

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4.10.6.1 Vertical Display Timing

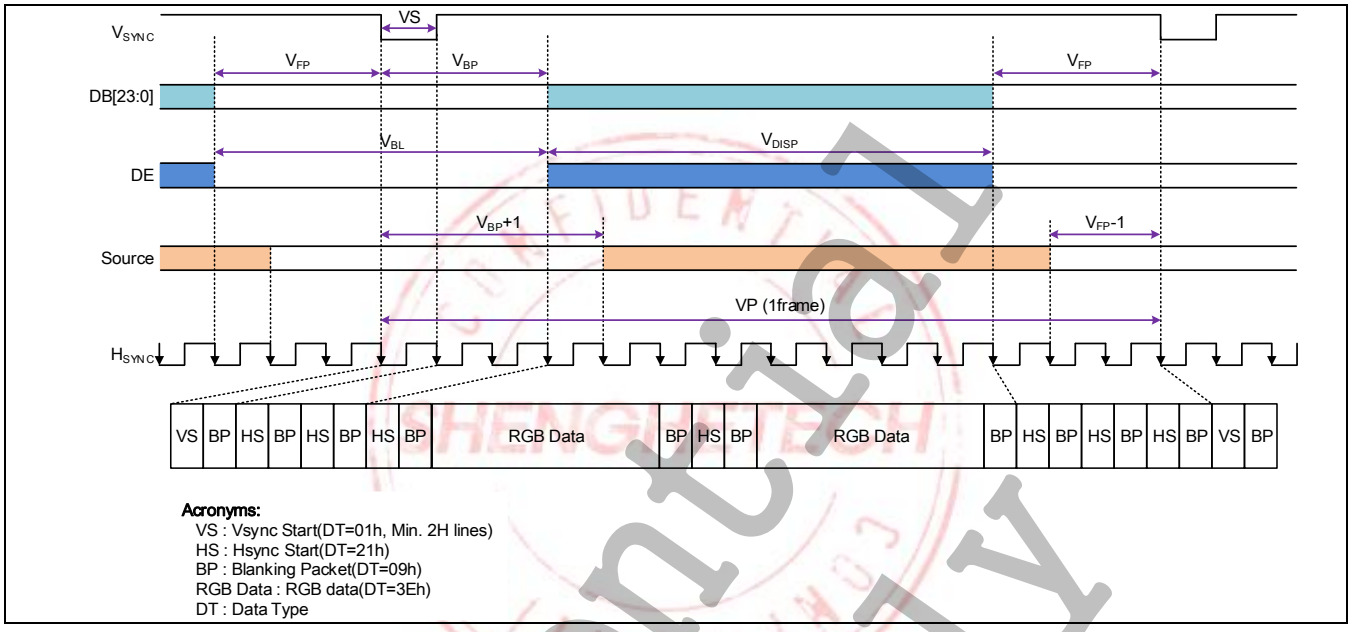

Figure 65 Vertical Display Timing

Table 35 Vertical Timing for Video Mode

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Vertical cycle	VP	–	200	496	-	line	(1)
Vertical low pulse width	VS	–	1	2	2		(1) (2) (3)
Vertical front porch	VFP	–	6	8	-		(1) (3)
Vertical back porch	VBP	–	6	8	255		(1) (2) (3)
Vertical blanking period	VBL	VBP + VFP	12	16	-		(1) (3)
Vertical active area	–	VDISP	192	480	960		
(Vertical refresh area)	(VRR)	–	–	60	–	Hz	

NOTE:

1. Typical values are for resolution of 480 x 480 application.
2. VBP are set as back porch by B1h NOR_VBP/VFP[11:0].
3. VS, VBP and VFP values are typical value.
4. 960 of vertical active area is available only at 192 x 960 resolution.

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4.10.6.2 Horizontal Display Timings

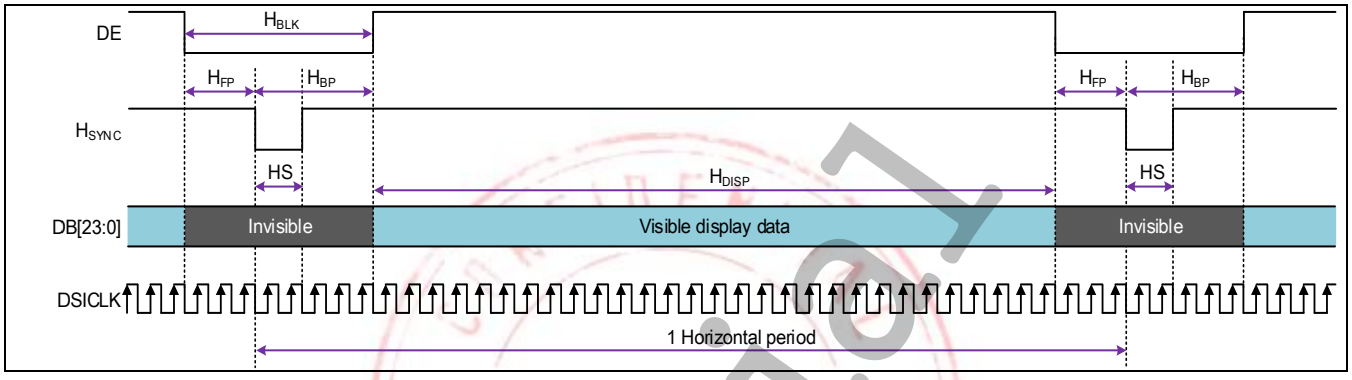

Figure 66 Horizontal Display Timing

Table 36 Horizontal Timings for Video Mode

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
HS cycle	HP	–	216	516	-	PCLK	(2)
HS low pulse width	HS	–	1	2	2		(1) (2) (3)
Horizontal back porch	HBP	–	8	16	-		(3)
Horizontal front porch	HFP	–	8	20	-		(3)
Horizontal data start point	–	HBP	8	16	-		
Horizontal blanking period	HBLK	HBP + HFP	16	36	-		
Horizontal active area	HDISP	–	192	480	480		(1)

NOTE:

1. Typical values are for resolution of 480 x 480 application.
2. PCLK is pixel clock and same as byte-clock that is generated by dividing CLK by 4 (ex. 500 Mbps, 16ns).
3. HS, HBP and HFP values are typical value.

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5 Command

5.1 List of User Command

Operational Code is abbreviated by Opcode, Read/Write/Command is abbreviated by RWC, and Number of Parameter bytes is abbreviated by Num. of Para.

Table 37 List of Level 1 Command

OpCode (Hex)	Function	R/W/C	Num. of Para.	Parameters
00	No Operation	C	-	NO operation
01	Software Reset	C	-	-
04	Read Display Identification Information	R	3	ID1/2/3
05	Read Number of Errors on DSI	R	1	Number of the error on DSI
0A	Read Display Power Mode	R	1	Display power mode
0B	Read Display MADCTL	R	1	MX, BGR
0C	Read Display Pixel Format	R	1	Display COLMOD
0D	Read Display Image Mode	R	1	Display image mode
0E	Read Display Signal Mode	R	1	Display signal mode
0F	Read Display Self-Diagnostic Result	R	1	Display self-diagnostic result
10	Sleep In	C	-	-
11	Sleep Out	C	-	-
12	Partial Display On	C	-	-
13	Normal Display mode on	C	-	-
20	Inversion Off	C	-	-
21	Inversion On	C	-	-
22	All pixels off	C	-	-
23	All pixels on	C	-	-
28	Display off	C	-	-
29	Display on	C	-	-
2A	Column Address Set	W	4	Start/End column address in memory write
2B	Page Address Set	W	4	Start/End page address in memory write
2C	Memory Write Start	W	Variable	Memory write data
30	Partial Area Row Set	W	4	Start/End row address in partial mode
31	Partial Area Column Set	W	4	Start/End page address in partial mode

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OpCode (Hex)	Function	R/W/C	Num. of Para.	Parameters
34	Tearing effect off	C	-	-
35	Tearing effect on	W/C	1	1 byte for tearing effect line mode selection.
36	Memory data access control	W	1	MX, BGR
38	Idle Mode Off	C	-	-
39	Idle Mode On	C	-	-
3A	Write Display Pixel Format	W	1	1byte for interface color selection
3C	Memory Write Continue	W	Variable	Memory write data
44	Write Tearing Effect Scan Line	W	2	2 byte for TE signal turns on when the display module reaches line N.
45	Read Scan Line Number	R	2	Scan line
46	SPI read Off	C	-	-
47	SPI read On	C	-	-
48	AOD Mode Off	C	-	
49	AOD Mode On	C	-	
4A	Write Display Brightness Value in AOD Mode	W	2	2 byte for display brightness value in AOD mode
4B	Read Display Brightness Value in AOD Mode	R	2	2 byte for display brightness value in AOD mode
4F	Deep Standby Mode On	W	1	1 byte for deep standby mode control
51	Write Display Brightness Value in Normal Mode	W	2	2 byte for display brightness value in normal mode
52	Read display brightness value in Normal Mode	R	2	2 byte for display brightness value in normal mode
53	Write CTRL Display1	W	1	1 byte for display control1
54	Read CTRL Display1	R	1	1 byte for display control1
55	Write CTRL Display2	W	1	1 byte for display control2
56	Read CTRL Display2	R	1	1 byte for display control2
58	Write CE	W	1	1 byte for CE control
59	Read CE	R	1	1 byte for CE control
63	Write Display Brightness Value in HBM Mode	W	2	2 byte for display brightness value in HBM mode
64	Read Display Brightness Value in HBM Mode	R	2	2 byte for display brightness value in HBM mode
66	Write HBM Control	W	1	1 byte for HBM control
A1	Read DDB start	R	8	8 byte for Read DDB start
A8	Read DDB Continue	R	8	8 byte for Read DDB continue

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OpCode (Hex)	Function	R/W/C	Num. of Para.	Parameters
AA	Read First Checksum	R	1	Read Checksum
AF	Read continue Checksum	R	1	Read Checksum
C4	SPI mode control	W	1	1 byte for SPI mode control
DA	Read ID1	R	1	Read ID1
DB	Read ID2	R	1	Read ID2
DC	Read ID3	R	1	Read ID3

NOTE:

1. Undefined commands are treated as NOP (00H) command.
2. Commands 10H, 28H, 29H, 36H, 51H, 53H, 55H, 61H, 63H, and 66H are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately.

   Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh), Read Display Self-Diagnostic Result (0Fh), Read Display Brightness Value in normal mode(52h), Read CTRL Display1 (54h), Read CTRL Display2 (56h), Read Display Brightness Value in AOD Mode (4BH), Read Display Brightness Value in HBM Mode (64H) are updated immediately both in Sleep In mode and Sleep Out mode.
3. Parameters of the command are stored onto registers when the last parameter of the command has been received. Also, parameters of the command are not stored onto registers if there has been happen a break. This note is valid when a number of the parameters are equal or less than 32.

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5.2 Description of User Command

5.2.1 NOP (00h): No Operation

00H	NOP (No Operation)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	0	0	0	0	00
Parameter	No Parameter									
Description	This command is an empty command. It does not have any effect on the display module.									
Restriction	–									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					N/A				
	S/W Reset					N/A				
	H/W Reset					N/A				
Flow Chart	–									

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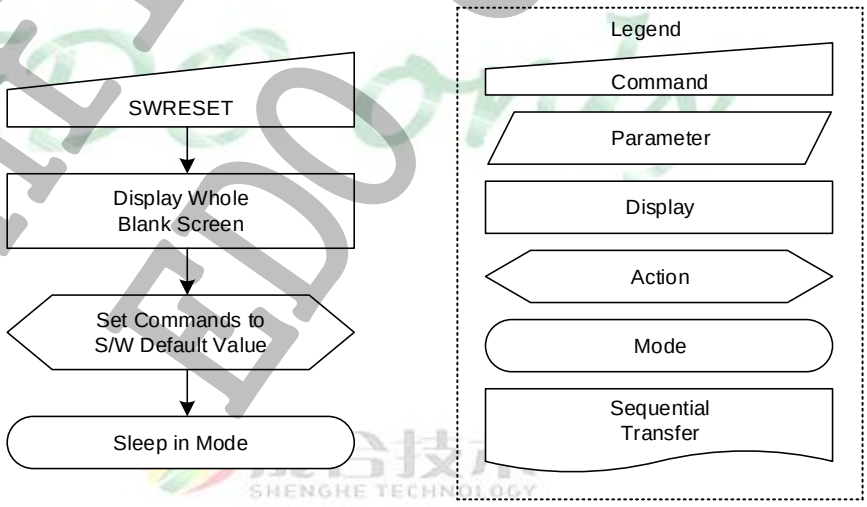
5.2.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	0	0	0	1	01
Parameter	No Parameter									
Description	When the software reset command is written, it causes a software reset. It resets the User, Manufacturer commands and parameters to their S/W Reset default values (See default tables in each command description.) and OTP is loaded. The display will be blanked. (The display will be blanked after first VSYNC, when Software Reset command is written in sleep out mode. The display remains the blank state in sleep in Mode.)									
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5 msec. If software reset is applied during sleep out mode, it will be necessary to wait 80ms before sending sleep out command. Software reset command cannot be sent during sleep out sequence.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					N/A				
	S/W Reset					N/A				
	H/W Reset					N/A				
Flow Chart										

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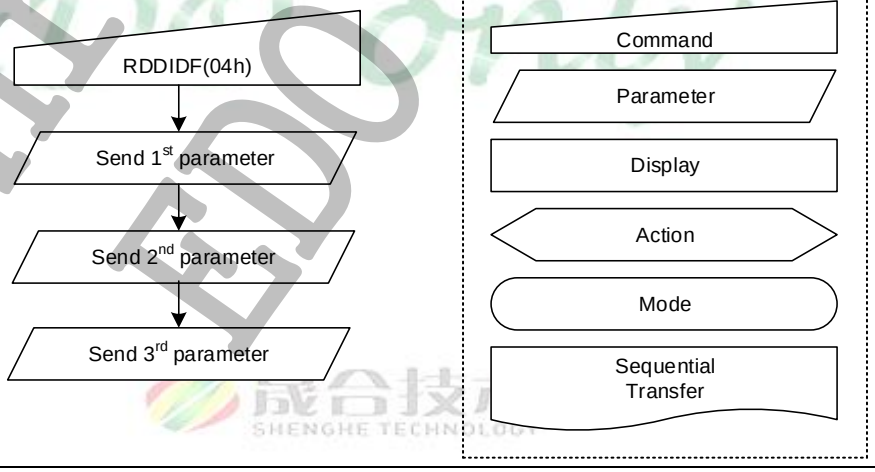
5.2.3 RDDIDIF (04h): Read Display Identification Information

04H	RDDIDIF (Read Display Identification Information)									
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	0	1	0	0	04
1st Para	Read	ID1[7:0]								00
2nd Para	Read	ID2[7:0]								00
3rd Para	Read	ID3[7:0]								00
Description	This command indicates the return value of 24-bit display identification information. **ID1[7:0]**: AMOLED module maker code (8-bit) **ID2[7:0]**: Driver IC and module version (8-bit) **ID3[7:0]**: Project code (8-bit) **NOTE:** Commands RDID1/2/3 (DAH, DBH, and DCH) reads data corresponding to the parameters 1, 2 and 3 of the command 04H, respectively.									
Restriction	There is one dummy clock before 1st parameter when using Serial interface.									

Register Availability	**Status**	**Availability**
	Sleep Out	Yes
	Sleep In	Yes

Default	**Status**	**Default Value**	
	Power On Sequence	00_00_00H	(OTP value)
	S/W Reset	00_00_00H	(OTP value)
	H/W Reset	00_00_00H	(OTP value)

Flow Chart



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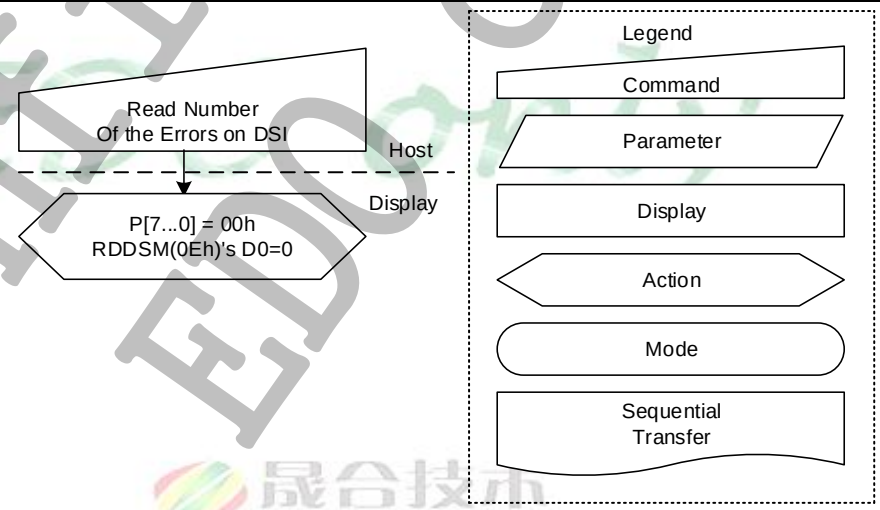
5.2.4 RDNUMED (05h): Read Number of the Errors on DSI

05H	RDNUMED (Read Number of the Errors on DSI)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	0	1	0	1	05
1st Para	Read	NUMED[7:0]								00
Description	This command returns the number of corrupted packets previously received on the DSI link. The NUMED[7:0] bits are set to '0's (as well as RDDSM (0Eh)'s D0 is set to '0' at the same time) after the parameter information is sent, indicating that the read function is completed. **NUMED[7]** bits is set to '1' if there is overflow with the NUMED[6:0] bits. **NUMED[6:0]** bits indicates a number of errors.									
Restriction	After the RESX goes high from low, all lanes should be "High". If all lanes are not high, DSI errors may occur and this parameter may not be all zero. The errors only include ECC 1BIT ERROR, ECC MULTIBIT ERROR and CHECKSUM ERROR. If you want specific description of ECC and CHECKSUM ERROR, refer to MIPI DSI document.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart										

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5.2.5 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	1	0	1	0	0A
Parameter	Read	BSTON	IDMON	PTLON	SLPOUT	NORON	DISPON	0	0	08

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Remark
D7	Booster Voltage Status	-
D6	Idle Mode On/Off	-
D5	Partial Display Mode On/Off	-
D4	Sleep In/Out	-
D3	Display Normal Mode On/Off	-
D2	Display On/Off	-
D1	Reserved	Set to "0"
D0	Reserved	Set to "0"

- **BSTON** - Booster Voltage Status
  0 = Booster off or has a fault
  1 = Booster on and working good
- **IDMON** - Idle Mode On/Off
  0 = Idle mode off
  1 = Ide mode on
- **PTLON** - Partial Display Mode On/Off
  0 = partial display off
  1 = partial display on
- **SLPOUT** - This bit is updated immediately after Sleep In (10h) / Sleep Out (11h) command is written.
  0 = Sleep in mode
  1 = Sleep out mode
- **NORON** - Normal Display Mode On
  0 = Normal display off
  1 = Normal display on
- **DISPON** - This bit is updated immediately after Display On (29h) / Off (28h) command is written.
  0 = Display is off
  1 = Display is on
- **D[1]** - Reserved
  This bit is not applicable for this project, so it is set to "0".
- **D[0]** - Reserved
  This bit is not applicable for this project, so it is set to "0".

Restriction: –

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

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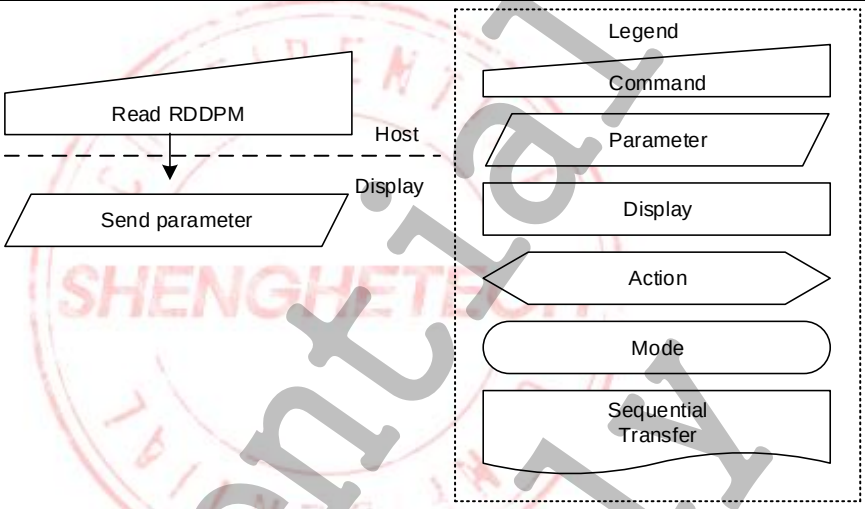
	Status	Default Value
Default	Power On Sequence	08h
	S/W Reset	08h
	H/W Reset	08h
Flow Chart		

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5.2.6 RDDMADCTL (0Bh): Read Display MADCTL

<table>
<tr><th>0BH</th><th colspan="10">RDDMADCTL (Read Display MADCTL)</th></tr>
<tr><td>–</td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0B</td></tr>
<tr><td>Parameter</td><td>Read</td><td>0</td><td>MX</td><td>0</td><td>0</td><td>BGR</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td rowspan="11">Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:</td></tr>
<tr><td colspan="2">Bit</td><td colspan="4">Description</td><td colspan="4">Remark</td></tr>
<tr><td colspan="2">D7</td><td colspan="4">Reserved</td><td colspan="4">Set to "0"</td></tr>
<tr><td colspan="2">D6</td><td colspan="4">Memory Write Direction Horizontal Flip</td><td colspan="4">-</td></tr>
<tr><td colspan="2">D5</td><td colspan="4">Reserved</td><td colspan="4">Set to "0"</td></tr>
<tr><td colspan="2">D4</td><td colspan="4">Reserved</td><td colspan="4">Set to "0"</td></tr>
<tr><td colspan="2">D3</td><td colspan="4">RGB/BGR Order</td><td colspan="4">–</td></tr>
<tr><td colspan="2">D2</td><td colspan="4">Reserved</td><td colspan="4">Set to "0"</td></tr>
<tr><td colspan="2">D1</td><td colspan="4">Reserved</td><td colspan="4">Set to "0"</td></tr>
<tr><td colspan="2">D0</td><td colspan="4">Reserved</td><td colspan="4">Set to "0"</td></tr>
<tr><td colspan="10">• D[7] - Reserved
This bit is not applicable for this project, so it is set to "0".
• MX - Memory Write Direction Horizontal Flip
0 = Memory write forward direction
1 = Memory write reverse direction
• D[5:4] - Reserved
These bits are not applicable for this project, so it is set to "0".
• BGR - RGB/BGR Order
0 = RGB (When MADCTL D3 = "0")
1 = BGR (When MADCTL D3 = "1")
• D[2:0] - Reserved
This bit is not applicable for this project, so it is set to "0".</td></tr>
<tr><td>Restriction</td><td colspan="10">–</td></tr>
<tr><td rowspan="3">Register Availability</td><td colspan="5">Status</td><td colspan="5">Availability</td></tr>
<tr><td colspan="5">Sleep Out</td><td colspan="5">Yes</td></tr>
<tr><td colspan="5">Sleep In</td><td colspan="5">Yes</td></tr>
<tr><td rowspan="4">Default</td><td colspan="5">Status</td><td colspan="5">Default Value</td></tr>
<tr><td colspan="5">Power On Sequence</td><td colspan="5">00h</td></tr>
<tr><td colspan="5">S/W Reset</td><td colspan="5">00h</td></tr>
<tr><td colspan="5">H/W Reset</td><td colspan="5">00h</td></tr>
</table>

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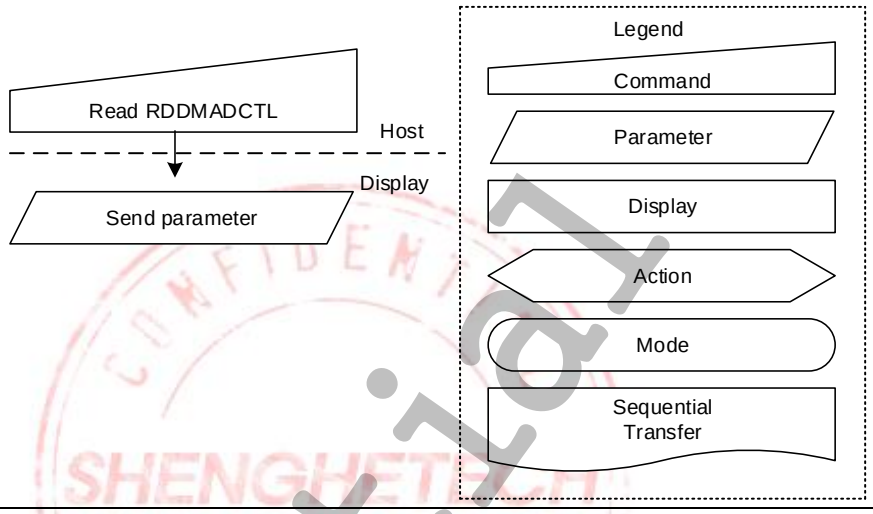
Flow Chart	

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5.2.7 RDDCOLMOD (0Ch): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	1	1	0	0	0C
Parameter	Read	SPI_PF_SEL	VIPF[2:0]			0	IFPF[2:0]			77

Description

This command indicates the current status of the display as described in the table below:

- **SPI_PF_SEL** – SPI Pixel Format Selection.
- **VIPF[2:0]** – Pixel Format Definition.
- **D[3]** - Reserved
  This bit is not applicable for this project, so it is set to "0".
- **IFPF[2:0]** - DBI Pixel Format Definition.

Refer to section : *COLMOD(3Ah) : Control Interface Pixel Format*

Control Interface Color Format	IFPF[2]	IFPF[1]	IFPF[0]
24-bit/pixel(16.7M Color)	1	1	1
18-bit/pixel(262K Color)	1	1	0
16-bit/pixel(65K Color)	1	0	1
Setting Disable	1	0	0
3-bit/pixel(8 Color)	0	1	1
8-bit/pixel(256 Color, 3-3-2)	0	1	0
8-bit/pixel(256 Gray)	0	0	1
Setting Disable	0	0	0

Restriction	–

Register Availability	Status	Availability
	Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	77h
	S/W Reset	77h
	H/W Reset	77h

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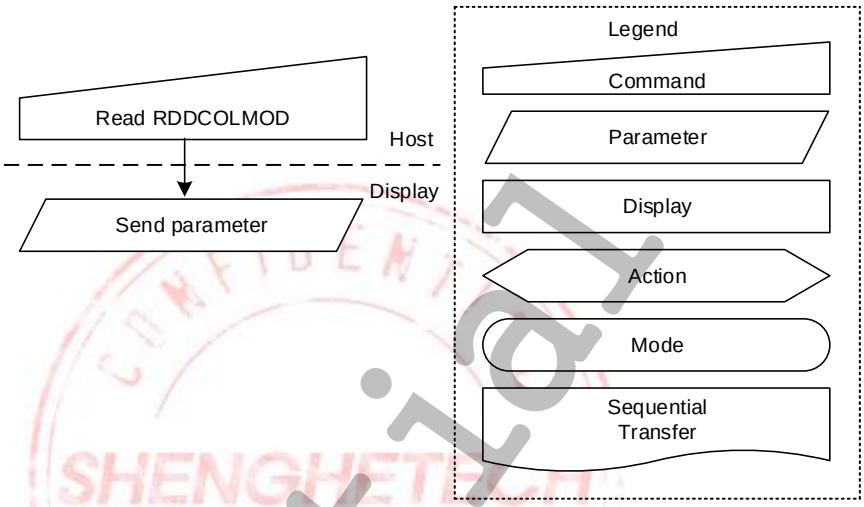
Flow Chart	

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5.2.8 RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	1	1	0	1	0D
Parameter	Read	0	0	INVON	ALLPON	ALLPOFF	0	0	0	00

Description

This command indicates the current status of the display as described in the table below:

- **D[7:6]** - Reserved
  These bits are not applicable for this project, so it is set to "0".
- **INVON** - Display Inversion On/Off
  0 = Display inversion Off
  1 = Display inversion On
- **ALLPON** - All Pixel On/Off
  0 = Normal display
  1 = All pixel is on
- **ALLPOFF** - All Pixel Off/On
  0 = Normal display
  1 = All pixel is off
- **D[2:0]** - Reserved
  These bits are not applicable for this project, so it is set to "0".

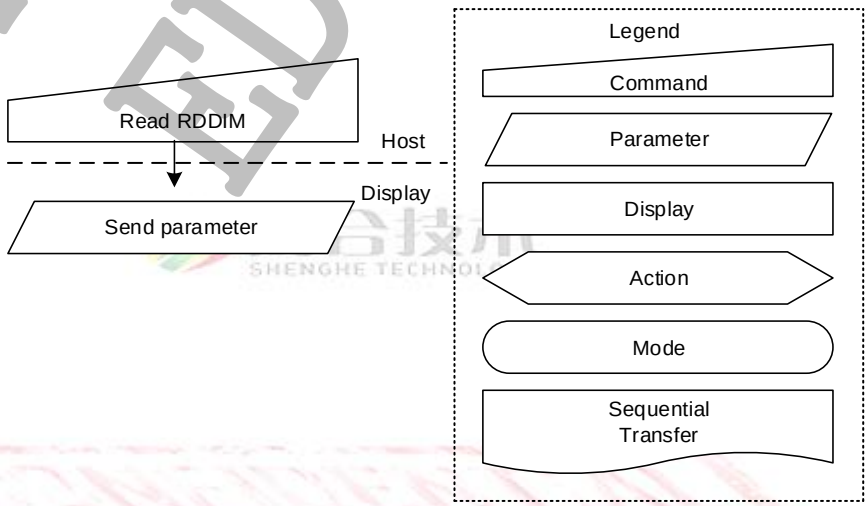
Restriction

–

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes
Status	**Default Value**
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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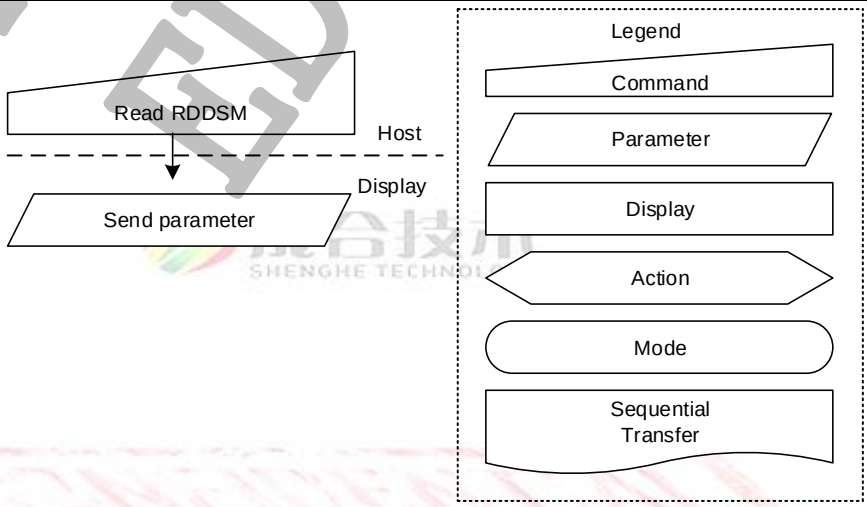
5.2.9 RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	1	1	1	0	0E
Parameter	Read	TEON	TEM	0	0	0	0	0	DSIE	00
Description	This command indicates the current status of the display as described below: • **TEON** - This bit is updated immediately after Tearing Effect On (35h) / Off (34h) command is written. 0 = Tearing effect off 1 = Tearing effect on • **TEM** - This bit is updated immediately after Tearing Effect On (35h) command is written. Refer to section *TEON: Tearing Effect On (35H)*. 0 = Mode 1. 1 = Mode 2. • **D[5:1]** - Reserved These bits are not applicable for this project, so it is set to "0". • **DSIE** - Error on DSI, refer to section RDNUMED(05h) : Read Number of the Errors on DSI. If you want specific description of ECC and CHECKSUM ERROR, refer to MIPI DSI document. This bit is only for MIPI interface. In other interface, D0 is set to "0". 0 = No Error 1 = Error									
Restriction	–									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart										

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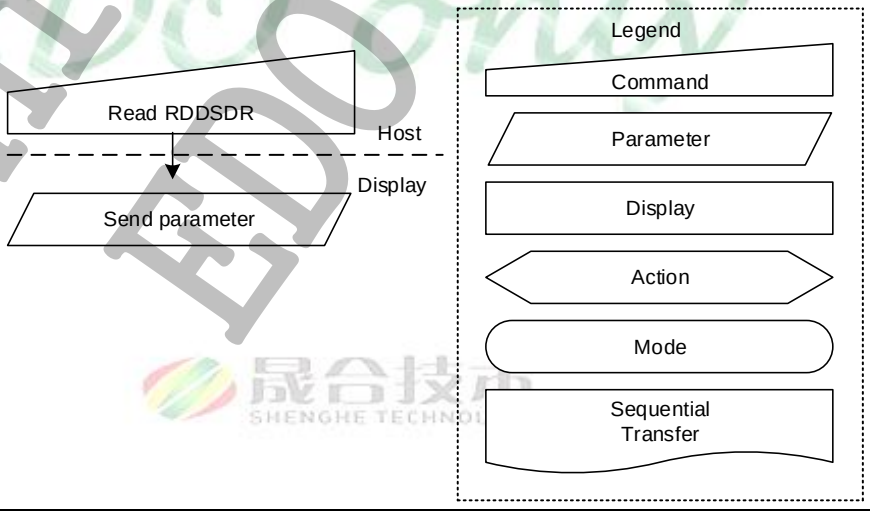
5.2.10 RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDDSDR (Read Display Self-Diagnostic Result)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	0	1	1	1	1	0F
Parameter	Read	RLDT	FNDT	0	0	0	0	0	CHKSUM_ERR	00
Description	This command indicates the status of the display self-diagnostic results after Sleep Out-command as described in the table below: • **RLDT** - Register Loading Detection. Refer to section "Register Loading Detection" • **FNDT** - Functionality Detection Refer to section" Functionality Detection" • **D[5:1]** - Reserved. These bits are not applicable for this project, so it is set to "0". • **CHKSUM_ERR** – Checksum Error Detection.									
Restriction	–									

Register Availability	Status	Availability
	Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

Flow Chart



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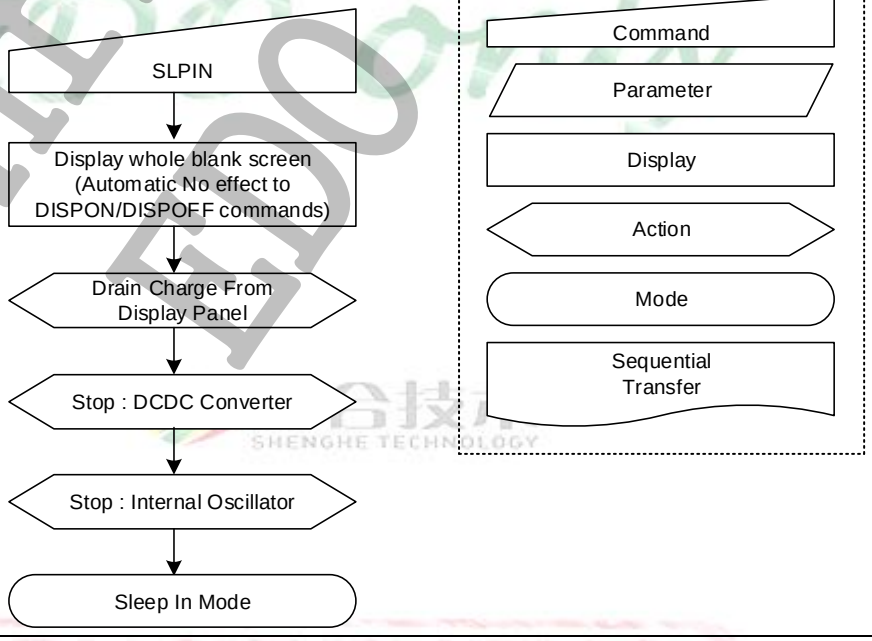
5.2.11 SLPIN (10h): Sleep In

10H	SLPIN (Sleep In)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	0	0	10
Parameter	No Parameter									
Description	This command causes the display module to enter the minimum power consumption mode. In this mode, the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.									
Restriction	This command has no effect when module is already in Sleep In mode. Sleep In mode can only be left by the Sleep Out command (11h). It will be necessary to wait 5ms before sending next command. This is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 80ms after sending Sleep Out command (when in Sleep In mode) before Sleep In command can be sent.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes (Reflect in the next V-sync period).				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					Sleep In Mode				
	S/W Reset					Sleep In Mode				
	H/W Reset					Sleep In Mode				
Flow Chart	It takes about 80ms before it goes into Sleep-in Mode (Booster off state) after SLPIN command.									



NOTE: Refer to customer appendix for SLPIN sequence

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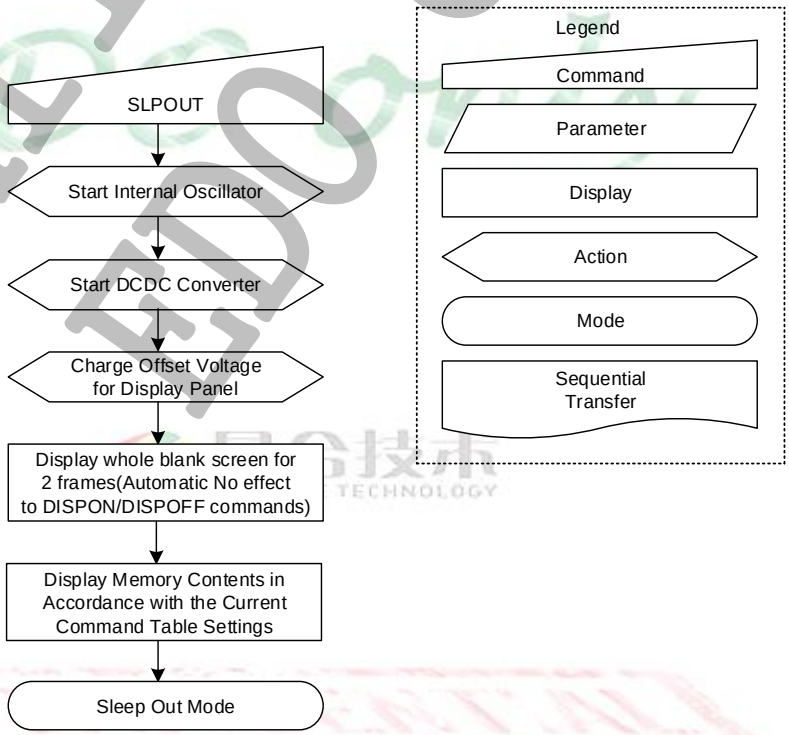
5.2.12 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	0	1	11
Parameter	No Parameter									
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.									
Restriction	This command shall not cause any visible effect on the display module when the module is already in Sleep Out mode. Sleep Out Mode can only be left by the Sleep In command (10h) This host processor must wait 5msec after sending this command before sending other command. The display module loads all display supplier's factory default values from internal OTP to the registers during this 5msec. Also the host processor must wait 85msec after sending a Sleep Out command before sending a Sleep In command to avoid abnormal Sleep In status. This delay time allows the internal power circuits and clock circuits to stabilize.									

Register Availability	**Status**	**Availability**
	Sleep Out	Yes
	Sleep In	Yes

Default	**Status**	**Default Value**
	Power On Sequence	Sleep In Mode
	S/W Reset	Sleep In Mode
	H/W Reset	Sleep In Mode

Flow Chart



It takes 150ms to become Sleep Out mode after SLPOUT command issued.

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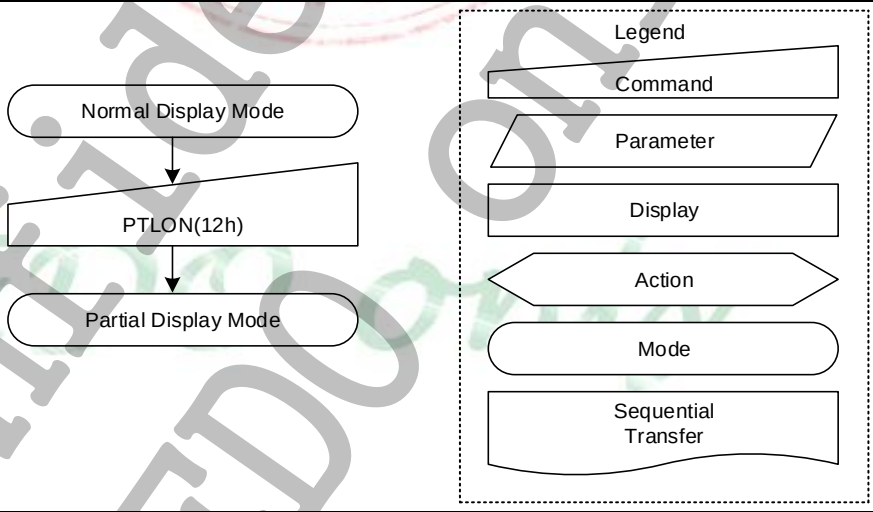
5.2.13 PTLON (12h): Partial Display Mode On

12H	PTLON (Partial Display Mode On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	1	0	12
Parameter	No Parameter									
Description	This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the PTLAR(30h)/PTLAC(31h). To leave the Partial Display Mode, NORON(13h) command should be used.									
Restriction	This command has no effect when partial display mode is already active.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes (Reflect in the next V-sync period).				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					Normal Display On				
	S/W Reset					Normal Display On				
	H/W Reset					Normal Display On				
Flow Chart										

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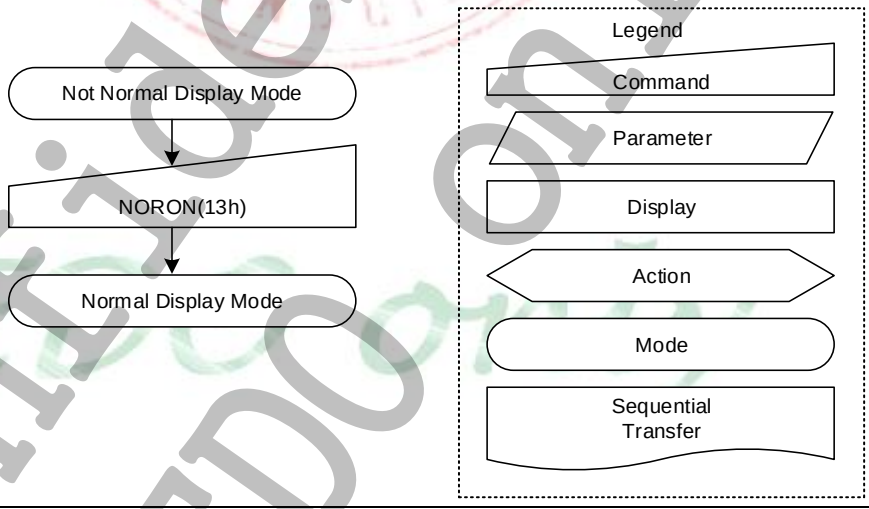
5.2.14 NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	0	1	0	0	1	1	13
Parameter	No Parameter									
Description	This command returns the display to normal mode. Normal display mode on means All Pixel Off(22h), All Pixel On(23h) and Partial mode(12h) are off.									
Restriction	This command has no effect if Normal Display mode is active.									
Register Availability	**Status**				**Availability**					
	Sleep Out				Yes (Reflect in the next V-sync period).					
	Sleep In				Yes					
Default	**Status**				**Default Value**					
	Power On Sequence				Normal Display Mode On					
	S/W Reset				Normal Display Mode On					
	H/W Reset				Normal Display Mode On					
Flow Chart										

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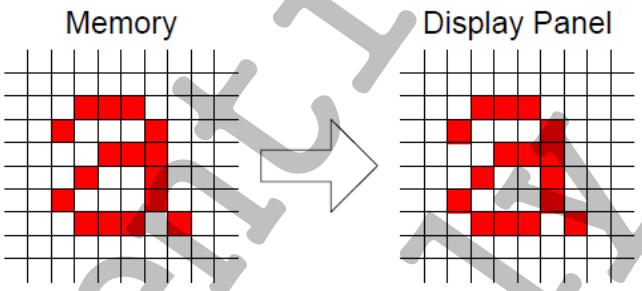
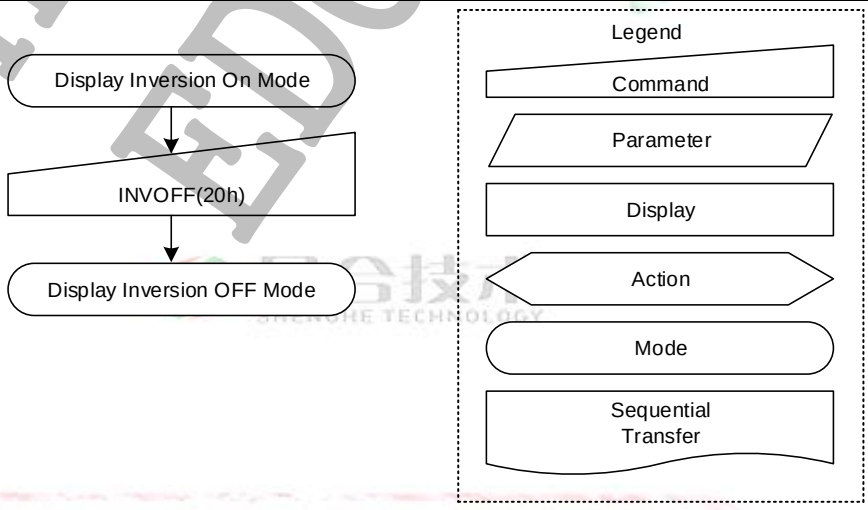
5.2.15 INVOFF (20h): Display Inversion Off

20H	INVOFF (Display Inversion Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	0	0	20
Parameter	No Parameter									
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. Example) 									
Restriction	This command has no effect if Normal Display mode is active.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes (Reflect in the next V-sync period).				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					Display Inversion Off				
	S/W Reset					Display Inversion Off				
	H/W Reset					Display Inversion Off				
Flow Chart										

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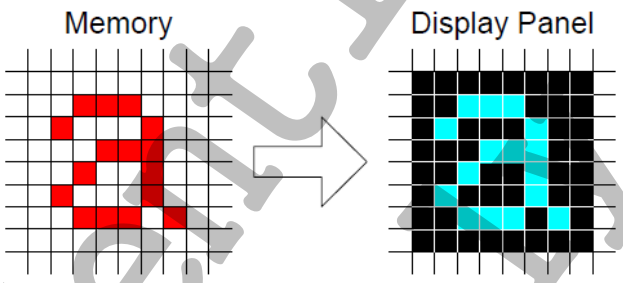
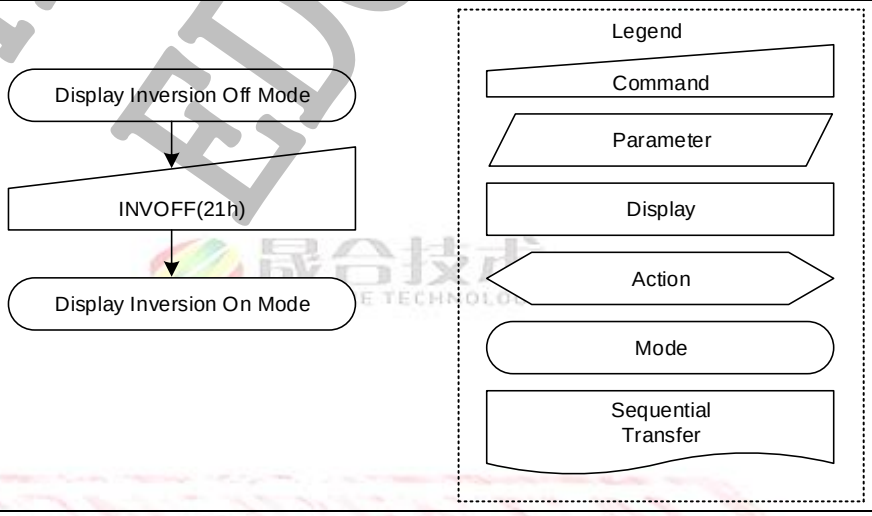
5.2.16 INVON (21h): Display Inversion On

21H	INVON (Display Inversion On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	0	1	21
Parameter	No Parameter									
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. Example) 									
Restriction	This command has no effect if Normal Display mode is active.									

Register Availability	**Status**	**Availability**
	Sleep Out	Yes (Reflect in the next V-sync period).
	Sleep In	Yes

Default	**Status**	**Default Value**
	Power On Sequence	Normal Display Mode On
	S/W Reset	Normal Display Mode On
	H/W Reset	Normal Display Mode On

Flow Chart



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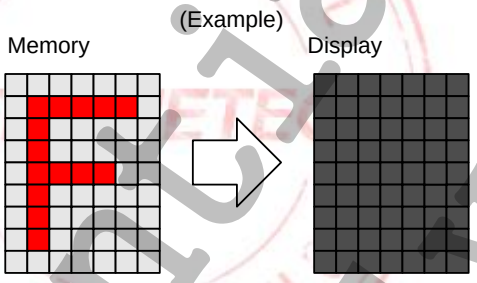
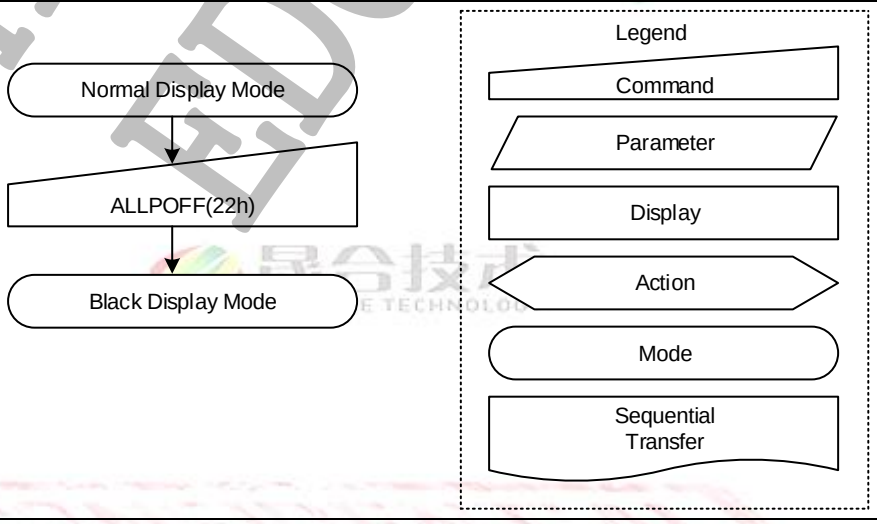
5.2.17 ALLPOFF (22h): All Pixel Off

22H	ALLPOFF (All Pixel Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	1	0	22
Parameter	No Parameter									
Description	This command turns the display panel black in sleep out mode. It also turns on/off the status of the DISPON/DISPOFF register. This command does not change the content of frame memory or any other status.  'All Pixel On'(23h) or 'Normal Display'(13h) commands are used to leave this mode. The display panel shows the display content from Host after 'Normal Display' command.									
Restriction	This command has no effect if module is already in all pixels off mode.									

Register Availability	**Status**	**Availability**
	Sleep Out	Yes (Reflect in the next V-sync period).
	Sleep In	Yes

Default	**Status**	**Default Value**
	Power On Sequence	Normal Display Mode On
	S/W Reset	Normal Display Mode On
	H/W Reset	Normal Display Mode On

Flow Chart



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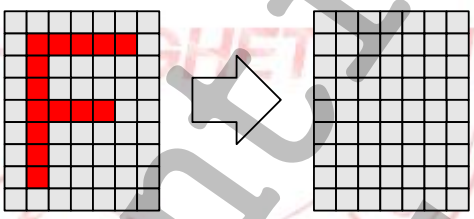
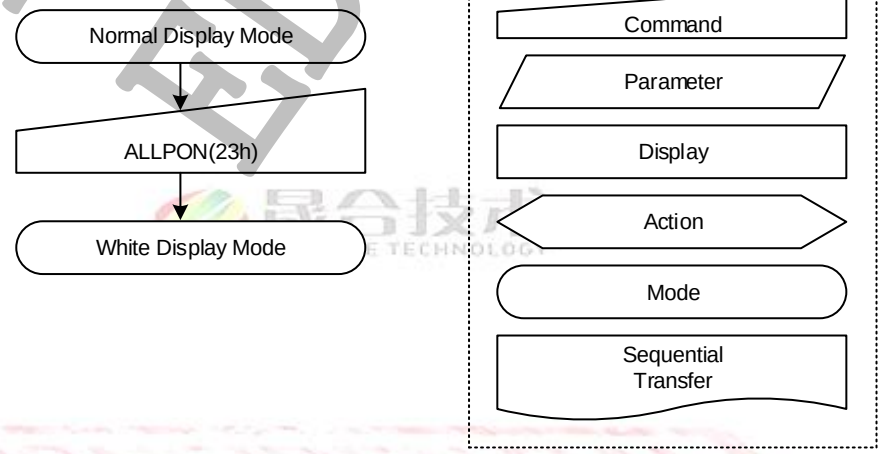
5.2.18 ALLPON (23h): All Pixel On

23H	ALLPON (All Pixel On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	0	0	1	1	23
Parameter	No Parameter									
Description	This command turns the display panel white in sleep out mode. It also turns out on/ off the status of the DISPON/DISPOFF register. This command does not change the content of frame memory or any other status. (Example) Memory Display  'All Pixel Off'(22h), 'Normal Display'(13h) commands are used to leave this mode. The display panel shows the display content after 'Normal Display' command.									
Restriction	This command has no effect If the module is already in all pixels on mode.									

Register Availability	**Status**	**Availability**
	Sleep Out	Yes (Reflect in the next V-sync period).
	Sleep In	Yes

Default	**Status**	**Default Value**
	Power On Sequence	Normal Display Mode On
	S/W Reset	Normal Display Mode On
	H/W Reset	Normal Display Mode On

Flow Chart



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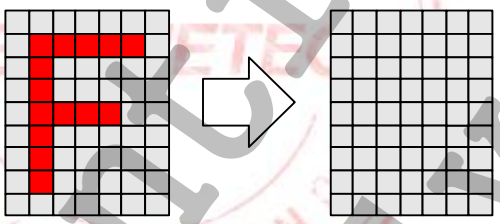
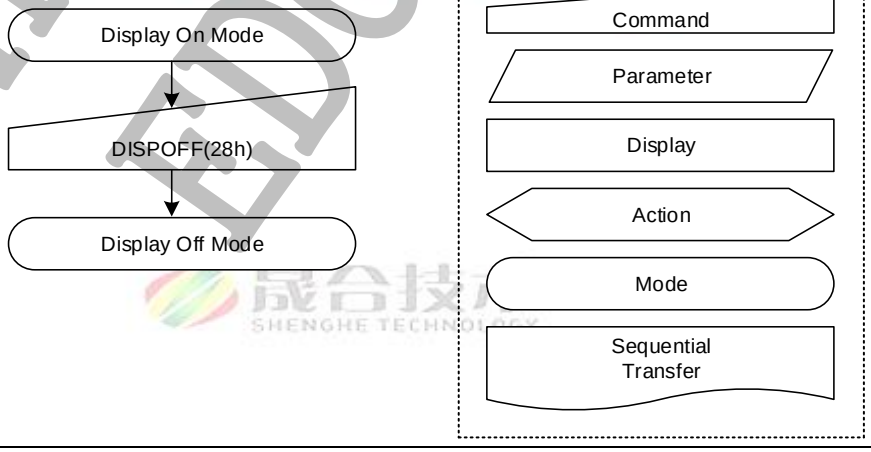
5.2.19 DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	0	0	28
Parameter	No Parameter									
Description	This command is used to enter into Display Off mode. This command does not change any other status except bit D2 of RDDPM command (0Ah). There will be no abnormal visible effect on the display (Example) Host Display 									
Restriction	This command has no effect when module is already in display off mode.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					Display Off				
	S/W Reset					Display Off				
	H/W Reset					Display Off				
Flow Chart										

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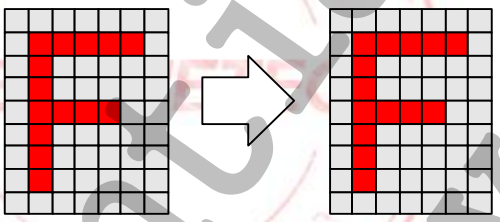
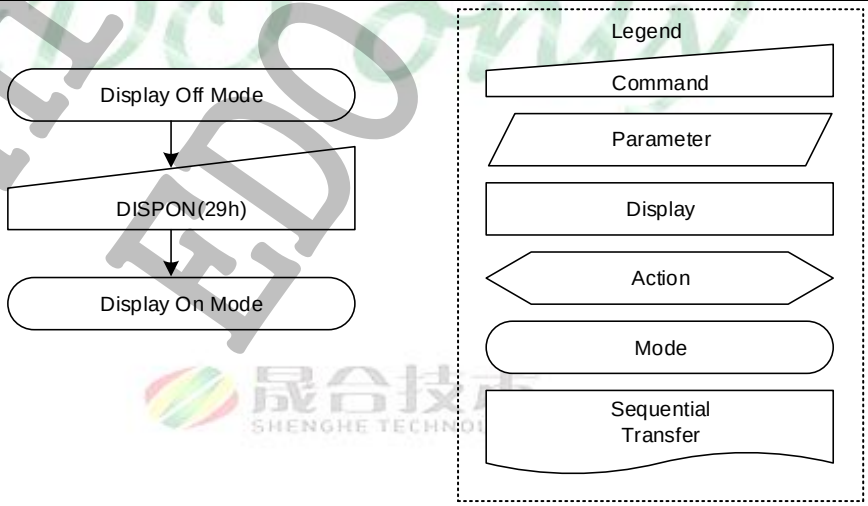
5.2.20 DISPON (29h): Display On

29H	DISPON (Display On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	0	1	29
Parameter	No Parameter									
Description	This command is used to recover from Display Off Mode. This command does not change any other status except bit D2 of RDDPM command (0Ah). (Example) Host Display 									
Restriction	This command has no effect when module is already in display on mode.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					Display Off				
	S/W Reset					Display Off				
	H/W Reset					Display Off				
Flow Chart										

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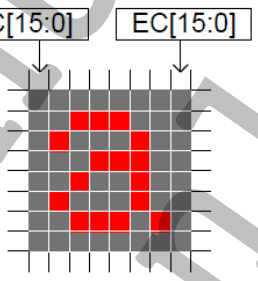
5.2.21 CASET (2Ah): Column Address Set

2AH	CASET (Column Address Set)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	1	0	2A
1st Para	Write	SC[15:8]								00
2nd Para	Write	SC[7:0]								00
3rd Para	Write	EC[15:8]								01
4th Para	Write	EC[7:0]								DF

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
Each value represents on column line in the frame memory.
Example)



- **SC[15:0]** : Start of Column
- **EC[15:0]** : End of Column

Restriction

SC[15:0] must always be less than EC[15:0]
If transferred image size is bigger than setting window size, abnormal display is occurred.
So transferred image size should be same as setting window size.
The SC[15:0] and EC[15:0]-SC[15:0]+1 must be divisible by 2.

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	SC[15:0]	EC[15:0]
Power On Sequence	00_00h	01_DFh
S/W Reset	00_00h	01_DFh
H/W Reset	00_00h	01_DFh

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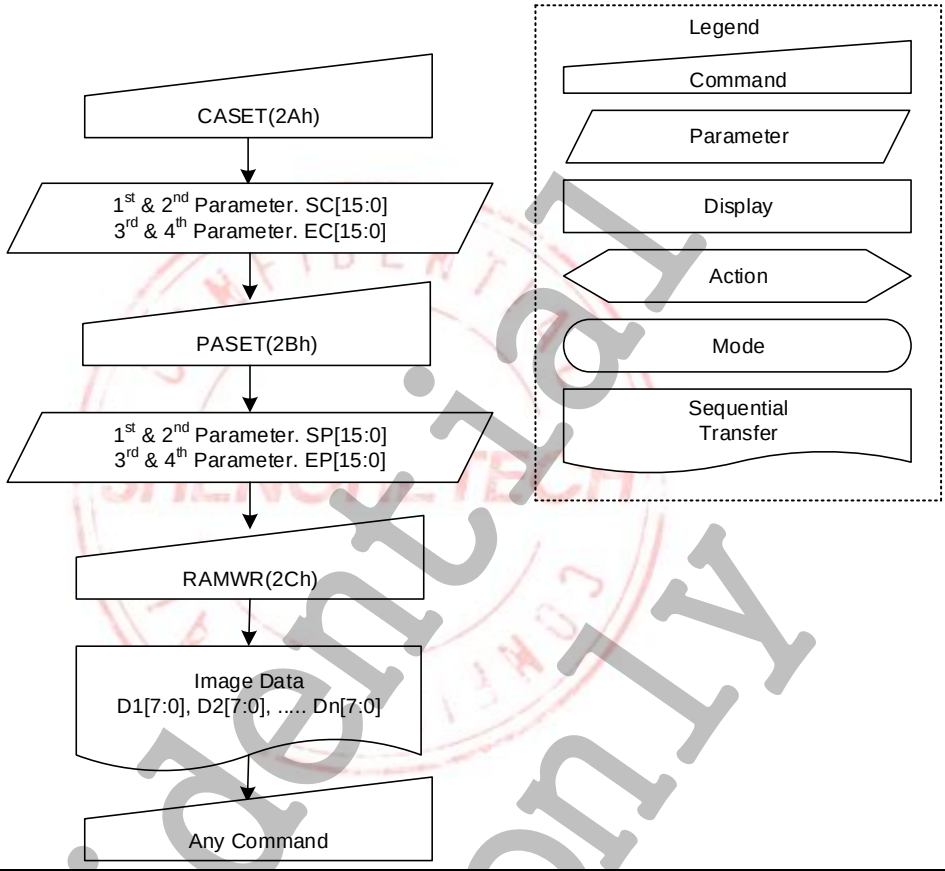
Flow Chart



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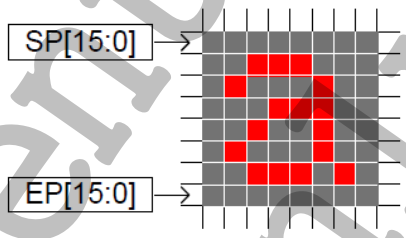
5.2.22 PASET (2Bh): Page Address Set

2BH	PASET (Page Address Set)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	0	1	1	2B
1st Para	Write	SP[15:8]								00
2nd Para	Write	SP[7:0]								00
3rd Para	Write	EP[15:8]								01
4th Para	Write	EP[7:0]								DF

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
Each value represents on page line in the frame memory.
Example)



- **SP[15:0]**: Start of Page
- **EP[15:0]**: End of Page

Restriction

SP[15:0] must always be less than EP[15:0]
If SP[15:0] or EP[15:0] is greater than the available frame memory, then the parameter is not updated.
The SP[15:0] and EP[15:0]-SP[15:0]+1 must be divisible by 2.

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	SP[15:0]	EP[15:0]
Power On Sequence	00_00h	01_DFh
S/W Reset	00_00h	01_DFh
H/W Reset	00_00h	01_DFh

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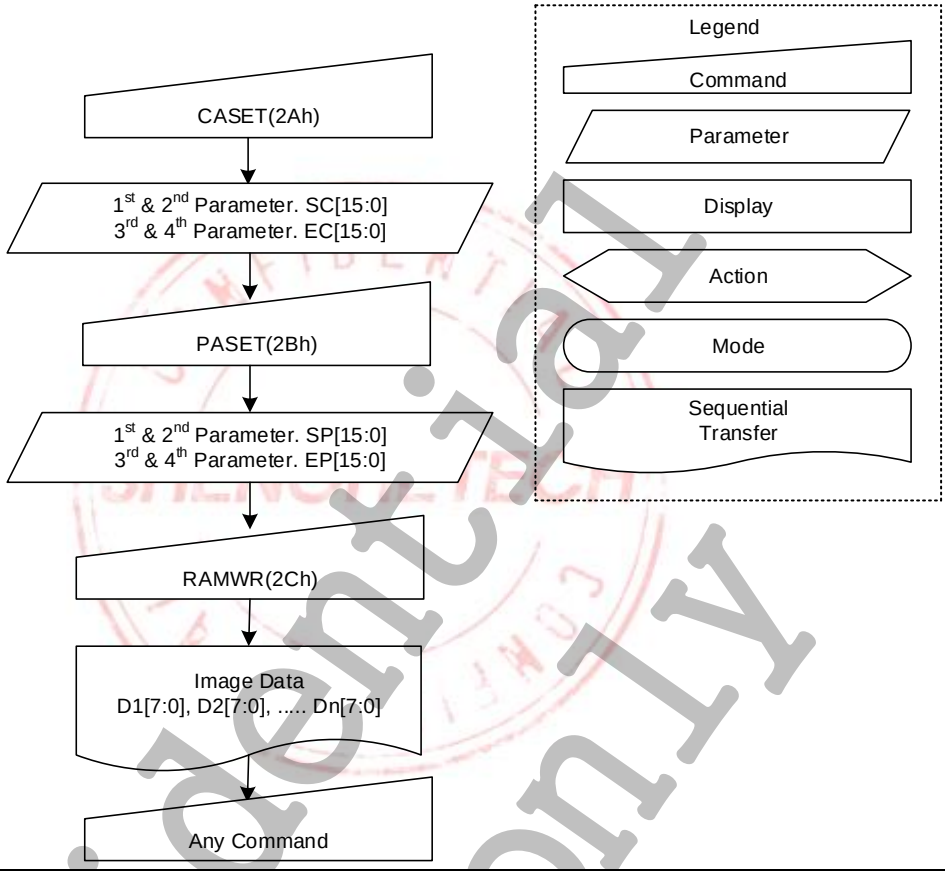
Flow Chart



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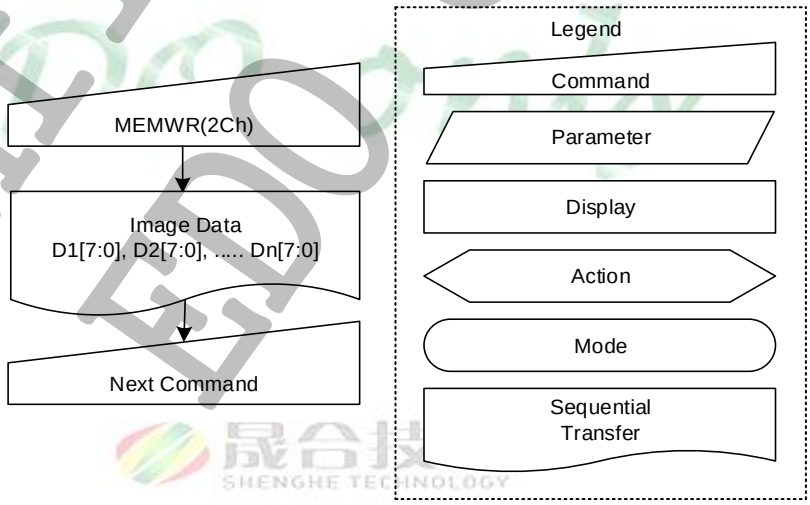
5.2.23 RAMWR (2Ch): Memory Write Start

2CH	RAMWR (Memory Write Start)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	0	1	1	0	0	2C
1st Para	Write	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	00
2nd Para	Write	D2[7]	D2[6]	D2[5]	D2[4]	D2[3]	D2[2]	D2[1]	D2[0]	00
…										
Nth Para	Write	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to (“0000”/”0000”). Then Dn[7:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame write.									
Restriction	There is no restriction on length of parameters. No access in the frame memory in sleep in mode.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					Contents of memory is set randomly				
	S/W Reset					Contents of memory is set randomly				
	H/W Reset					Contents of memory is set randomly				
Flow Chart										

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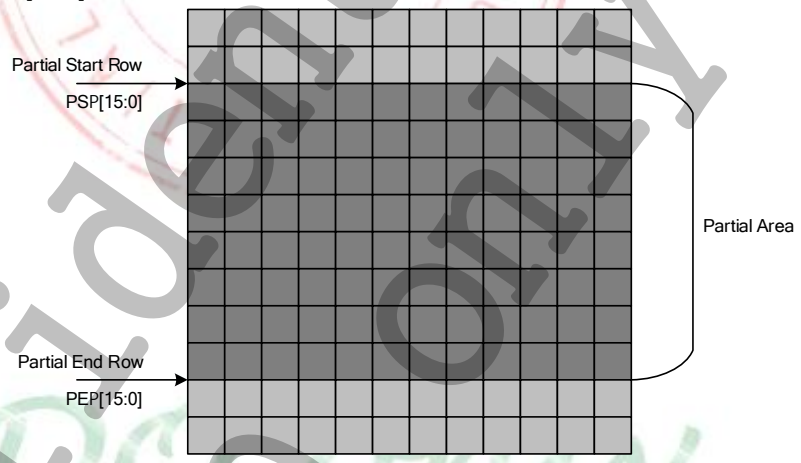
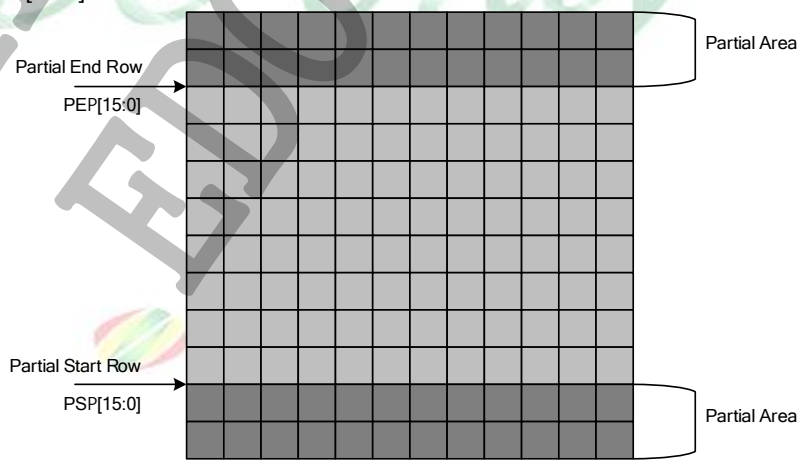
5.2.24 PTLAR (30h): Partial Area Row Set

30H	PTLAR (Partial Area Row Set)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	0	0	0	0	30
1st Para	Write	PSP[15:8]								00
2nd Para	Write	PSP[7:0]								00
3rd Para	Write	PEP[15:8]								01
4th Para	Write	PEP[7:0]								DF
Description	This command defines the partial display mode's display area. There are two parameters associated with this command, the first defines the partial start row(PSP) and the second the partial end row(PEP). As illustrated in the figures below. PSP[15:0] and PEP[15:0] refer to the Frame Memory Line Pointer. Example) If PEP[15:0] > PSP[15:0]  If PSP[15:0] > PEP[15:0]  									
Restriction	PSP[15:0] and PEP[15:0] cannot be 0000h nor exceed the last vertical line number. The setting of PSP[15:0] and PEP[15:0] must be a multiple of 2.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes (Reflect in the next V-sync period).				

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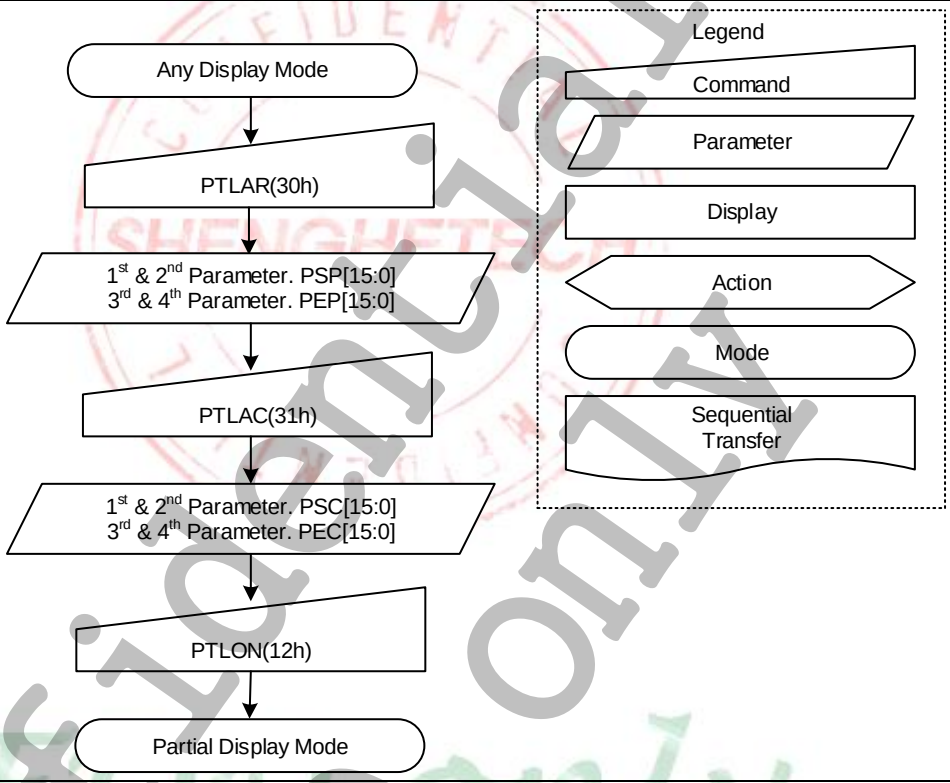
	Sleep In	Yes
Default	**Status**	**Default Value**
	Power On Sequence	00_00h / 01_DFh
	S/W Reset	00_00h / 01_DFh
	H/W Reset	00_00h / 01_DFh
Flow Chart		

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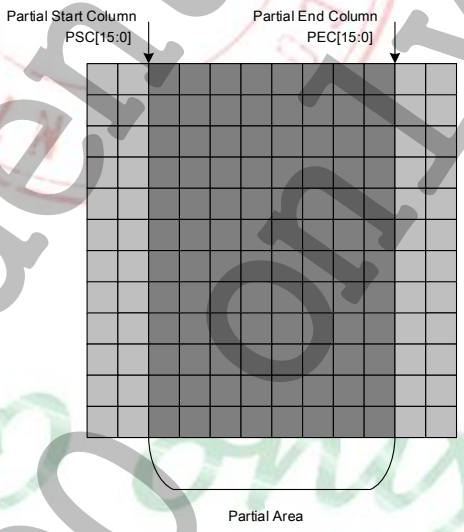
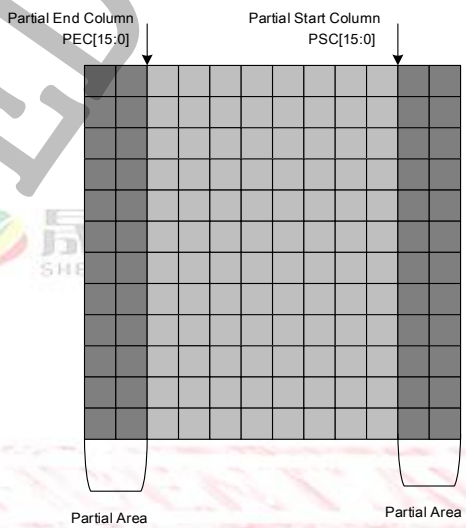
5.2.25 PTLAC (31h): Partial Area Column Set

31H	PTLAC (Partial Area Column Set)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	0	0	0	1	31
1st Para	Write	PSC[15:8]								00
2nd Para	Write	PSC[7:0]								00
3rd Para	Write	PEC[15:8]								01
4th Para	Write	PEC[7:0]								DF
Description	This command defines the partial display mode's display area. There are two parameters associated with this command, the first defines the partial start column(PSC) and the second the partial end column(PEC). As illustrated in the figures below. PSC[15:0] and PEC[15:0] refer to the Frame Memory Line Pointer. Example) If PEC[15:0] > PSC[15:0]  If PSC[15:0] > PEC[15:0]  									

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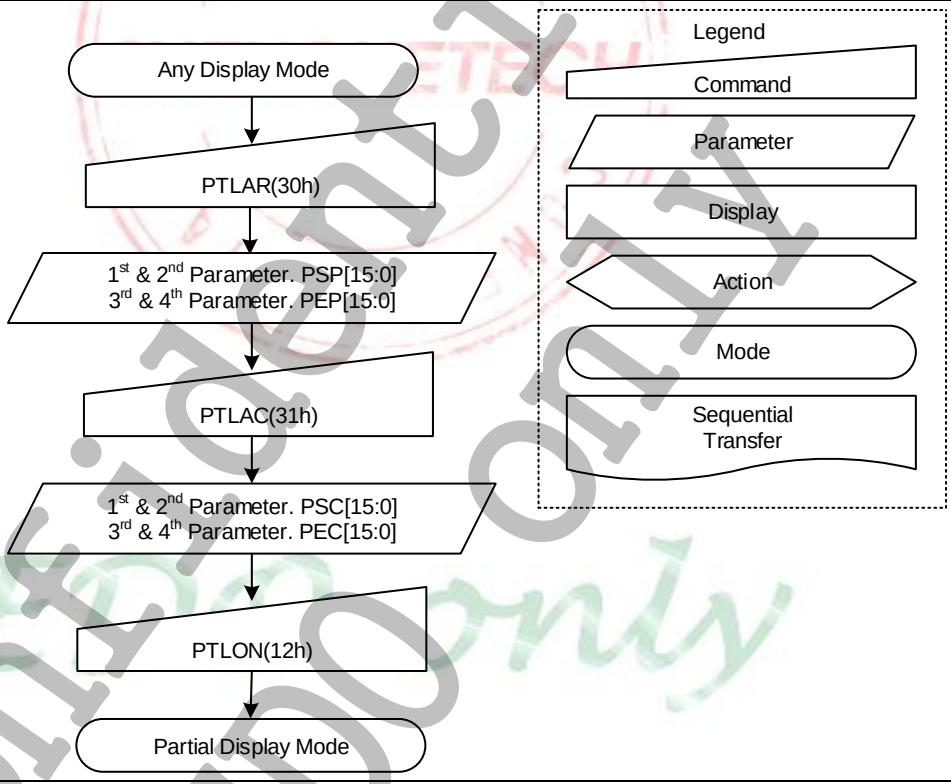
Restriction	PSC[15:0] and PEC[15:0] cannot be 0000h nor exceed the last pixel number. The setting of PSC[15:0] and PEC[15:0] must be a multiple of 2.	
Register Availability	**Status**	**Availability**
	Sleep Out	Yes (Reflect in the next V-sync period).
	Sleep In	Yes
Default	**Status**	**Default Value**
	Power On Sequence	00_00h / 01_DFh
	S/W Reset	00_00h / 01_DFh
	H/W Reset	00_00h / 01_DFh
Flow Chart		

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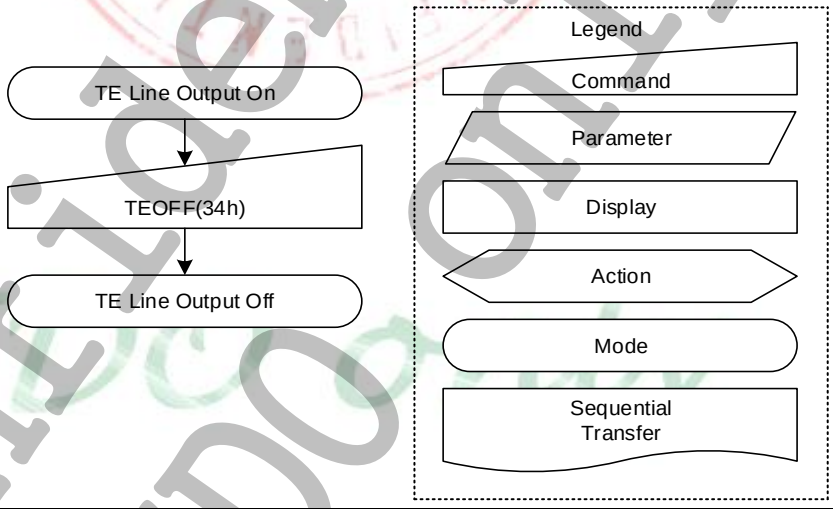
5.2.26 TEOFF (34h): Tearing Effect Off

34H	TEOFF (Tearing Effect Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	0	1	0	0	34
Parameter	No Parameter									
Description	This command is used to turn off (Active Low) the Tearing Effect output signal from TE signal line.									
Restriction	This command has no effect when Tearing Effect output is already OFF.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					Off				
	S/W Reset					Off				
	H/W Reset					Off				
Flow Chart										

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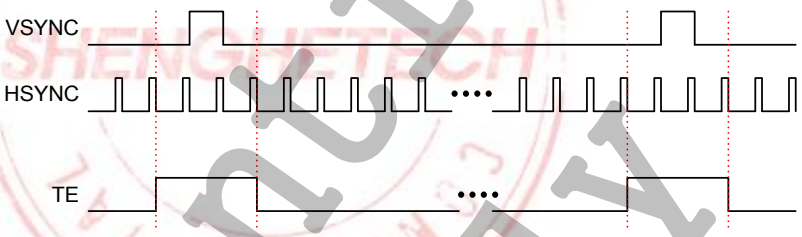
5.2.27 TEON (35h): Tearing Effect On

35H	TEON (Tearing Effect On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	0	1	0	1	35
1st Para	Write	0	0	0	0	0	0	0	TEM	00

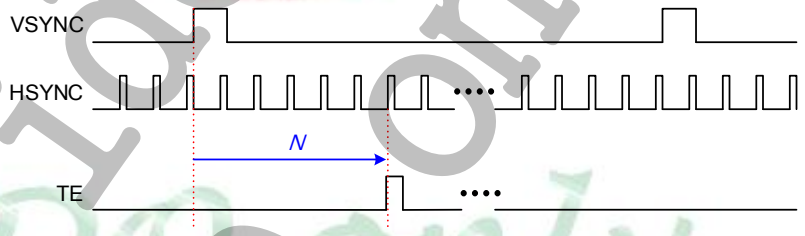
Description

This command is used to turn on the Tearing Effect output signal from the TE signal line.
The TEON has one parameter that describes the mode of the Tearing Effect Output Line.

When **TEM** = 0 & **TE_SCANLINE** (in TESCAN, 44h) = 0: TE Output line consists of V-Blanking information only



When **TEM** = 0 & **TE_SCANLINE** (in TESCAN, 44h) = N (N≠0): TE Output line consists of one H-Blanking information only



When **TEM** = 1: TE Output line consists of one V-Blanking and H-Blanking information

NOTE: NOTE: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already On.
For enabling Tearing Effect Bus Trigger information, parameter TEM should be "0".

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing effect off & TEM = "0"
S/W Reset	Tearing effect off & TEM = "0"
H/W Reset	Tearing effect off & TEM = "0"

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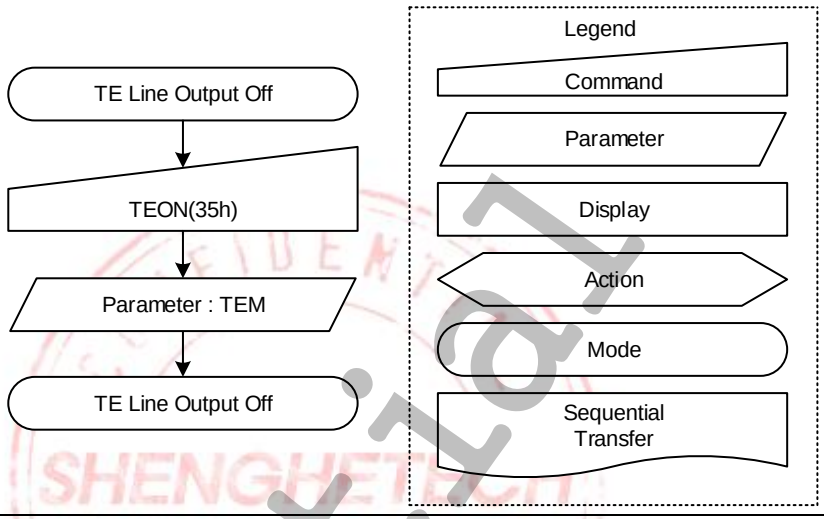
Flow Chart	

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5.2.28 MADCTL (36h): Memory Data Access Control

<table>
<tr><th>36H</th><th colspan="10">MADCTL (Memory Data Access Control)</th></tr>
<tr><td>–</td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36</td></tr>
<tr><td>Parameter</td><td>Write</td><td>0</td><td>MX</td><td>0</td><td>0</td><td>BGR</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td rowspan="11">Description</td><td colspan="10">This command indicates the current status of the display as described in the table below</td></tr>
<tr><td colspan="2">Bit</td><td colspan="4">Description</td><td colspan="4">Remark</td></tr>
<tr><td colspan="2">D7</td><td colspan="4">Reserved</td><td colspan="4">Set to "0"</td></tr>
<tr><td colspan="2">D6</td><td colspan="4">Memory Write Direction Horizontal Flip</td><td colspan="4">-</td></tr>
<tr><td colspan="2">D5</td><td colspan="4">Reserved</td><td colspan="4">Set to "0"</td></tr>
<tr><td colspan="2">D4</td><td colspan="4">Reserved</td><td colspan="4">Set to "0"</td></tr>
<tr><td colspan="2">D3</td><td colspan="4">RGB/BGR Order</td><td colspan="4">–</td></tr>
<tr><td colspan="2">D2</td><td colspan="4">Reserved</td><td colspan="4">Set to "0"</td></tr>
<tr><td colspan="2">D1</td><td colspan="4">Reserved</td><td colspan="4">Set to "0"</td></tr>
<tr><td colspan="2">D0</td><td colspan="4">Reserved</td><td colspan="4">Set to "0"</td></tr>
<tr><td colspan="10">• D[7] - Reserved
This bit is not applicable for this project, so it is set to "0".
• MX - Memory Write Direction Horizontal Flip
0 = Memory write forward direction
1 = Memory write reverse direction
• D[5:4] - Reserved
These bits are not applicable for this project, sot it is set to “0”.
• BGR - RGB/BGR Order
0 = RGB Order
1 = BGR Order
• D[2:0] - Reserved
This bit is not applicable for this project, so it is set to "0".</td></tr>
<tr><td>Restriction</td><td colspan="10">–</td></tr>
<tr><td rowspan="3">Register Availability</td><td colspan="5">Status</td><td colspan="5">Availability</td></tr>
<tr><td colspan="5">Sleep Out</td><td colspan="5">D[3] : Yes (Reflect in next V-sync period)</td></tr>
<tr><td colspan="5">Sleep In</td><td colspan="5">Yes</td></tr>
<tr><td rowspan="4">Default</td><td colspan="5">Status</td><td colspan="5">Default Value</td></tr>
<tr><td colspan="5">Power On Sequence</td><td colspan="5">00h</td></tr>
<tr><td colspan="5">S/W Reset</td><td colspan="5">00h</td></tr>
<tr><td colspan="5">H/W Reset</td><td colspan="5">00h</td></tr>
</table>

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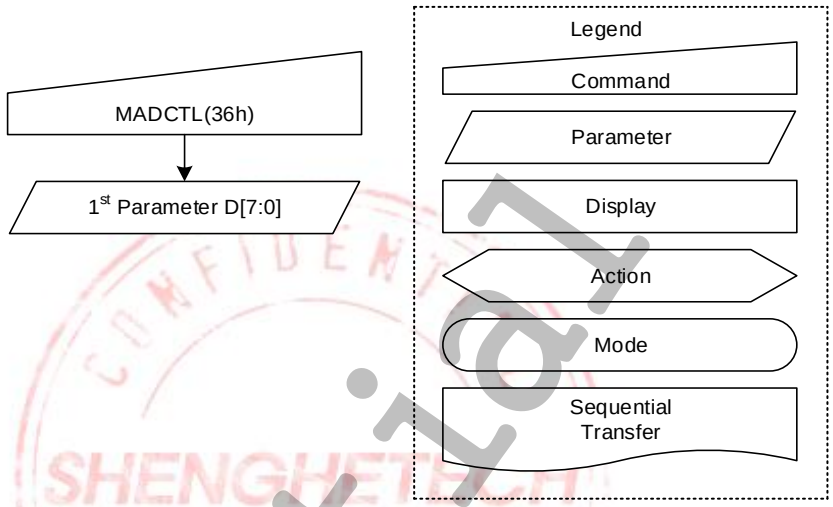
Flow Chart	

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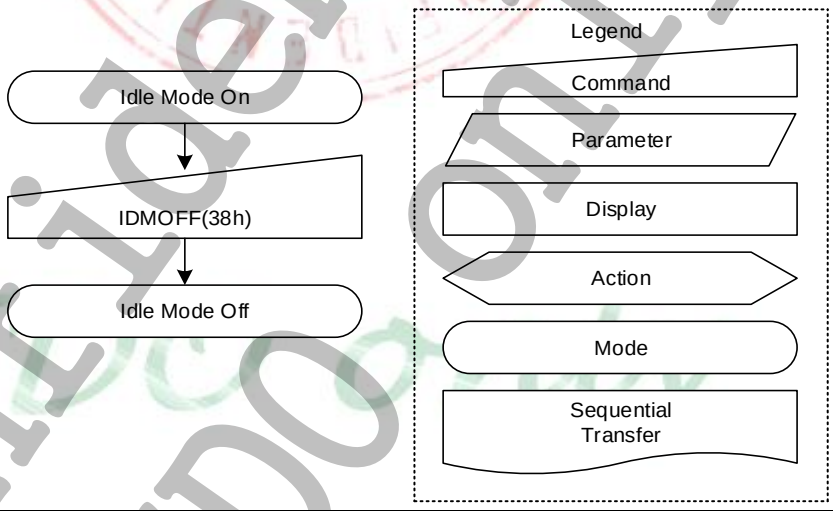
5.2.29 IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	0	0	0	38
Parameter	No Parameter									
Description	This command causes the display module to exit Idle mode.									
Restriction	This command has no effect when the display module is not in Idle mode.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					Off				
	S/W Reset					Off				
	H/W Reset					Off				
Flow Chart										

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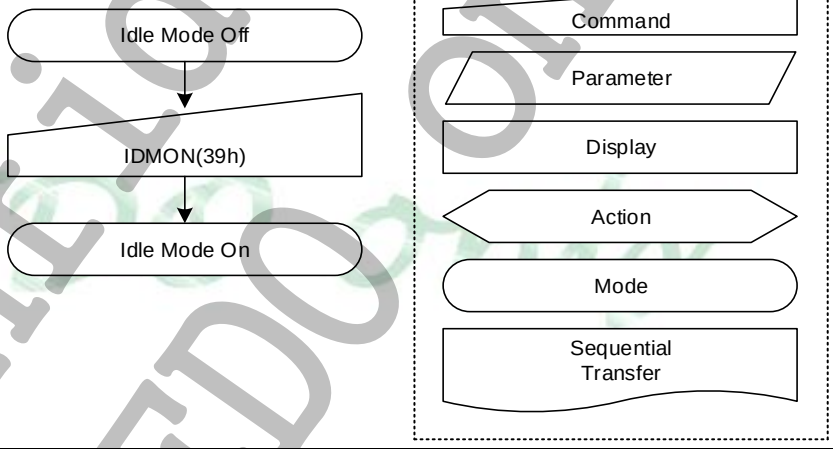
5.2.30 IDMON (39h): Idle Mode On

39H	IDMON (Idle Mode On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	0	0	1	39
Parameter	No Parameter									
Description	This command causes the display module to enter Idle mode. In idle mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the frame memory.									
Restriction	This command has no effect when the display module is in Idle mode.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes (Reflect in next V-sync period)				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					Off				
	S/W Reset					Off				
	H/W Reset					Off				
Flow Chart										

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5.2.31 COLMOD (3Ah): Control Interface Pixel Format

<table>
<tr><th>3AH</th><th colspan="10">COLMOD (Control Interface Pixel Format)</th></tr>
<tr><td>–</td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3A</td></tr>
<tr><td>1st Para</td><td>Write</td><td>SPI_PF_SEL</td><td colspan="3">VIPF[2:0]</td><td>0</td><td colspan="3">IFPF[2:0]</td><td>77</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to define the format of RGB picture data.
The formats are shown in the table:
• SPI_PF_SEL – SPI Pixel Format Selection.
0 = IFPF[2:0] is used by the SPI interface.
1 = VIPF[2:0] is used by the SPI interface.
• VIPF[2:0] – This command is used by SPI_PF_SEL=1.
• D[3] - Reserved
This bit is not applicable for this project, so it is set to "0".
• IFPF[2:0] – This command is used by SPI_PF_SEL=0 or MIPI command mode.</td></tr>
<tr><td></td><td colspan="5">Control Interface Pixel Format</td><td colspan="2">IFPF[2]</td><td colspan="2">IFPF[1]</td><td>IFPF[0]</td></tr>
<tr><td></td><td colspan="5">24-bit/pixel(16.7M Color)</td><td colspan="2">1</td><td colspan="2">1</td><td>1</td></tr>
<tr><td></td><td colspan="5">18-bit/pixel(262K Color)</td><td colspan="2">1</td><td colspan="2">1</td><td>0</td></tr>
<tr><td></td><td colspan="5">16-bit/pixel(65K Color)</td><td colspan="2">1</td><td colspan="2">0</td><td>1</td></tr>
<tr><td></td><td colspan="5">Setting Disable</td><td colspan="2">1</td><td colspan="2">0</td><td>0</td></tr>
<tr><td></td><td colspan="5">3-bit/pixel(8 Color)</td><td colspan="2">0</td><td colspan="2">1</td><td>1</td></tr>
<tr><td></td><td colspan="5">8-bit/pixel(256 Color, 3-3-2)</td><td colspan="2">0</td><td colspan="2">1</td><td>0</td></tr>
<tr><td></td><td colspan="5">8-bit/pixel(256 Gray)</td><td colspan="2">0</td><td colspan="2">0</td><td>1</td></tr>
<tr><td></td><td colspan="5">Setting Disable</td><td colspan="2">0</td><td colspan="2">0</td><td>0</td></tr>
<tr><td></td><td colspan="10">NOTE: Pixel Format is set by video packet header in video mode.</td></tr>
<tr><td>Restriction</td><td colspan="10">–</td></tr>
<tr><td rowspan="3">Register Availability</td><td colspan="6">Status</td><td colspan="4">Availability</td></tr>
<tr><td colspan="6">Sleep Out</td><td colspan="4">Yes</td></tr>
<tr><td colspan="6">Sleep In</td><td colspan="4">Yes</td></tr>
<tr><td rowspan="4">Default</td><td colspan="6">Status</td><td colspan="4">Default Value</td></tr>
<tr><td colspan="6">Power On Sequence</td><td colspan="4">77h</td></tr>
<tr><td colspan="6">S/W Reset</td><td colspan="4">77h</td></tr>
<tr><td colspan="6">H/W Reset</td><td colspan="4">77h</td></tr>
</table>

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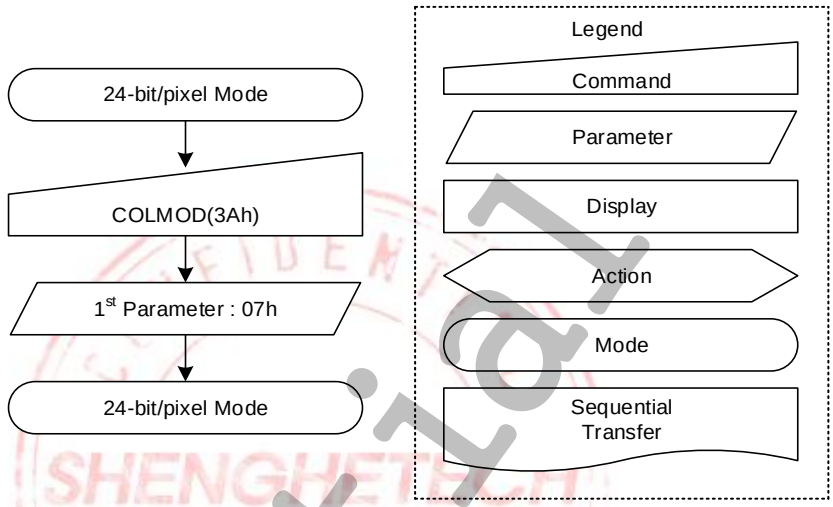
Flow Chart	

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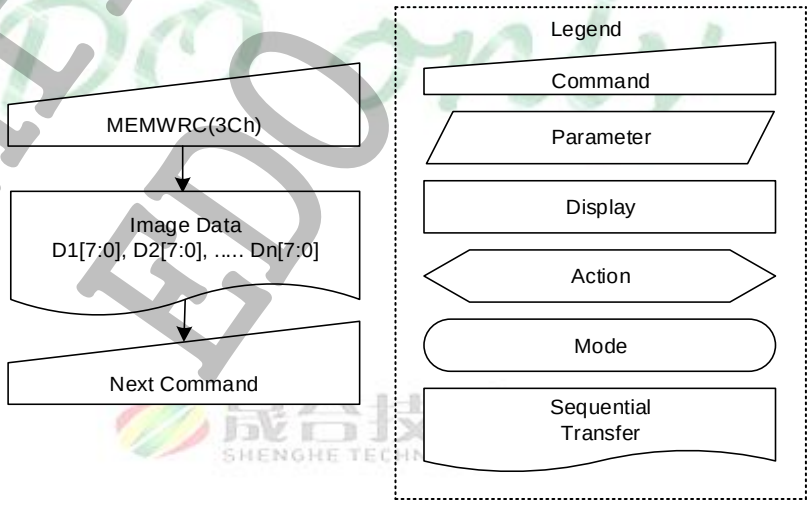
5.2.32 RAMWRC (3Ch): Memory Write Continue

3CH	RAMWRC (Memory Write Continue)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	0	1	1	1	1	0	0	3C
1st Para	Write	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	00
2nd Para	Write	D2[7]	D2[6]	D2[5]	D2[4]	D2[3]	D2[2]	D2[1]	D2[0]	00
---	---	---	---	---	---	---	---	---	---	00
Nth Para	Write	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	00
Description	This command is used to transfer data from MCU to frame memory if user wants to continue memory write after “Memory Write Start(2Ch)” command or “Memory Write Continue(3Ch)”. This command makes no change to the other driver status. When this command is accepted and Dn[7:0] is transferred from MCU, the column register and the page register are incremented from the value which has been arrived by previous memory write operation(2CH or 3Ch).									
Restriction	Host Must send multiple of 4 parameters at once. If host does not, memory write function will not operate properly.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					Contents of memory is set randomly				
	S/W Reset					Contents of memory is set randomly				
	H/W Reset					Contents of memory is set randomly				
Flow Chart										

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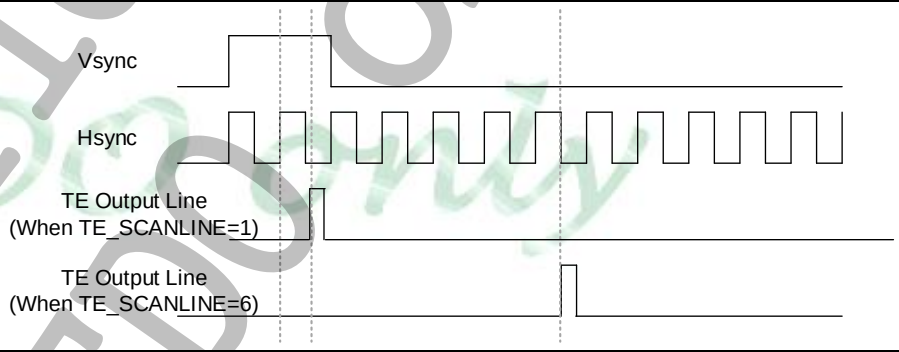
5.2.33 TESCAN (44h): Set Tear Scan Line

<table>
<tr><td>44H</td><td colspan="11">TESCAN (Set Tear Scan line)</td></tr>
<tr><td>–</td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>44</td></tr>
<tr><td>1st Para</td><td>Write</td><td colspan="8">TE_SCANLINE[15:8]</td><td>00</td></tr>
<tr><td>2nd Para</td><td>Write</td><td colspan="8">TE_SCANLINE[7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="11">This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. When TE_SCANLINE = "1", Tearing Effect Output Line is on at the second line of VSYNC.
The Tearing Effect Output line shall be active low when the display module is in Sleep mode.
Note that TE_SCANLINE with N = "0" is equivalent to TEON with TEM = "0".
<table>
<tr><td>35h</td><td>44h</td><td colspan="9" rowspan="2">TE Output</td></tr>
<tr><td>TEM</td><td>TE_SCANLINE</td></tr>
<tr><td>0</td><td>0</td><td colspan="9">The Tearing Effect Output line consists of V-blanking information only.
 
</td></tr>
<tr><td>0</td><td>≠0</td><td colspan="9">The Tearing Effect Output Line consists of Nth line information
 
</td></tr>
<tr><td>1</td><td>X</td><td colspan="9">The Tearing Effect Output line consists of V-blanking information only.
 
</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="11">This command takes effect on the frame following the current frame. Therefore, if the Tear Effect (TE) output is already ON, the TE output shall continue to operate as programmed by the previous TEON, or TESCAN, command until the end of the frame.
TE_SCANLINE[15:0] always must be less than VBP + VFP + VACT.</td></tr>
<tr><td>Register Availability</td><td colspan="6">Status</td><td colspan="5">Availability</td></tr>
<tr><td colspan="6">Sleep Out</td><td colspan="5">Yes</td></tr>
</table>

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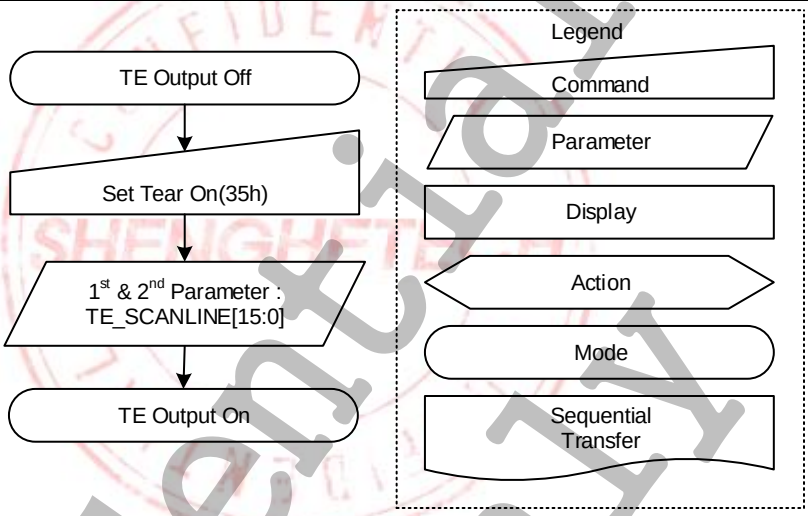
	Sleep In	Yes
Default	**Status**	**Default Value**
	Power On Sequence	00_00h
	S/W Reset	00_00h
	H/W Reset	00_00h
Flow Chart		

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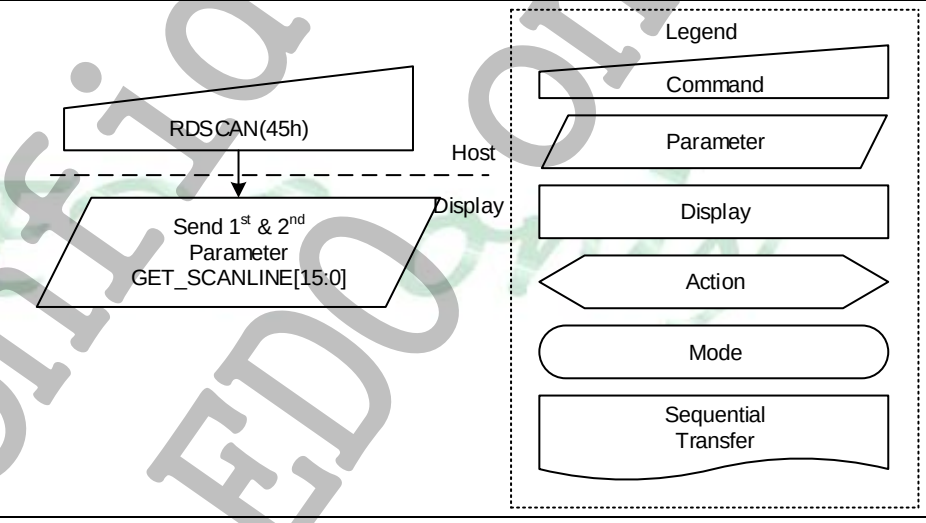
5.2.34 RDSCAN (45h): Read Scan Line Number

45H	RDSCAN (Read Scan Line Number)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	0	1	0	1	45
1st Para	Read	GET_SCANLINE[15:8]								00
2nd Para	Read	GET_SCANLINE[7:0]								00
Description	The display module returns the current scanline, N, used to update the display device. The first scanline is defined as the first line of Vsync and is denoted as line “0”. When in sleep mode, the value returned by RDSCAN is undefined.									
Restriction										

Register Availability	**Status**	**Availability**
	Sleep Out	Yes
	Sleep In	Yes

Default	**Status**	**Default Value**
	Power On Sequence	00_00h
	S/W Reset	00_00h
	H/W Reset	00_00h

Flow Chart



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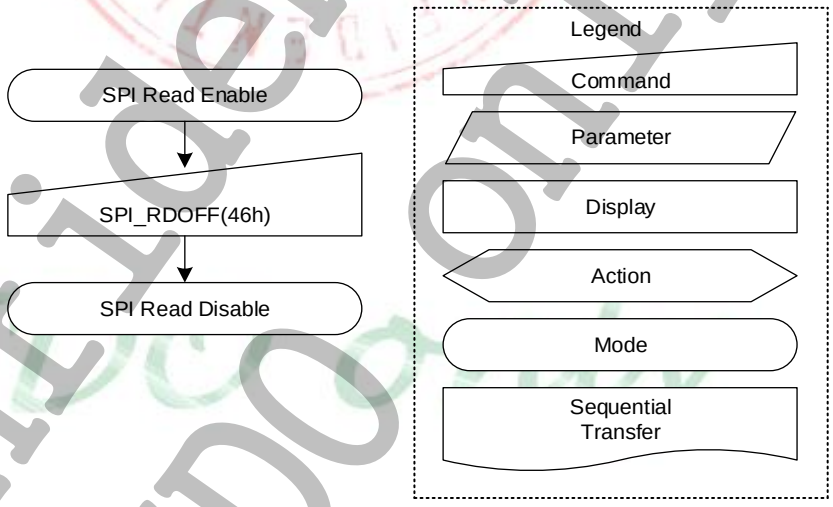
5.2.35 SPI_RDOFF (46h): SPI Read Off

46H	SPI_RDOFF (SPI Read Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	0	1	1	0	46
Parameter	No Parameter									
Description	This command disables SPI Read.									
Restriction	-									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes				
	Sleep In					No				
Default	**Status**					**Default Value**				
	Power On Sequence					Off				
	S/W Reset					Off				
	H/W Reset					Off				
Flow Chart										

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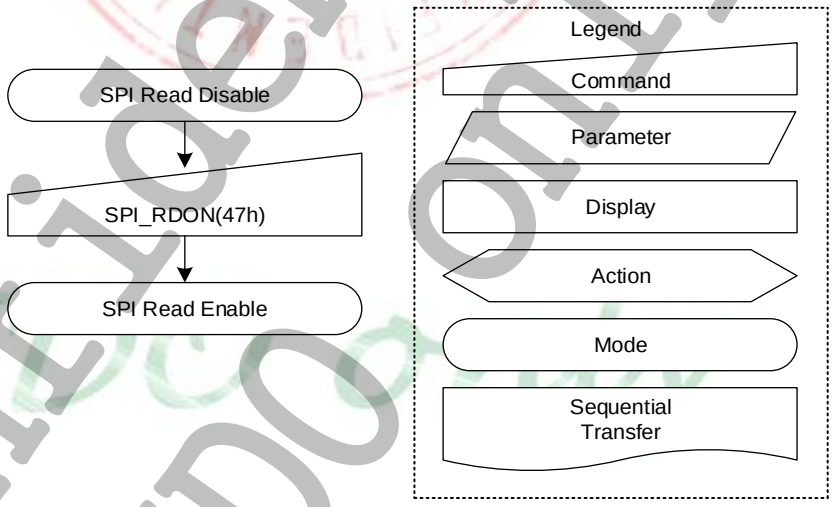
5.2.36 SPI_RDON(47h): SPI Read On

47H	SPI_RDON (SPI Read On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	0	1	1	1	47
Parameter	No Parameter									
Description	This command enables SPI Read.									
Restriction	-									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes				
	Sleep In					No				
Default	**Status**					**Default Value**				
	Power On Sequence					Off				
	S/W Reset					Off				
	H/W Reset					Off				
Flow Chart										

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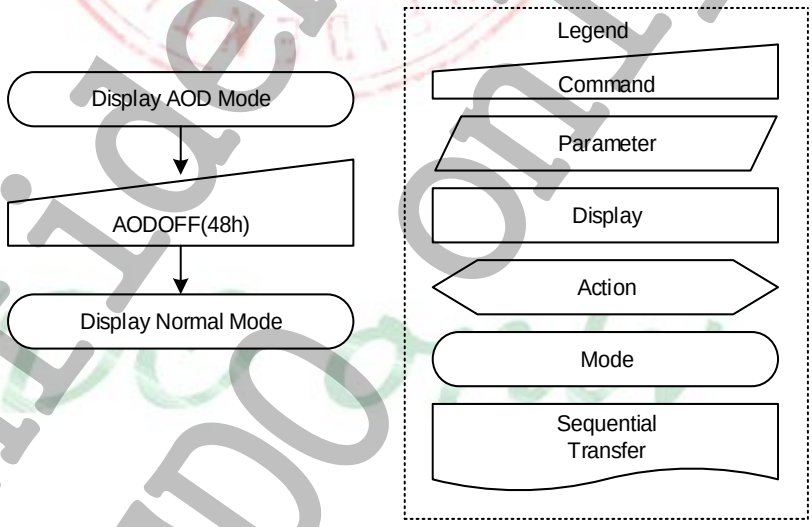
5.2.37 AODOFF (48h): AOD Mode Off

48H	AODOFF (AOD Mode Off)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	1	0	0	0	48
Parameter	No Parameter									
Description	This command turns off AOD mode.									
Restriction	-									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					AOD Off Mode				
	S/W Reset					AOD Off Mode				
	H/W Reset					AOD Off Mode				
Flow Chart										

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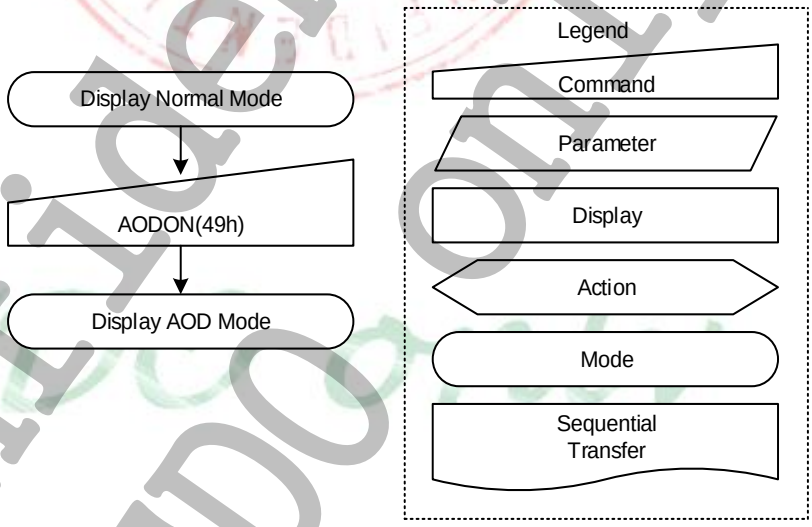
5.2.38 AODON (49h): AOD Mode On

49H	AODON (AOD Mode On)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	1	0	0	1	49
Parameter	No Parameter									
Description	This command turns on AOD mode.									
Restriction	-									

Register Availability	**Status**	**Availability**
	Sleep Out	Yes
	Sleep In	Yes

Default	**Status**	**Default Value**
	Power On Sequence	AOD Off Mode
	S/W Reset	AOD Off Mode
	H/W Reset	AOD Off Mode

Flow Chart



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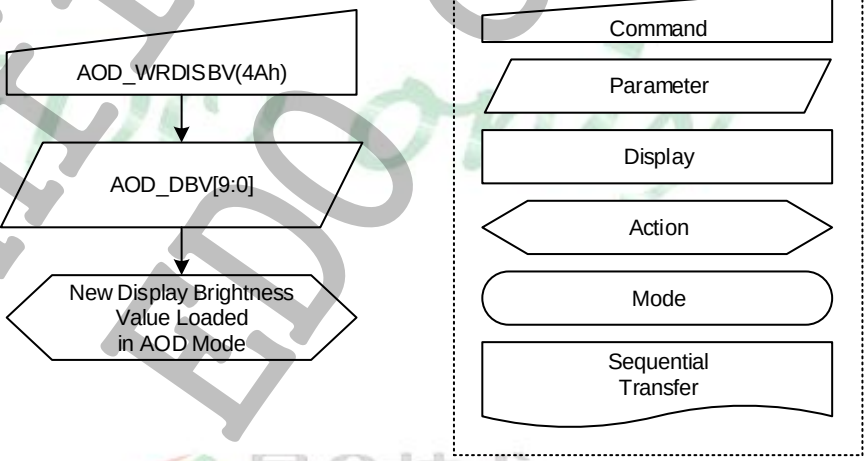
5.2.39 AOD_WRDISBV (4Ah): Write Display Brightness Value in AOD Mode

4AH	AOD_WRDISBV (Write Display Brightness Value in AOD Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	1	0	1	0	4A
1st Para	Write	AOD_DBV[7:0]								FF
2nd Para	Write	0	0	0	0	0	0	AOD_DBV[9:8]		00
Description	This command is used to adjust the brightness value of the display in AOD Mode. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 000h value means the lowest brightness and 3FFh value means the highest brightness.									
Restriction	–									

Register Availability	Status	Availability
	Sleep Out	Yes (Reflect in next V-sync period)
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	0_FFh
	S/W Reset	0_FFh
	H/W Reset	0_FFh

Flow Chart



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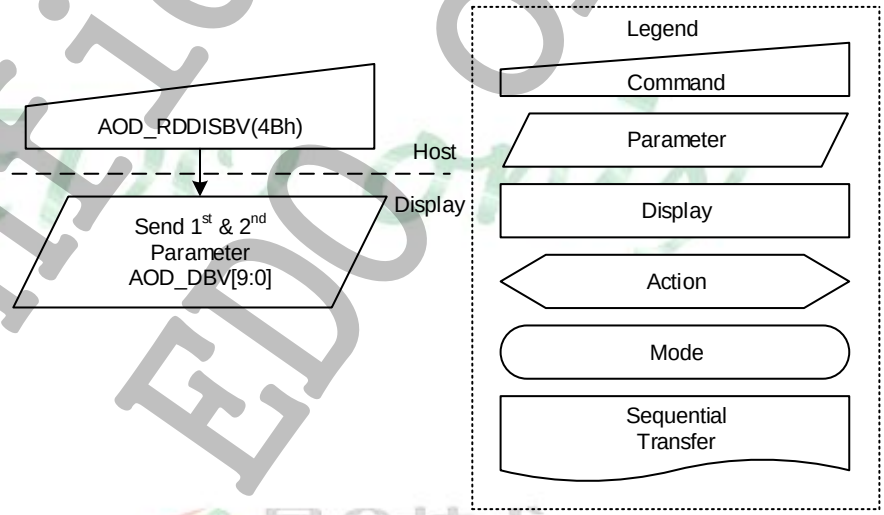
5.2.40 AOD_RDDISBV (4Bh): Read Display Brightness Value in AOD Mode

4BH	AOD_RDDISBV (Read Display Brightness Value in AOD Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	1	0	1	1	4B
1st Para	Read	AOD_DBV[7:0]								FF
2nd Para	Read	0	0	0	0	0	0	AOD_DBV[9:8]		00
Description	This command returns the brightness value of the display in AOD Mode. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. In principal relationship is that 000h value means the lowest brightness and 3FFh value means the highest brightness.									
Restriction	–									

Register Availability	Status	Availability
	Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	0_FFh
	S/W Reset	0_FFh
	H/W Reset	0_FFh

Flow Chart



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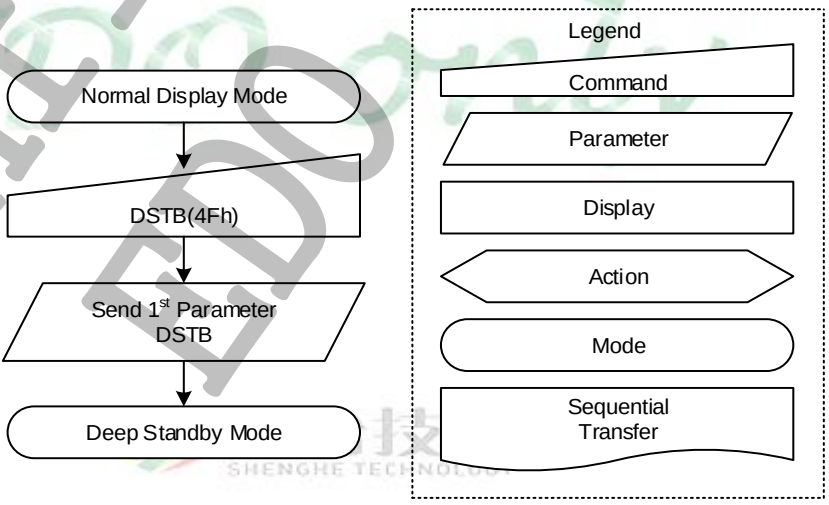
5.2.41 DSTB (4Fh): Deep Standby Control

4FH	DSTB (Deep Standby Control)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	0	1	1	1	1	4F
1st Para	Write	0	0	0	0	0	0	0	DSTB	00
Parameter	No Parameter									
Description	This command is used to control signal which are related to deep standby mode control ● **DSTB** : Deep standby mode control. 0 = Deep standby mode disable 1 = Deep standby mode enable To exit deep standby mode, set RESX low pulse more than 3ms to pin RESX. If user wants to enter deep standby mode from normal display directly, it shall enter sleep in mode & display off mode first, and wait 2 frames or more time for completing power off sequence, and then execute this command to enter deep standby mode									
Restriction	-									

Register Availability	**Status**	**Availability**
	Sleep Out	Yes
	Sleep In	Yes

Default	**Status**	**Default Value**
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

Flow Chart



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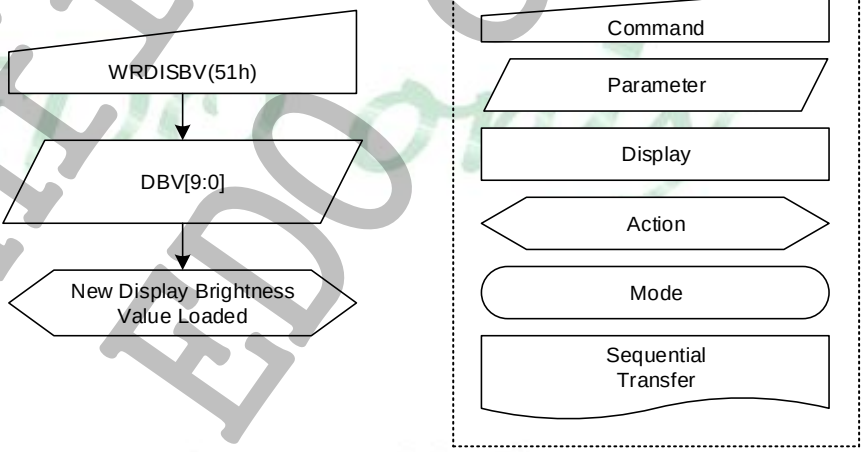
5.2.42 WRDISBV (51h): Write Display Brightness Value

51H	WRDISBV (Write Display Brightness Value)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	0	0	1	51
1st Para	Write	DBV[7:0]								FF
2nd Para	Write	0	0	0	0	0	0	DBV[9:8]		00
Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 000h value means the lowest brightness and 3FFh value means the highest brightness.									
Restriction	–									

Register Availability	**Status**	**Availability**
	Sleep Out	Yes (Reflect in next V-sync period)
	Sleep In	Yes

Default	**Status**	**Default Value**
	Power On Sequence	0_FFh
	S/W Reset	0_FFh
	H/W Reset	0_FFh

Flow Chart



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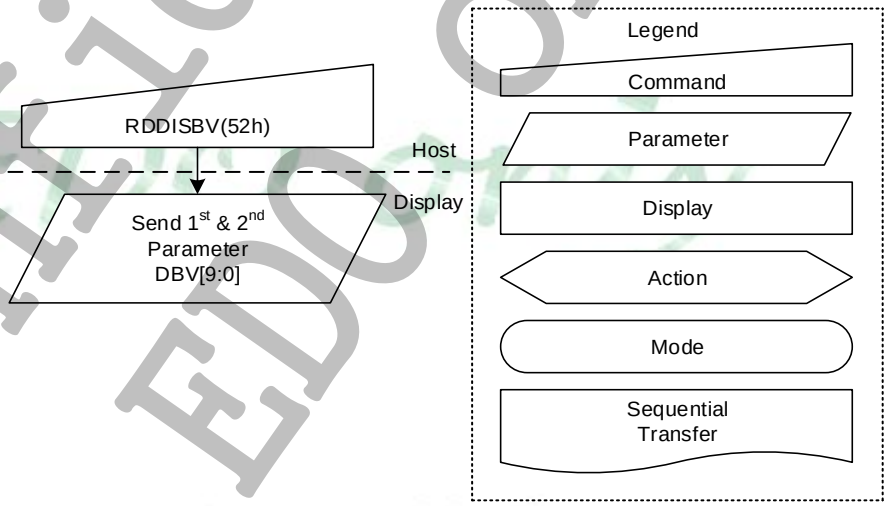
5.2.43 RDDISBV (52h): Read Display Brightness Value

52H	RDDISBV (Read Display Brightness Value)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	0	1	0	52
1st Para	Read	DBV[7:0]								FF
2nd Para	Read	0	0	0	0	0	0	DBV[9:8]		00
Description	This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. In principal relationship is that 000h value means the lowest brightness and 3FFh value means the highest brightness.									
Restriction	–									

Register Availability	Status	Availability
	Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	0_FFh
	S/W Reset	0_FFh
	H/W Reset	0_FFh

Flow Chart



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5.2.44 WRCTRLD1 (53h): Write CTRL Display 1

53H	WRCTRLD1 (Write CTRL Display 1)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	0	1	1	53
1st Para	Write	0	0	BCTRL	0	DISP_DIM	0	0	0	28

Description

This command control related display brightness.

- **D[7:6]** - Reserved.
  These bits are not applicable for this project, so it is set to "0".
- **BCTRL** - Brightness Control
  0 = Off
  1 = On
- **D[4]** - Reserved
  This bit is not applicable for this project, so it is set to “0”.
- **DISP_DIM** – Display Dimming
  0 = Display Dimming Off
  1 = Display Dimming On
- **D[2:0]** - Reserved
  These bits are not applicable for this project, so it is set to “0”.

Restriction

–

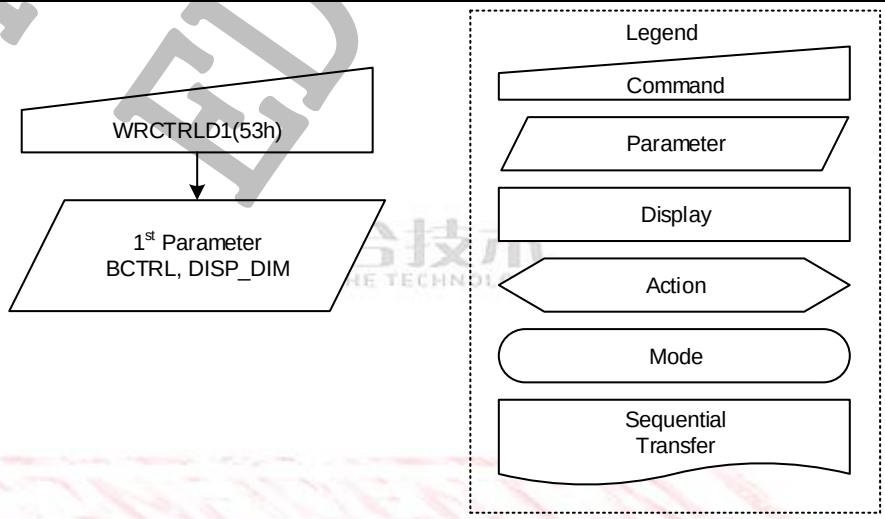
Register Availability

Status	Availability
Sleep Out	Yes (Reflect in next V-sync period)
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	28h
S/W Reset	28h
H/W Reset	28h

Flow Chart



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5.2.45 RDCTRLD1 (54h): Read CTRL Display 1

54H	RDCTRLD1 (Read CTRL Display 1)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	1	0	0	54
1st Para	Read	0	0	BCTRL	0	DISP_DIM	0	0	0	28

Description

This command returns the brightness value of 'Write CTRL Display 1'.

- **D[7:6]** - Reserved.
  These bits are not applicable for this project, so it is set to "0".
- **BCTRL** - Brightness Control
  0 = Off
  1 = On
- **D[4]** - Reserved
  This bit is not applicable for this project, so it is set to "0".
- **DISP_DIM** – Display Dimming
  0 = Display Dimming Off
  1 = Display Dimming On
- **D[2:0]** - Reserved
  These bits are not applicable for this project, so it is set to "0".

Restriction

–

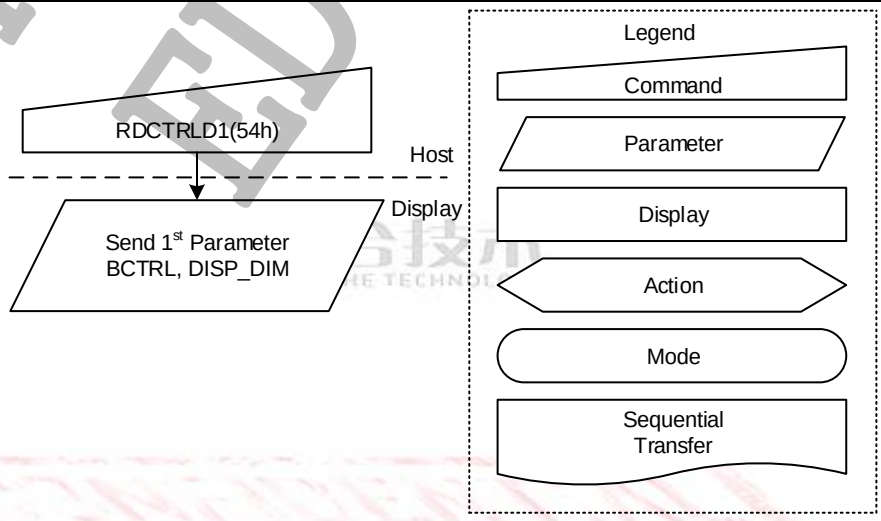
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	28h
S/W Reset	28h
H/W Reset	28h

Flow Chart



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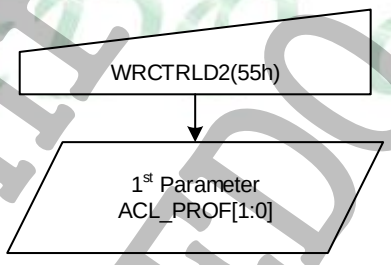
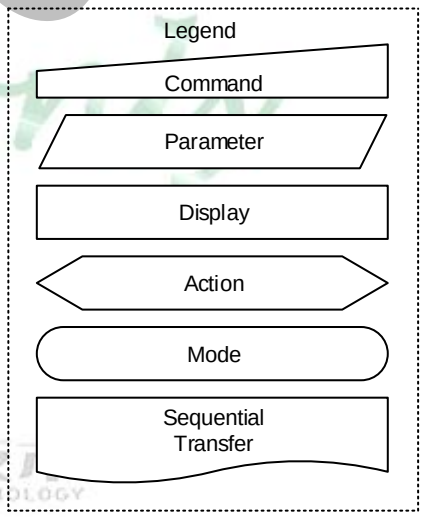
5.2.46 WRCTRLD2 (55h): Write CTRL Display 2

55H	WRCTRLD2 (Write CTRL Display 2)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	1	0	1	55
1st Para	Write	0	0	0	0	0	0	ACL_PROF[1:0]		00
Description	This command control related display brightness. • **D[7:2]** - Reserved These bits are not applicable for this project, so it is set to "0" • **ACL_PROF[1:0]** – Select ACL Profile 0 = ACL Off 1 = Profile 1 2 = Profile 2 3 = Profile 3									
Restriction	–									
Register Availability	**Status**							**Availability**		
	Sleep Out							Yes (Reflect in next V-sync period)		
	Sleep In							Yes		
Default	**Status**							**Default Value**		
	Power On Sequence							00h		
	S/W Reset							00h		
	H/W Reset							00h		
Flow Chart	 									

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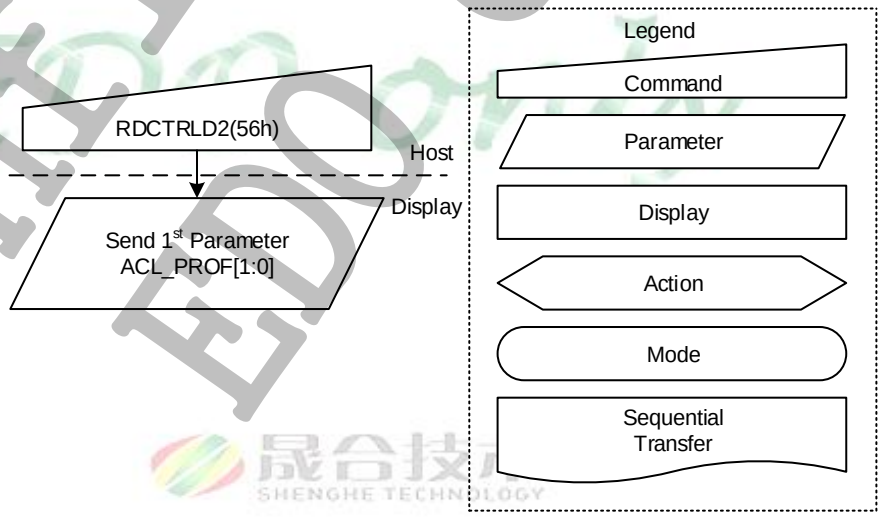
5.2.47 RDCTRLD2 (56h): Read CTRL Display 2

56H	RDCTRLD2 (Read CTRL Display 2)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	0	1	1	0	56
1st Para	Read	0	0	0	0	0	0	ACL_PROF[1:0]		00
Description	This command returns the brightness value of 'Write CTRL Display 1'. • **D[7:2]** - Reserved These bits are not applicable for this project. It is "0" • **ACL_PROF[1:0]** – Select ACL Profile 0 = ACL Off 1 = Profile 1 2 = Profile 2 3 = Profile 3									
Restriction	–									
Register Availability	**Status**							**Availability**		
	Sleep Out							Yes		
	Sleep In							Yes		
Default	**Status**							**Default Value**		
	Power On Sequence							00h		
	S/W Reset							00h		
	H/W Reset							00h		
Flow Chart										

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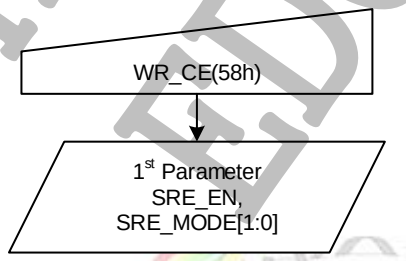
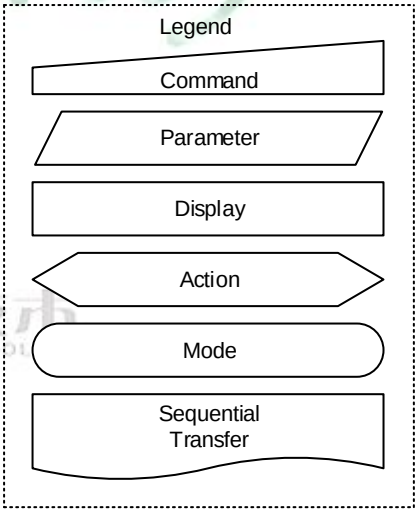
5.2.48 WR_CE (58h): Write CE

58H	WR_CE (Write CE)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	1	0	0	0	58
1st Para	Write	0	0	0	0	0	SRE_EN	SRE_MODE[1:0]		00
Description	This command control related SRE (Sunlight Readability Enhancement) • **D[7:3]** - Reserved. These bits are not applicable for this project, so it is set to "0". • **SRE_EN** – SRE Control 0 = Off 1 = On • **SRE_MODE[1:0]** – Sunlight Readability Mode 0 = Low 1 = Low 2 = Medium 3 = High									
Restriction	–									
Register Availability	**Status**						**Availability**			
	Sleep Out						Yes (Reflect in next V-sync period)			
	Sleep In						Yes			
Default	**Status**						**Default Value**			
	Power On Sequence						00h			
	S/W Reset						00h			
	H/W Reset						00h			
Flow Chart	 									

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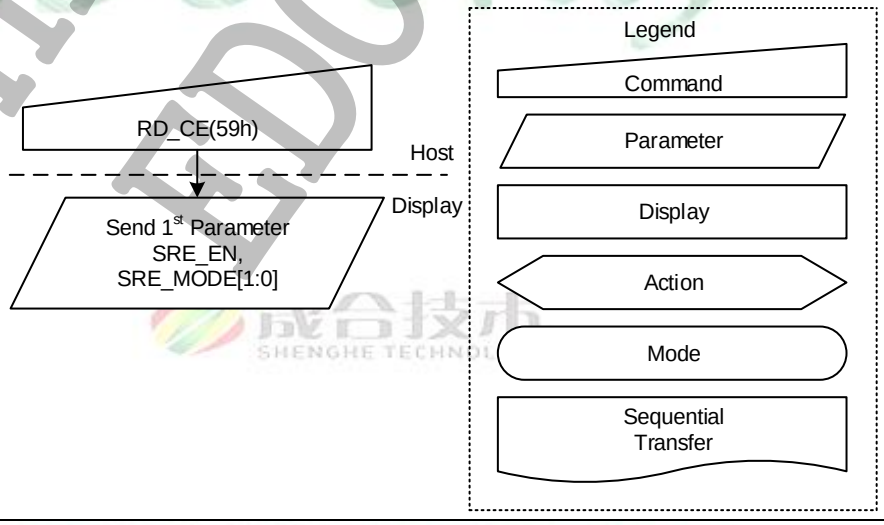
5.2.49 RD_CE (59h): Read CE

59H	RD_CE (Read CE)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	0	1	1	0	0	1	59
1st Para	Read	0	0	0	0	0	SRE_EN	SRE_MODE[1:0]		00
Description	This command control related SRE (Sunlight Readability Enhancement) • **D[7:3]** - Reserved. These bits are not applicable for this project, so it is set to "0". • **SRE_EN** – SRE Control 0 = Off 1 = On • **SRE_MODE[1:0]** – Sunlight Readability Mode 0 = Low 1 = Low 2 = Medium 3 = High									
Restriction	–									

Register Availability	**Status**	**Availability**
	Sleep Out	Yes
	Sleep In	Yes

Default	**Status**	**Default Value**
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

Flow Chart



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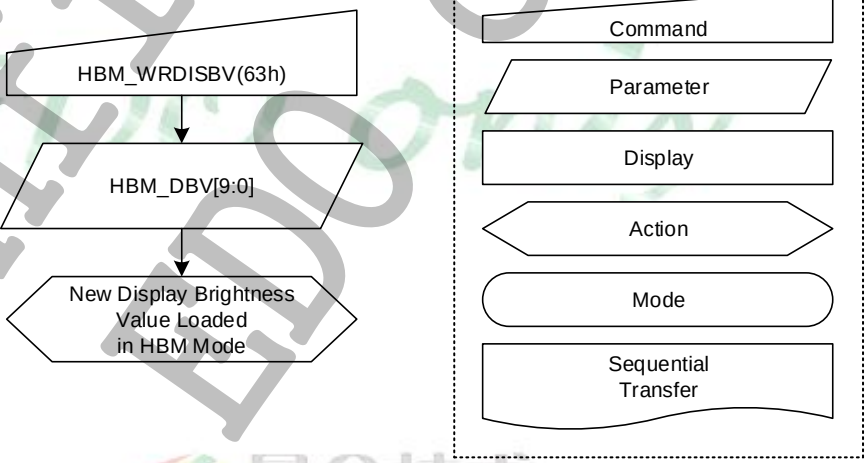
5.2.50 HBM_WRDISBV (63h): Write Display Brightness Value in HBM Mode

63H	HBM_WRDISBV (Write Display Brightness Value in HBM Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	1	0	0	0	1	1	63
1st Para	Write	HBM_DBV[7:0]								FF
2nd Para	Write	0	0	0	0	0	0	HBM_DBV[9:8]		00
Description	This command is used to adjust the brightness value of the display in HBM Mode. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 000h value means the lowest brightness and 3FFh value means the highest brightness.									
Restriction	–									

Register Availability	Status	Availability
	Sleep Out	Yes (Reflect in next V-sync period)
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	0_FFh
	S/W Reset	0_FFh
	H/W Reset	0_FFh

Flow Chart



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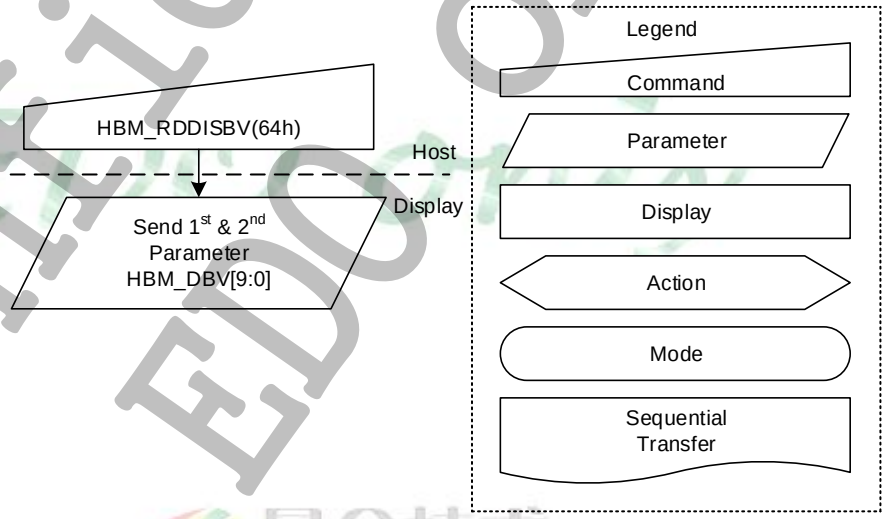
5.2.51 HBM_RDDISBV (64h): Read Display Brightness Value in HBM Mode

64H	HBM_RDDISBV (Read Display Brightness Value in HBM Mode)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	1	0	0	1	0	0	64
1st Para	Read	HBM_DBV[7:0]								FF
2nd Para	Read	0	00	0	0	0	0	HBM_DBV[9:8]		00
Description	This command returns the brightness value of the display in HBM Mode. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. In principal relationship is that 000h value means the lowest brightness and 3FFh value means the highest brightness.									
Restriction	–									

Register Availability	Status	Availability
	Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	0_FFh
	S/W Reset	0_FFh
	H/W Reset	0_FFh

Flow Chart



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5.2.52 HBMCTL (66h): HBM Control

66H	HBMCTL (HBM Control)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	0	1	1	0	0	1	1	0	66
1st Para	Write	0	0	HBM_MODE[1:0]		0	0	HBM_ EN	0	10

Description

This command control related high brightness mode.

- **D[7:6]** - Reserved.
  These bits are not applicable for this project, so it is set to "0".
- **HBM_MODE[1:0]** – High Brightness Mode
  0 = HBM MODE0: Interpolation in HBM
  1 = HBM MODE0: Interpolation in HBM
  2 = HBM MODE1: Immediately changes Gamma HBM set1 in HBM
  3 = HBM MODE2: Immediately changes Gamma HBM set2 in HBM
- **D[3:2]** - Reserved.
  These bits are not applicable for this project, so it is set to "0".
- **HBM_EN** – HBM Control
  0 = Off
  1 = On
- **D[0]** - Reserved.
  This bit is not applicable for this project, so it is set to "0".

Restriction

–

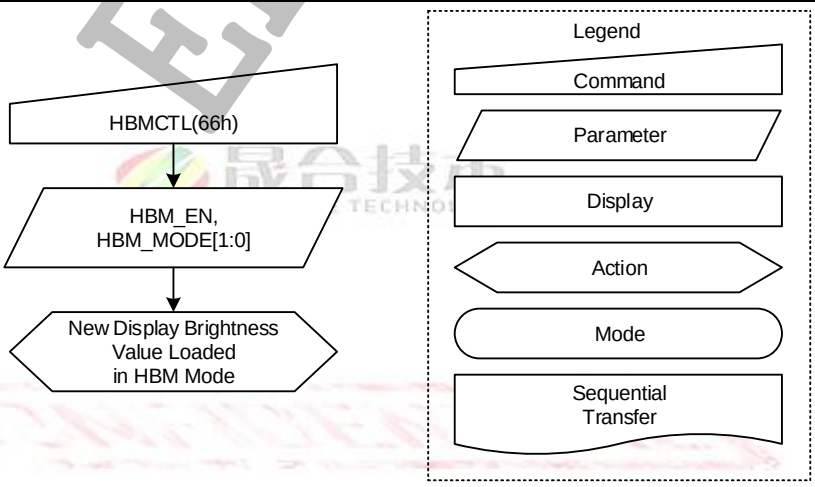
Register Availability

Status	Availability
Sleep Out	Yes (Reflect in next V-sync period)
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	10h
S/W Reset	10h
H/W Reset	10h

Flow Chart



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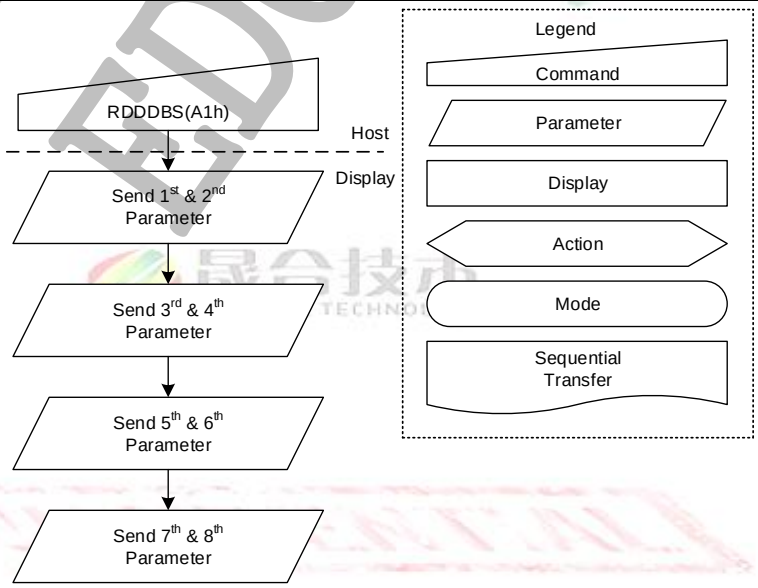
5.2.53 RDDDBS (A1h): Read DDB Start

A1H	RDDDBS (Read DDB Start)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	0	1	0	0	0	0	1	A1
1st Para	Read	DDB1[7:0]								00
2nd Para	Read	DDB2[7:0]								00
3rd Para	Read	DDB3[7:0]								00
4th Para	Read	DDB4[7:0]								00
5th Para	Read	DDB5[7:0]								00
6th Para	Read	DDB6[7:0]								00
7th Para	Read	DDB7[7:0]								00
8th Para	Read	DDB8[7:0]								00
9th Para	Read	1	1	1	1	1	1	1	1	FF
Description	This command returns supplier identification and display module model/revision information of DDh. NOTE: This information is not the same RDID1(DAh) : Read ID1, RDID2(DBh) : Read ID2. and RDID3(DCh) : Read ID3 commands are returning.									
Restriction	–									

Register Availability	Status	Availability
	Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	(OTP value)
	S/W Reset	(OTP value)
	H/W Reset	(OTP value)

Flow Chart



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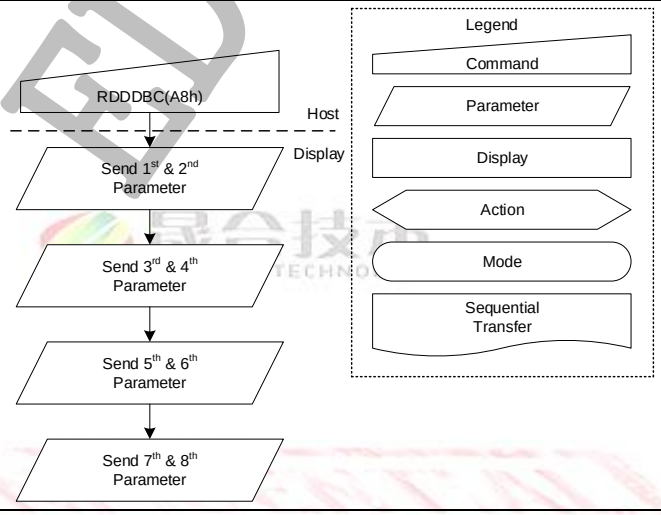
5.2.54 RDDDBC (A8h): Read DDB Continue

A8H	RDDDBC (Read DDB Continue)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	0	1	0	1	0	0	0	A8
1st Para	Read	DDBn+1[7:0]								00
2nd Para	Read	DDBn+2[7:0]								00
3rd Para	Read	DDBn+3[7:0]								00
4th Para	Read	DDBn+4[7:0]								00
5th Para	Read	DDBn+5[7:0]								00
6th Para	Read	DDBn+6[7:0]								00
7th Para	Read	DDBn+7[7:0]								00
8th Para	Read	DDBn+8[7:0]								00
9th Para	Read	1	1	1	1	1	1	1	1	FF
Description	This command returns supplier identification and display module model/revision information of DDh. NOTE: This information is not the same RDID1(DAh) : Read ID1, RDID2(DBh) : Read ID2 and RDID3(DCh) : Read ID3 commands are returning. Use when want to read DDh continuously after used A1h.									
Restriction	–									

Register Availability	Status	Availability
	Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	(OTP value)
	S/W Reset	(OTP value)
	H/W Reset	(OTP value)

Flow Chart



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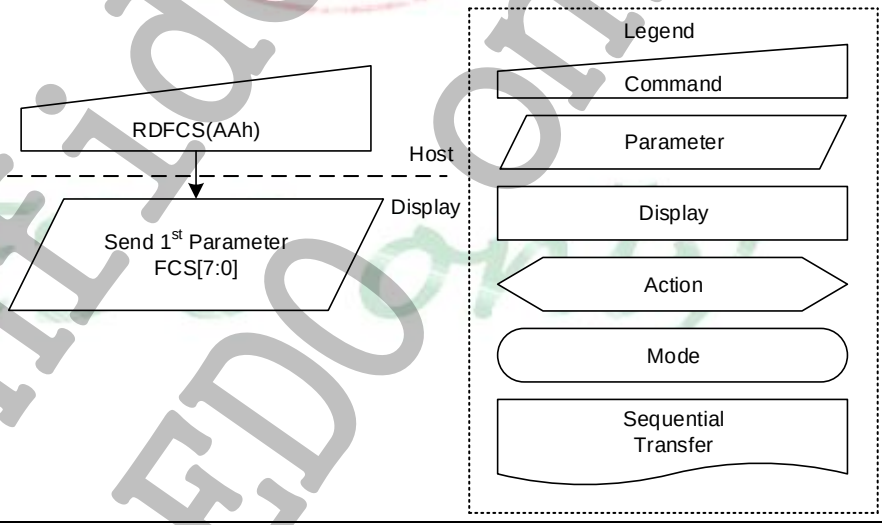
5.2.55 RDFCS (AAh): Read First Checksum

AAH	RDFCS (Read First Checksum)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	0	1	0	1	0	1	0	AA
1st Para	Read	FCS[7:0]								00
Description	This command returns the first checksum what has been calculated from “User Command Set” area registers(not include “Manufacture Command Set”) and the frame memory after write access to those registers and/or frame memory has been done.									
Restriction	It will be necessary to wait 150ms after there is the last access on “User Command Set” area registers before there can read this checksum value.									
Register Availability	**Status**					**Availability**				
	Sleep Out					Yes				
	Sleep In					Yes				
Default	**Status**					**Default Value**				
	Power On Sequence					00h				
	S/W Reset					00h				
	H/W Reset					00h				
Flow Chart										

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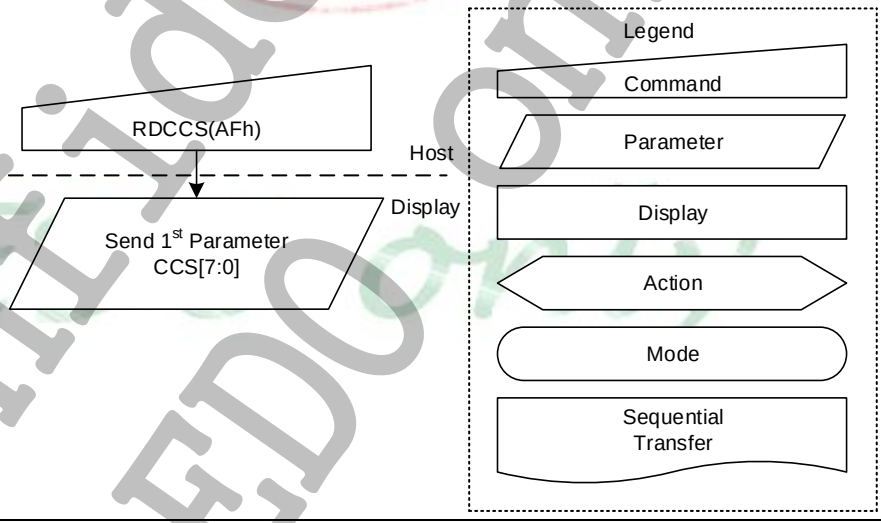
5.2.56 RDCCS (AFh): Read Continue Checksum

AFH	RDCCS (Read Continue Checksum)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	0	1	0	1	1	1	1	AF
1st Para	Read	CCS[7:0]								00
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from “User Command Set” area registers and the frame memory after the write access to those registers and/or frame memory has been done.									
Restriction	It will be necessary to wait 300ms after there is the last access on “User Command Set” area registers before there can read this checksum value in the first time.									
Register Availability	**Status**	**Availability**								
	Sleep Out	Yes								
	Sleep In	Yes								
Default	**Status**	**Default Value**								
	Power On Sequence	00h								
	S/W Reset	00h								
	H/W Reset	00h								
Flow Chart										

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5.2.57 SPI_MODE (C4h): SPI Mode Control

C4H	SPI_MODE (SPI Mode Control)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	1	0	0	0	1	0	0	C4
1st Para	Write	SRAM _WR_ MODE	0	DUAL_PMODE[1 :0]		0	QUAD _LINE	SDIO_ MODE	DUAL_ EN	00
Description	This command control interface mode. • **SRAM_WR_MODE** – SRAM Write Enable in SPI+MIPI interface mode 0 = Disable 1 = Enable • **D[6]** - Reserved This bit is not applicable for this project, so it is set to “0”. • **DUAL_PMODE[1:0]** – RGB image data transfer format in SPI3,4W interface mode 0 = 1P / 1T 1 line 1 = 1P / 1T for 2 line 2 = 2P / 3T for 2 line • **D[3]** - Reserved This bit is not applicable for this project, so it is set to “0”. • **QUAD_LINE** – Quad line 0 = SDIO, SDI1, SDI2, SDI3 (4 line) 1 = SDIO (1 line) • **SDIO_MODE** – Read protocol in SPI3,4W interface mode 0 = SDI 1 = SDI + SDO • **DUAL_EN** – Dual mode enable in SPI3,4W interface mode 0 = Disable 1 = Enable									
Restriction	–									
Register Availability	**Status**						**Availability**			
	Sleep Out						Yes			
	Sleep In						Yes			
Default	**Status**						**Default Value**			
	Power On Sequence						00h			
	S/W Reset						00h			
	H/W Reset						00h			

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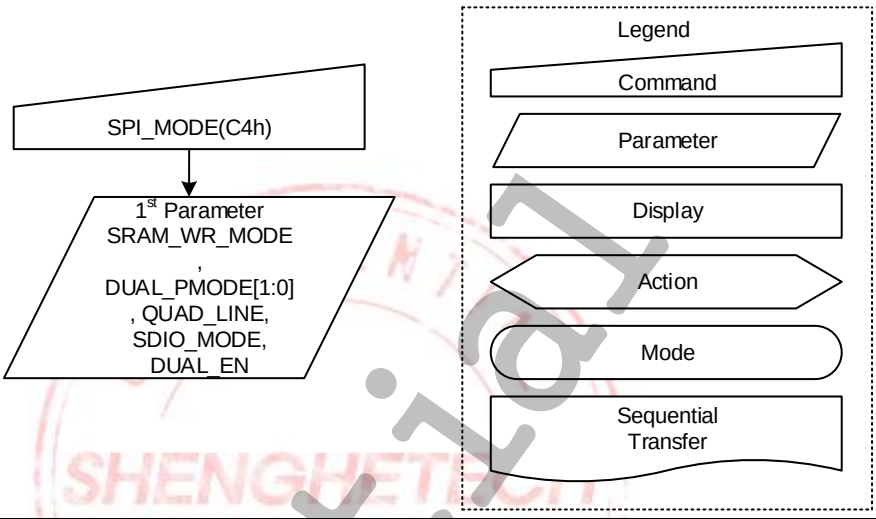
Flow Chart	

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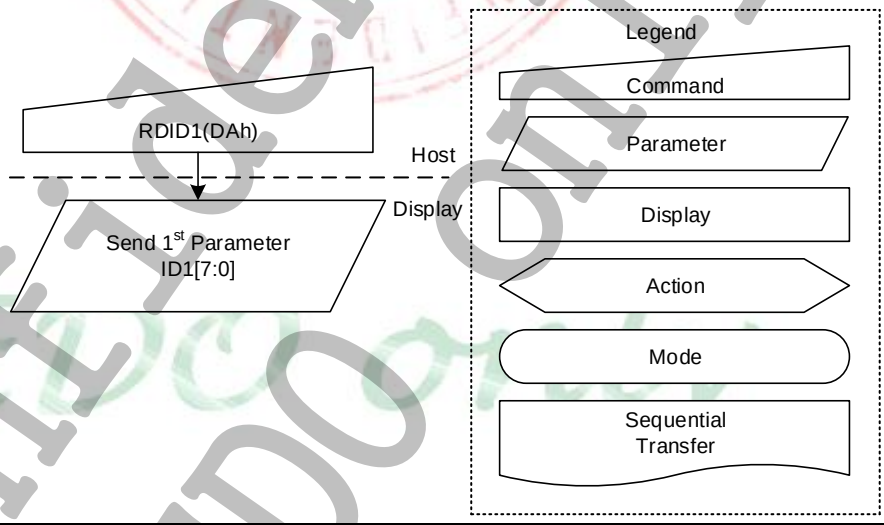
5.2.58 RDID1 (DAh): Read ID1

DAH	RDID1 (Read ID1)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	1	0	1	1	0	1	0	DA
1st Para	Read	ID1[7:0]								00
Description	This read byte is an identifier. It is specified by Module maker code.									
Restriction	–									

Register Availability	Status	Availability
	Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	(OTP value)
	S/W Reset	(OTP value)
	H/W Reset	(OTP value)

Flow Chart



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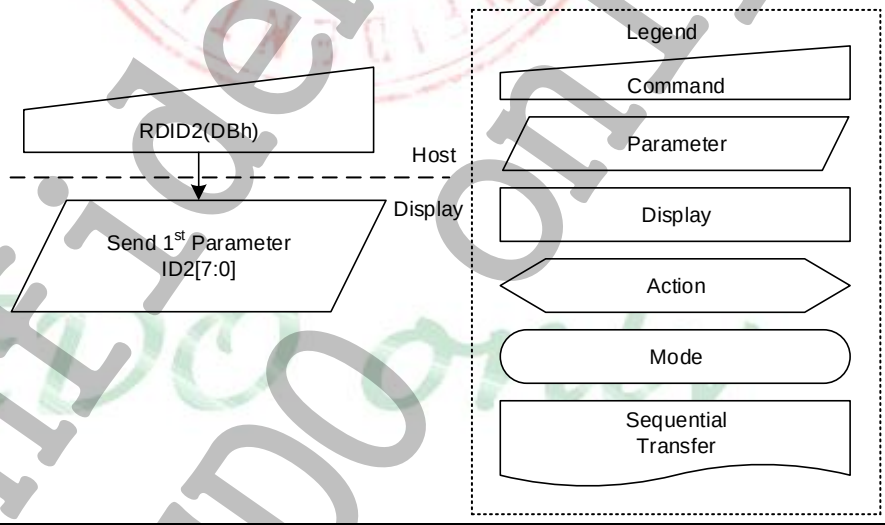
5.2.59 RDID2 (DBh): Read ID2

DBH	RDID2 (Read ID2)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	1	0	1	1	0	1	1	DB
1st Para	Read	ID2[7:0]								00
Description	This read byte is an identifier. It is specified by Module/Driver version.									
Restriction	–									
Register Availability	**Status**						**Availability**			
	Sleep Out						Yes			
	Sleep In						Yes			
Default	**Status**						**Default Value**			
	Power On Sequence						(OTP value)			
	S/W Reset						(OTP value)			
	H/W Reset						(OTP value)			
Flow Chart										

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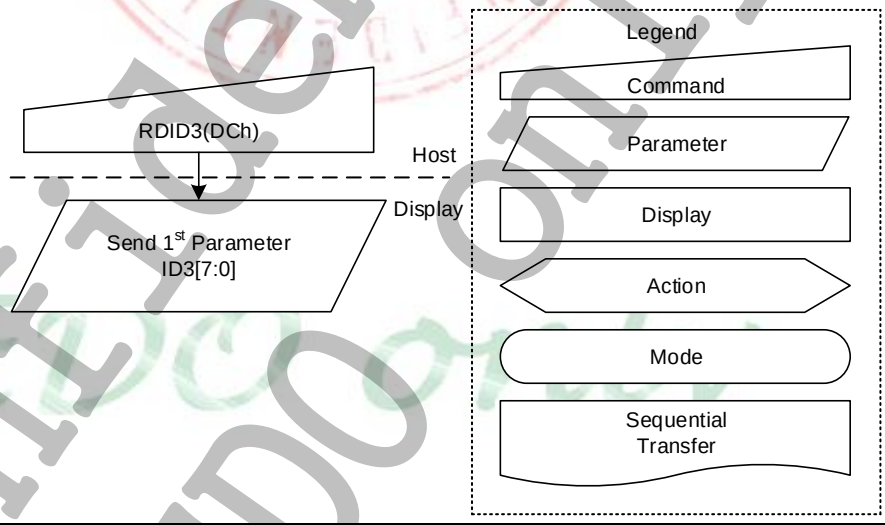
5.2.60 RDID3 (DCh): Read ID3

DCH	RDID3 (Read ID3)									
–	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	Write	1	1	0	1	1	1	0	0	DC
1st Para	Read	ID3[7:0]								00
Description	This read byte is an identifier. It is specified by Module/Driver project code.									
Restriction	–									
Register Availability	**Status**						**Availability**			
	Sleep Out						Yes			
	Sleep In						Yes			
Default	**Status**						**Default Value**			
	Power On Sequence						(OTP value)			
	S/W Reset						(OTP value)			
	H/W Reset						(OTP value)			
Flow Chart										

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