# L-WEA2012



## *Product Preview*

## 400x400 TDDI for IOT/Wearable



 

SOLOMON SYSTECH

**APPENDIX: IC REVISION HISTORY OF L-WEA2012 SPECIFICATION**

| Version | Change Items | Effective Date |
|---|---|---|
| 0.10 | 1st Release | 20-Jan-2021 |
| 0.20 | Section 2, for MIPI section, removed Video mode | 05-Feb-2021 |
| 0.30 | Section 5, added die floor plan<br>Section 6, added SPI/DSPI/QSPI timing, RAM block description<br>Section 8, updated un-used pin setting<br>Section 15, updated Power on/off sequence | 29-Mar-2021 |

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**FIGURES**

# 1 GENERAL DESCRIPTION

L-WEA2012 is a display driver supporting a-Si panel up to 400RGB x 400 resolution with 24bit color depth. The IC has integrated with RAM and self-cap incell touch controller.

# 2 FEATURES

**Display**

- IOT solution for TFT display
- Support various resolution, from 240RGB x 240 to 400RGB x 400
- Display color modes: 16.7M color (24bit – 8R:8G:8B)
- Support Column/1dot/2dot inversion
- Dual Gate GIP driving

**Touch**

- Low Power Touch Standby mode
- Support max 49 touch nodes sensing signal
- Support Vblank touch sensing mode, up to 60Hz report rate
- I2C/SPI for communication with Host (AP)
- 8 channels virtual touch key

**Interface**

- MIPI
  - MIPI lane speed up to 500Mbps per lane
  - MIPI DSI (version 1.1) with D-PHY (version 1.1)
  - Support command mode
  - Command set compliant with MIPI DCS (version 1.4)
  - 1 data lane and 1 clock lane
- SPI
  - Support SPI/DSPI/QSPI
  - 1/2/4 data lane and 1 clock lane
  - Data rate up to 40Mbps

**RAM**

- Embedded 80000 bytes RAM (400x400/2)

**Power**

- Power Supply
  - VDDIO: 1.65V – 3.3V
  - VCI: 2.5V ~ 3.3V
- Max VGH – VGL: 28Vp-p
- Low Current Sleep Mode and 8-color display mode for power saving

**Function**

- Programmable Gamma Correction Curve
- Programmable VCOM (-0.2V ~ -2.7V)
- CABC dynamics backlight control with PWM output

# 3 ORDERING INFORMATION

**Table 3-1: Ordering Information**

| Ordering Part Number | Package Form | Remark |
|---|---|---|
| L-WEA2012Z | COG | |

# 4 BLOCK DIAGRAM

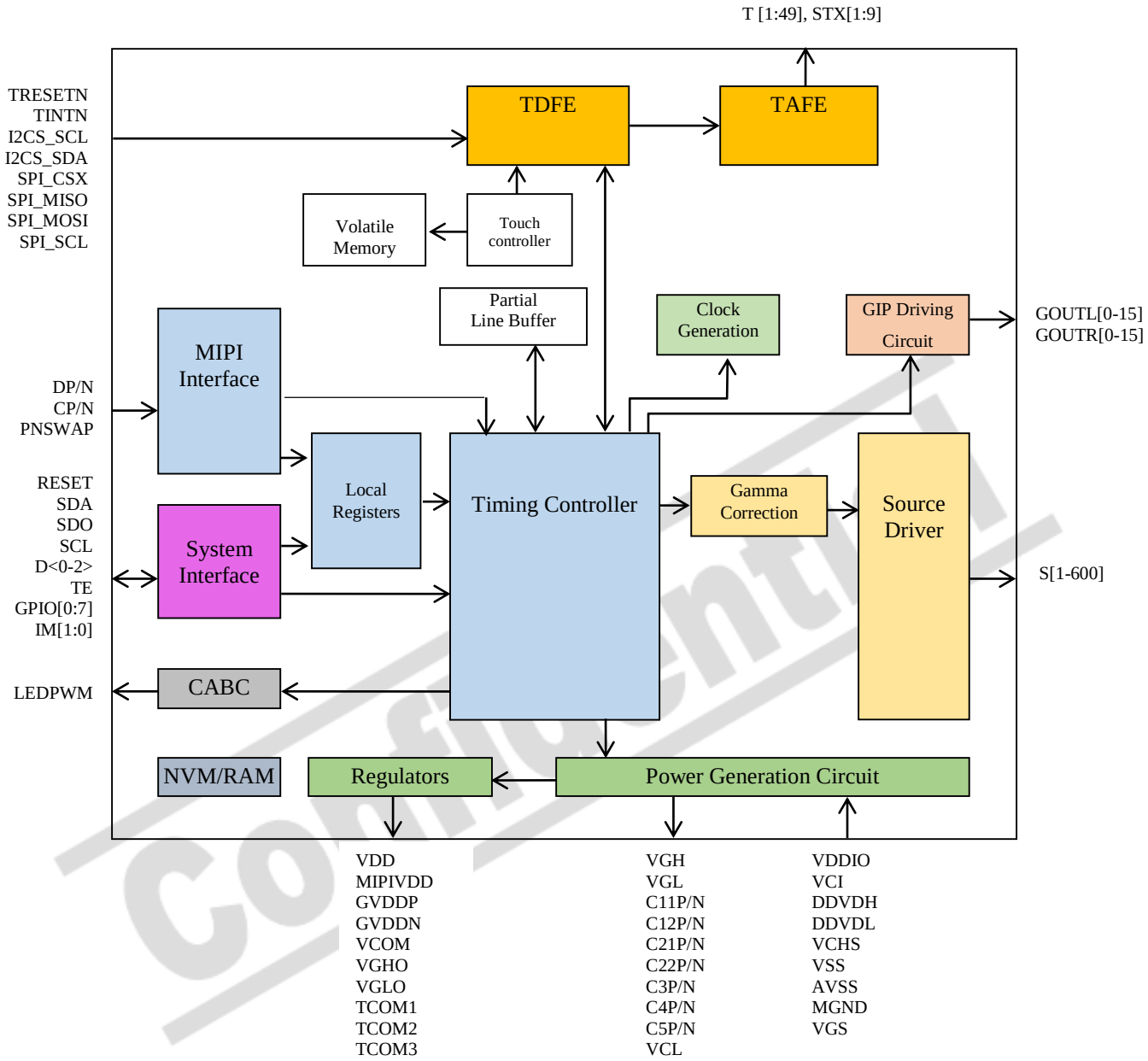



**Figure 4-1: L-WEA2012 Block Diagram**

# 5 DIE PAD FLOOR PLAN

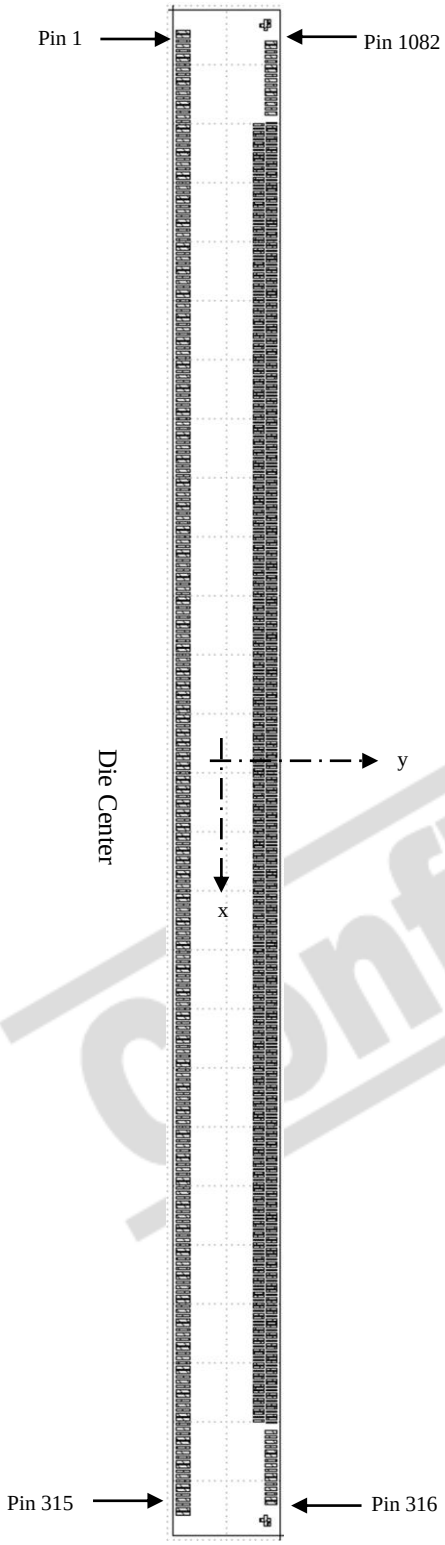



Figure 5-3: L-WEA2012 Die Pad Floor Plan (die face up)

| Alignment Mark (center) | X (um) | Y (um) |
|---|---|---|
| Left | -6333.8 | 330.8 |
| Right | 6333.8 | 330.8 |

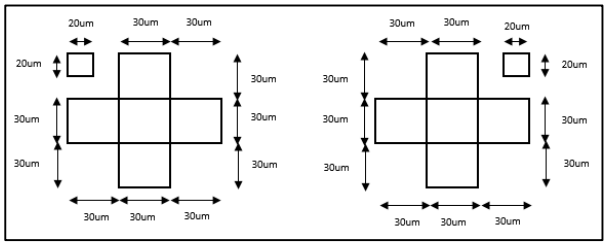



Figure 5-1: Alignment Marks

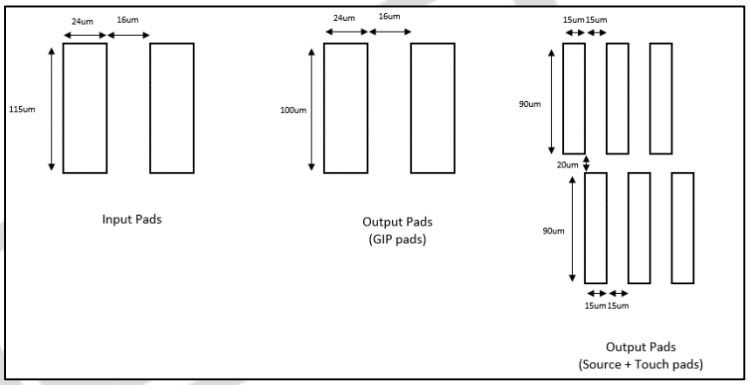



Figure 5-2: Pad Arrangement (die face-up, all in um)

Table 5-1: Die Information

| | |
|---|---|
| Die Size | 13004um x 998um (w/ scribe line) |
| Die Thickness | 200um |
| Typical Bump Height | 9 um |
| Bump Co-planarity (within die) | ≤ 2 um |
| Bump Size 1 | 24 x 115 $\mu m^2$ (pin 1-315) |
| Pad Pitch 1 | 40 μm |
| Bump Size 2 | 24 x 100 $\mu m^2$ (pin 316-331,1067-1082) |
| Pad Pitch 2 | 40 um |
| Bump Size 3 | 15 x 90 $\mu m^2$ (pin 332-1066) |
| Pad Pitch 3 | 30 um, 2 layers stagger |
| Bump Hardness | 90 +/-20 Hv |

**Note**

(1) Coordinates are referenced to center of the chip.

(2) Coordinate units and size of all alignment marks are in um.

(3) All alignment keys do not contain gold bump.

# 6 BLOCK FUNCTION DESCRIPTION

## 6.1 MIPI Interface

L-WEA2012 supports MIPI DSI interface which can be used to transmit display data. It can also be used to program the L-WEA2012 registers.

The MIPI DPHY in L-WEA2012 supports flexible data and clock lane polarity swap. It is controlled by hardware pin. Please see the diagram below for possible arrangement.

**Table 6-1: MIPI Bus Configuration**

| Physical Pin | DP | DN | CP | CN |
|---|---|---|---|---|
| PNSWAP | Functional Output | | | |
| 1 | DP | DN | CP | CN |
| 0 | DN | DP | CN | CP |

## 6.2 System Interface

L-WEA2012 supports SPI interface which can be used to transmit display data. It can also be used to program the L-WEA2012 registers.

SPI/DSPI/QSPI are supported.

SPI interface or MIPI interface is selected by hardwire pins IM[0:1].

**Table 6-2: Interface Selection**

| IM[1] | IM[0] | Interface | Used pins |
|---|---|---|---|
| 0 | 0 | Reserved | - |
| 0 | 1 | 4-wire SPI (0xE4=0) | PNSWAP(CSX), TEST_I[2](DCX), SCL, SDA |
| 0 | 1 | 4-wire DSPI (0xE4=1) | PNSWAP(CSX), TEST_I[2](DCX), SCL, SDA, D[0] |
| 1 | 0 | MIPI | PNSWAP, CP, CN, DP, DN |
| 1 | 1 | 3-wire SPI | PNSWAP(CSX), TEST_I[2](DCX)=GND, SCL, SDA |
| 1 | 1 | QSPI | PNSWAP(CSX), TEST_I[2](DCX)=VDDIO, SCL, SDA, D[0:2] |

### 6.2.1 4-wire SPI Timing

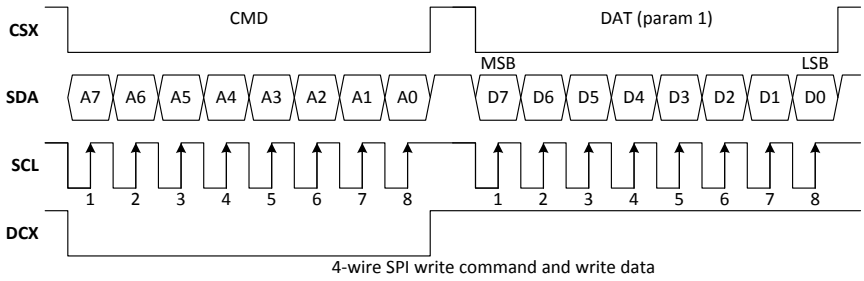



Figure 6-1: 4-wire SPI write command and write data

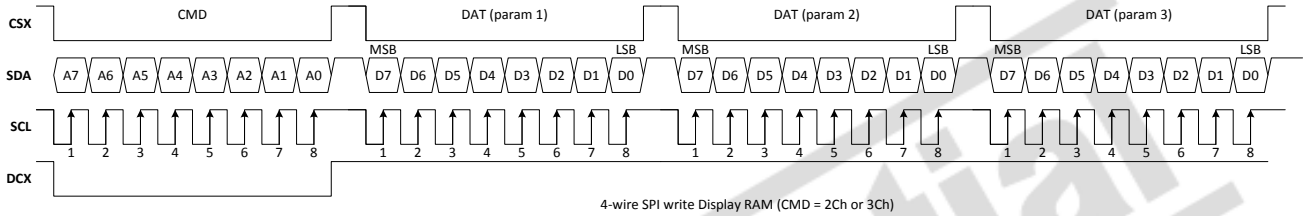



Figure 6-2: 4-wire SPI write RAM data
(Note: for each time using 0x2C or 0x3C cmd to write RAM data, please write 4 pixels data or more.)

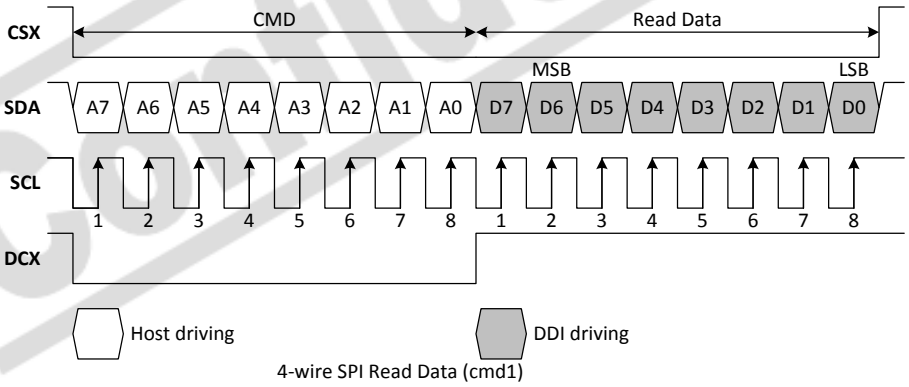



Figure 6-3: 4-wire SPI Read

### 6.2.2 4-wire DSPI Timing

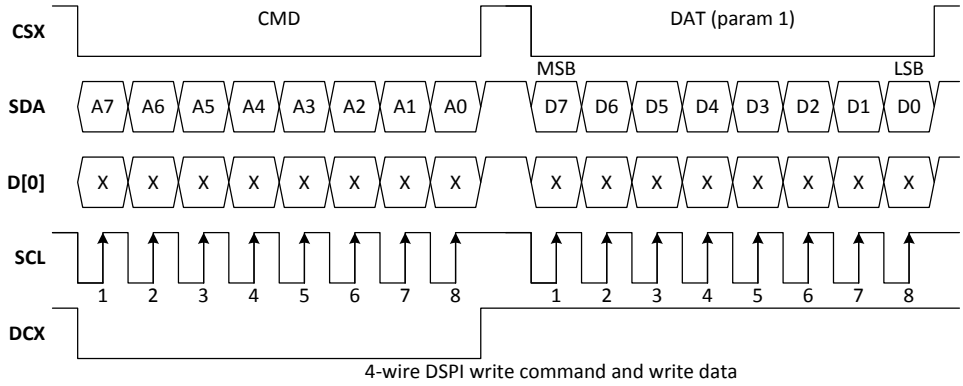



Figure 6-4: 4-wire DSPI write command and write data

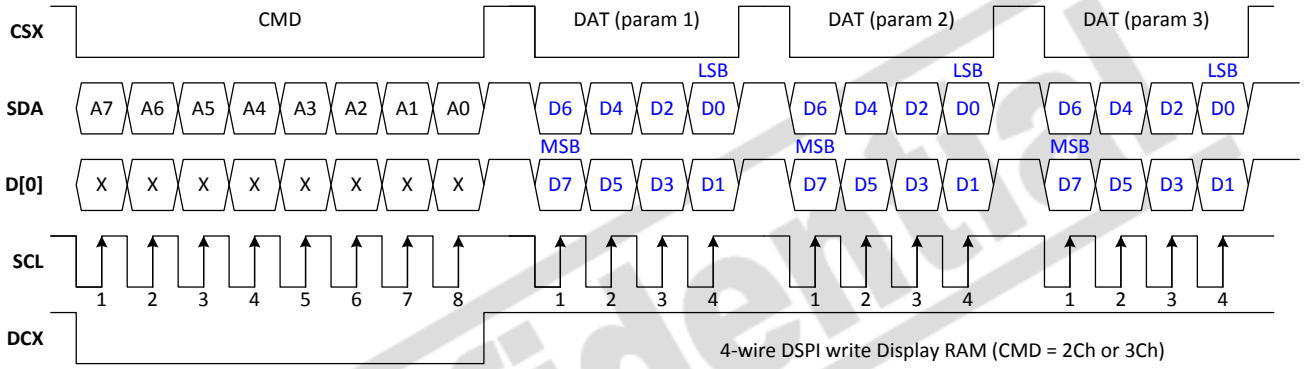



Figure 6-5: 4-wire DSPI write RAM data
(Note: for each time using 0x2C or 0x3C cmd to write RAM data, please write 4 pixels data or more.)

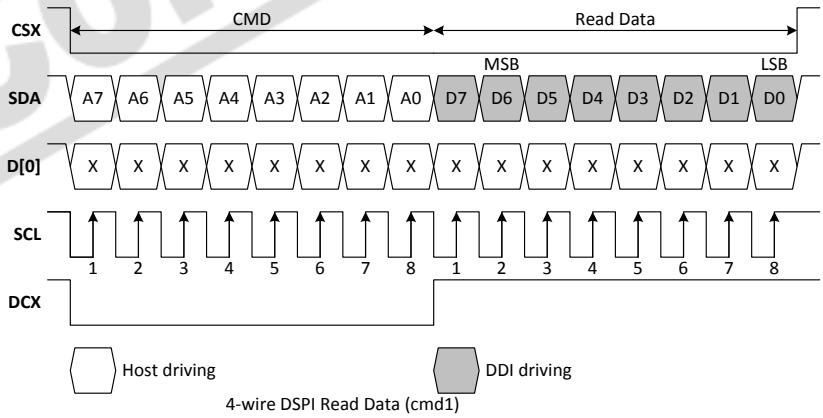



Figure 6-6: 4-wire DSPI Read

### 6.2.3 3-wire SPI Timing

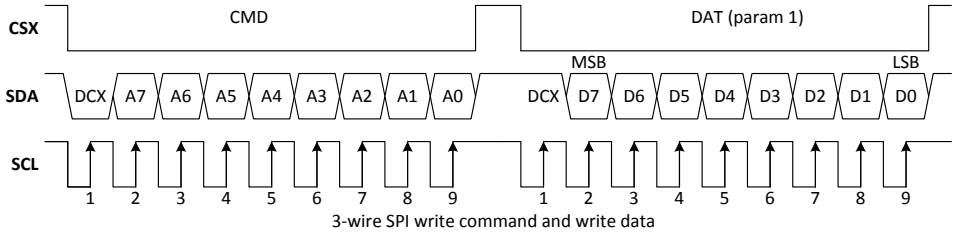



Figure 6-7: 3-wire SPI write command and write data

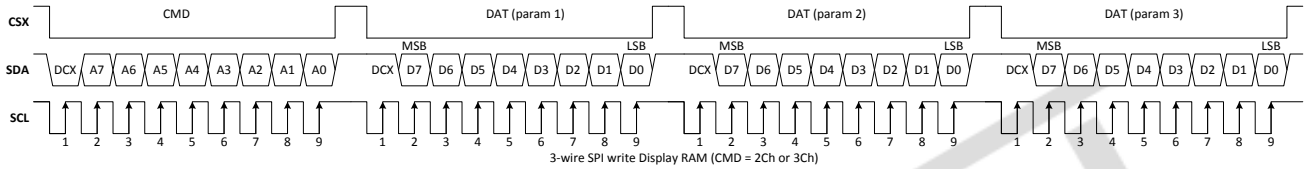



Figure 6-8: 3-wire SPI write RAM data
(Note: for each time using 0x2C or 0x3C cmd to write RAM data, please write 4 pixels data or more.)

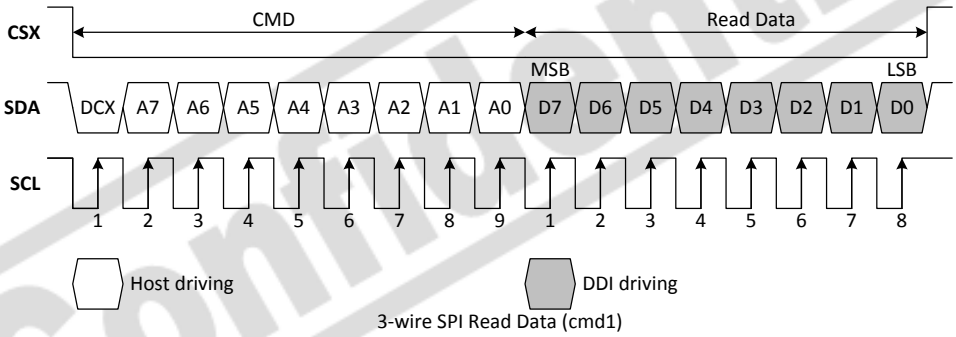



Figure 6-9: 3-wire SPI Read

### 6.2.4 QSPI Timing

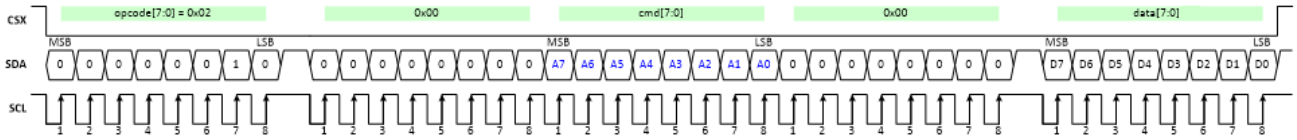



Figure 6-10: QSPI write command and write data (1 data lane)

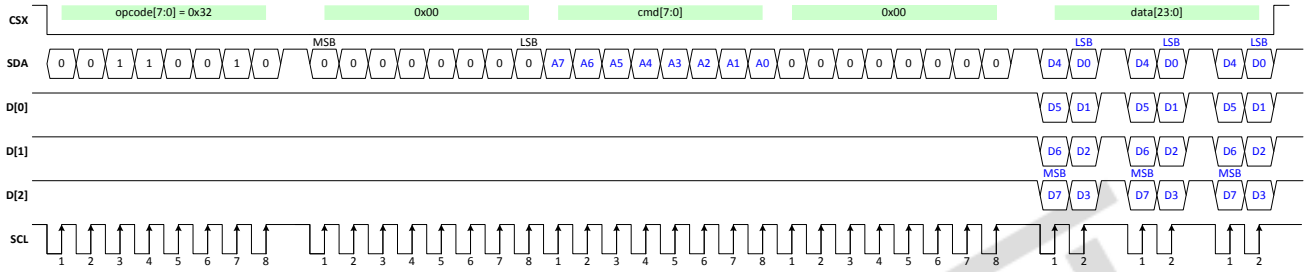



Figure 6-11: QSPI write command and write data (4 data lanes)
(Note: for each time using 0x2C or 0x3C cmd to write RAM data, please write 4 pixels data or more.)

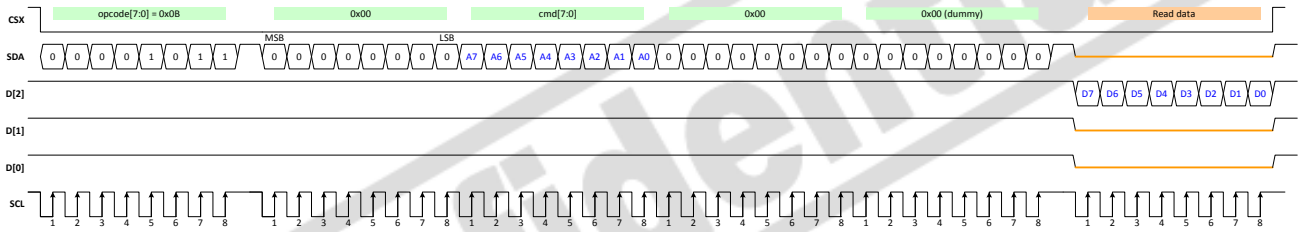


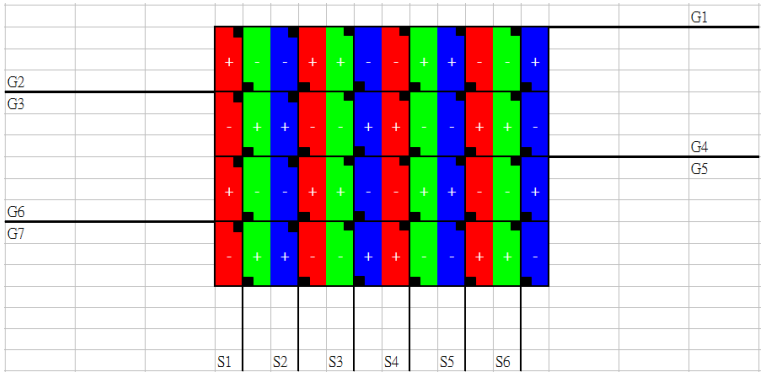

Figure 6-12: QSPI Read

## 6.3 Regulator / Power Generation Circuit

This block generates the voltage of VGH, VGL, VCOM etc which are necessary for operating L-WEA2012.

## 6.4 GIP Driving Circuits

This block generates the controls signals that are used in the Gate-Driver In Panel (GIP). Dual gate driving is supported.



## 6.5 RAM

There are 80000 bytes RAM (400x400/2). RAM must be written as 1 pixel (3 bytes for 16.7M/262k color format, 2 bytes for 65k color format). Number of pixel must be in multiple of 4.

Use 0x2C and 0x3C to write whole frame data. (Please do not only use 0x2C to write whole frame data.)
For each time using 0x2C or 0x3C command to write RAM data, please write 4 pixels data or more.

Read RAM is not supported.

## 6.6 Non-Volatile Memory (NVM)

NVM is available. It has a reserved area for below purpose. Each one can be programmed.

- Vendor ID
- VCOM tuning
- Full Gamma setting

## 6.7 Clock Generation Circuit

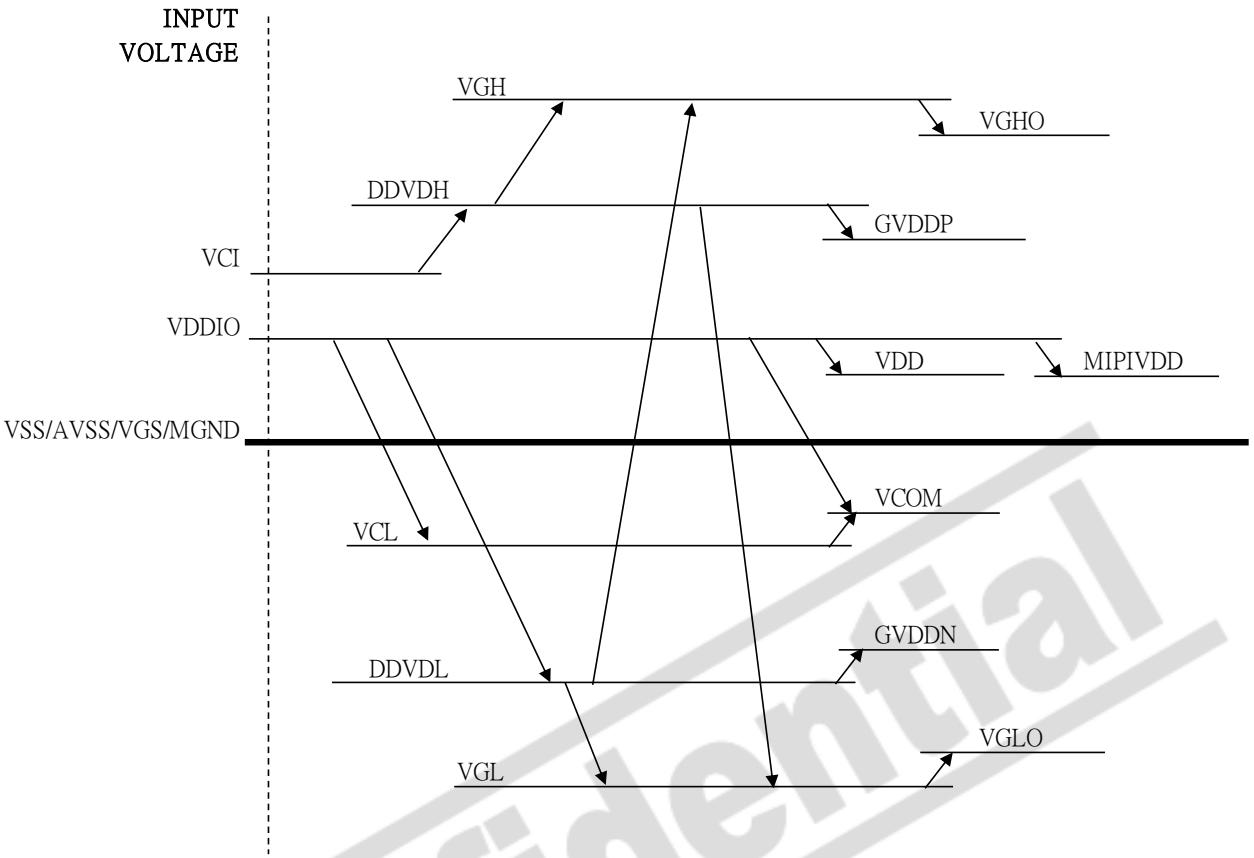
L-WEA2012 supports generating operational clock by itself through local oscillator and PLL.

## 6.8 Touch

L-WEA2012 has integrated the Touch Module Controller (TMC), Touch Digital Front End (TDFE), and Touch Analog Front End (TAFE).

TMC is able to process all the raw touch data and generate the final touch location and communicate with the AP.

# 7 POWER SCHEME



# 8 PIN DESCRIPTIONS

**Key:**

I = Input
O =Output
IO = Bi-directional (input/output)
P = Power pin
GIP = Gate In Panel
BLU = Back Light Unit

## 8.1 Power Pins

**Table 8-1: Power Supply Pins**

| Name | Type | Connect to | Function | Description | When not in use |
|---|---|---|---|---|---|
| VDDIO | P | Power Supply | Power supply for logic I/O | Power Supply for logic I/O<br>- Connect to voltage source between 1.65V to 3.3V | - |
| VCI | P | Power Supply | Power supply for Analog | Power Supply for analog circuit<br>- Connect to voltage source between 2.5V to 3.3V | |
| AVSS | P | GND | Ground of the Power Supply | Analog circuit ground | - |
| VSS | P | GND | Ground of the Power Supply | System ground pin | - |
| MGND | P | GND | Ground of MIPI logic | MIPI analog circuit ground pin | - |
| VGS | P | GND | Reference Voltage | VGS is the ground reference voltage for gamma circuit. | - |

**Table 8-2: Power Generation / Regulation Pins**

| Name | Type | Connect to | Function | Description | When not in use |
|---|---|---|---|---|---|
| VCOM | O | LCD | LCD Driving Voltage | Supply voltage to the common electrode of TFT panel | - |
| VGH | I/O | Stabilizing Capacitor | LCD Driving Voltage | A positive power output pin for gate driver | - |
| VGL | I/O | Stabilizing Capacitor | LCD Driving Voltage | A negative power output pin for gate driver | - |
| VGHO | O | Stabilizing Capacitor | LCD Driving Voltage | A regulated positive power output pin for gate driver | - |
| VGLO | O | Stabilizing Capacitor | LCD Driving Voltage | A regulated negative power output pin for gate driver | - |
| DDVDH | O | Stabilizing Capacitor | LCD Driving Voltage | Positive power supply for LCD driving | - |
| DDVDL | O | Stabilizing Capacitor | LCD Driving Voltage | Positive power supply for LCD driving | - |
| VCL | O | Stabilizing Capacitor | LCD Driving Voltage | A negative power output pin for driver IC internal circuit. | - |
| GVDDP | O | Stabilizing Capacitor | Reference Voltage | VREG1OUT is a positive source driver grayscale reference voltage | - |
| GVDDN | O | Stabilizing Capacitor | Reference Voltage | VREG2OUT is a negative source driver grayscale reference voltage | - |
| MIPIVDD | O | Stabilizing Capacitor | Power supply for MIPI circuits | Regulator output that needed to be connected with stabilizing capacitor for MIPI block | - |
| VDD | O | Stabilizing Capacitor | Power supply for logic circuits | Power Supply for logic circuits | - |
| C21N, C21P | I/O | Step-up capacitor | Booster Circuit | Connect booster capacitors to generate DDVDL. | Open |
| C22N, C22P | I/O | Step-up capacitor | Booster Circuit | Connect booster capacitors to generate DDVDL | Open |
| C11N, C11P | I/O | Step-up capacitor | Booster Circuit | Connect booster capacitors to generate DDVDH | Open |
| C12N, C12P | I/O | Step-up capacitor | Booster Circuit | Connect booster capacitors to generate DDVDH | Open |
| C3N, C3P | I/O | Step-up capacitor | Booster Circuit | Connect booster capacitors to generate VCL | Open |

| Name | Type | Connect to | Function | Description | When not in use |
|---|---|---|---|---|---|
| C4N, C4P | I/O | Step-up capacitor | Booster Circuit | Connect booster capacitors to generate VGH | Open |
| C5N, C5P | I/O | Step-up capacitor | Booster Circuit | Connect booster capacitors to generate VGL | Open |
| TCOM1 | O | Stabilizing Capacitor | Touch Driving Voltage | Used for touch application | Open |
| TCOM2 | O | Stabilizing Capacitor | Touch Driving Voltage | Used for touch application | Open |
| TCOM3 | O | Stabilizing Capacitor | Touch Driving Voltage | Used for touch application | Open |

## 8.2 Interfaces Logic Pins

**Table 8-3: Interfaces Logic Pins**

<table>
<tr><th>Name</th><th>Type</th><th>Connect to</th><th>Function</th><th>Description</th><th>When not in use</th></tr>
<tr><td>RESET</td><td>I</td><td>MPU</td><td>System Reset</td><td>System reset pin. (active low)</td><td>VDDIO</td></tr>
<tr><td>TE</td><td>O</td><td>MPU</td><td>Logic Control</td><td>Frame head pulse signal. Utilize this signal when synchronizing RAM data write operations.</td><td>Open</td></tr>
<tr><td>LED_PWM</td><td>O</td><td>BLU</td><td>-</td><td>BLU PWM signal</td><td>Open</td></tr>
<tr><td>IM[0:1]</td><td>I</td><td>MPU</td><td>-</td><td>Interface selection:
<table>
<tr><th>IM[1]</th><th>IM[0]</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>4-wire SPI (0xE4=0)</td></tr>
<tr><td>0</td><td>1</td><td>4-wire DSPI (0xE4=1)</td></tr>
<tr><td>1</td><td>0</td><td>MIPI</td></tr>
<tr><td>1</td><td>1</td><td>3-wire SPI (DCX=GND)</td></tr>
<tr><td>1</td><td>1</td><td>QSPI (DCX=VDDIO)</td></tr>
</table></td><td>-</td></tr>
</table>

## 8.3 Output Driver Pins

**Table 8-4: Output Driver Pins**

| Name | Type | Connect to | Function | Description | When not in use |
|---|---|---|---|---|---|
| GOUTL[0-15]<br>GOUTR[0-15] | O | LCD | GIP Control Signals | These pins are used for GIP control signal. Unused pins should leave open | Open |
| S[1–600] | O | LCD | LCD Driving Signals | Source driver output pins | Open |

## 8.4 MIPI Interface

**Table 8-5: MIPI Interfaces Pins**

| Name | Type | Connect to | Function | Description | When not in use |
|---|---|---|---|---|---|
| DP | I/O | MIPI Interface Signal | MIPI differential Data Pair | Positive polarity of low voltage differential data signal | Open/VSS |
| DN | | | | Negative polarity of low voltage differential data signal | Open/VSS |
| CP | I | | MIPI differential Clock Pair | Positive polarity of low voltage differential clock signal | Open/VSS |
| CN | I | | | Negative polarity of low voltage differential clock signal | Open/VSS |
| PNSWAP | I | MPU | Logic Control | PNSWAP polarity swap of MIPI signal | VDDIO |

## 8.5 SPI Interface

**Table 8-6: SPI Interfaces Pins**

| Name | Type | Connect to | Function | Description | When not in use |
|---|---|---|---|---|---|
| SCL | I | MPU | SPI | SPI clock signal | VSS |
| SDA | I | | SPI | SPI data signal | VSS |
| D[0:2] | I | | SPI | SPI data signal | VSS |

## 8.6 Touch Interface

**Table 8-7: Touch Interfaces Pins**

| Name | Type | Connect to | Function | Description | When not in use |
|---|---|---|---|---|---|
| TRESETN | I | MPU | Touch reset | Reset signal for touch circuit | VSS |
| SPI_CSX | I | Flash/MPU | SPI | SPI chip selection pin | VSS |
| SPI_MISO | I | Flash/MPU | SPI | SPI Data Output pin | VSS |
| SPI_MOSI | O | Flash/MPU | SPI | SPI Data Input pin | Open |
| SPI_SCL | I | Flash/MPU | SPI | SPI Clock pin | VSS |
| I2CS_SDA | I | MPU | I2C | Serial data pin of I2C interface for touch circuit | VSS |
| I2CS_SCL | I | MPU | I2C | Serial clock pin of I2C interface for touch circuit | VSS |
| TINTN | I | MPU | Touch interrupt | Interrupt signal for touch circuit | VSS |
| STX[1:9] | O | LCD | Touch control signal | Touch key channels | Open |
| T[1-49] | I/O | LCD | Touch control signal/VCOM | Touch channels/VCOM | Open |

## 8.7 Other Pins

**Table 8-8: Other Pins**

| Name | Type | Connect to | Function | Description | When not in use |
|---|---|---|---|---|---|
| DBIST | I | - | - | Test pin | VSS |
| GPO[0:7] | I/O | - | - | Test pin | Open |
| CL | O | - | - | Test pin | Open |
| VCOM_OPT[0:1] | O | | | Test pin | Open |
| DUMMY | - | - | - | Dummy pin | Open |
| TEST_I[0:2] | I | | | Test pin | VSS |

# 9 MAXIMUM RATINGS

**Table 9-1: Maximum Rating (Voltage reference to VSS)**

| Symbol | Parameter | Pin | Value | Unit |
|---|---|---|---|---|
| VDDIO | Supply Voltage | VDDIO | -0.3 to +3.3 | V |
| VCI | | VCI | -0.3 to +3.3 | V |
| VGH-VGL | Gate Driver Supply Voltage | - | -0.3 to +28.0 | V |
| DP, DN<br>CP,CN | Differential Input Voltage | - | 1.65 | V |
| $T_A$ | Operating Temperature | - | -40 to +85 | ºC |
| $T_{STG}$ | Storage Temperature | - | -55 to +125 | ºC |

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

Display driver IC is a UV sensitive device; so do not let the front or backside of an IC under UV exposure. An appropriate coating, module design and assembly methods to adequately protect the IC from UV are required for application.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

# 10 AC CHARACTERISTICS

## 10.1 MIPI CHARACTERISTICS

**Table 10-1: MIPI DPHY Characteristics**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| MIPI HS Receiver | | | | | | |
| $F_{SPEED}$ | MIPI Data Lane Speed | Please see Note 1 | 400 | | 500 | Mbps |
| UI | Unit Interval | Please see Note 2 | 2 | | | ns |
| $T_{SETUP}$ | Data to Clock Setup Time | Please see Note 3 | 0.2 | | | UI |
| $T_{HOLD}$ | Data to Clock Hold Time | Please see Note 3 | 0.2 | | | UI |
| $T_{SKEW}$ | Data to Clock Skew | Please see Note 4 | -0.2 | | | UI |
| MIPI LP Receiver | | | | | | |
| $T_{LPX}$ | LP transmission pulse width | | 50 | | | ns |

**Note 1:** The MIPI data lane speed depends on the number of data lanes, the bit per pixel (bpp) value of the display data and the operation mode (command mode).
**Note 2:** UI = 1 / $F_{SPEED}$
**Note 3:** Total setup and hold window for receiver of 0.3*UI when max rate less than 1Gbps.
**Note 4:** Total silicon and package skew delay budget of 0.3*UI when max rate less than 1Gbps.

**Table 10-2: Global Operation Timing Parameters**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CLK-POST}$ | Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$. | 60ns + 52UI | | | ns |
| $T_{CLK-PRE}$ | Minimum time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode | 8 | | | UI |
| $T_{CLK-PREPARE}$ | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | | 95 | ns |
| $T_{CLK-SETTLE}$ | Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$. | 95 | | 300 | ns |
| $T_{CLK-TERM-EN}$ | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$. | | | 38 | ns |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | | | ns |
| $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | | | ns |
| $T_{D-TERM-EN}$ | Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$. | | | 35ns + 4UI | ns |
| $T_{EOT}$ | Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLKTRAIL}$, to the start of the LP-11 state following a HS burst. | | | 105ns + n*12UI | ns |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | 100 | | | ns |
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40ns + 4UI | | 85ns + 6UI | ns |
| $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ | $T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | 145ns + 10UI | | | ns |
| $T_{HS-ZERO}$ | Time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence | 100 | | | ns |
| $T_{HS-SETTLE}$ | Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$. | 85ns + 6UI | | 145ns + 10UI | ns |
| $T_{HS-SKIP}$ | Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst. | 40 | | 55 ns + 4*UI | ns |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst. | 100 | | | ns |
| $T_{LPX}$ | Transmitted length of any Low-Power state period | | 100 | | ns |
| Ratio $T_{LPX}$ | Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side | 2/3 | | 3/2 | |
| $T_{TA-GET}$ | Time to drive LP-00 by new TX | 5TLPX | | | |
| $T_{TA-GO}$ | Time to drive LP-00 after Turnaround Request | 4TLPX | | | |
| $T_{TA-SURE}$ | Time-out before new TX side starts driving | 1*TLPX | | 2*TLPX | |
| $T_{WAKEUP}$ | Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS. | 1 | | | ms |

**Note:** Please refer to the diagram below for the definition of the MIPI parameter.

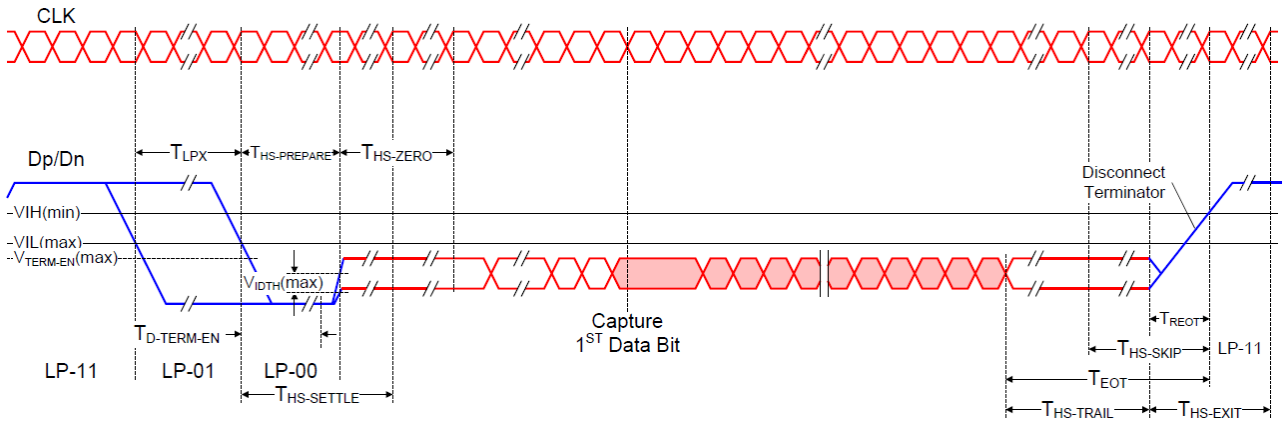



**Figure 10-1: High-Speed Data Transmission in Bursts**

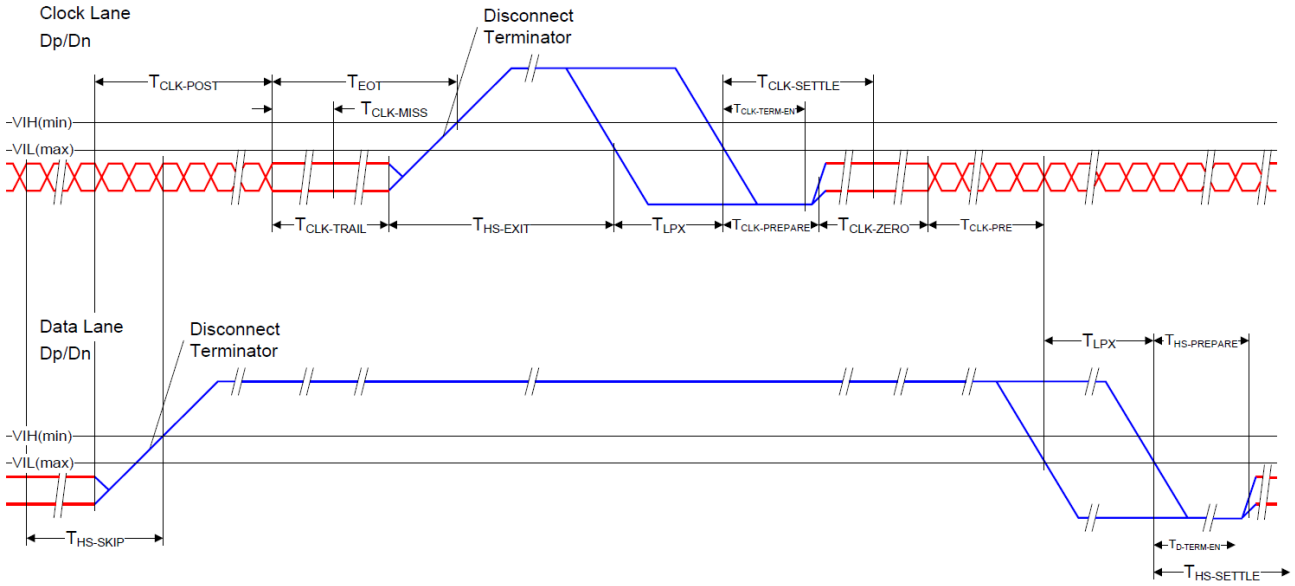



**Figure 10-2: Switching the Clock Lane between Clock Transmission and Low Power Mode**

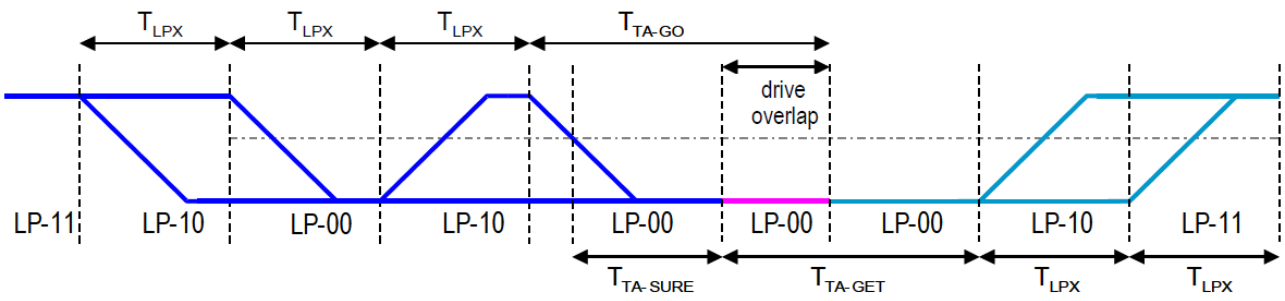



**Figure 10-3: MIPI BUS Turnaround Procedure**

# 11 DC CHARACTERISTICS

**Table 11-1: DC Characteristics**

(Unless otherwise specified, Voltage Referenced to VSS, TA = -40 to 85 ºC)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| VDDIO | Power Supply for Logic circuit | - | 1.65 | - | 3.30 | V |
| VCI | Power Supply for Analog circuit | | 2.5 | | 3.30 | V |
| **Digital IO Input/Output** | | | | | | |
| $V_{IH}$ | Logic High Level Input voltage | - | 0.8 * VDDIO | - | VDDIO | V |
| $V_{IL}$ | Logic Low Level Input voltage | - | VSS | - | 0.2 * VDDIO | V |
| $V_{OH}$ | Logic High Level Output Voltage | Iout= 1mA | 0.9 * VDDIO | - | VDDIO | V |
| $V_{OL}$ | Logic Low Level Output Voltage | Iout= -1mA | VSS | - | 0.1 * VDDIO | V |
| $I_{IH}$ | Logic High Input Current Source (Non MIPI Pin) | - | - | - | 1 | µA |
| $I_{IL}$ | Logic Low Input Current Drain (Non MIPI Pin) | - | -1 | - | - | µA |
| $I_{IH\_M}$ | Logic High Input Current Source (MIPI Pin Only) | - | - | - | 10 | µA |
| $I_{IL\_M}$ | Logic Low Input Current Drain (MIPI Pin Only) | - | -10 | - | - | µA |
| **Power Generation / Regulation Output** | | | | | | |
| VDD | Power supply for Logic circuit | - | - | 1.2 | - | V |
| MIPIVDD | Regulated Output for MIPI logic circuits | - | - | 1.2 | - | V |
| VCOM | VCOM Voltage | | -2.7 | - | 0 | V |
| DDVDH | Source Circuit Positive Power Supply | - | 4.50 | - | 6.00 | V |
| DDVDL | Source Circuit Negative Power Supply | - | -6.00 | - | -4.50 | V |
| VGH | GIP Pin Positive Power Supply | VCI=3.3V with No Loading | DDVDH+ VDDIO | - | 2x DDVDH - DDVDL | V |
| VGL | GIP Pin Negative Power Supply | - | 2x DDVDL - DDVDH | - | DDVDL- VDDIO | V |
| | VGH-VGL | - | - | - | 30 | V |
| VGHO | Regulated positive power output pin for gate driver | - | 6 | - | 15 | V |
| VGLO | Regulated negative power output pin for gate driver | - | -14 | - | -5 | V |
| **Source Driver** | | | | | | |
| Deviation | GVDDP/GVDDN deviation | Note 1,2 GVDDP/GVDDN set @ +/- 5.00V | - | - | 45 | mV |
| $S_{off}$ | Source Output offset voltage | Note 1,2 VREG1OUT/VREG2OUT set @ +/-5.00V | - | - | 45 | mV |

Note 1: VDDIO = 1.8V and at Room Temperature (25℃)
Note 2: VCI = 3V

**Table 11-2: Current Consumptions (to be updated)**

(Unless otherwise specified, Voltage Referenced to VSS, TA = 25 ºC, Display Resolution is 400x400 @ 60Hz)

| Symbol | Parameter | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Current Consumptions** | | | | | | | |
| $I_{sleep}$ | Sleep mode current | VDDIO = 1.8V<br>VCI = 3V | VDDIO | - | TBD | - | µA |
| | | | VCI | - | TBD | - | µA |
| $I_{DISPLAY}$ | Display on current | VDDIO = 1.8V<br>VCI = 3V<br>White pattern | VDDIO | - | TBD | - | mA |
| | | | VCI | - | TBD | - | mA |

Note 1: VDDIO= 1.8V, VCI = 3V at Room Temperature (25℃)

**Table 11-3: MIPI DC Characteristics**

(Unless otherwise specified, Voltage Referenced to VSS, TA = -40 to 85 ºC)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **MIPI LP Transmitter** | | | | | | |
| $V_{OH}$ | Thevenin output high level | - | 1.15 | 1.2 | 1.35 | V |
| $V_{OL}$ | Thevenin output low level | - | -50 | - | 50 | mV |
| **MIPI LP Receiver** | | | | | | |
| $V_{IH}$ | Logic 1 input voltage | - | 880 | - | - | mV |
| $V_{IL}$ | Logic 0 input voltage | - | - | - | 550 | mV |
| **MIPI HS Receiver** | | | | | | |
| $V_{CMRX(}$DC) | Common mode voltage, HS Receiver mode | - | 70 | - | 330 | mV |
| $V_{IDTH}$ | Differential input high threshold | - | - | - | 70 | mV |
| $V_{IDTL}$ | Differential input low threshold | - | -70 | - | - | mV |
| $V_{IHHS}$ | Single-ended input high voltage | - | - | - | 460 | mV |
| $V_{ILHS}$ | Single-ended input low voltage | - | -40 | - | - | mV |
| $V_{TERM-EN}$ | Single-ended threshold for HS termination enable | - | - | - | 450 | mV |
| $Z_{ID}$ | Differential input impedance | - | 80 | 100 | 125 | ohm |

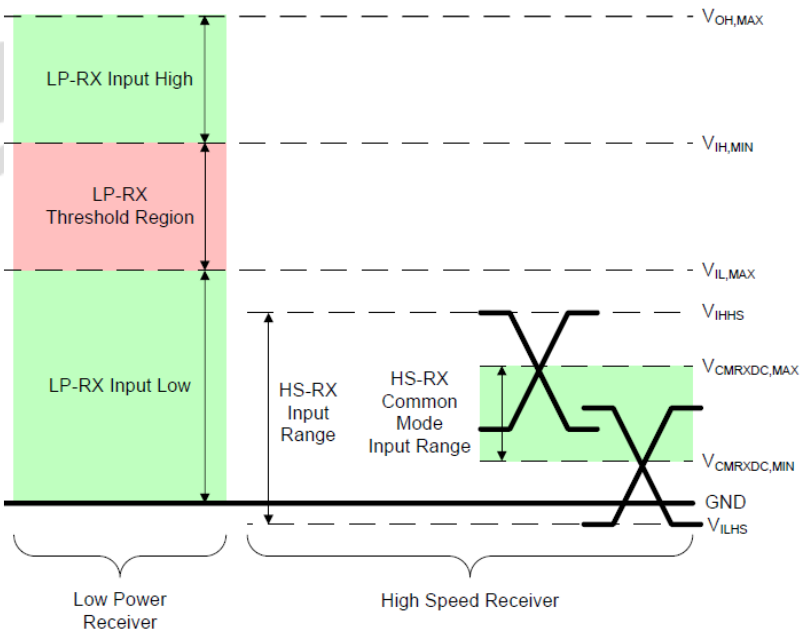


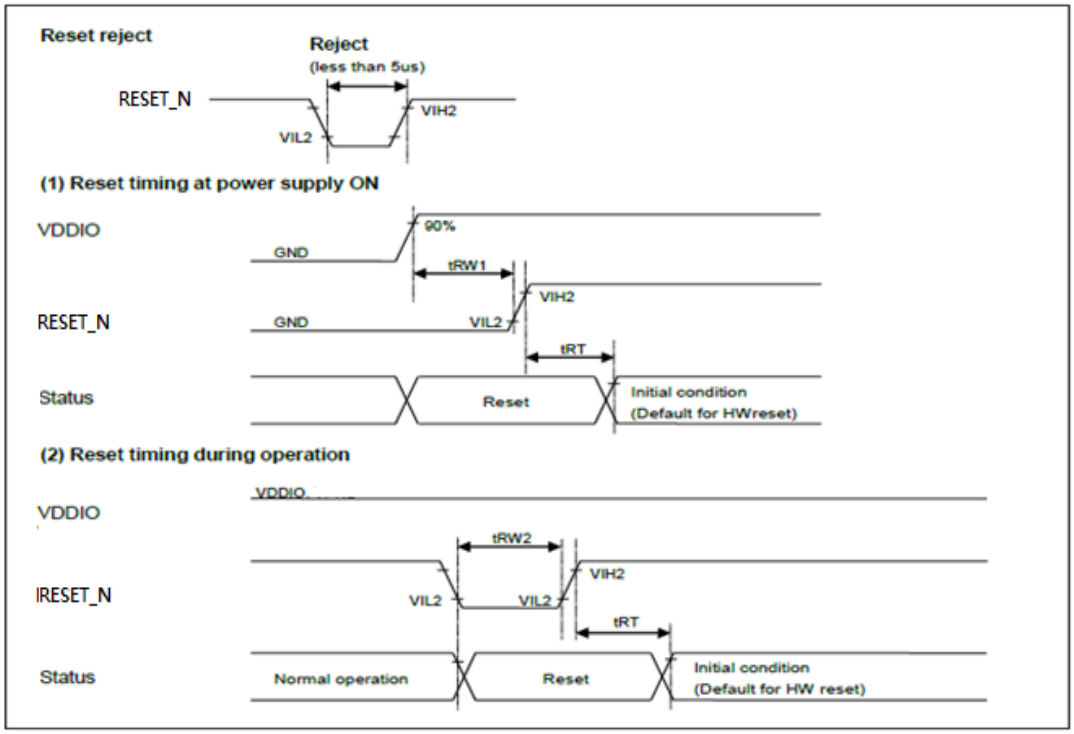

**Figure 11-1: MIPI Signal Voltage Level**

# 12 RESET CHARACTERISTICS

**Table 12-1: Reset Characteristics**

| Item | Symbol | Unit | Test Condition | Min. | Typ. | Max. |
|---|---|---|---|---|---|---|
| Reset "Low" level width 1 | tRW1 | ms | Power On | 1 | - | - |
| Reset "Low" level width 2 | tRW2 | ms | Operation | 1 | - | - |
| Reset time | tRT | ms | - | 20 | - | - |

**Figure 12-1: Reset Operation**



# 13 COMMAND TABLE

**Table 13-1: User Command Set Table**

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R00h | NOP | C | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R01h | SWRESET | D | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| R04h | ID | C | W | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | 1st Parameter | D | R | ID1[7:0] | | | | | | | |
| | 2nd Parameter | D | R | ID2[7:0] | | | | | | | |
| | 3rd Parameter | D | R | ID3[7:0] | | | | | | | |
| R09h | RDISPMODE | C | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| | 1st Parameter | D | R | 0 | 0 | 0 | 0 | RGB | 0 | SS | GS |
| | 2nd Parameter | D | R | 0 | 0 | 0 | 0 | IDMON | 0 | SLPOUT | NORM |
| | 3rd Parameter | D | R | 0 | 0 | INV | 0 | 0 | DISPON | TEON | 0 |
| | 4th Parameter | D | R | 0 | 0 | TELOM | 0 | 0 | 0 | 0 | 0 |
| R0Ah | RDDPM | C | W | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| | 1st Parameter | D | R | 0 | IDMON | 0 | SLPOUT | NORON | DISON | 0 | 0 |
| R0Bh | RDDMADCTL | C | W | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| | 1st Parameter | D | R | 0 | 0 | 0 | 0 | BGR | 0 | SS | GS |
| R0Ch | RDPIX | C | W | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| | 1st Parameter | D | R | 0 | | 0 | 0 | 0 | DBI[2:0] | | |
| R0Dh | RDDIM | C | W | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| | 1st Parameter | D | R | 0 | 0 | INV | 0 | 0 | 0 | 0 | 0 |
| R0Eh | RDDSM | C | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | 1st Parameter | D | R | TEON | TELOM | 0 | 0 | 0 | 0 | 0 | EDSI |
| R0Fh | RDDSDR | C | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| | 1st Parameter | D | R | NVLD | FUND | 0 | 0 | 0 | 0 | 0 | 0 |
| R10h | SLPIN | C | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| R11h | SLPOUT | C | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| R13h | NORON | C | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| R20h | INVOFF | C | W | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| R21h | INVON | C | W | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| R28h | DISPOFF | C | W | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| R29h | DISPON | C | W | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| R2Ah | SETCOL | C | W | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | 1st Parameter | D | W | SC[15;8] | | | | | | | |
| | 2nd Parameter | D | W | SC[7:0] | | | | | | | |
| | 3rd Parameter | D | W | EC[15:8] | | | | | | | |
| | 4th Parameter | D | W | EC[7:0] | | | | | | | |
| R2Bh | SETPAGE | C | W | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| | 1st Parameter | D | W | SP[15;8] | | | | | | | |
| | 2nd Parameter | D | W | SP[7:0] | | | | | | | |
| | 3rd Parameter | D | W | EP[15:8] | | | | | | | |
| | 4th Parameter | D | W | EP[7:0] | | | | | | | |
| R2Ch | WRMEMST | C | W | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| R34h | TEOFF | C | W | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| R35h | TEON | C | W | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| | 1st Parameter | D | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TELOM |
| R36h | MADCTR | C | W | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| | 1st Parameter | D | W | 0 | 0 | 0 | ML | BGR | 0 | SS | GS |
| R38h | IDMOFF | C | W | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| R39h | IDMON | C | W | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| R3Ah | SETPIXEL | C | W | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| | 1st Parameter | D | W | 0 | 0 | 0 | 0 | 0 | DBI[2:0] | | |
| R3Ch | WRMEMCONT | C | W | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| R44h | TESS | C | W | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| | 1st Parameter | D | W | STS [15:8] | | | | | | | |
| | 2nd Parameter | D | W | STS[7:0] | | | | | | | |
| R45h | RSS | C | W | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| | 1st Parameter | D | R | GTS [15:8] | | | | | | | |
| | 2nd Parameter | D | R | GTS[7:0] | | | | | | | |
| R51h | SETBR | C | W | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| | 1st Parameter | D | W | DBV[13:6] | | | | | | | |
| | 2nd Parameter | D | W | 0 | 0 | DBV[5:0] | | | | | |
| R53h | SETMODE | C | W | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| | 1st Parameter | D | W | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 |
| R54h | RDMODE | C | W | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| | 1st Parameter | D | R | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 |
| R55h | SETPWR | C | W | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| | 1st Parameter | D | W | 0 | 0 | 0 | 0 | 0 | PS[2:0] | | |

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R56h | RDPWR | C | W | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| | 1st Parameter | D | R | 0 | 0 | 0 | 0 | 0 | PS[2:0] | | |
| R5Eh | SETMINBR | C | W | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| | 1st Parameter | D | W | CMB[13:6] | | | | | | | |
| | 2nd Parameter | D | W | 0 | 0 | CMB[5:0] | | | | | |
| R5Fh | RDMINBR | C | W | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| | 1st Parameter | D | R | CMB[15:8] | | | | | | | |
| | 2nd Parameter | D | R | 0 | 0 | CMB[5:0] | | | | | |
| A1h | RDDDBST | C | W | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| A8h | RDDDBCON | C | W | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | | | | | | | | | | | |
| | | | | | | | | | | | |

# 14 COMMAND DESCRIPTION

## 14.1 User Command Set

### 14.1.1 NOP (00h)

| Hex Code | Command | D/C | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R00h | NOP | C | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |

| | |
|---|---|
| Description | - This command is an empty command; it does not have any effect on the display module. |
| Restriction | - |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.2 Software Reset (01h)

| Hex Code | Command | D/C | WR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R01h | SWRESET | C | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | - |

| | |
|---|---|
| Description | - When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values<br>(See default tables in each command description.).<br>- The display is blank immediately. The display turns black or white immediately that depends on the panel type. |
| Restriction | - It will be necessary to wait 5msec before sending new command following software reset.<br>- The display module loads all display module factory default values to the registers during 5msec.<br>- If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command.<br>- Software Reset Command cannot be sent during Sleep Out sequence.<br>- NVM will reload when hardware reset is applied. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |

### 14.1.3 Read ID (04h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R04h | ID | C | W | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | - |
| | 1st Parameter | D | R | ID1[7:0] | | | | | | | | 00h |
| | 2nd Parameter | D | R | ID2[7:0] | | | | | | | | 00h |
| | 3rd Parameter | D | R | ID3[7:0] | | | | | | | | 00h |

| | |
|---|---|
| Description | - This command read back ID code. |
| Restriction | - |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.4 Read Display Mode (09h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R09h | RDISPMODE | C | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | - |
| | 1st Parameter | D | R | 0 | 0 | 0 | 0 | RGB | 0 | SS | GS | 00h |
| | 2nd Parameter | D | R | 0 | 0 | 0 | 0 | IDMON | 0 | SLPOUT | NORM | 01h |
| | 3rd Parameter | D | R | 0 | 0 | INV | 0 | 0 | DISPON | TEON | 0 | 00h |
| | 4th Parameter | D | R | 0 | 0 | TELOM | 0 | 0 | 0 | 0 | 0 | 00h |

| | |
|---|---|
| Description | RGB: RGB/BGR order status<br>SS: Flip horizontal status<br>GS: Flip vertical status<br>IDMON: Idle mode status<br>SLPOUT: Sleep out status<br>NORM: Normal mode status<br>INV: Inversion mode status<br>DISPON: Display on status<br>TEON: TE status<br>TELOM: TE mode status |
| Restriction | - |
| Register Availability | Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Sleep In — Availability: Yes |

### 14.1.5 Read Display Power Mode (0Ah)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R0Ah | RDDPM | 0 | W | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | - |
| | 1st Parameter | 1 | R | 0 | IDMON | 0 | SLPOUT | NORON | DISON | 0 | 0 | 08h |

**Description**

-This command indicates the current status of the display as described in the table below:

| Bit | Bit Symbol | Description | Value |
|---|---|---|---|
| D7 | Reserved | - | - |
| D6 | IDMON | Idle Mode On/Off | '0' = Idle Mode Off,<br>'1' = Idle Mode On, |
| D5 | Reserved | - | - |
| D4 | SLPOUT | Sleep In/Out | '0' = Sleep In<br>'1' = Sleep Out, |
| D3 | NORON | Display Normal mode On/Off | '0' = Normal Display Off,<br>'1' = Normal Display On, |
| D2 | DISON | Display On/Off | '0' = Display Off,<br>'1' = Display On, |
| D1 | Reserved | - | - |
| D0 | Reserved | - | - |

**Restriction**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.6 Read Display MADCTL (0Bh)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R0Bh | RDDMADCTL | 0 | W | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | - |
| | 1st Parameter | 1 | R | 0 | 0 | 0 | 0 | BGR | 0 | SS | GS | 00h |

**Description**

-This command indicates the current status of the display as described in the table below:

| Bit | Bit Symbol | Description | Value |
|---|---|---|---|
| D7 | Reserved | - | 0 |
| D6 | Reserved | - | 0 |
| D5 | Reserved | - | 0 |
| D4 | Reserved | - | 0 |
| D3 | BGR | RGB/BGR Order | '0' =RGB, '1' =BGR |
| D2 | Reserved | - | 0 |
| D1 | SS | Flip Horizontal | '0' = Normal<br>'1' = Flipped horizontally |
| D0 | GS | Flip Vertical | '0' = Normal<br>'1' = Flipped vertically |

**Restriction**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.7 Read Color format (0Ch)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R0Ch | RDPIX | 0 | W | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | - |
| | 1st Parameter | 1 | R | 0 | 0 | 0 | 0 | 0 | DBI[2:0] | | | 07h |

| | |
|---|---|
| Description | -This command read pixel color format. |
| Restriction | - |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |

### 14.1.8 Read Display Image Mode (0Dh)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R0Dh | RDDIM | 0 | W | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | - |
| | 1st Parameter | 1 | R | 0 | 0 | INVON | 0 | 0 | 0 | 0 | 0 | 00h |

**Description**

-This command indicates the current status of the display as described in the table below:

| Bit | Bit Symbol | Description | Value |
|---|---|---|---|
| D7 | D7 | Revered | '0' |
| D6 | D6 | | |
| D5 | INVON | Inversion On/Off | '0' = Inversion is Off.<br>'1' = Inversion is On. |
| D4 | D4 | Reserved | '0' |
| D3 | D3 | | |
| D2 | D2 | | |
| D1 | D1 | | |
| D0 | D0 | | |

**Restriction**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.9 Read Signal Mode (0Eh)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R0Eh | RDDIM | 0 | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | - |
| | 1st Parameter | 1 | R | TEON | TELOM | 0 | 0 | 0 | 0 | 0 | 0 | 00h |

**Description**

-This command indicates the current status of the display as described in the table below:

| Bit | Bit Symbol | Description | Value |
|---|---|---|---|
| D7 | TEON | Tearing Effect Line | '0' : Off<br>'1' : On |
| D6 | TELOM | Tearing Effect Line Output Mode | '0' : Mode 0<br>'1' : Mode 1 |
| D5 | D5 | Revered | '0' |
| D4 | D4 | | |
| D3 | D3 | | |
| D2 | D2 | | |
| D1 | D1 | | |
| D0 | D0 | | |

**Restriction**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.10Read Signal Mode (0Fh)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R0Fh | RDDSDR | 0 | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | - |
| | 1st Parameter | 1 | R | NVLD | FUND | 0 | 0 | 0 | 0 | 0 | 0 | 00h |

**Description**

-This command indicates the current status of the display as described in the table below:

| Bit | Bit Symbol | Description | Value |
|---|---|---|---|
| D7 | NVLD | NVM Loading Detection | '0' : Not OK<br>'1' : OK |
| D6 | FUND | Functionality Detection | '0' : Not OK<br>'1' : OK |
| D5 | D5 | Revered | '0' |
| D4 | D4 | | |
| D3 | D3 | | |
| D2 | D2 | | |
| D1 | D1 | | |
| D0 | D0 | | |

**Restriction**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.11Sleep In (10h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R10h | SLPIN | C | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | - |

| | |
|---|---|
| Description | - This command causes the LCD module to enter the low power consumption mode.<br>- In this mode the DC/DC converter is disabled, and panel scanning is stopped. |
| Restriction | - This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11H).<br>- It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.<br>- It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.<br>- During sleep in mode, display data needed to be re-written into RAM before sleep out. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |

### 14.1.12Sleep Out (11h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R11h | SLPOUT | C | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | - |

| | |
|---|---|
| Description | - This command turns off sleep mode.<br>- In this mode the DC/DC converter is enabled, and panel scanning is started. |
| Restriction | -This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10H), SW Reset Command (01H) or HW Reset.<br>- It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.<br>- It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.<br>- During sleep in mode, display data needed to be re-written into RAM before sleep out. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |

### 14.1.13Normal Display Mode On (13h)

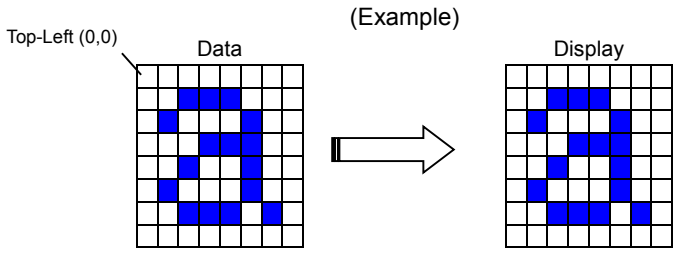
| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R13h | NORON | C | W | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | - |

| | |
|---|---|
| Description | - This command causes the display module to enter the Normal Mode. |
| Restriction | -This command has no effect when Normal mode is already active. |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

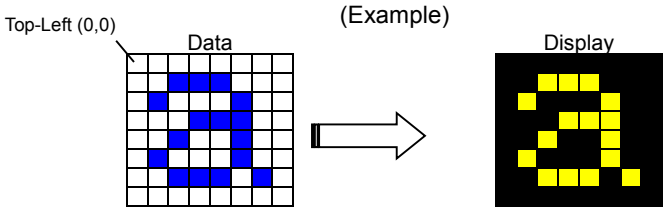
### 14.1.14Display Invert Mode Off (20h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R20h | INVOFF | C | W | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | - |

<table>
<tr><td>Description</td><td>-This command is used to recover from display inversion mode.<br>-This command does not change any other status.<br> 
</td></tr>
<tr><td>Restriction</td><td>-This command has no effect when module is already inversion off mode.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

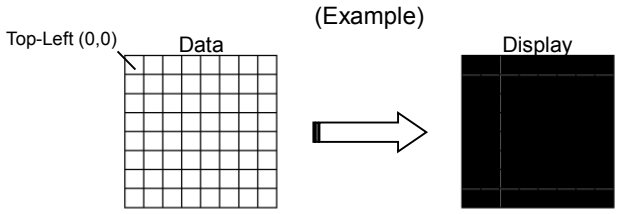
### 14.1.15Display Invert Mode On (21h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R21h | INVON | C | W | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | - |

<table>
<tr><td>Description</td><td>-This command is used to enter into display inversion mode<br>-This command does not change any other status.<br>-To exit from Display Inversion On, the Display Inversion Off command (20H) should be written.<br> 
</td></tr>
<tr><td>Restriction</td><td>-This command has no effect when module is already Inversion On mode.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

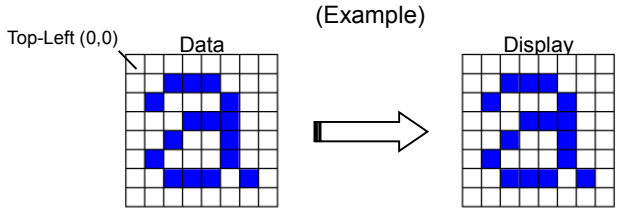
### 14.1.16Display Off (28h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R28h | DISPOFF | C | W | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | - |

| | |
|---|---|
| Description | -This command is used to enter into DISPLAY OFF mode.<br>- In this mode, the white or black image is displayed, which depends on the panel type.<br>-This command does not change any other status.<br>-There will be no abnormal visible effect on the display.<br>-Exit from this command by Display On (29H)<br>  |
| Restriction | -This command has no effect when module is already in display off mode. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |

### 14.1.17Display On (29h)

| Hex Code | Command | D/C | RDX | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R29h | DISPON | C | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | - |

| | |
|---|---|
| Description | -This command is used to recover from DISPLAY OFF mode.<br>-This command does not change any other status.<br>  |
| Restriction | -This command has no effect when module is already in display on mode. |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |

### 14.1.18Set Column (2AH)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R2Ah | SELCOL | C | W | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | - |
| | 1st Parameter | D | W | SC[15;8] | | | | | | | | 00h |
| | 2nd Parameter | D | W | SC[7:0] | | | | | | | | 00h |
| | 3rd Parameter | D | W | EC[15:8] | | | | | | | | 01h |
| | 4th Parameter | D | W | EC[7:0] | | | | | | | | 8Fh |

| | |
|---|---|
| Description | SC[15:0]: set start column<br>EC[15:0]: set end column |
| Restriction | - SC must be 4M, where M is integer<br>- EC must be 4N-1, where N is integer |
| Register Availability | Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Sleep In — Availability: Yes |

### 14.1.19Set Row (2BH)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R2Bh | SELPAGE | C | W | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | - |
| | 1st Parameter | D | W | SP[15;8] | | | | | | | | 00h |
| | 2nd Parameter | D | W | SP[7:0] | | | | | | | | 00h |
| | 3rd Parameter | D | W | EP[15:8] | | | | | | | | 01h |
| | 4th Parameter | D | W | EP[7:0] | | | | | | | | 8Fh |

| | |
|---|---|
| Description | SP[15:0]: set start row<br>EP[15:0]: set end row |
| Restriction | - |
| Register Availability | Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Sleep In — Availability: Yes |

### 14.1.20Write memory start (2CH)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R2Ch | WRMEMST | C | W | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | - |

| | |
|---|---|
| Description | Start to write memory data |
| Restriction | - Cannot write whole frame data using 0x2C.<br>- Separate whole frame into several segment. Use 0x2C and 0x3C to write whole frame data. |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.21Set Tearing Off (34H)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R34h | TEOFF | C | W | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | - |

| | |
|---|---|
| Description | - This command turns off the Tearing effect output signal from the TE signal line |
| Restriction | - This command has no effect when Tearing Effect output is already off. |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.22Set Tearing On(35H)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R35h | TEON | C | W | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | - |
| | 1st Parameter | D | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TELOM | 00h |

| | |
|---|---|
| Description | - This command turns on the Tearing effect output signal from the TE signal line. |
| Restriction | - This command has no effect when Tearing Effect output is already off.<br>- Changes in parameter TELOM is enabled form the next frame period. |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

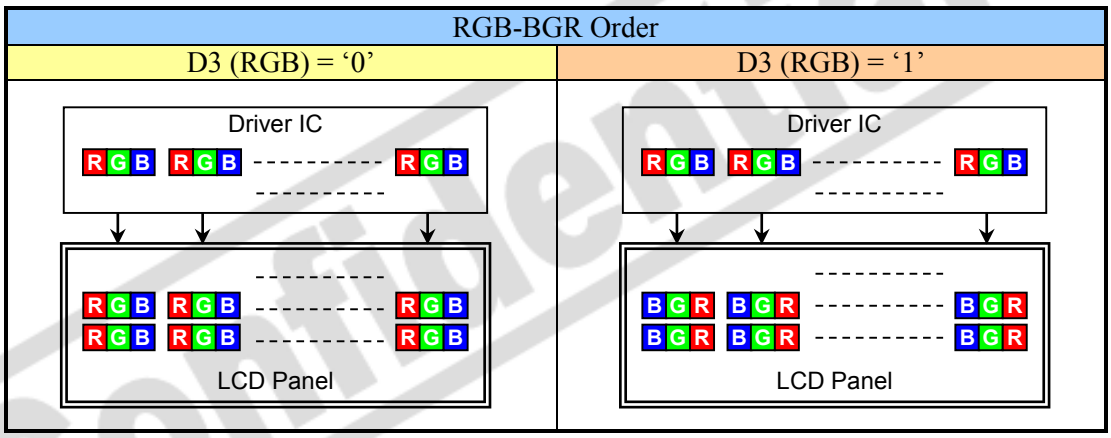
### 14.1.23Data Access Control (36H)

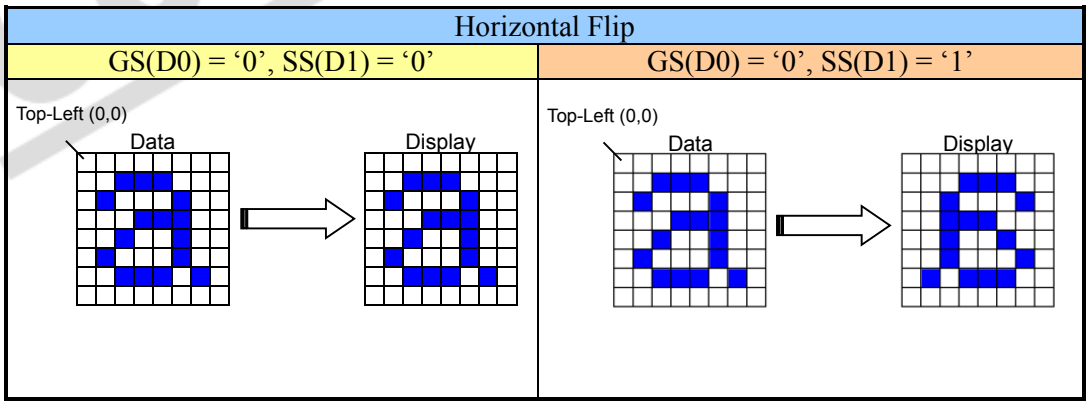
| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R36h | MADCTR | C | W | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | - |
| | 1st Parameter | D | W | 0 | 0 | 0 | 0 | RGB | 0 | SS | GS | 00h |

Description

-This command defines write scanning direction from the host processor.

| Bit | Bit Symbol | Description | Value |
|---|---|---|---|
| D7 | Revered | - | 0 |
| D6 | Revered | - | 0 |
| D5 | Revered | - | 0 |
| D4 | Revered | - | 0 |
| D3 | BGR | RGB/BGR Order | '0' =RGB, '1' =BGR |
| D2 | Revered | - | 0 |
| D1 | SS | Flip Horizontal | '0' = Normal<br>'1' = Flipped horizontally |
| D0 | GS | Flip Vertical | '0' = Normal<br>'1' = Flipped vertically |

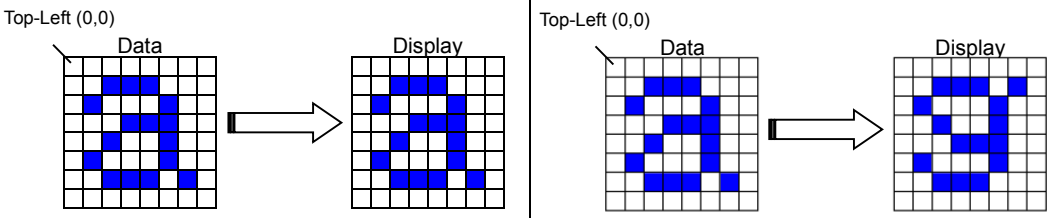


Description

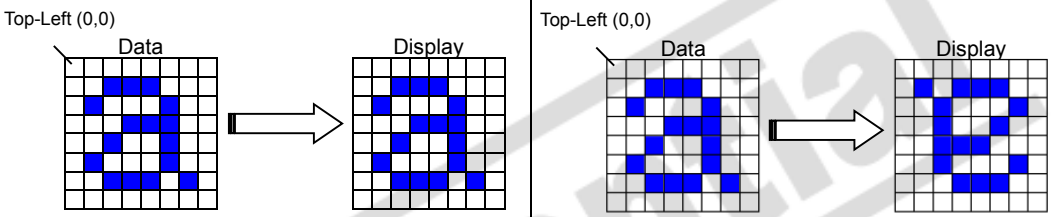
Vertical Flip

| GS(D0) = ‘0’, SS(D1) = ‘0’ | GS(D0) = ‘1’, SS(D1) = ‘0’ |
|---|---|




Vertical & Horizontal Flip

| GS(D0) = ‘0’, SS(D1) = ‘0’ | GS(D0) = ‘1’, SS(D1) = ‘1’ |
|---|---|




Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.24Idle Mode Off (38H)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R38h | IDMOFF | C | W | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | - |

| | |
|---|---|
| Description | -This command is used to recover from Idle mode on. |
| Restriction | - This command has no effect when module is already in idle off mode. |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

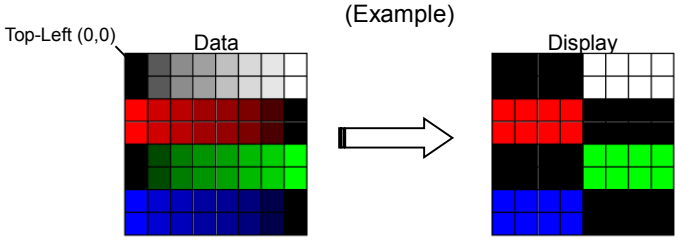
### 14.1.26Idle Mode On (39H)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R39h | IDMON | C | W | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | - |

**Description**

- This command is used to enter into Idle mode on.
- In the idle on mode, colour expression is reduced. The primary and the secondary colours using MSB of each R, G and B in the Frame Memory, 8 colour depth data is displayed.

(Example)




| Color | $R_7$ $R_6$ $R_5$ $R_4$ $R_3$ $R_2$ $R_1$ $R_0$ | $G_7$ $G_6$ $G_5$ $G_4$ $G_3$ $G_2$ $G_1$ $G_0$ | $B_7$ $B_6$ $B_5$ $B_4$ $B_3$ $B_4$ $B_1$ $B_0$ |
|---|---|---|---|
| Black | 0xxxxxxx | 0xxxxxxx | 0xxxxxxx |
| Blue | 0xxxxxxx | 0xxxxxxx | 1xxxxxxx |
| Red | 1xxxxxxx | 0xxxxxxx | 0xxxxxxx |
| Magenta | 1xxxxxxx | 0xxxxxxx | 1xxxxxxx |
| Green | 0xxxxxxx | 1xxxxxxx | 0xxxxxxx |
| Cyan | 0xxxxxxx | 1xxxxxxx | 1xxxxxxx |
| Yellow | 1xxxxxxx | 1xxxxxxx | 0xxxxxxx |
| White | 1xxxxxxx | 1xxxxxxx | 1xxxxxxx |

**Restriction**

- This command has no effect when module is already in idle off mode.

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.27Set Color format (3Ah)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R3Ah | SETPIXEL | C | W | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | - |
| | 1st Parameter | D | W | 0 | 0 | 0 | 0 | 0 | DBI[2:0] | | | 07h |

| | |
|---|---|
| Description | -This command set pixel color format.<br><br>DBI[2:-0]=7: 16.7M color<br>DBI[2:-0]=6: 262k color<br>DBI[2:-0]=5: 65k color |
| Restriction | - |
| Register Availability | Status / Availability<br>Normal Mode On, Idle Mode Off, Sleep Out / Yes<br>Normal Mode On, Idle Mode On, Sleep Out / Yes<br>Sleep In / Yes |

### 14.1.28Write memory Continue (3CH)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R3Ch | WRMEMCONT | C | W | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | - |

| | |
|---|---|
| Description | Continue to write memory data |
| Restriction | - |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.29Set Tear Scanline (44h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R44h | TESS | C | W | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | - |
| | 1st parameter | D | W | STS[15:8] | | | | | | | | 00h |
| | 2nd parameter | D | W | STS[7:0] | | | | | | | | 00h |

| | |
|---|---|
| Description | This command turns on the Tearing effect output signal from the TE signal line. |
| Restriction | This command takes effect on the frame following the current frame. Therefore, if the TE signal is already ON, TE signal is output according to the old set tear on and set tear scanline commands until the end of currently scanned frame. |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.30Get Scanline (45h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R45h | RSS | C | W | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | - |
| | 1st parameter | D | R | GTS[15:8] | | | | | | | | 00h |
| | 2nd parameter | D | R | GTS[7:0] | | | | | | | | 00h |

| | |
|---|---|
| Description | The display module returns the current scan line.<br>The first scan line of back porch period is defined as line 0. |
| Restriction | - |
| Register Availability | Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Sleep In — Availability: Yes |

### 14.1.31Write Display Brightness (51h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R51h | SETBR | C | W | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | - |
| | 1st parameter | D | W | DBV[13:6] | | | | | | | | 00h |
| | 2nd parameter | D | W | 0 | 0 | DBV[5:0] | | | | | | 00h |

| | |
|---|---|
| Description | - This command is used to set the display brightness value. |
| Restriction | - |
| Register Availability | |

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.32Set Display Brightness mode(53h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R53h | SETMODE | C | W | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | - |
| | 1st parameter | D | W | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | 00h |

**Description**

This command is used to set the value of display brightness control.

| Bit | Bit Symbol | Description |
|---|---|---|
| D7 | D7 | Reserved |
| D6 | D6 | |
| D5 | BCTRL | Brightness Control Block On/Off, This bit is always used to switch brightness for display<br>0 = Off<br>1 = On<br>When this bit is set to off, the setting on DBV(51h) will be ignored. The PWM duty will be controlled only by CABC function. |
| D4 | D4 | Reserved |
| D3 | DD | Display Dimming (DD): (Only for manual brightness setting)<br>0 = Off<br>1 = On:<br>This bit is used to enable/disable PWM dimming function. When this bit is set to "1", the PWM duty will change from existing value to the target value (DBV) in a constant speed while the transition timing is control by the field "BCB" of command 0xC8. |
| D2 | BL | BL: Backlight Control On/Off<br>0 = Off (Completely turn off backlight circuit. Control lines must be low.)<br>1 = On |
| D1 | D1 | Reserved |
| D0 | D0 | |

**Restriction**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.33Read Display Brightness mode(54h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R54h | RDMODE | C | W | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | - |
| | 1st parameter | D | R | 0 | 0 | BCTRL | 0 | DD | BL | 0 | 0 | 00h |

**Description**

This command returns the value of display brightness control.

| Bit | Bit Symbol | Description |
|---|---|---|
| D7 | D7 | Reserved |
| D6 | D6 | |
| D5 | BCTRL | Brightness Control Block On/Off, This bit is always used to switch brightness for display<br>0 = Off<br>1 = On<br>When this bit is set to off, the setting on DBV(51h) will be ignored. The PWM duty will be controlled only by CABC function. |
| D4 | D4 | Reserved |
| D3 | DD | Display Dimming (DD): (Only for manual brightness setting)<br>0 = Off<br>1 = On:<br>This bit is used to enable/disable PWM dimming function. When this bit is set to "1", the PWM duty will change from existing value to the target value (DBV) in a constant speed while the transition timing is control by the field "BCB" of command 0xC8. |
| D2 | BL | BL: Backlight Control On/Off<br>0 = Off (Completely turn off backlight circuit. Control lines must be low.)<br>1 = On |
| D1 | D1 | Reserved |
| D0 | D0 | |

**Restriction**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.34Set CABC control (55h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R55h | SETPWR | C | W | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | - |
| | 1st parameter | D | W | 0 | 0 | 0 | 0 | 0 | 0 | CABC[1:0] | | 00h |

**Description**

This command set the power saving level.

| Bit | Bit Symbol | Description |
|---|---|---|
| D7 | D7 | Reserved |
| D6 | D6 | |
| D5 | D5 | |
| D4 | D4 | |
| D3 | D3 | |
| D2 | D2 | |
| D1 | CABC[1:0] | ‘00’ = Disable<br>‘01’ = low<br>‘10’ = middle<br>‘11’ = high |
| D0 | | |

**Restriction**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.35Read CABC control (56h)

| Hex Code | Command | D/C | W/R | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R56h | RDPWR | C | W | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | - |
| | 1st parameter | D | R | 0 | 0 | 0 | 0 | 0 | 0 | CABC[1:0] | | 00h |

**Description**

This command returns the power saving level.

| Bit | Bit Symbol | Description |
|---|---|---|
| D7 | D7 | Reserved |
| D6 | D6 | |
| D5 | D5 | |
| D4 | D4 | |
| D3 | D3 | |
| D2 | D2 | |
| D1 | CABC[1:0] | ‘00’ = Disable<br>‘01’ = low<br>‘10’ = middle<br>‘11’ = high |
| D0 | | |

**Restriction**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.36Set CABC Minimum Brightness (5Eh)

| Hex Code | Command | D/C | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R5Eh | SETMINBR | C | W | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | - |
| | 1st parameter | D | W | CMB[13:6] | | | | | | | | |
| | 1nd parameter | D | W | 0 | 0 | CMB[5:0] | | | | | | 00h |

| | |
|---|---|
| Description | This command set CABC minimum brightness. |
| Restriction | - |

Register Availability

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.37Read CABC Minimum Brightness (5Fh)

| Hex Code | Command | D/C | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R5Fh | RDMINBR | C | W | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | - |
| | 1st parameter | D | R | CMB[13:6] | | | | | | | | |
| | 2nd parameter | D | R | 0 | 0 | CMB[5:0] | | | | | | 00h |

| | |
|---|---|
| Description | This command returns CABC minimum brightness. |
| Restriction | - |
| Register Availability | Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes<br>Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes<br>Status: Sleep In — Availability: Yes |

### 14.1.38Read DDB Start (A1h)

| Hex Code | Command | D/C | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA1h | RDDDBS | C | W | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | - |
| | 1st parameter | D | R | SID[7:0] | | | | | | | | 00h |
| | 2nd parameter | D | R | SID[15:8] | | | | | | | | 00h |
| | 3rd parameter | D | R | MID[7:0] | | | | | | | | 00h |
| | 4th parameter | D | R | MID[15:8] | | | | | | | | 00h |
| | 5th parameter | D | R | RID[7:0] | | | | | | | | 00h |
| | 6th parameter | D | R | RID[15:8] | | | | | | | | 00h |

**Description**

Start to read manufacturer ID

| Parameter | Code | Description |
|---|---|---|
| 1st Parameter | SID[7:0] | Upper Byte of SSL ID code |
| 2nd Parameter | SID[15:8] | Lower Byte of SSL ID code |
| 3rd Parameter | MID[7:0] | Upper Byte of Manufacturer version |
| 4th Parameter | MID[15:8] | Lower Byte of Manufacturer version |
| 5th Parameter | RID [7:0] | SSL INTERNAL USED |
| 6th Parameter | RID [15:8] | SSL INTERNAL USED |

**Restriction**

-

**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

### 14.1.39Read DDB Continue (A8h)

| Hex Code | Command | D/C | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | POR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RA8h | RDDDBCON | C | W | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | - |
| | 1st parameter | D | R | SID[7:0] | | | | | | | | 00h |
| | 2nd parameter | D | R | SID[15:8] | | | | | | | | 00h |
| | 3rd parameter | D | R | MID[7:0] | | | | | | | | 00h |
| | 4th parameter | D | R | MID[15:8] | | | | | | | | 00h |
| | 5th parameter | D | R | RID[7:0] | | | | | | | | 00h |
| | 6th parameter | D | R | RID[15:8] | | | | | | | | 00h |

**Description**

Continue to read manufacturer ID

| Parameter | Code | Description |
|---|---|---|
| 1st Parameter | SID[7:0] | Upper Byte of SSL ID code |
| 2nd Parameter | SID[15:8] | Lower Byte of SSL ID code |
| 3rd Parameter | MID[7:0] | Upper Byte of Manufacturer version |
| 4th Parameter | MID[15:8] | Lower Byte of Manufacturer version |
| 5th Parameter | RID [7:0] | SSL INTERNAL USED |
| 6th Parameter | RID [15:8] | SSL INTERNAL USED |

**Restriction**

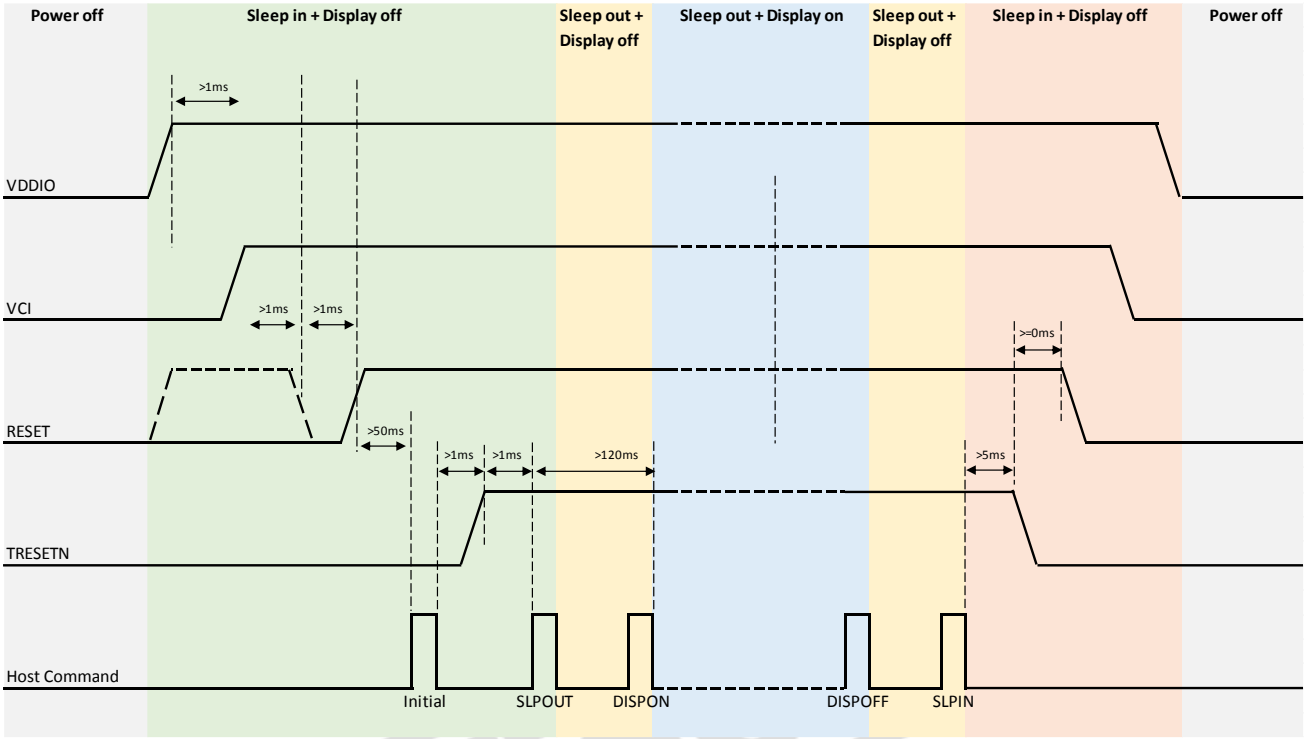
-

**Register Availability**

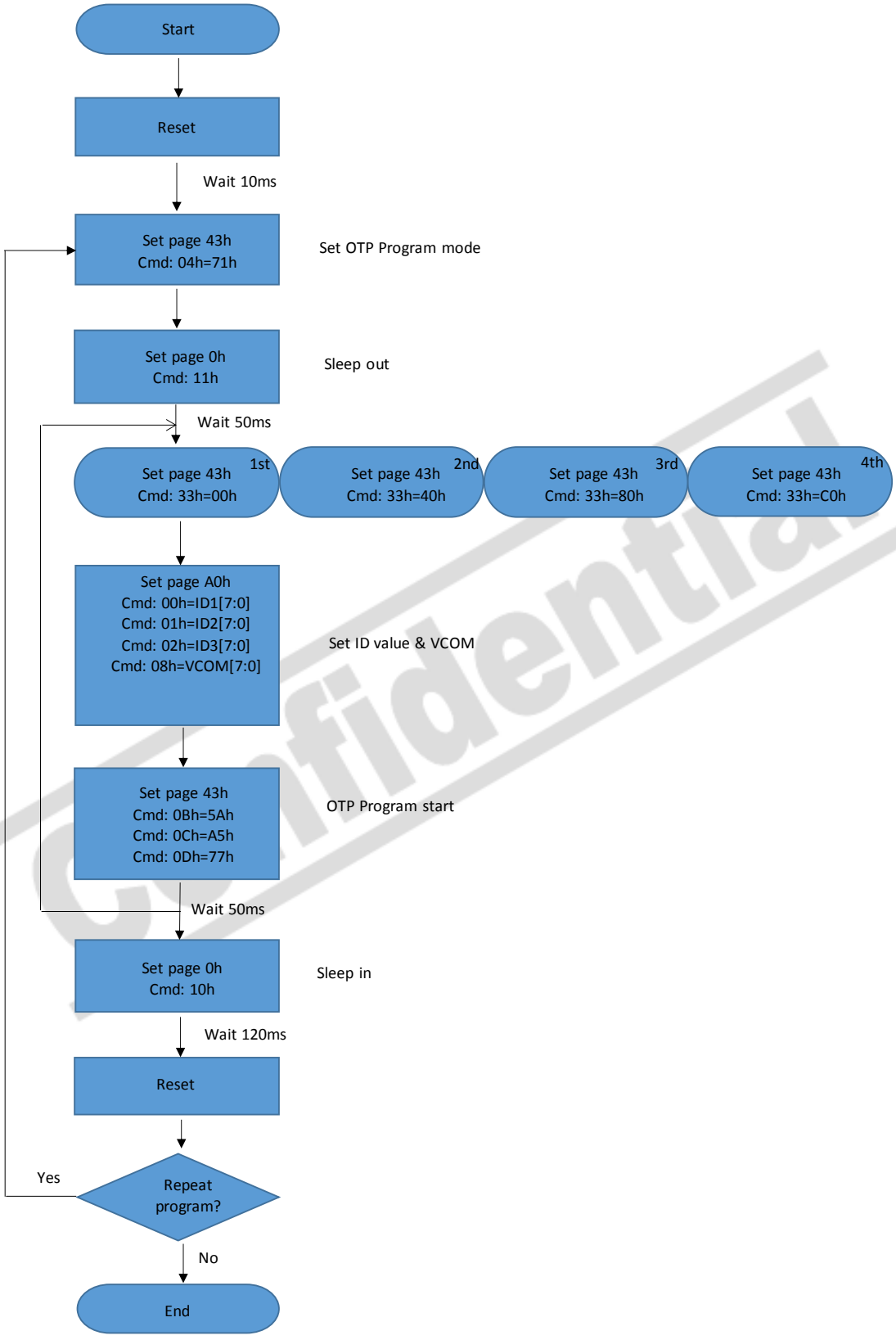
| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

# 15 POWER ON/OFF SEQUENCES

Figure 15-1: Power On/Off Sequence

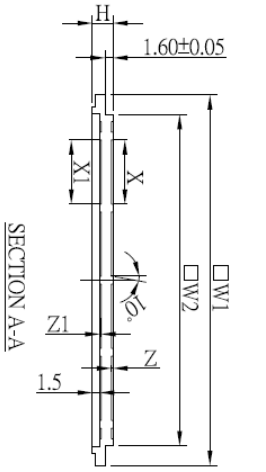


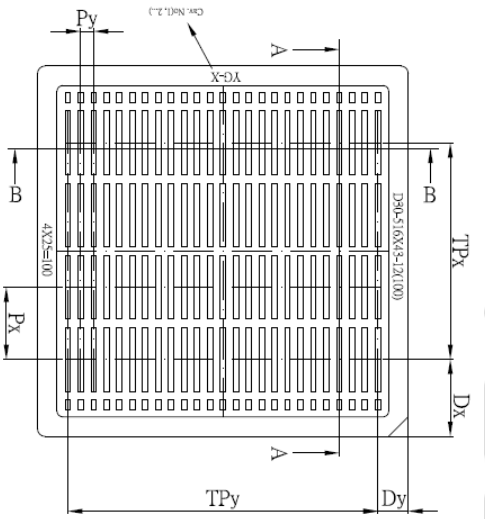
# 16 OTP PROGRAM FLOW CHART



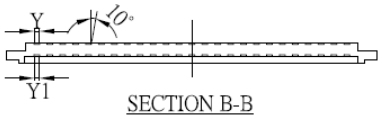
# 17 PACKAGE INFORMATION

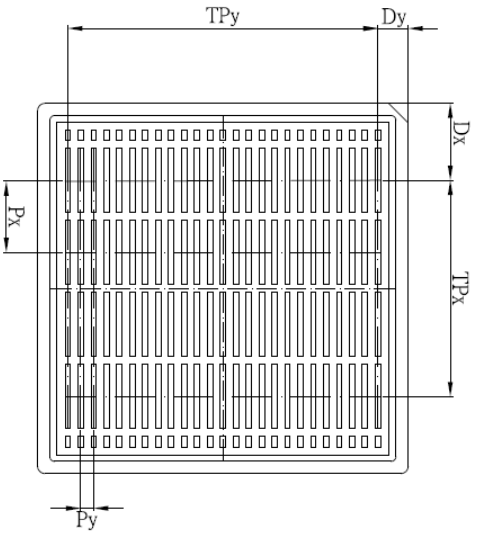
## 17.1 Chip Tray Information




| | Spec. | |
|---|---|---|
| W1 | 76.00±0.10 | (2992) |
| W2 | 68.00±0.10 | (2677) |
| W3 | 68.30±0.10 | (2689) |
| H | 4.20±0.10 | (165) |
| Px | 14.80±0.05 | (583) |
| Py | 2.65±0.05 | (104) |
| Dx | 15.80±0.05 | (622) |
| TPx | 44.40±0.10 | (1748) |
| Dy | 6.20±0.05 | (244) |
| TPy | 63.60±0.10 | (2504) |
| X | 13.104±0.05 | (516) |
| Y | 1.098±0.05 | (43) |
| Z | 0.80±0.05 | (12) |
| X1 | 13.104±0.05 | (516) |
| Y1 | 1.098±0.05 | (43) |
| Z1 | 0.80±0.05 | (12) |
| N | 100(pocket number) | |




Remark:

1.Tray material : ABS
2.Tray color code: Black
3.Tray warpage: Max. ± 0.1mm
4.Surface resistance:$10^{9}$~$10^{12}$Ω/sq
5.Pocket size(top side): 13.104 x1.098 x 0.30 mm
6.Pocket size(bottom side): 13.104 x1.098 x 0.30 mm
7.Bump face down
8.Chip size:13.004 x0.998 x 0.20 mm(with scribe line)
9.Bottom of pocket Rough surface

The product(s) listed in this datasheet comply with Directive (EU) 2015/863 of 31 March 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances and People's Republic of China Electronic Industry Standard GB/T 26572-2011 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子电器产品中限用物質的限用要求)". Hazardous Substances test report is available upon request.

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