

SSD1351

Advance Information

128 RGB x 128 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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SSD1351

Rev 1.4

P 1/58

Jul 2010

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Appendix: IC Revision history of SSD1351 Specification

| Version | Change Items | Effective Date |
|----------------|---|-----------------------|
| 0.10 | 1. 1 st release | 10-Jun-08 |
| 1.0 | <ol style="list-style-type: none"> 1. Change to Advance Info 2. Revise die thickness tolerance from $\pm 25\mu\text{m}$ to $\pm 15\mu\text{m}$ 3. Revise table 12-1 DC characteristic 4. Revise tables 13 AC characteristic 5. Revise command table 6. Revise V_{CC} voltage range | 12-Dec-08 |
| 1.1 | 1. Revised section 8.1 MCU interface | 19-Feb-09 |
| 1.2 | <ol style="list-style-type: none"> 1 Change “Gold Bump Die” to “COG” for SSD1351Z in Table 3-1 Ordering information 2 Revise typo in Figure 5 1: SSD1351Z Die Drawing (position of L, T alignment mark) 3 Revise typo in P.45 : 10.1.9 Set Function selection (ABh) 4 Add Note 2 in application example Fig 14-1 | 31-Aug-09 |
| 1.3 | <ol style="list-style-type: none"> 1 Added +/- 0.05mm tolerance for Die Size (after sawing) in Section 5 – P.9 2 Added command C1h in the description of command FDh – P.37 3 Revised typo error on the description of command C1h – P.46 4 Updated the $I_{SLP_{VCI}}$ sleep mode current section of Table 12-1 (Max = 50uA when internal V_{DD} is enabled) – P.49 5 Revised declaimer | 27-Oct-09 |
| 1.4 | <ol style="list-style-type: none"> 1 P.30 Update Power On/OFF sequence 2 P.51 Revise Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics 3 P.52 Revise Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics 4 P.53 Revise Table 13-4 : Serial Interface Timing Characteristics (4-wire SPI) 5 P.54 Revise Table 13-5: Serial Interface Timing Characteristics (3-wire SPI) | 23-Jul-10 |

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1 GENERAL DESCRIPTION

The SSD1351 is a CMOS OLED/PLED driver with 384 segments and 128 commons output, supporting up to 128RGB x 128 dot matrix display. This chip is designed for Common Cathode type OLED/PLED panel.

The SSD1351 has embedded Graphic Display Data RAM (GDDRAM). It supports with 8, 16, 18 bits 8080 / 6800 parallel interface, Serial Peripheral Interface. It has 256-step contrast and 262K color control, giving vivid color display on OLED panels.

2 FEATURES

- Resolution: 128 RGB x 128 dot matrix panel
- 262k color depth supported by embedded 128x128x18 bit SRAM display buffer
- Power supply
 - $V_{DD} = 2.4V - 2.6V$ (Core V_{DD} power supply, can be regulated from V_{CI})
 - $V_{DDIO} = 1.65V - V_{CI}$ (MCU interface logic level)
 - $V_{CI} = 2.4V - 3.5V$ (Low voltage power supply)
 - $V_{CC} = 10.0V - 18.0V$ (Panel driving power supply)
 - When V_{CI} is lower than 2.6V, V_{DD} should be supplied by external power source
- Segment maximum source current: 200uA
- Common maximum sink current: 70mA
- 256 step brightness current control for the each color component plus 16 step master current control
- Pin selectable MCU Interfaces:
 - 8/16/18 bits 6800-series parallel interface
 - 8/16/18 bits 8080-series parallel interface
 - 3-wire and 4-wire Serial Peripheral Interface
- Support various color depths
 - 262k color (6:6:6)
 - 65k color (5:6:5)
- Gamma Look Up Tables (GLUT) with 8 bit entry
- Row re-mapping and Column re-mapping
- Vertical and horizontal scrolling
- Programmable Frame Rate and Multiplexing Ratio
- On-Chip Oscillator
- Color Swapping Function (RGB – BGR), arranged in RGB sequence when reset
- Slim chip layout for COF
- Operating temperature range -40°C to 85°C.

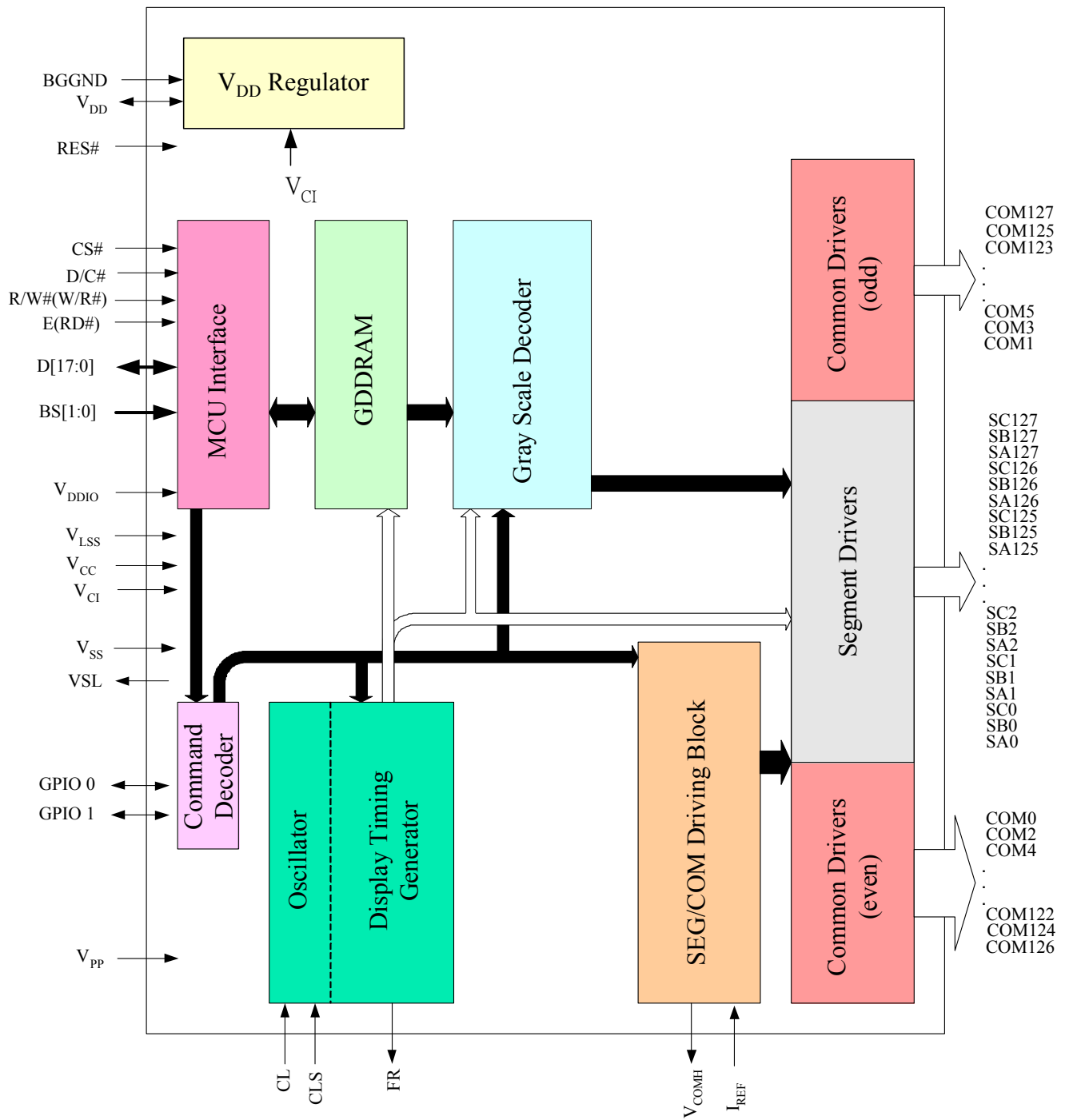
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

| Ordering Part Number | SEG | COM | Package Form | Reference | Remark |
|----------------------|--------|-----|--------------|-----------|--|
| SSD1351Z | 128RGB | 128 | COG | 9 , 57 | <ul style="list-style-type: none"> • Min SEG pad pitch: 25um • Min COM pad pitch: 35um • Die thickness : 300 +/- 15um |
| SSD1351UR1 | 128RGB | 128 | COF | 12 , 56 | <ul style="list-style-type: none"> • 48mm film, 4 sprocket hole • Hot bar type COF • 8/16/18-bit 80/68/SPI interface • SEG lead pitch: 0.050x0.999=0.04995mm • COM lead pitch: 0.06x0.999=0.05994mm |

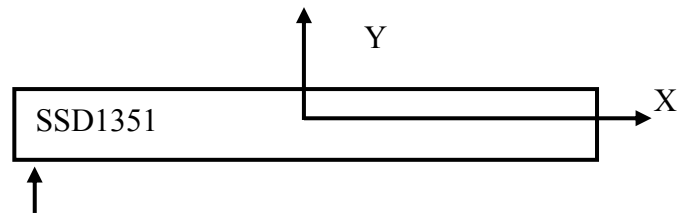
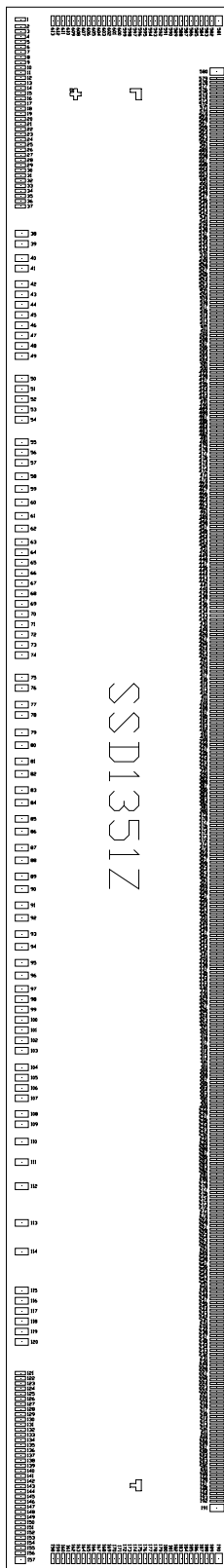
4 BLOCK DIAGRAM

Figure 4-1 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1: SSD1351Z Die Drawing



Pad 1,2,3,->613
Gold Bumps face up

| | |
|-------------------------|--|
| Die size (after sawing) | 10.7mm \pm 0.05mm x 1.5mm \pm 0.05mm |
| Die Thickness | 300 +/- 15um |
| Min I/O pad pitch | 70um |
| Min SEG pad pitch | 25um |
| Min COM pad pitch | 35um |

| | |
|----------------------|--------------|
| Bump height | Nominal 15um |
| Bump size | |
| Pad 1, 157 | 49um x 70um |
| Pad 2-37, 121-156 | 23um x 70um |
| Pad 38-120 | 45um x 90um |
| Pad 158-189, 582-613 | 70um x 23um |
| Pad 192-579 | 13um x 96um |
| Pad 190,581 | 70um x 49um |
| Pad 191,580 | 50um x 96um |

| Alignment mark | | |
|----------------|---------------------|-------------|
| L shape | (-4736.35, 126.58) | 75um x 75um |
| T shape | (4736.35, 126.58) | 75um x 75um |
| + shape | (-4736.35, -284.77) | 75um x 75um |

Table 5-1: SSD1351Z Bump Die Pad Coordinates

| Pad # | Pad Name | X-Axis | Y-Axis | Pad # | Pad Name | X-Axis | Y-Axis | Pad # | Pad Name | X-Axis | Y-Axis | Pad # | Pad Name | X-Axis | Y-Axis |
|-------|------------|----------|---------|-------|----------|---------|---------|-------|----------|---------|---------|-------|----------|---------|--------|
| 1 | NC | -5245.12 | -662.08 | 81 | D2 | -193.30 | -651.82 | 161 | COM28 | 5234.62 | -335.04 | 241 | SB16 | 3618.00 | 681.25 |
| 2 | COM94 | -5197.62 | -662.08 | 82 | D3 | -107.30 | -651.82 | 162 | COM27 | 5234.62 | -300.04 | 242 | SC16 | 3593.00 | 681.25 |
| 3 | COM95 | -5162.62 | -662.08 | 83 | D4 | 2.70 | -651.82 | 163 | COM26 | 5234.62 | -265.04 | 243 | SA17 | 3568.00 | 681.25 |
| 4 | COM96 | -5127.62 | -662.08 | 84 | D5 | 88.70 | -651.82 | 164 | COM25 | 5234.62 | -230.04 | 244 | SB17 | 3543.00 | 681.25 |
| 5 | COM97 | -5092.62 | -662.08 | 85 | D6 | 198.70 | -651.82 | 165 | COM24 | 5234.62 | -195.04 | 245 | SC17 | 3518.00 | 681.25 |
| 6 | COM98 | -5057.62 | -662.08 | 86 | D7 | 284.70 | -651.82 | 166 | COM23 | 5234.62 | -160.04 | 246 | SA18 | 3493.00 | 681.25 |
| 7 | COM99 | -5022.62 | -662.08 | 87 | D8 | 394.70 | -651.82 | 167 | COM22 | 5234.62 | -125.04 | 247 | SB18 | 3468.00 | 681.25 |
| 8 | COM100 | -4987.62 | -662.08 | 88 | D9 | 480.70 | -651.82 | 168 | COM21 | 5234.62 | -90.04 | 248 | SC18 | 3443.00 | 681.25 |
| 9 | COM101 | -4952.62 | -662.08 | 89 | D10 | 590.70 | -651.82 | 169 | COM20 | 5234.62 | -55.04 | 249 | SA19 | 3418.00 | 681.25 |
| 10 | COM102 | -4917.62 | -662.08 | 90 | D11 | 676.70 | -651.82 | 170 | COM19 | 5234.62 | -20.04 | 250 | SB19 | 3393.00 | 681.25 |
| 11 | COM103 | -4882.62 | -662.08 | 91 | D12 | 786.70 | -651.82 | 171 | COM18 | 5234.62 | 14.96 | 251 | SC19 | 3368.00 | 681.25 |
| 12 | COM104 | -4847.62 | -662.08 | 92 | D13 | 872.70 | -651.82 | 172 | COM17 | 5234.62 | 49.96 | 252 | SA20 | 3343.00 | 681.25 |
| 13 | COM105 | -4812.62 | -662.08 | 93 | D14 | 982.70 | -651.82 | 173 | COM16 | 5234.62 | 84.96 | 253 | SB20 | 3318.00 | 681.25 |
| 14 | COM106 | -4777.62 | -662.08 | 94 | D15 | 1068.70 | -651.82 | 174 | COM15 | 5234.62 | 119.96 | 254 | SC20 | 3293.00 | 681.25 |
| 15 | COM107 | -4742.62 | -662.08 | 95 | D16 | 1178.70 | -651.82 | 175 | COM14 | 5234.62 | 154.96 | 255 | SA21 | 3268.00 | 681.25 |
| 16 | COM108 | -4707.62 | -662.08 | 96 | D17 | 1264.70 | -651.82 | 176 | COM13 | 5234.62 | 189.96 | 256 | SB21 | 3243.00 | 681.25 |
| 17 | COM109 | -4672.62 | -662.08 | 97 | VSS | 1356.70 | -651.82 | 177 | COM12 | 5234.62 | 224.96 | 257 | SC21 | 3218.00 | 681.25 |
| 18 | COM110 | -4637.62 | -662.08 | 98 | BGGND | 1426.70 | -651.82 | 178 | COM11 | 5234.62 | 259.96 | 258 | SA22 | 3193.00 | 681.25 |
| 19 | COM111 | -4602.62 | -662.08 | 99 | VSL | 1496.70 | -651.82 | 179 | COM10 | 5234.62 | 294.96 | 259 | SB22 | 3168.00 | 681.25 |
| 20 | COM112 | -4567.62 | -662.08 | 100 | VSL | 1566.70 | -651.82 | 180 | COM9 | 5234.62 | 329.96 | 260 | SC22 | 3143.00 | 681.25 |
| 21 | COM113 | -4532.62 | -662.08 | 101 | CLS | 1636.70 | -651.82 | 181 | COM8 | 5234.62 | 364.96 | 261 | SA23 | 3118.00 | 681.25 |
| 22 | COM114 | -4497.62 | -662.08 | 102 | VDDIO | 1706.70 | -651.82 | 182 | COM7 | 5234.62 | 399.96 | 262 | SB23 | 3093.00 | 681.25 |
| 23 | COM115 | -4462.62 | -662.08 | 103 | VDDIO | 1776.70 | -651.82 | 183 | COM6 | 5234.62 | 434.96 | 263 | SC23 | 3068.00 | 681.25 |
| 24 | COM116 | -4427.62 | -662.08 | 104 | VSS | 1890.70 | -651.82 | 184 | COM5 | 5234.62 | 469.96 | 264 | SA24 | 3043.00 | 681.25 |
| 25 | COM117 | -4392.62 | -662.08 | 105 | VLSS | 1960.70 | -651.82 | 185 | COM4 | 5234.62 | 504.96 | 265 | SB24 | 3018.00 | 681.25 |
| 26 | COM118 | -4357.62 | -662.08 | 106 | VCOMH | 2030.70 | -651.82 | 186 | COM3 | 5234.62 | 539.96 | 266 | SC24 | 2993.00 | 681.25 |
| 27 | COM119 | -4322.62 | -662.08 | 107 | VCOMH | 2100.70 | -651.82 | 187 | COM2 | 5234.62 | 574.96 | 267 | SA25 | 2968.00 | 681.25 |
| 28 | COM120 | -4287.62 | -662.08 | 108 | VCC | 2207.70 | -651.82 | 188 | COM1 | 5234.62 | 609.96 | 268 | SB25 | 2943.00 | 681.25 |
| 29 | COM121 | -4252.62 | -662.08 | 109 | VCC | 2277.70 | -651.82 | 189 | COM0 | 5234.62 | 644.96 | 269 | SC25 | 2918.00 | 681.25 |
| 30 | COM122 | -4217.62 | -662.08 | 110 | TR0 | 2395.70 | -651.82 | 190 | NC | 5234.62 | 692.96 | 270 | SA26 | 2893.00 | 681.25 |
| 31 | COM123 | -4182.62 | -662.08 | 111 | VC1 | 2535.70 | -651.82 | 191 | VLSS | 4890.00 | 681.25 | 271 | SB26 | 2868.00 | 681.25 |
| 32 | COM124 | -4147.62 | -662.08 | 112 | TR1 | 2699.70 | -651.82 | 192 | SA0 | 4843.00 | 681.25 | 272 | SC26 | 2843.00 | 681.25 |
| 33 | COM125 | -4112.62 | -662.08 | 113 | TR2 | 2949.70 | -651.82 | 193 | SB0 | 4818.00 | 681.25 | 273 | SA27 | 2818.00 | 681.25 |
| 34 | COM126 | -4077.62 | -662.08 | 114 | TR3 | 3144.70 | -651.82 | 194 | SC0 | 4793.00 | 681.25 | 274 | SB27 | 2793.00 | 681.25 |
| 35 | COM127 | -4042.62 | -662.08 | 115 | TR4 | 3409.70 | -651.82 | 195 | SA1 | 4768.00 | 681.25 | 275 | SC27 | 2768.00 | 681.25 |
| 36 | VLSS | -4007.62 | -662.08 | 116 | VSS1 | 3479.70 | -651.82 | 196 | SB1 | 4743.00 | 681.25 | 276 | SA28 | 2743.00 | 681.25 |
| 37 | VLSS | -3972.62 | -662.08 | 117 | VLSS | 3549.70 | -651.82 | 197 | SC1 | 4718.00 | 681.25 | 277 | SB28 | 2718.00 | 681.25 |
| 38 | VLSS | -3786.30 | -651.82 | 118 | VLSS | 3619.70 | -651.82 | 198 | SA2 | 4693.00 | 681.25 | 278 | SC28 | 2693.00 | 681.25 |
| 39 | VSS | -3716.30 | -651.82 | 119 | VSS | 3689.70 | -651.82 | 199 | SB2 | 4668.00 | 681.25 | 279 | SA29 | 2668.00 | 681.25 |
| 40 | VCC | -3619.30 | -651.82 | 120 | VSS | 3759.70 | -651.82 | 200 | SC2 | 4643.00 | 681.25 | 280 | SB29 | 2643.00 | 681.25 |
| 41 | VCC | -3549.30 | -651.82 | 121 | VLSS | 3972.62 | -662.08 | 201 | SA3 | 4618.00 | 681.25 | 281 | SC29 | 2618.00 | 681.25 |
| 42 | VCOMH | -3442.30 | -651.82 | 122 | VLSS | 4007.62 | -662.08 | 202 | SB3 | 4593.00 | 681.25 | 282 | SA30 | 2593.00 | 681.25 |
| 43 | VLSS | -3372.30 | -651.82 | 123 | COM63 | 4042.62 | -662.08 | 203 | SC3 | 4568.00 | 681.25 | 283 | SB30 | 2568.00 | 681.25 |
| 44 | VLSS | -3302.30 | -651.82 | 124 | COM62 | 4077.62 | -662.08 | 204 | SA4 | 4543.00 | 681.25 | 284 | SC30 | 2543.00 | 681.25 |
| 45 | VSS | -3232.30 | -651.82 | 125 | COM61 | 4112.62 | -662.08 | 205 | SB4 | 4518.00 | 681.25 | 285 | SA31 | 2518.00 | 681.25 |
| 46 | VSS | -3162.30 | -651.82 | 126 | COM60 | 4147.62 | -662.08 | 206 | SC4 | 4493.00 | 681.25 | 286 | SB31 | 2493.00 | 681.25 |
| 47 | VSL | -3092.30 | -651.82 | 127 | COM59 | 4182.62 | -662.08 | 207 | SA5 | 4468.00 | 681.25 | 287 | SC31 | 2468.00 | 681.25 |
| 48 | VCI | -3022.30 | -651.82 | 128 | COM58 | 4217.62 | -662.08 | 208 | SB5 | 4443.00 | 681.25 | 288 | SA32 | 2443.00 | 681.25 |
| 49 | VCI | -2952.30 | -651.82 | 129 | COM57 | 4252.62 | -662.08 | 209 | SC5 | 4418.00 | 681.25 | 289 | SB32 | 2418.00 | 681.25 |
| 50 | VDD | -2799.30 | -651.82 | 130 | COM56 | 4287.62 | -662.08 | 210 | SA6 | 4393.00 | 681.25 | 290 | SC32 | 2393.00 | 681.25 |
| 51 | VDD | -2729.30 | -651.82 | 131 | COM55 | 4322.62 | -662.08 | 211 | SB6 | 4368.00 | 681.25 | 291 | SA33 | 2368.00 | 681.25 |
| 52 | VDD | -2659.30 | -651.82 | 132 | COM54 | 4357.62 | -662.08 | 212 | SC6 | 4343.00 | 681.25 | 292 | SB33 | 2343.00 | 681.25 |
| 53 | VDD | -2589.30 | -651.82 | 133 | COM53 | 4392.62 | -662.08 | 213 | SA7 | 4318.00 | 681.25 | 293 | SC33 | 2318.00 | 681.25 |
| 54 | VDD | -2519.30 | -651.82 | 134 | COM52 | 4427.62 | -662.08 | 214 | SB7 | 4293.00 | 681.25 | 294 | SA34 | 2293.00 | 681.25 |
| 55 | VDDIO | -2366.30 | -651.82 | 135 | COM51 | 4462.62 | -662.08 | 215 | SC7 | 4268.00 | 681.25 | 295 | SB34 | 2268.00 | 681.25 |
| 56 | VDDIO | -2296.30 | -651.82 | 136 | COM50 | 4497.62 | -662.08 | 216 | SA8 | 4243.00 | 681.25 | 296 | SC34 | 2243.00 | 681.25 |
| 57 | VLSS | -2226.30 | -651.82 | 137 | COM49 | 4532.62 | -662.08 | 217 | SB8 | 4218.00 | 681.25 | 297 | SA35 | 2218.00 | 681.25 |
| 58 | GPIO0 | -2134.30 | -651.82 | 138 | COM48 | 4567.62 | -662.08 | 218 | SC8 | 4193.00 | 681.25 | 298 | SB35 | 2193.00 | 681.25 |
| 59 | GPIO1 | -2048.30 | -651.82 | 139 | COM47 | 4602.62 | -662.08 | 219 | SA9 | 4168.00 | 681.25 | 299 | SC35 | 2168.00 | 681.25 |
| 60 | IREF | -1956.30 | -651.82 | 140 | COM46 | 4637.62 | -662.08 | 220 | SB9 | 4143.00 | 681.25 | 300 | SA36 | 2143.00 | 681.25 |
| 61 | FR | -1864.30 | -651.82 | 141 | COM45 | 4672.62 | -662.08 | 221 | SC9 | 4118.00 | 681.25 | 301 | SB36 | 2118.00 | 681.25 |
| 62 | CL | -1778.30 | -651.82 | 142 | COM44 | 4707.62 | -662.08 | 222 | SA10 | 4093.00 | 681.25 | 302 | SC36 | 2093.00 | 681.25 |
| 63 | VSS | -1686.30 | -651.82 | 143 | COM43 | 4742.62 | -662.08 | 223 | SB10 | 4068.00 | 681.25 | 303 | SA37 | 2068.00 | 681.25 |
| 64 | RES# | -1616.30 | -651.82 | 144 | COM42 | 4777.62 | -662.08 | 224 | SC10 | 4043.00 | 681.25 | 304 | SB37 | 2043.00 | 681.25 |
| 65 | D/C# | -1546.30 | -651.82 | 145 | COM41 | 4812.62 | -662.08 | 225 | SA11 | 4018.00 | 681.25 | 305 | SC37 | 2018.00 | 681.25 |
| 66 | CS# | -1476.30 | -651.82 | 146 | COM40 | 4847.62 | -662.08 | 226 | SB11 | 3993.00 | 681.25 | 306 | SA38 | 1993.00 | 681.25 |
| 67 | VSS | -1406.30 | -651.82 | 147 | COM39 | 4882.62 | -662.08 | 227 | SC11 | 3968.00 | 681.25 | 307 | SB38 | 1968.00 | 681.25 |
| 68 | BS1 | -1336.30 | -651.82 | 148 | COM38 | 4917.62 | -662.08 | 228 | SA12 | 3943.00 | 681.25 | 308 | SC38 | 1943.00 | 681.25 |
| 69 | VDDIO | -1266.30 | -651.82 | 149 | COM37 | 4952.62 | -662.08 | 229 | SB12 | 3918.00 | 681.25 | 309 | SA39 | 1918.00 | 681.25 |
| 70 | BS0 | -1196.30 | -651.82 | 150 | COM36 | 4987.62 | -662.08 | 230 | SC12 | 3893.00 | 681.25 | 310 | SB39 | 1893.00 | 681.25 |
| 71 | VSS | -1126.30 | -651.82 | 151 | COM35 | 5022.62 | -662.08 | 231 | SA13 | 3868.00 | 681.25 | 311 | SC39 | 1868.00 | 681.25 |
| 72 | R/W# (WR#) | -1056.30 | -651.82 | 152 | COM34 | 5057.62 | -662.08 | 232 | SB13 | 3843.00 | 681.25 | 312 | SA40 | 1843.00 | 681.25 |
| 73 | E(RD#) | -986.30 | -651.82 | 153 | COM33 | 5092.62 | -662.08 | 233 | SC13 | 3818.00 | 681.25 | 313 | SB40 | 1818.00 | 681.25 |
| 74 | VDDIO | -916.30 | -651.82 | 154 | COM32 | 5127.62 | -662.08 | 234 | SA14 | 3793.00 | 681.25 | 314 | SC40 | 1793.00 | 681.25 |
| 75 | VCI | -763.30 | -651.82 | 155 | COM31 | 5162.62 | -662.08 | 235 | SB14 | 3768.00 | 681.25 | 315 | SA41 | 1768.00 | 681.25 |
| 76 | VDD | -693.30 | -651.82 | 156 | COM30 | 5197.62 | -662.08 | 236 | SC14 | 3743.00 | 681.25 | 316 | SB41 | 1743.00 | 681.25 |
| 77 | VPP | -579.30 | -651.82 | 157 | NC | 5245.12 | -662.08 | 237 | SA15 | 3718.00 | 681.25 | 317 | SC41 | 1718.00 | 681.25 |
| 78 | VPP | - | | | | | | | | | | | | | |

| Pad # | Pad Name | X-Axis | Y-Axis | Pad # | Pad Name | X-Axis | Y-Axis | Pad # | Pad Name | X-Axis | Y-Axis | Pad # | Pad Name | X-Axis | Y-Axis |
|-------|----------|---------|--------|-------|----------|----------|--------|-------|----------|----------|--------|-------|----------|----------|---------|
| 321 | SA43 | 1618.00 | 681.25 | 401 | SC69 | -382.00 | 681.25 | 481 | SA95 | -2393.00 | 681.25 | 561 | SC121 | -4393.00 | 681.25 |
| 322 | SB43 | 1593.00 | 681.25 | 402 | SA70 | -407.00 | 681.25 | 482 | SB95 | -2418.00 | 681.25 | 562 | SA122 | -4418.00 | 681.25 |
| 323 | SC43 | 1568.00 | 681.25 | 403 | SB70 | -432.00 | 681.25 | 483 | SC95 | -2443.00 | 681.25 | 563 | SB122 | -4443.00 | 681.25 |
| 324 | SA44 | 1543.00 | 681.25 | 404 | SC70 | -457.00 | 681.25 | 484 | SA96 | -2468.00 | 681.25 | 564 | SC122 | -4468.00 | 681.25 |
| 325 | SB44 | 1518.00 | 681.25 | 405 | SA71 | -482.00 | 681.25 | 485 | SB96 | -2493.00 | 681.25 | 565 | SA123 | -4493.00 | 681.25 |
| 326 | SC44 | 1493.00 | 681.25 | 406 | SB71 | -507.00 | 681.25 | 486 | SC96 | -2518.00 | 681.25 | 566 | SB123 | -4518.00 | 681.25 |
| 327 | SA45 | 1468.00 | 681.25 | 407 | SC71 | -532.00 | 681.25 | 487 | SA97 | -2543.00 | 681.25 | 567 | SC123 | -4543.00 | 681.25 |
| 328 | SB45 | 1443.00 | 681.25 | 408 | SA72 | -557.00 | 681.25 | 488 | SB97 | -2568.00 | 681.25 | 568 | SA124 | -4568.00 | 681.25 |
| 329 | SC45 | 1418.00 | 681.25 | 409 | SB72 | -582.00 | 681.25 | 489 | SC97 | -2593.00 | 681.25 | 569 | SB124 | -4593.00 | 681.25 |
| 330 | SA46 | 1393.00 | 681.25 | 410 | SC72 | -607.00 | 681.25 | 490 | SA98 | -2618.00 | 681.25 | 570 | SC124 | -4618.00 | 681.25 |
| 331 | SB46 | 1368.00 | 681.25 | 411 | SA73 | -632.00 | 681.25 | 491 | SB98 | -2643.00 | 681.25 | 571 | SA125 | -4643.00 | 681.25 |
| 332 | SC46 | 1343.00 | 681.25 | 412 | SB73 | -657.00 | 681.25 | 492 | SC98 | -2668.00 | 681.25 | 572 | SB125 | -4668.00 | 681.25 |
| 333 | SA47 | 1318.00 | 681.25 | 413 | SC73 | -682.00 | 681.25 | 493 | SA99 | -2693.00 | 681.25 | 573 | SC125 | -4693.00 | 681.25 |
| 334 | SB47 | 1293.00 | 681.25 | 414 | SA74 | -707.00 | 681.25 | 494 | SB99 | -2718.00 | 681.25 | 574 | SA126 | -4718.00 | 681.25 |
| 335 | SC47 | 1268.00 | 681.25 | 415 | SB74 | -732.00 | 681.25 | 495 | SC99 | -2743.00 | 681.25 | 575 | SB126 | -4743.00 | 681.25 |
| 336 | SA48 | 1243.00 | 681.25 | 416 | SC74 | -757.00 | 681.25 | 496 | SA100 | -2768.00 | 681.25 | 576 | SC126 | -4768.00 | 681.25 |
| 337 | SB48 | 1218.00 | 681.25 | 417 | SA75 | -782.00 | 681.25 | 497 | SB100 | -2793.00 | 681.25 | 577 | SA127 | -4793.00 | 681.25 |
| 338 | SC48 | 1193.00 | 681.25 | 418 | SB75 | -807.00 | 681.25 | 498 | SC100 | -2818.00 | 681.25 | 578 | SB127 | -4818.00 | 681.25 |
| 339 | SA49 | 1168.00 | 681.25 | 419 | SC75 | -832.00 | 681.25 | 499 | SA101 | -2843.00 | 681.25 | 579 | SC127 | -4843.00 | 681.25 |
| 340 | SB49 | 1143.00 | 681.25 | 420 | SA76 | -857.00 | 681.25 | 500 | SB101 | -2868.00 | 681.25 | 580 | VLSS | -4890.00 | 681.25 |
| 341 | SC49 | 1118.00 | 681.25 | 421 | SB76 | -882.00 | 681.25 | 501 | SC101 | -2893.00 | 681.25 | 581 | NC | -5234.62 | 692.96 |
| 342 | SA50 | 1093.00 | 681.25 | 422 | SC76 | -907.00 | 681.25 | 502 | SA102 | -2918.00 | 681.25 | 582 | COM64 | -5234.62 | 644.96 |
| 343 | SB50 | 1068.00 | 681.25 | 423 | SA77 | -932.00 | 681.25 | 503 | SB102 | -2943.00 | 681.25 | 583 | COM65 | -5234.62 | 609.96 |
| 344 | SC50 | 1043.00 | 681.25 | 424 | SB77 | -957.00 | 681.25 | 504 | SC102 | -2968.00 | 681.25 | 584 | COM66 | -5234.62 | 574.96 |
| 345 | SA51 | 1018.00 | 681.25 | 425 | SC77 | -982.00 | 681.25 | 505 | SA103 | -2993.00 | 681.25 | 585 | COM67 | -5234.62 | 539.96 |
| 346 | SB51 | 993.00 | 681.25 | 426 | SA78 | -1007.00 | 681.25 | 506 | SB103 | -3018.00 | 681.25 | 586 | COM68 | -5234.62 | 504.96 |
| 347 | SC51 | 968.00 | 681.25 | 427 | SB78 | -1032.00 | 681.25 | 507 | SC103 | -3043.00 | 681.25 | 587 | COM69 | -5234.62 | 469.96 |
| 348 | SA52 | 943.00 | 681.25 | 428 | SC78 | -1057.00 | 681.25 | 508 | SA104 | -3068.00 | 681.25 | 588 | COM70 | -5234.62 | 434.96 |
| 349 | SB52 | 918.00 | 681.25 | 429 | SA79 | -1082.00 | 681.25 | 509 | SB104 | -3093.00 | 681.25 | 589 | COM71 | -5234.62 | 399.96 |
| 350 | SC52 | 893.00 | 681.25 | 430 | SB79 | -1107.00 | 681.25 | 510 | SC104 | -3118.00 | 681.25 | 590 | COM72 | -5234.62 | 364.96 |
| 351 | SA53 | 868.00 | 681.25 | 431 | SC79 | -1132.00 | 681.25 | 511 | SA105 | -3143.00 | 681.25 | 591 | COM73 | -5234.62 | 329.96 |
| 352 | SB53 | 843.00 | 681.25 | 432 | VCC | -1158.00 | 681.25 | 512 | SB105 | -3168.00 | 681.25 | 592 | COM74 | -5234.62 | 294.96 |
| 353 | SC53 | 818.00 | 681.25 | 433 | VCC | -1186.00 | 681.25 | 513 | SC105 | -3193.00 | 681.25 | 593 | COM75 | -5234.62 | 259.96 |
| 354 | SA54 | 793.00 | 681.25 | 434 | VCC | -1214.00 | 681.25 | 514 | SA106 | -3218.00 | 681.25 | 594 | COM76 | -5234.62 | 224.96 |
| 355 | SB54 | 768.00 | 681.25 | 435 | VCC | -1242.00 | 681.25 | 515 | SB106 | -3243.00 | 681.25 | 595 | COM77 | -5234.62 | 189.96 |
| 356 | SC54 | 743.00 | 681.25 | 436 | SA80 | -1268.00 | 681.25 | 516 | SC106 | -3268.00 | 681.25 | 596 | COM78 | -5234.62 | 154.96 |
| 357 | SA55 | 718.00 | 681.25 | 437 | SB80 | -1293.00 | 681.25 | 517 | SA107 | -3293.00 | 681.25 | 597 | COM79 | -5234.62 | 119.96 |
| 358 | SB55 | 693.00 | 681.25 | 438 | SC80 | -1318.00 | 681.25 | 518 | SB107 | -3318.00 | 681.25 | 598 | COM80 | -5234.62 | 84.96 |
| 359 | SC55 | 668.00 | 681.25 | 439 | SA81 | -1343.00 | 681.25 | 519 | SC107 | -3343.00 | 681.25 | 599 | COM81 | -5234.62 | 49.96 |
| 360 | SA56 | 643.00 | 681.25 | 440 | SB81 | -1368.00 | 681.25 | 520 | SA108 | -3368.00 | 681.25 | 600 | COM82 | -5234.62 | 14.96 |
| 361 | SB56 | 618.00 | 681.25 | 441 | SC81 | -1393.00 | 681.25 | 521 | SB108 | -3393.00 | 681.25 | 601 | COM83 | -5234.62 | -20.04 |
| 362 | SC56 | 593.00 | 681.25 | 442 | SA82 | -1418.00 | 681.25 | 522 | SC108 | -3418.00 | 681.25 | 602 | COM84 | -5234.62 | -55.04 |
| 363 | SA57 | 568.00 | 681.25 | 443 | SB82 | -1443.00 | 681.25 | 523 | SA109 | -3443.00 | 681.25 | 603 | COM85 | -5234.62 | -90.04 |
| 364 | SB57 | 543.00 | 681.25 | 444 | SC82 | -1468.00 | 681.25 | 524 | SB109 | -3468.00 | 681.25 | 604 | COM86 | -5234.62 | -125.04 |
| 365 | SC57 | 518.00 | 681.25 | 445 | SA83 | -1493.00 | 681.25 | 525 | SC109 | -3493.00 | 681.25 | 605 | COM87 | -5234.62 | -160.04 |
| 366 | SA58 | 493.00 | 681.25 | 446 | SB83 | -1518.00 | 681.25 | 526 | SA110 | -3518.00 | 681.25 | 606 | COM88 | -5234.62 | -195.04 |
| 367 | SB58 | 468.00 | 681.25 | 447 | SC83 | -1543.00 | 681.25 | 527 | SB110 | -3543.00 | 681.25 | 607 | COM89 | -5234.62 | -230.04 |
| 368 | SC58 | 443.00 | 681.25 | 448 | SA84 | -1568.00 | 681.25 | 528 | SC110 | -3568.00 | 681.25 | 608 | COM90 | -5234.62 | -265.04 |
| 369 | SA59 | 418.00 | 681.25 | 449 | SB84 | -1593.00 | 681.25 | 529 | SA111 | -3593.00 | 681.25 | 609 | COM91 | -5234.62 | -300.04 |
| 370 | SB59 | 393.00 | 681.25 | 450 | SC84 | -1618.00 | 681.25 | 530 | SB111 | -3618.00 | 681.25 | 610 | COM92 | -5234.62 | -335.04 |
| 371 | SC59 | 368.00 | 681.25 | 451 | SA85 | -1643.00 | 681.25 | 531 | SC111 | -3643.00 | 681.25 | 611 | COM93 | -5234.62 | -370.04 |
| 372 | SA60 | 343.00 | 681.25 | 452 | SB85 | -1668.00 | 681.25 | 532 | SA112 | -3668.00 | 681.25 | 612 | VLSS | -5234.62 | -405.04 |
| 373 | SB60 | 318.00 | 681.25 | 453 | SC85 | -1693.00 | 681.25 | 533 | SB112 | -3693.00 | 681.25 | 613 | VLSS | -5234.62 | -440.04 |
| 374 | SC60 | 293.00 | 681.25 | 454 | SA86 | -1718.00 | 681.25 | 534 | SC112 | -3718.00 | 681.25 | | | | |
| 375 | SA61 | 268.00 | 681.25 | 455 | SB86 | -1743.00 | 681.25 | 535 | SA113 | -3743.00 | 681.25 | | | | |
| 376 | SB61 | 243.00 | 681.25 | 456 | SC86 | -1768.00 | 681.25 | 536 | SB113 | -3768.00 | 681.25 | | | | |
| 377 | SC61 | 218.00 | 681.25 | 457 | SA87 | -1793.00 | 681.25 | 537 | SC113 | -3793.00 | 681.25 | | | | |
| 378 | SA62 | 193.00 | 681.25 | 458 | SB87 | -1818.00 | 681.25 | 538 | SA114 | -3818.00 | 681.25 | | | | |
| 379 | SB62 | 168.00 | 681.25 | 459 | SC87 | -1843.00 | 681.25 | 539 | SB114 | -3843.00 | 681.25 | | | | |
| 380 | SC62 | 143.00 | 681.25 | 460 | SA88 | -1868.00 | 681.25 | 540 | SC114 | -3868.00 | 681.25 | | | | |
| 381 | SA63 | 118.00 | 681.25 | 461 | SB88 | -1893.00 | 681.25 | 541 | SA115 | -3893.00 | 681.25 | | | | |
| 382 | SB63 | 93.00 | 681.25 | 462 | SC88 | -1918.00 | 681.25 | 542 | SB115 | -3918.00 | 681.25 | | | | |
| 383 | SC63 | 68.00 | 681.25 | 463 | SA89 | -1943.00 | 681.25 | 543 | SC115 | -3943.00 | 681.25 | | | | |
| 384 | SA64 | 43.00 | 681.25 | 464 | SB89 | -1968.00 | 681.25 | 544 | SA116 | -3968.00 | 681.25 | | | | |
| 385 | SB64 | 18.00 | 681.25 | 465 | SC89 | -1993.00 | 681.25 | 545 | SB116 | -3993.00 | 681.25 | | | | |
| 386 | SC64 | -7.00 | 681.25 | 466 | SA90 | -2018.00 | 681.25 | 546 | SC116 | -4018.00 | 681.25 | | | | |
| 387 | SA65 | -32.00 | 681.25 | 467 | SB90 | -2043.00 | 681.25 | 547 | SA117 | -4043.00 | 681.25 | | | | |
| 388 | SB65 | -57.00 | 681.25 | 468 | SC90 | -2068.00 | 681.25 | 548 | SB117 | -4068.00 | 681.25 | | | | |
| 389 | SC65 | -82.00 | 681.25 | 469 | SA91 | -2093.00 | 681.25 | 549 | SC117 | -4093.00 | 681.25 | | | | |
| 390 | SA66 | -107.00 | 681.25 | 470 | SB91 | -2118.00 | 681.25 | 550 | SA118 | -4118.00 | 681.25 | | | | |
| 391 | SB66 | -132.00 | 681.25 | 471 | SC91 | -2143.00 | 681.25 | 551 | SB118 | -4143.00 | 681.25 | | | | |
| 392 | SC66 | -157.00 | 681.25 | 472 | SA92 | -2168.00 | 681.25 | 552 | SC118 | -4168.00 | 681.25 | | | | |
| 393 | SA67 | -182.00 | 681.25 | 473 | SB92 | -2193.00 | 681.25 | 553 | SA119 | -4193.00 | 681.25 | | | | |
| 394 | SB67 | -207.00 | 681.25 | 474 | SC92 | -2218.00 | 681.25 | 554 | SB119 | -4218.00 | 681.25 | | | | |
| 395 | SC67 | -232.00 | 681.25 | 475 | SA93 | -2243.00 | 681.25 | 555 | SC119 | -4243.00 | 681.25 | | | | |
| 396 | SA68 | -257.00 | 681.25 | 476 | SB93 | -2268.00 | 681.25 | 556 | SA120 | -4268.00 | 681.25 | | | | |
| 397 | SB68 | -282.00 | 681.25 | 477 | SC93 | -2293.00 | 681.25 | 557 | SB120 | -4293.00 | 681.25 | | | | |
| 398 | SC68 | -307.00 | 681.25 | 478 | SA94 | -2318.00 | 681.25 | 558 | SC120 | -4318.00 | 681.25 | | | | |
| 399 | SA69 | -332.00 | 681.25 | 479 | SB94 | -2343.00 | 681.25 | 559 | SA121 | -4343.00 | 681.25 | | | | |
| 400 | SB69 | -357.00 | 681.25 | 480 | SC94 | -2368.00 | 681.25 | 560 | SB121 | -4368.00 | 681.25 | | | | |

6 PIN ARRANGEMENT

6.1 SSD1351UR1 pin assignment

Figure 6-1: SSD1351UR1 Pin Assignment

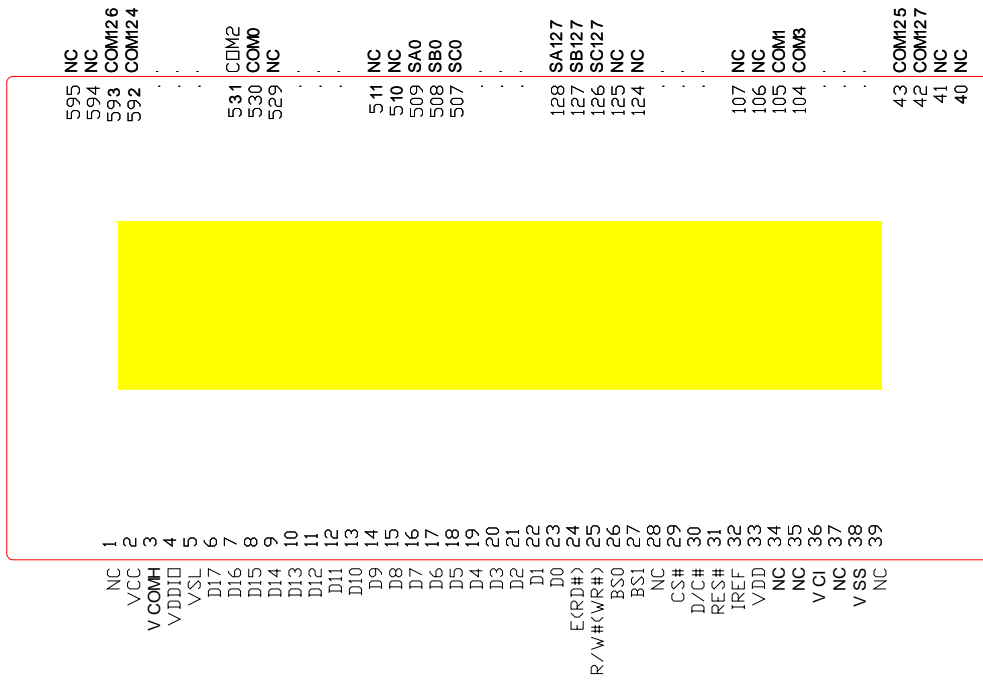


Table 6-1: SSD1351UR1 Pin Assignment Table

| Pad# | Pad Name | Pad# | Pad Name | Pad# | Pad Name | Pad# | Pad Name |
|------|------------|------|----------|------|----------|------|----------|
| 1 | NC | 81 | COM88 | 161 | SA116 | 241 | SB89 |
| 2 | VCC | 82 | COM87 | 162 | SC115 | 242 | SA89 |
| 3 | VCOMH | 83 | COM86 | 163 | SB115 | 243 | SC88 |
| 4 | VDDIO | 84 | COM85 | 164 | SA115 | 244 | SB88 |
| 5 | VSL | 85 | COM84 | 165 | SC114 | 245 | SA88 |
| 6 | D17 | 86 | COM83 | 166 | SB114 | 246 | SC87 |
| 7 | D16 | 87 | COM82 | 167 | SA114 | 247 | SB87 |
| 8 | D15 | 88 | COM81 | 168 | SC113 | 248 | SA87 |
| 9 | D14 | 89 | COM80 | 169 | SB113 | 249 | SC86 |
| 10 | D13 | 90 | COM79 | 170 | SA113 | 250 | SB86 |
| 11 | D12 | 91 | COM78 | 171 | SC112 | 251 | SA86 |
| 12 | D11 | 92 | COM77 | 172 | SB112 | 252 | SC85 |
| 13 | D10 | 93 | COM76 | 173 | SA112 | 253 | SB85 |
| 14 | D9 | 94 | COM75 | 174 | SC111 | 254 | SA85 |
| 15 | D8 | 95 | COM74 | 175 | SB111 | 255 | SC84 |
| 16 | D7 | 96 | COM73 | 176 | SA111 | 256 | SB84 |
| 17 | D6 | 97 | COM72 | 177 | SC110 | 257 | SA84 |
| 18 | D5 | 98 | COM71 | 178 | SB110 | 258 | SC83 |
| 19 | D4 | 99 | COM70 | 179 | SA110 | 259 | SB83 |
| 20 | D3 | 100 | COM69 | 180 | SC109 | 260 | SA83 |
| 21 | D2 | 101 | COM68 | 181 | SB109 | 261 | SC82 |
| 22 | D1 | 102 | COM67 | 182 | SA109 | 262 | SB82 |
| 23 | D0 | 103 | COM66 | 183 | SC108 | 263 | SA82 |
| 24 | E (RD#) | 104 | COM65 | 184 | SB108 | 264 | SC81 |
| 25 | R/W# (WR#) | 105 | COM64 | 185 | SA108 | 265 | SB81 |
| 26 | BS0 | 106 | NC | 186 | SC107 | 266 | SA81 |
| 27 | BS1 | 107 | NC | 187 | SB107 | 267 | SC80 |
| 28 | NC | 108 | NC | 188 | SA107 | 268 | SB80 |
| 29 | CS# | 109 | NC | 189 | SC106 | 269 | SA80 |
| 30 | D/C# | 110 | NC | 190 | SB106 | 270 | SC79 |
| 31 | RES# | 111 | NC | 191 | SA106 | 271 | SB79 |
| 32 | IREF | 112 | NC | 192 | SC105 | 272 | SA79 |
| 33 | VDD | 113 | NC | 193 | SB105 | 273 | SC78 |
| 34 | NC | 114 | NC | 194 | SA105 | 274 | SB78 |
| 35 | NC | 115 | NC | 195 | SC104 | 275 | SA78 |
| 36 | VCI | 116 | NC | 196 | SB104 | 276 | SC77 |
| 37 | NC | 117 | NC | 197 | SA104 | 277 | SB77 |
| 38 | VSS | 118 | NC | 198 | SC103 | 278 | SA77 |
| 39 | NC | 119 | NC | 199 | SB103 | 279 | SC76 |
| 40 | NC | 120 | NC | 200 | SA103 | 280 | SB76 |
| 41 | NC | 121 | NC | 201 | SC102 | 281 | SA76 |
| 42 | COM127 | 122 | NC | 202 | SB102 | 282 | SC75 |
| 43 | COM126 | 123 | NC | 203 | SA102 | 283 | SB75 |
| 44 | COM125 | 124 | NC | 204 | SC101 | 284 | SA75 |
| 45 | COM124 | 125 | NC | 205 | SB101 | 285 | SC74 |
| 46 | COM123 | 126 | SC127 | 206 | SA101 | 286 | SB74 |
| 47 | COM122 | 127 | SB127 | 207 | SC100 | 287 | SA74 |
| 48 | COM121 | 128 | SA127 | 208 | SB100 | 288 | SC73 |
| 49 | COM120 | 129 | SC126 | 209 | SA100 | 289 | SB73 |
| 50 | COM119 | 130 | SB126 | 210 | SC99 | 290 | SA73 |
| 51 | COM118 | 131 | SA126 | 211 | SB99 | 291 | SC72 |
| 52 | COM117 | 132 | SC125 | 212 | SA99 | 292 | SB72 |
| 53 | COM116 | 133 | SB125 | 213 | SC98 | 293 | SA72 |
| 54 | COM115 | 134 | SA125 | 214 | SB98 | 294 | SC71 |
| 55 | COM114 | 135 | SC124 | 215 | SA98 | 295 | SB71 |
| 56 | COM113 | 136 | SB124 | 216 | SC97 | 296 | SA71 |
| 57 | COM112 | 137 | SA124 | 217 | SB97 | 297 | SC70 |
| 58 | COM111 | 138 | SC123 | 218 | SA97 | 298 | SB70 |
| 59 | COM110 | 139 | SB123 | 219 | SC96 | 299 | SA70 |
| 60 | COM109 | 140 | SA123 | 220 | SB96 | 300 | SC69 |
| 61 | COM108 | 141 | SC122 | 221 | SA96 | 301 | SB69 |
| 62 | COM107 | 142 | SB122 | 222 | SC95 | 302 | SA69 |
| 63 | COM106 | 143 | SA122 | 223 | SB95 | 303 | SC68 |
| 64 | COM105 | 144 | SC121 | 224 | SA95 | 304 | SB68 |
| 65 | COM104 | 145 | SB121 | 225 | SC94 | 305 | SA68 |
| 66 | COM103 | 146 | SA121 | 226 | SB94 | 306 | SC67 |
| 67 | COM102 | 147 | SC120 | 227 | SA94 | 307 | SB67 |
| 68 | COM101 | 148 | SB120 | 228 | SC93 | 308 | SA67 |
| 69 | COM100 | 149 | SA120 | 229 | SB93 | 309 | SC66 |
| 70 | COM99 | 150 | SC119 | 230 | SA93 | 310 | SB66 |
| 71 | COM98 | 151 | SB119 | 231 | SC92 | 311 | SA66 |
| 72 | COM97 | 152 | SA119 | 232 | SB92 | 312 | SC65 |
| 73 | COM96 | 153 | SC118 | 233 | SA92 | 313 | SB65 |
| 74 | COM95 | 154 | SB118 | 234 | SC91 | 314 | SA65 |
| 75 | COM94 | 155 | SA118 | 235 | SB91 | 315 | SC64 |
| 76 | COM93 | 156 | SC117 | 236 | SA91 | 316 | SB64 |
| 77 | COM92 | 157 | SB117 | 237 | SC90 | 317 | SA64 |
| 78 | COM91 | 158 | SA117 | 238 | SB90 | 318 | SC63 |
| 79 | COM90 | 159 | SC116 | 239 | SA90 | 319 | SB63 |
| 80 | COM89 | 160 | SB116 | 240 | SC89 | 320 | SA63 |

| Pad# | Pad Name |
|------|----------|
| 321 | SC62 |
| 322 | SB62 |
| 323 | SA62 |
| 324 | SC61 |
| 325 | SB61 |
| 326 | SA61 |
| 327 | SC60 |
| 328 | SB60 |
| 329 | SA60 |
| 330 | SC59 |
| 331 | SB59 |
| 332 | SA59 |
| 333 | SC58 |
| 334 | SB58 |
| 335 | SA58 |
| 336 | SC57 |
| 337 | SB57 |
| 338 | SA57 |
| 339 | SC56 |
| 340 | SB56 |
| 341 | SA56 |
| 342 | SC55 |
| 343 | SB55 |
| 344 | SA55 |
| 345 | SC54 |
| 346 | SB54 |
| 347 | SA54 |
| 348 | SC53 |
| 349 | SB53 |
| 350 | SA53 |
| 351 | SC52 |
| 352 | SB52 |
| 353 | SA52 |
| 354 | SC51 |
| 355 | SB51 |
| 356 | SA51 |
| 357 | SC50 |
| 358 | SB50 |
| 359 | SA50 |
| 360 | SC49 |
| 361 | SB49 |
| 362 | SA49 |
| 363 | SC48 |
| 364 | SB48 |
| 365 | SA48 |
| 366 | SC47 |
| 367 | SB47 |
| 368 | SA47 |
| 369 | SC46 |
| 370 | SB46 |
| 371 | SA46 |
| 372 | SC45 |
| 373 | SB45 |
| 374 | SA45 |
| 375 | SC44 |
| 376 | SB44 |
| 377 | SA44 |
| 378 | SC43 |
| 379 | SB43 |
| 380 | SA43 |
| 381 | SC42 |
| 382 | SB42 |
| 383 | SA42 |
| 384 | SC41 |
| 385 | SB41 |
| 386 | SA41 |
| 387 | SC40 |
| 388 | SB40 |
| 389 | SA40 |
| 390 | SC39 |
| 391 | SB39 |
| 392 | SA39 |
| 393 | SC38 |
| 394 | SB38 |
| 395 | SA38 |
| 396 | SC37 |
| 397 | SB37 |
| 398 | SA37 |
| 399 | SC36 |
| 400 | SB36 |

| Pad# | Pad Name |
|------|----------|
| 401 | SA36 |
| 402 | SC35 |
| 403 | SB35 |
| 404 | SA35 |
| 405 | SC34 |
| 406 | SB34 |
| 407 | SA34 |
| 408 | SC33 |
| 409 | SB33 |
| 410 | SA33 |
| 411 | SC32 |
| 412 | SB32 |
| 413 | SA32 |
| 414 | SC31 |
| 415 | SB31 |
| 416 | SA31 |
| 417 | SC30 |
| 418 | SB30 |
| 419 | SA30 |
| 420 | SC29 |
| 421 | SB29 |
| 422 | SA29 |
| 423 | SC28 |
| 424 | SB28 |
| 425 | SA28 |
| 426 | SC27 |
| 427 | SB27 |
| 428 | SA27 |
| 429 | SC26 |
| 430 | SB26 |
| 431 | SA26 |
| 432 | SC25 |
| 433 | SB25 |
| 434 | SA25 |
| 435 | SC24 |
| 436 | SB24 |
| 437 | SA24 |
| 438 | SC23 |
| 439 | SB23 |
| 440 | SA23 |
| 441 | SC22 |
| 442 | SB22 |
| 443 | SA22 |
| 444 | SC21 |
| 445 | SB21 |
| 446 | SA21 |
| 447 | SC20 |
| 448 | SB20 |
| 449 | SA20 |
| 450 | SC19 |
| 451 | SB19 |
| 452 | SA19 |
| 453 | SC18 |
| 454 | SB18 |
| 455 | SA18 |
| 456 | SC17 |
| 457 | SB17 |
| 458 | SA17 |
| 459 | SC16 |
| 460 | SB16 |
| 461 | SA16 |
| 462 | SC15 |
| 463 | SB15 |
| 464 | SA15 |
| 465 | SC14 |
| 466 | SB14 |
| 467 | SA14 |
| 468 | SC13 |
| 469 | SB13 |
| 470 | SA13 |
| 471 | SC12 |
| 472 | SB12 |
| 473 | SA12 |
| 474 | SC11 |
| 475 | SB11 |
| 476 | SA11 |
| 477 | SC10 |
| 478 | SB10 |
| 479 | SA10 |
| 480 | SC9 |

| Pad# | Pad Name |
|------|----------|
| 481 | SB9 |
| 482 | SA9 |
| 483 | SC8 |
| 484 | SB8 |
| 485 | SA8 |
| 486 | SC7 |
| 487 | SB7 |
| 488 | SA7 |
| 489 | SC6 |
| 490 | SB6 |
| 491 | SA6 |
| 492 | SC5 |
| 493 | SB5 |
| 494 | SA5 |
| 495 | SC4 |
| 496 | SB4 |
| 497 | SA4 |
| 498 | SC3 |
| 499 | SB3 |
| 500 | SA3 |
| 501 | SC2 |
| 502 | SB2 |
| 503 | SA2 |
| 504 | SC1 |
| 505 | SB1 |
| 506 | SA1 |
| 507 | SC0 |
| 508 | SB0 |
| 509 | SA0 |
| 510 | NC |
| 511 | NC |
| 512 | NC |
| 513 | NC |
| 514 | NC |
| 515 | NC |
| 516 | NC |
| 517 | NC |
| 518 | NC |
| 519 | NC |
| 520 | NC |
| 521 | NC |
| 522 | NC |
| 523 | NC |
| 524 | NC |
| 525 | NC |
| 526 | NC |
| 527 | NC |
| 528 | NC |
| 529 | NC |
| 530 | COM0 |
| 531 | COM1 |
| 532 | COM2 |
| 533 | COM3 |
| 534 | COM4 |
| 535 | COM5 |
| 536 | COM6 |
| 537 | COM7 |
| 538 | COM8 |
| 539 | COM9 |
| 540 | COM10 |
| 541 | COM11 |
| 542 | COM12 |
| 543 | COM13 |
| 544 | COM14 |
| 545 | COM15 |
| 546 | COM16 |
| 547 | COM17 |
| 548 | COM18 |
| 549 | COM19 |
| 550 | COM20 |
| 551 | COM21 |
| 552 | COM22 |
| 553 | COM23 |
| 554 | COM24 |
| 555 | COM25 |
| 556 | COM26 |
| 557 | COM27 |
| 558 | COM28 |
| 559 | COM29 |
| 560 | COM30 |

| Pad# | Pad Name |
|------|----------|
| 561 | COM31 |
| 562 | COM32 |
| 563 | COM33 |
| 564 | COM34 |
| 565 | COM35 |
| 566 | COM36 |
| 567 | COM37 |
| 568 | COM38 |
| 569 | COM39 |
| 570 | COM40 |
| 571 | COM41 |
| 572 | COM42 |
| 573 | COM43 |
| 574 | COM44 |
| 575 | COM45 |
| 576 | COM46 |
| 577 | COM47 |
| 578 | COM48 |
| 579 | COM49 |
| 580 | COM50 |
| 581 | COM51 |
| 582 | COM52 |
| 583 | COM53 |
| 584 | COM54 |
| 585 | COM55 |
| 586 | COM56 |
| 587 | COM57 |
| 588 | COM58 |
| 589 | COM59 |
| 590 | COM60 |
| 591 | COM61 |
| 592 | COM62 |
| 593 | COM63 |
| 594 | NC |
| 595 | NC |

7 PIN DESCRIPTIONS

Key:

| | |
|-------------------------------------|----------------------------------|
| I = Input | NC = Not Connected |
| O =Output | Pull LOW= connect to Ground |
| I/O = Bi-directional (input/output) | Pull HIGH= connect to V_{DDIO} |
| P = Power pin | |

Table 7-1 : SSD1351 Pin Description

| Pin Name | Pin Type | Description |
|------------|----------|---|
| V_{DD} | P | Power supply pin for core logic operation. V_{DD} can be supplied externally (within the range of 2.4V to 2.6V) or regulated internally from V_{CI} . A capacitor should be connected between V_{DD} and V_{SS} under all circumstances. Refer to Section 8.10 for details. |
| V_{DDIO} | P | Power supply for interface logic level. It should match with the MCU interface voltage level and must be connected to external source. |
| V_{CI} | P | Low voltage power supply V_{CI} must always be equal to or higher than V_{DD} and V_{DDIO} . Refer to Section 8.10 for details. |
| V_{CC} | P | Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source. |
| V_{PP} | P | Reserved pin. It must be connected to V_{DD} . |
| V_{SS} | P | Ground pin |
| V_{LSS} | P | Analog system ground pin |
| V_{COMH} | P | COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS} . |
| BGGND | P | It should be connected to Ground. |
| GPIO0 | I/O | Detail refer to Command B5h |
| GPIO1 | I/O | Detail refer to Command B5h |
| VSL | P | This is segment voltage reference pin. External VSL is set as default. This pin has to connect with resistor and diode to ground. (details depend on application) Refer to Command B4h for details. |

| Pin Name | Pin Type | Description | | | | | | | | | | | | | | | | | | |
|------------------|----------------------|--|---------|-----------|------|------------|------|------------|------|---------------------|------|---------------------|------|----------------------|------|----------------------|------|----------------------|------|----------------------|
| BS[1:0] | I | <p>MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS3 and BS2 are command programmable (by command ABh). [reset = 00]. BS1 and BS0 are pin select.</p> <p style="text-align: center;">Table 7-2 : Bus Interface selection</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BS[3:0]</th> <th>Interface</th> </tr> </thead> <tbody> <tr> <td>XX00</td> <td>4 line SPI</td> </tr> <tr> <td>XX01</td> <td>3 line SPI</td> </tr> <tr> <td>0011</td> <td>8-bit 6800 parallel</td> </tr> <tr> <td>0010</td> <td>8-bit 8080 parallel</td> </tr> <tr> <td>0111</td> <td>16-bit 6800 parallel</td> </tr> <tr> <td>0110</td> <td>16-bit 8080 parallel</td> </tr> <tr> <td>1111</td> <td>18-bit 6800 parallel</td> </tr> <tr> <td>1110</td> <td>18-bit 8080 parallel</td> </tr> </tbody> </table> <p>Note ⁽¹⁾ 0 is connected to V_{SS} ⁽²⁾ 1 is connected to V_{DDIO}</p> | BS[3:0] | Interface | XX00 | 4 line SPI | XX01 | 3 line SPI | 0011 | 8-bit 6800 parallel | 0010 | 8-bit 8080 parallel | 0111 | 16-bit 6800 parallel | 0110 | 16-bit 8080 parallel | 1111 | 18-bit 6800 parallel | 1110 | 18-bit 8080 parallel |
| BS[3:0] | Interface | | | | | | | | | | | | | | | | | | | |
| XX00 | 4 line SPI | | | | | | | | | | | | | | | | | | | |
| XX01 | 3 line SPI | | | | | | | | | | | | | | | | | | | |
| 0011 | 8-bit 6800 parallel | | | | | | | | | | | | | | | | | | | |
| 0010 | 8-bit 8080 parallel | | | | | | | | | | | | | | | | | | | |
| 0111 | 16-bit 6800 parallel | | | | | | | | | | | | | | | | | | | |
| 0110 | 16-bit 8080 parallel | | | | | | | | | | | | | | | | | | | |
| 1111 | 18-bit 6800 parallel | | | | | | | | | | | | | | | | | | | |
| 1110 | 18-bit 8080 parallel | | | | | | | | | | | | | | | | | | | |
| I _{REF} | I | This pin is the segment output current reference pin. A resistor should be connected between this pin and V _{SS} . | | | | | | | | | | | | | | | | | | |
| CL | I | <p>External clock input pin.</p> <p>When internal clock is enable (i.e. pull HIGH in CLS pin), this pin is not used and should be connected to Ground.</p> <p>When internal clock is disable (i.e. pull LOW in CLS pin), this pin is the external clock source input pin.</p> | | | | | | | | | | | | | | | | | | |
| CLS | I | <p>Internal clock selection pin.</p> <p>When this pin is pulled HIGH, internal oscillator is enabled (normal operation). When this pin is pulled LOW, an external clock signal should be connected to CL.</p> | | | | | | | | | | | | | | | | | | |
| CS# | I | <p>This pin is the chip select input connecting to the MCU.</p> <p>The chip is enabled for MCU communication only when CS# is pulled LOW.</p> | | | | | | | | | | | | | | | | | | |
| RES# | I | <p>This pin is reset signal input.</p> <p>When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.</p> | | | | | | | | | | | | | | | | | | |
| D/C# | I | <p>This pin is Data/Command control pin connecting to the MCU.</p> <p>When the pin is pulled HIGH, the data at D[17:0] will be interpreted as data. When the pin is pulled LOW, the data at D[17:0] will be interpreted as command.</p> | | | | | | | | | | | | | | | | | | |
| R/W# (WR#) | I | <p>This pin is read / write control input pin connecting to the MCU interface.</p> <p>When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.</p> <p>When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.</p> <p>When serial interface is selected, this pin R/W (WR#) must be connected to V_{SS}.</p> | | | | | | | | | | | | | | | | | | |

| Pin Name | Pin Type | Description |
|-------------------------------------|----------|--|
| E (RD#) | I | <p>This pin is MCU interface input.</p> <p>When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.</p> <p>When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.</p> <p>When serial interface is selected, this pin E(RD#) must be connected to V_{SS}.</p> |
| D[17:0] | I/O | <p>These pins are bi-directional data bus connecting to the MCU data bus.</p> <p>Unused pins are recommended to tie LOW. (Except for D2 pin in SPI mode)</p> |
| FR | O | This pin is reserved pin. No connection is necessary and should be left open individually. |
| TR[4:0] | O | These are reserved pins. No connection is necessary and should be left open individually. |
| V _{SS1} | P | This pin is reserved pin. It should be connected to V _{SS} . |
| V _{CH1} | P | This pin is reserved pin. No connection is necessary and should be left open individually. |
| SA[127:0] SB[127:0] SC[127:0] | O | <p>These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF.</p> <p>The 384 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.</p> |
| COM[127:0] | I/O | These pins provide the Common switch signals to the OLED panel. |

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface

SSD1351 MCU interface consist of 18 data pin and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[1:0] pins and software command on BS[3:0].(refer to Table 7-2 for BS[3:0] setting)

Table 8-1 : MCU interface assignment under different bus interface mode

| Pin Name Bus Interface | Data / Command Interface | | | | | | | | | | | | | | Control Signal | | | | | | | |
|---------------------------|--------------------------|---------|-----|-----|-----|-----|-----|-----|----|----|--------|----|----|----|----------------|------|---------|------|------|---------|------|------|
| | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | E | R/W# | CS# | D/C# |
| 8b / 8080 | Tie Low | | | | | | | | | | D[7:0] | | | | RD# | WR# | CS# | D/C# | RES# | | | |
| 8b / 6800 | Tie Low | | | | | | | | | | D[7:0] | | | | E | R/W# | CS# | D/C# | RES# | | | |
| 16b / 8080 | Tie Low | D[15:0] | | | | | | | | | | | | | RD# | WR# | CS# | D/C# | RES# | | | |
| 16b / 6800 | Tie Low | D[15:0] | | | | | | | | | | | | | E | R/W# | CS# | D/C# | RES# | | | |
| 18b / 8080 | D[17:0] | | | | | | | | | | | | | | | | | RD# | WR# | CS# | D/C# | RES# |
| 18b / 6800 | D[17:0] | | | | | | | | | | | | | | | | | E | R/W# | CS# | D/C# | RES# |
| SPI 4-wire | Tie Low | | | | | | | | | | | | | NC | SDIN | SCLK | Tie Low | | CS# | D/C# | RES# | |
| SPI 3-Wire | Tie Low | | | | | | | | | | | | | NC | SDIN | SCLK | Tie Low | | CS# | Tie Low | RES# | |

Table 8-2 : Data bus selection modes

| | 6800 – series Parallel Interface | 8080 – series Parallel Interface | 3-wire Serial Interface or 4-wire Serial Interface |
|---------------|----------------------------------|----------------------------------|--|
| Data Read | 18-/16-/8-bits | 18-/16-/8-bits | No |
| Data Write | 18-/16-/8-bits | 18-/16-/8-bits | 8-bits |
| Command Read | Yes. Refer to section 9 | Yes. Refer to section 9 | No |
| Command Write | Yes | Yes | Yes |

8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 18 bi-directional data pins (D[17:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

Table 8-3 : Control pins of 6800 interface

| Function | E | R/W# | CS# | D/C# |
|---------------|---|------|-----|------|
| Write command | ↓ | L | L | L |
| Read status | ↓ | H | L | L |
| Write data | ↓ | L | L | H |
| Read data | ↓ | H | L | H |

Note

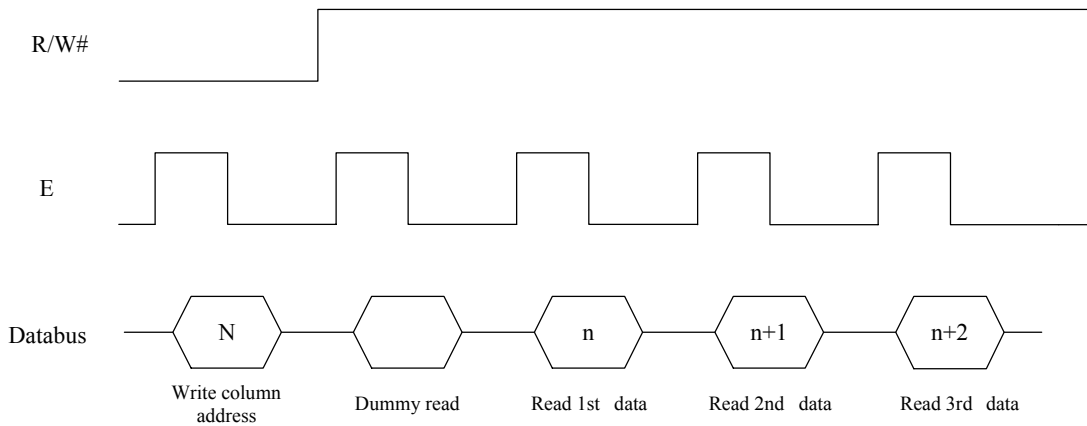
(1) ↓ stands for falling edge of signal

(2) H stands for HIGH in signal

(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 18 bi-directional data pins (D[17:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.

A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

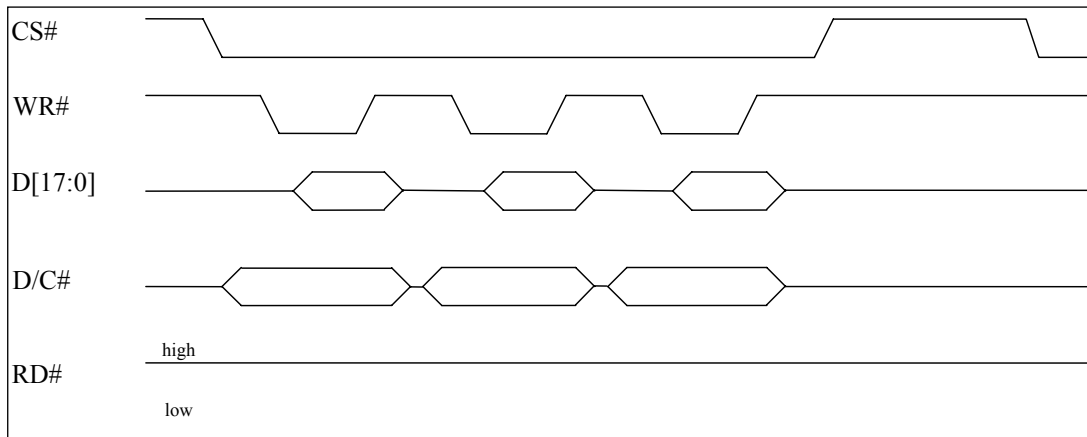


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

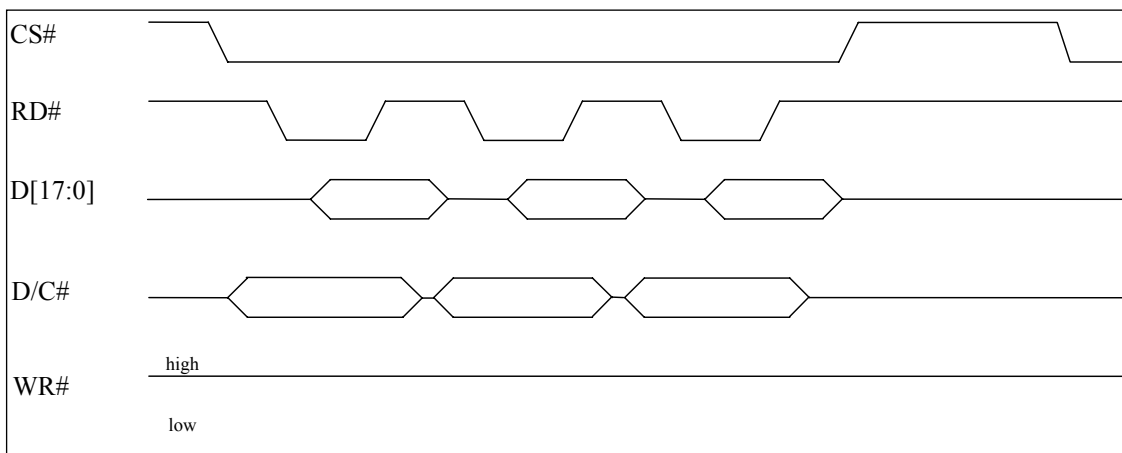


Table 8-4 : Control pins of 8080 interface

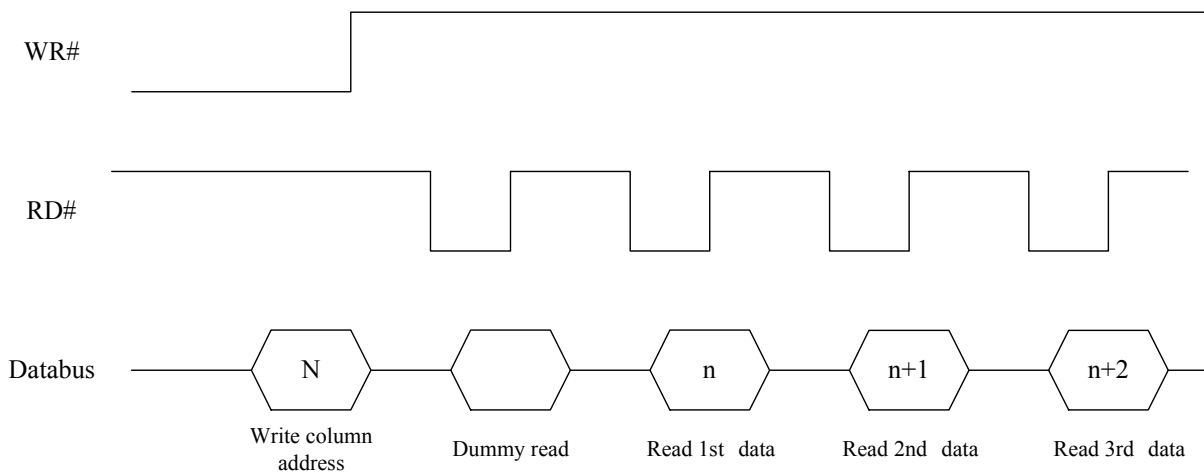
| Function | RD# | WR# | CS# | D/C# |
|---------------|-----|-----|-----|------|
| Write command | H | ↑ | L | L |
| Read status | ↑ | H | L | L |
| Write data | H | ↑ | L | H |
| Read data | ↑ | H | L | H |

Note

- (1) ↑ stands for rising edge of signal
- (2) H stands for HIGH in signal
- (3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4 : Display data read back procedure - insertion of dummy read



8.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D17 and E can be connected to an external ground.

Table 8-5 : Control pins of 4-wire Serial interface

| Function | E | CS# | D/C# |
|---------------|---------|-----|------|
| Write command | Tie LOW | L | L |
| Write data | Tie LOW | L | H |

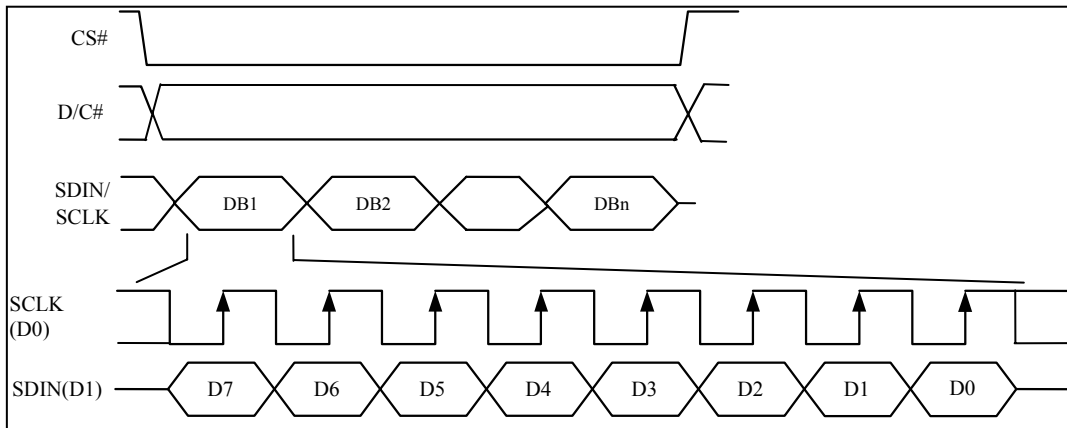
Note

- (1) H stands for HIGH in signal
- (2) L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in 4-wire Serial interface mode



8.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D17, R/W# (WR#), E(RD#) and D/C# can be connected to an external ground.

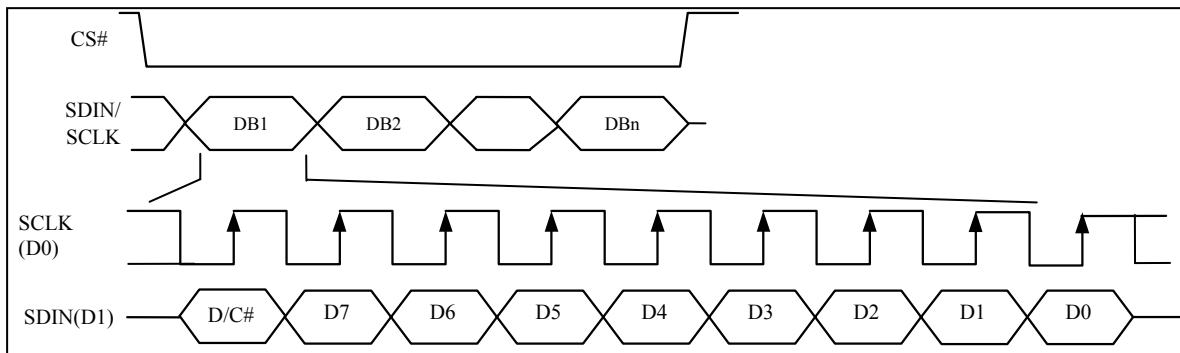
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 8-6 : Control pins of 3-wire Serial interface

| Function | E(RD#) | R/W#(WR#) | CS# | D/C# | D0 |
|---------------|---------|-----------|-----|---------|----|
| Write command | Tie LOW | Tie LOW | L | Tie LOW | ↑ |
| Write data | Tie LOW | Tie LOW | L | Tie LOW | ↑ |

Note
⁽¹⁾ L stands for LOW in signal

Figure 8-6 : Write procedure in 3-wire Serial interface mode



8.2 Reset Circuit

When RES# input is pulled LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 MUX Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Command A2h,B1h,B3h,BBh,BEh are locked by command FDh

8.3 GDDRAM

8.3.1 GDDRAM structure

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 128 x 128 x 18bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown in Table 8-7

Table 8-7 : 262k Color Depth Graphic Display Data RAM Structure

| Segment Address | Normal | 0 | | | 1 | | | 2 | | | 126 | 127 | | | | |
|-----------------|----------|----------|----|----|-------------------------|----|----|-----|-------|-------|-------|-----|----|----|---------------|--------|
| Address | Remapped | 127 | | | 126 | | | 125 | | | 1 | 0 | | | | |
| Color | | A | B | C | A | B | C | A | | | C | A | B | C | | |
| Data Format | | A5 | B5 | C5 | A5 | B5 | C5 | A5 | | | C5 | A5 | B5 | C5 | | |
| | | A4 | B4 | C4 | A4 | B4 | C4 | A4 | | | C4 | A4 | B4 | C4 | | |
| | | A3 | B3 | C3 | A3 | B3 | C3 | A3 | | | C3 | A3 | B3 | C3 | | |
| | | A2 | B2 | C2 | A2 | B2 | C2 | A2 | | | C2 | A2 | B2 | C2 | | |
| | | A1 | B1 | C1 | A1 | B1 | C1 | A1 | | | C1 | A1 | B1 | C1 | | |
| | | A0 | B0 | C0 | A0 | B0 | C0 | A0 | | | C0 | A0 | B0 | C0 | | |
| Common Address | Normal | Remapped | | | | | | | | | | | | | Common output | |
| 0 | 127 | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | | | 6 | 6 | 6 | 6 | COM0 |
| 1 | 126 | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | | | 6 | 6 | 6 | 6 | COM1 |
| 2 | 125 | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | | | 6 | 6 | 6 | 6 | COM2 |
| 3 | 124 | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | | | 6 | 6 | 6 | 6 | COM3 |
| 4 | 123 | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | | | 6 | 6 | 6 | 6 | COM4 |
| 5 | 122 | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | | | 6 | 6 | 6 | 6 | COM5 |
| 6 | 121 | | 6 | 6 | no of bits in this cell | | | 6 | 6 | | | 6 | 6 | 6 | 6 | COM6 |
| 7 | 120 | | | | | | | | | | | 6 | 6 | 6 | 6 | COM7 |
| : | : | | : | : | : | : | : | : | : | | | : | : | : | : | : |
| : | : | | : | : | : | : | : | : | : | | | : | : | : | : | : |
| : | : | | : | : | : | : | : | : | : | | | : | : | : | : | : |
| 123 | 4 | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | | | 6 | 6 | 6 | 6 | : |
| 124 | 3 | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | | | 6 | 6 | 6 | 6 | COM124 |
| 125 | 2 | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | | | 6 | 6 | 6 | 6 | COM125 |
| 126 | 1 | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | | | 6 | 6 | 6 | 6 | COM126 |
| 127 | 0 | | 6 | 6 | 6 | 6 | 6 | 6 | 6 | | | 6 | 6 | 6 | 6 | COM127 |

| | | | | | | | | | | | | | |
|------------|-----|-----|-----|-----|-----|-----|-----|-------|-------|-------|-------|-------|-------|
| SEG output | SA0 | SB0 | SC0 | SA1 | SB1 | SC1 | SA2 | | | SC126 | SA127 | SB127 | SC127 |
|------------|-----|-----|-----|-----|-----|-----|-----|-------|-------|-------|-------|-------|-------|

8.3.2 Data bus to RAM mapping under different input mode

Table 8-8 : Write Data bus usage under different bus width and color depth mode

| Write Data | | | Data bus | | | | | | | | | | | | | | | | | | |
|---------------|---------------|-------------|----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|-----|-----|-----|-----|-----|-----|----|
| Bus width | Color Depth | Input order | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 8 bits/Serial | 65k | 1st | X | X | X | X | X | X | X | X | X | X | X | C4 | C3 | C2 | C1 | C0 | B5 | B4 | B3 |
| | | 2nd | X | X | X | X | X | X | X | X | X | X | X | B2 | B1 | B0 | A4 | A3 | A2 | A1 | A0 |
| 8 bits/Serial | 262k | 1st | X | X | X | X | X | X | X | X | X | X | X | X | C5 | C4 | C3 | C2 | C1 | C0 | |
| | | 2nd | X | X | X | X | X | X | X | X | X | X | X | X | B5 | B4 | B3 | B2 | B1 | B0 | |
| | | 3rd | X | X | X | X | X | X | X | X | X | X | X | X | X | A5 | A4 | A3 | A2 | A1 | A0 |
| 16 bits | 65k | | X | X | C4 | C3 | C2 | C1 | C0 | B5 | B4 | B3 | B2 | B1 | B0 | A4 | A3 | A2 | A1 | A0 | |
| 16 bits | 262k format 1 | 1st | X | X | X | X | X | X | X | X | X | X | X | X | C5 | C4 | C3 | C2 | C1 | C0 | |
| | | 2nd | X | X | X | X | B5 | B4 | B3 | B2 | B1 | B0 | X | X | A5 | A4 | A3 | A2 | A1 | A0 | |
| 16 bits | 262k format 2 | 1st | X | X | X | X | C15 | C14 | C13 | C12 | C11 | C10 | X | X | B15 | B14 | B13 | B12 | B11 | B10 | |
| | | 2nd | X | X | X | X | A15 | A14 | A13 | A12 | A11 | A10 | X | X | C25 | C24 | C23 | C22 | C21 | C20 | |
| | | 3rd | X | X | X | X | B25 | B24 | B23 | B22 | B21 | B20 | X | X | A25 | A24 | A23 | A22 | A21 | A20 | |
| 18 bits | 262k | | C5 | C4 | C3 | C2 | C1 | C0 | B5 | B4 | B3 | B2 | B1 | B0 | A5 | A4 | A3 | A2 | A1 | A0 | |

Table 8-9 : Read Data bus usage under different bus width and color depth mode

| Read Data | | | Data bus | | | | | | | | | | | | | | | | | | |
|-----------|---------------|-------------|----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|-----|-----|-----|-----|-----|-----|----|
| Bus width | Color Depth | Input order | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 8 bits | 65k | 1st | X | X | X | X | X | X | X | X | X | X | X | C4 | C3 | C2 | C1 | C0 | B5 | B4 | B3 |
| | | 2nd | X | X | X | X | X | X | X | X | X | X | X | B2 | B1 | B0 | A4 | A3 | A2 | A1 | A0 |
| 8 bits | 262k | 1st | X | X | X | X | X | X | X | X | X | X | X | X | C5 | C4 | C3 | C2 | C1 | C0 | |
| | | 2nd | X | X | X | X | X | X | X | X | X | X | X | X | B5 | B4 | B3 | B2 | B1 | B0 | |
| | | 3rd | X | X | X | X | X | X | X | X | X | X | X | X | X | A5 | A4 | A3 | A2 | A1 | A0 |
| 16 bits | 65k | | X | X | C4 | C3 | C2 | C1 | C0 | B5 | B4 | B3 | B2 | B1 | B0 | A4 | A3 | A2 | A1 | A0 | |
| 16 bits | 262k format 1 | 1st | X | X | X | X | X | X | X | X | X | X | X | X | C5 | C4 | C3 | C2 | C1 | C0 | |
| | | 2nd | X | X | X | X | B5 | B4 | B3 | B2 | B1 | B0 | X | X | A5 | A4 | A3 | A2 | A1 | A0 | |
| 16 bits | 262k format 2 | 1st | X | X | X | X | C15 | C14 | C13 | C12 | C11 | C10 | X | X | B15 | B14 | B13 | B12 | B11 | B10 | |
| | | 2nd | X | X | X | X | A15 | A14 | A13 | A12 | A11 | A10 | X | X | C25 | C24 | C23 | C22 | C21 | C20 | |
| | | 3rd | X | X | X | X | B25 | B24 | B23 | B22 | B21 | B20 | X | X | A25 | A24 | A23 | A22 | A21 | A20 | |
| 18 bits | 262k | | C5 | C4 | C3 | C2 | C1 | C0 | B5 | B4 | B3 | B2 | B1 | B0 | A5 | A4 | A3 | A2 | A1 | A0 | |

8.4 Command Decoder

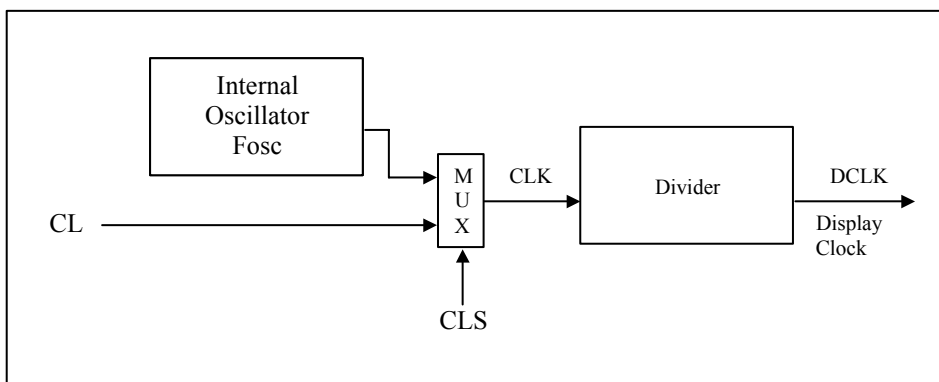
This module determines whether the input should be interpreted as data or command based upon the input of the D/C# pin.

If D/C# pin is HIGH, data is written to Graphic Display Data RAM (GDDRAM). If it is LOW, the inputs at D0-D17 are interpreted as a Command and it will be decoded and be written to the corresponding command register.

8.5 Oscillator & Timing Generator

8.5.1 Oscillator

Figure 8-7 : Oscillator Circuit



This module is an On-Chip low power RC oscillator circuitry (Figure 8-7). The operation clock (CLK) can be generated either from internal oscillator or external source CL pin by CLS pin. If CLS pin is HIGH, internal oscillator is selected. If CLS pin is LOW, external clock from CL pin will be used for CLK. The frequency of internal oscillator F_{OSC} can be programmed by command B3h.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor “D” can be programmed from 1 to 16 by command B3h.

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula:

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 1024 .
- K is the number of display clocks per row. The value is derived by
 $K = \text{Phase 1 period} + \text{Phase 2 period} + X$
 $X = \text{DCLKs in current drive period. Default } X = 134$
 Default K is $5 + 8 + 134 = 147$
- Number of multiplex ratio is set by command CAh. The reset value is 127 (i.e. 128MUX).
- F_{osc} is the oscillator frequency. It can be changed by command B3h A[7:4]. The higher the register setting results in higher frequency.

If the frame frequency is set too low, flickering may occur. On the other hand, higher frame frequency leads to higher power consumption on the whole system.

8.6 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current for segment current drivers I_{SEG} . The relationship between reference current and segment current of a color is:

$$I_{SEG} = \text{Contrast} / 256 * I_{REF} * \text{scale factor}$$

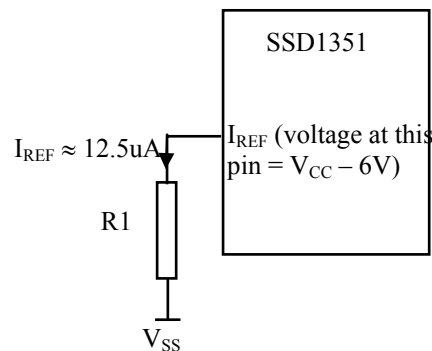
in which

the contrast is set by Set Contrast command (C1h); and
the scale factor (1 ~ 16) is set by Master Current Control command (C7h).

A resistor should be connected between I_{REF} pin and V_{SS} pin.

For example, in order to achieve $I_{SEG} = 200\mu\text{A}$ at maximum contrast 255, I_{REF} is set to around $12.5\mu\text{A}$. This current value is obtained by connecting an appropriate resistor from I_{REF} pin to V_{SS} as shown in Figure 8-8.

Figure 8-8 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is $V_{CC} - 6V$, the value of resistor $R1$ can be found as below:

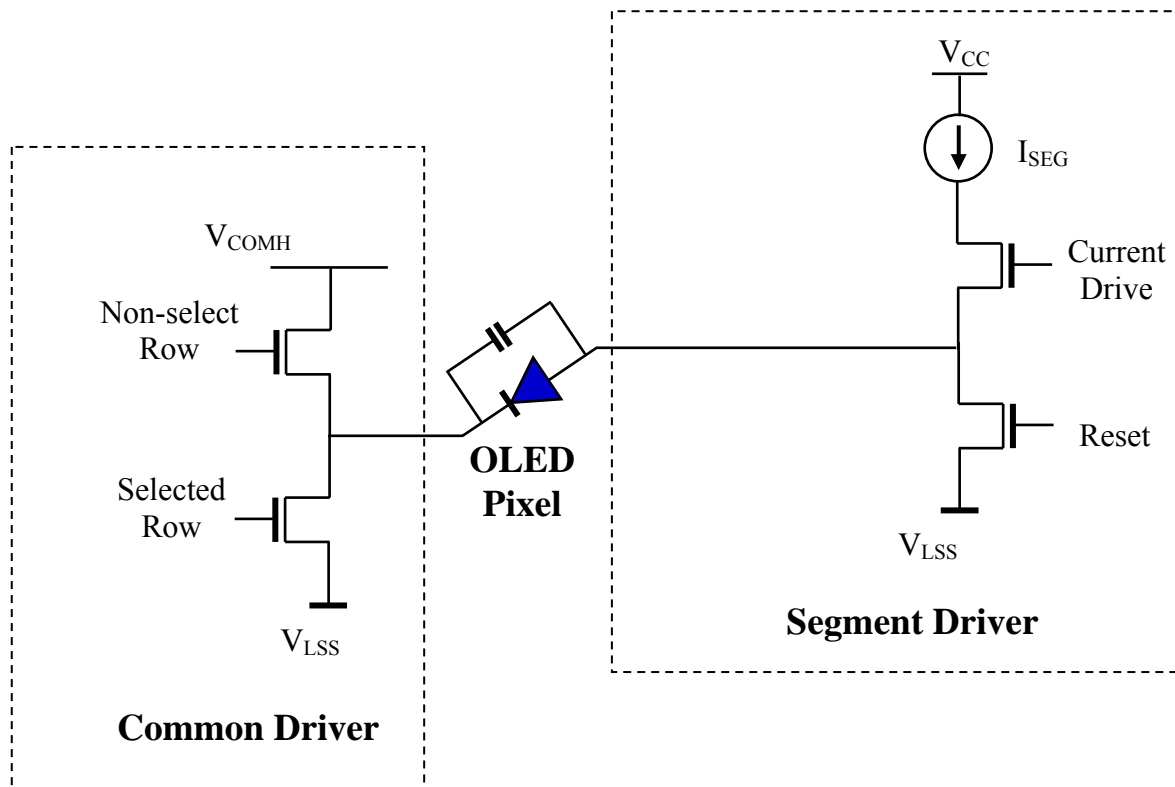
For $I_{REF} = 12.5\mu\text{A}$, $V_{CC} = 16V$:

$$\begin{aligned} R1 &= (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF} \\ &\approx (16 - 6) / 12.5\mu\text{A} \\ &\approx 800K\Omega \end{aligned}$$

8.7 SEG / COM Driver

Segment drivers consist of 384 (128 x 3 colors) current sources to drive OLED panel. The driving current can be adjusted from 0 to 200uA with 256 steps by contrast setting command (C1h). Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

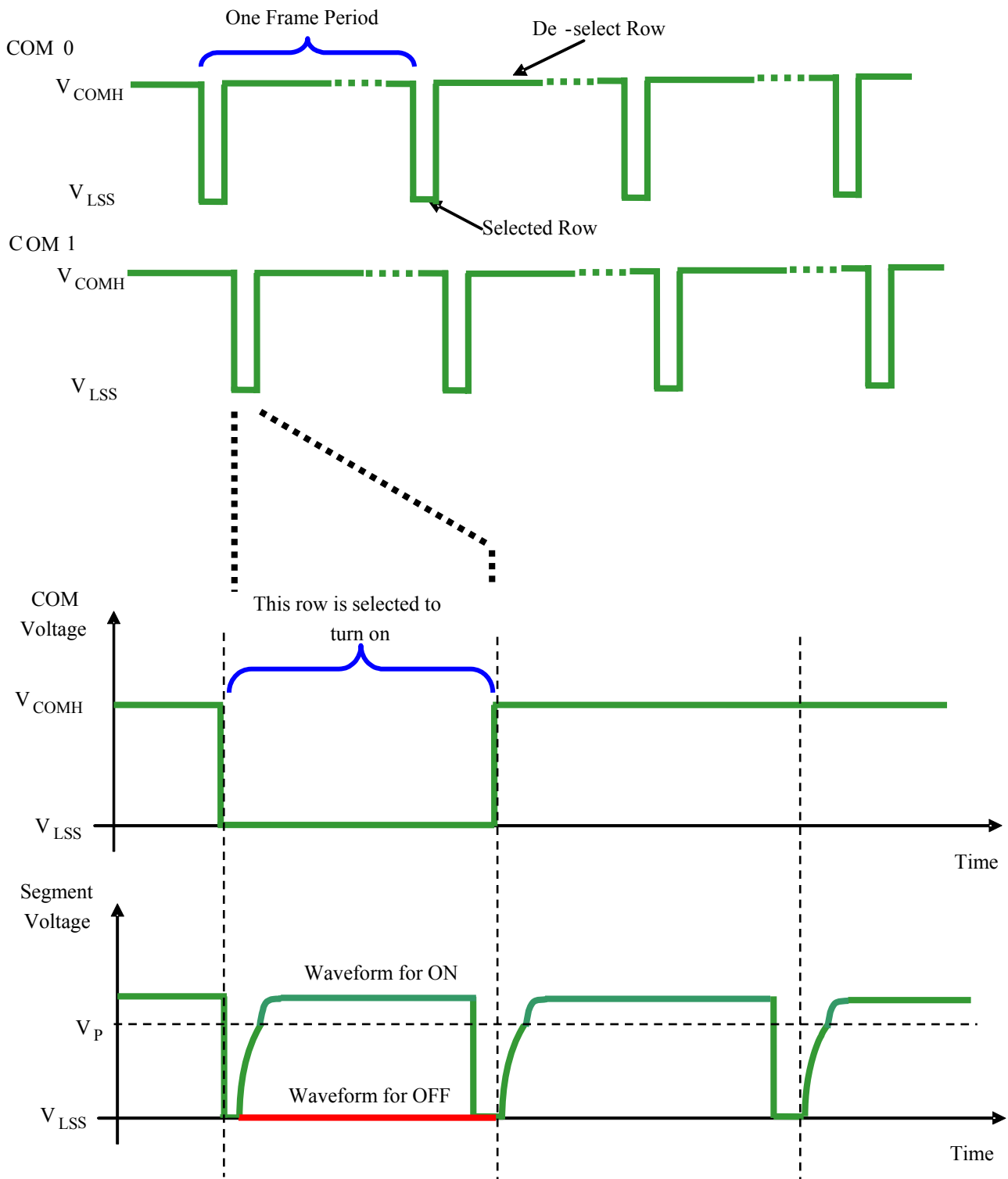
Figure 8-9 : Segment and Common Driver Block Diagram



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 8-10.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is disabled and the Reset switch is enabled. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Figure 8-10 : Segment and Common Driver Signal Waveform



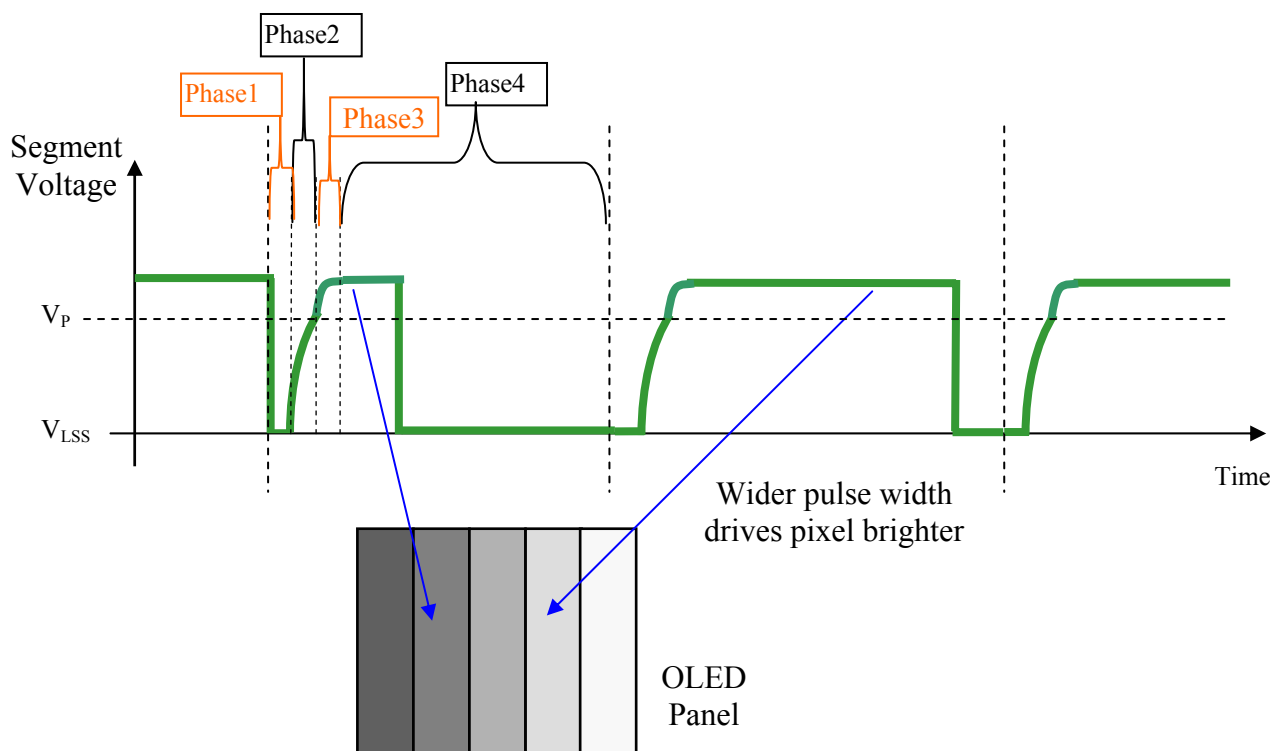
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0]. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS} . The amplitude of V_P can be programmed by the command BBh. The period of phase 2 can be programmed by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by command B6h.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The gray scale can be programmed into different Gamma settings by command B8h/B9h. The bigger gamma setting in the current drive stage results in brighter pixels and vice versa (Details refer to Section 8.8). This is shown in the following figure.

Figure 8-11: Gray Scale Control in Segment



After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.

The length of phase 4 is defined by command B8h "Look Up Table for Gray Scale Pulse width" or B9h "Use Built-in Linear LUT". In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

8.8 Gray Scale Decoder

The gray scale effect is generated by controlling the segment current in current drive phase. The segment current is controlled by the Gamma Settings (Setting 0~ Setting 180) through command B8h. The larger the setting, the brighter the pixel will be. The Gray Scale Table stores the corresponding Gamma Setting of the 64 gray scale levels (GS0~GS63) through the software commands B8h or B9h. Three programmable Gray Scale Tables (Gamma Look Up table) support the three colors A, B and C.

As shown in Figure 8-12, color A, B, C sub-pixel RAM data has 6 bits, represent the 64 gray scale level from GS0 to GS63.

Figure 8-12 : Relation between GDDRAM content and Gray Scale table entry for three colors in 262K color mode (under command B9h Use Built-in Linear LUT)

| Color A, B or C GDDRAM data (6 bits) | Gray Scale Table | Default Gamma Setting (Command B9h Linear Gamma Look Up Table) |
|---|------------------|---|
| 000000 | GS0 | Setting 0 |
| 000001 | GS1 | Setting 0 |
| 000010 | GS2 | Setting 2 |
| 000011 | GS3 | Setting 4 |
| 000100 | GS4 | Setting 6 |
| ⋮ | ⋮ | ⋮ |
| 111101 | GS61 | Setting 120 |
| 111110 | GS62 | Setting 122 |
| 111111 | GS63 | Setting 124 |

In command B8h, there are total 180 Gamma Settings (Setting 0 to Setting 180) available for the Gray Scale table. GS0 has no pre-charge and current drive stages so it is in Gamma Setting 0. GS1 can be set as only pre-charge but no current drive stage by input Gamma Setting 0.

When setting the Gray Scale Table (by B8h command) , the rules below must follow:

- 1) All Gamma Settings (i.e. GS1, GS2, GS3,.....GS63) are entered after command B8h.
- 2) The gray scale is defined in incremental way, with reference to the length of previous table entry:
 - Setting of GS1 has to be ≥ 0
 - Setting of GS2 has to be $> \text{Setting of GS1} + 1$
 - Setting of GS3 has to be $> \text{Setting of GS2} + 1$
 - ⋮
 - Setting of GS63 has to be $> \text{Setting of GS62} + 1$

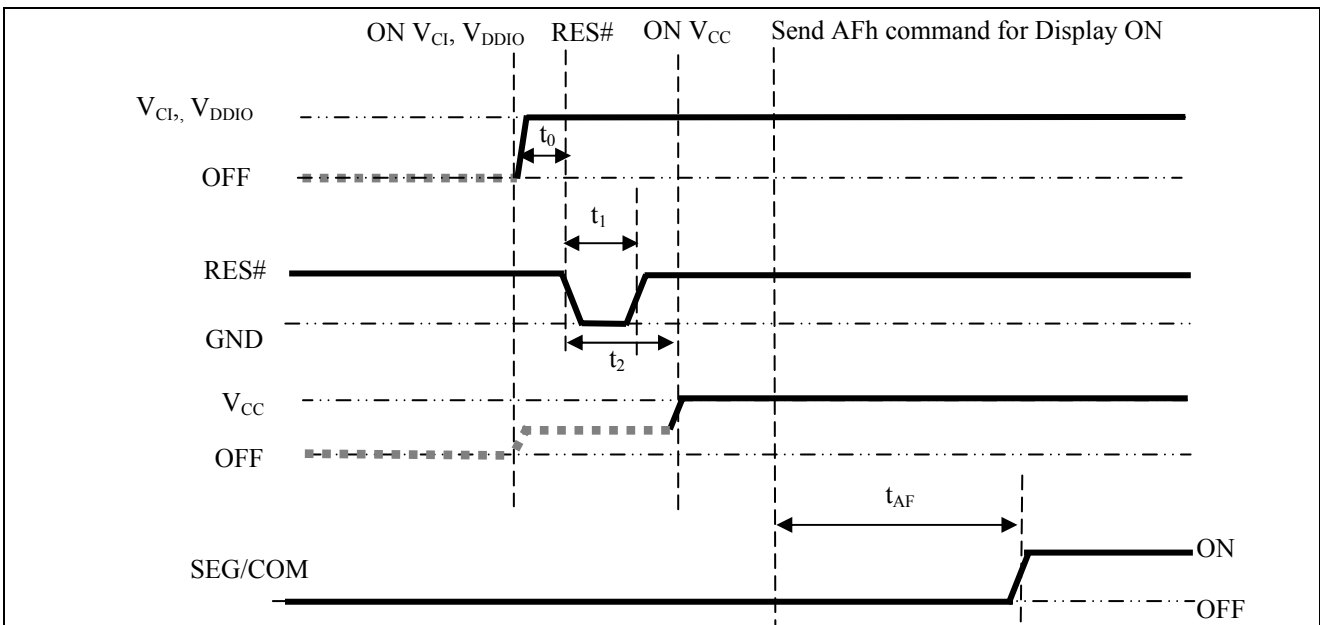
8.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351 (assume V_{CI} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

Power ON sequence:

1. Power ON V_{CI} , V_{DDIO} .
2. After V_{CI} , V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 2us (t_1)⁽⁴⁾ and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t_2). Then Power ON V_{CC} .⁽¹⁾
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (t_{AF}).
5. After V_{CI} become stable, wait for at least 300ms to send command.

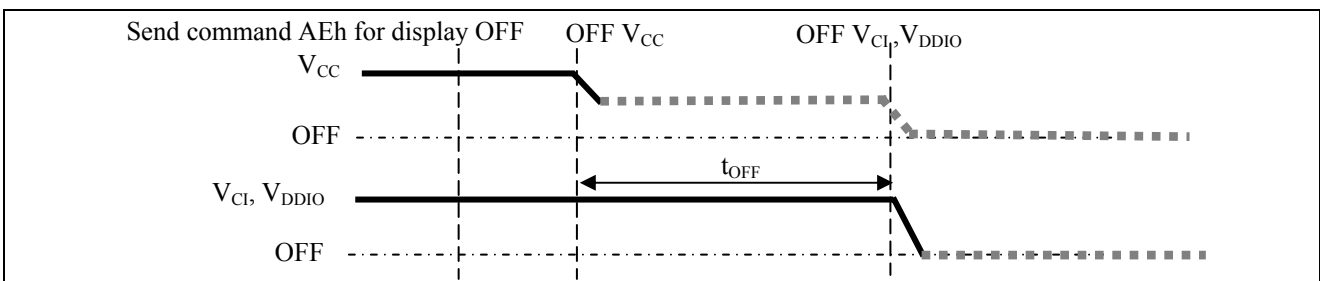
Figure 8-13 : The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC} .^{(1), (2)}
3. Wait for t_{OFF} . Power OFF V_{CI} , V_{DDIO} . (where Minimum $t_{OFF}=0ms$ ⁽³⁾, Typical $t_{OFF}=100ms$)

Figure 8-14 : The Power OFF sequence



Note:

- (1) Since an ESD protection circuit is connected between V_{CI} , V_{DDIO} and V_{CC} , V_{CC} becomes lower than V_{CI} whenever V_{CI} , V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 8-13 and Figure 8-14.
- (2) V_{CC} should be kept float (disable) when it is OFF.
- (3) V_{CI} , V_{DDIO} should not be Power OFF before V_{CC} Power OFF.
- (4) The register values are reset after t_1 .
- (5) Power pins (V_{CI} , V_{DDIO} and V_{CC}) can never be pulled to ground under any circumstance.

8.10 V_{DD} Regulator

In SSD1351, the power supply pin for core logic operation: V_{DD}, can be supplied by external source or internally regulated through the V_{DD} regulator.

When the command ABh, bit A[0] is set to 1b, the internal V_{DD} regulator is enabled. V_{CI} should be larger than 2.6V when using the internal V_{DD} regulator.

When the command ABh, bit A[0] is set to 0b, external V_{DD} should be used. (external V_{DD} range : 2.4V~2.6V)

It should be notice that, no matter V_{DD} is supplied by external source or internally regulated, V_{CI} must always be equal or higher than V_{DD} and V_{DDIO}.

The following figure shows the V_{DD} regulator pin connection scheme:

Figure 8-15 V_{CI} > 2.6V, V_{DD} regulator enable : pin connection scheme

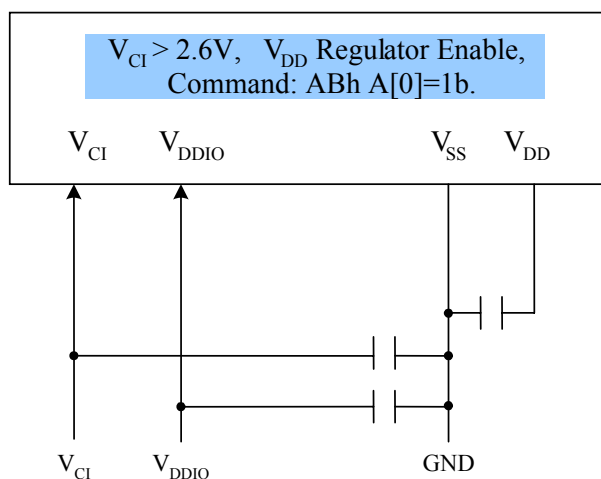
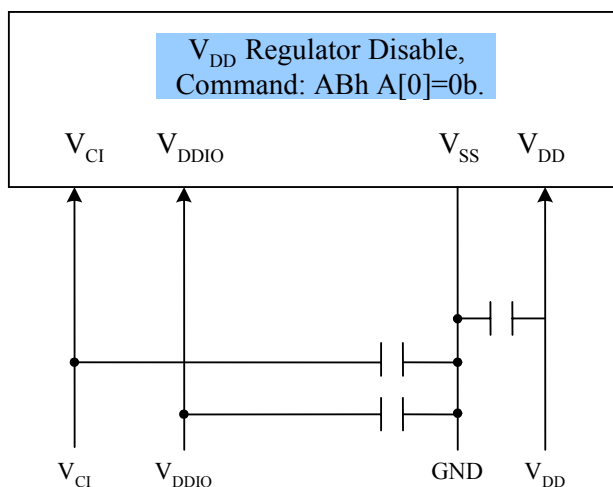


Figure 8-16 V_{DD} regulator disable : pin connection scheme



8.10.1 V_{DD} Regulator in Sleep Mode

Power can be saved by disable the internal V_{DD} regulator during Sleep mode. The following figures show the corresponding command sequence:

Figure 8-17 : Case 1 - Command sequence for just entering/ exiting sleep mode

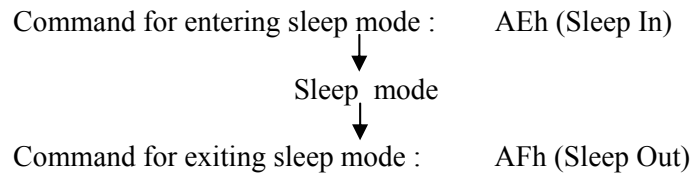
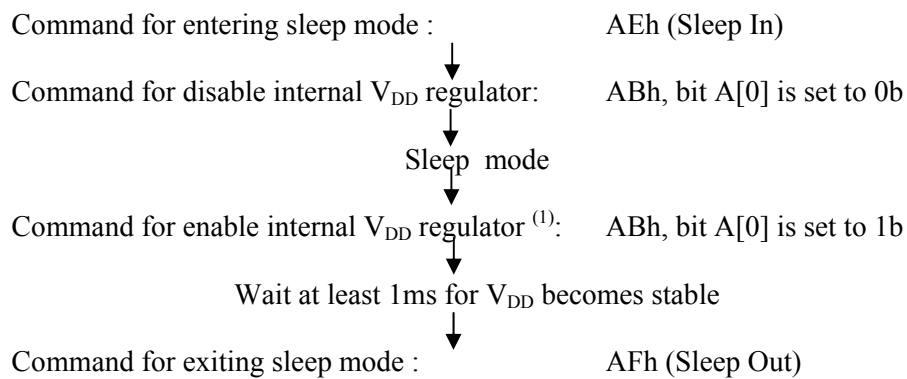


Figure 8-18 : Case 2 - Command sequence for disabling internal V_{DD} regulator during sleep mode



In the above two cases, the RAM content can also be kept during the sleep mode.

Note:

⁽¹⁾ It should be noted that the internal V_{DD} regulator should be enabled before exiting sleep mode (issuing command AFh).

⁽²⁾ No RAM access through MCU interface when there is no external/ internal V_{DD}.

9 COMMAND

9.1 Basic Command List

Table 9-1 : Command table

(D/C# = 0, R/W#(WR#)=0, E(RD#) = 1) unless specific setting is stated

Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

| Fundamental Command Table | | | | | | | | | | | |
|---------------------------|--------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---|---|
| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description |
| 0 | 15 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | Set Column Address | A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127 |
| 1 | A[6:0] | * | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | |
| 1 | B[6:0] | * | B ₆ | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | | |
| 0 | 75 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | Set Row Address | A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127 |
| 1 | A[6:0] | * | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | |
| 1 | B[6:0] | * | B ₆ | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | | |
| 0 | 5C | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Write RAM Command | Enable MCU to write Data into RAM |
| 0 | 5D | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | Read RAM Command | Enable MCU to read Data from RAM |
| 0 | A0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Set Re-map / Color Depth (Display RAM to Panel) | A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment |
| 1 | A[7:0] | A ₇ | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | <p>A[1]=0b, Column address 0 is mapped to SEG0 [reset] A[1]=1b, Column address 127 is mapped to SEG0</p> <p>A[2]=0b, Color sequence: A → B → C [reset] A[2]=1b, Color sequence is swapped: C → B → A</p> <p>A[3]=0b, Reserved A[3]=1b, Reserved</p> <p>A[4]=0b, Scan from COM0 to COM[N-1] [reset] A[4]=1b, Scan from COM[N-1] to COM0. Where N is the Multiplex ratio.</p> <p>A[5]=0b, Disable COM Split Odd Even A[5]=1b, Enable COM Split Odd Even [reset]</p> <p>A[7:6] Set Color Depth, 00b / 01b: 65k color [reset] 10b: 262k color 11b 262k color, 16-bit format 2</p> <p>Refer to Table 8-8 for details</p> |

Fundamental Command Table

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description |
|--------|--------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---|--|
| 0 1 | A1 A[6:0] | 1 * | 0 A ₆ | 1 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 1 A ₀ | Set Display Start Line | Set vertical scroll by RAM from 0~127. [reset=00h] |
| 0 1 | A2 A[6:0] | 1 * | 0 A ₆ | 1 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 0 A ₀ | Set Display Offset | Set vertical scroll by Row from 0-127. [reset=60h] Note (1) This command is locked by Command FDh by default. To unlock it, please refer to Command FDh. |
| 0 | A4~A7 | 1 | 0 | 1 | 0 | 0 | 1 | X ₁ | X ₀ | Set Display Mode | A4h: All OFF A5h: All ON (All pixels have GS63) A6h : Reset to normal display [reset] A7h: Inverse Display (GS0 -> GS63, GS1 -> GS62,) |
| 0 1 | AB A[7:0] | 1 A ₇ | 0 A ₆ | 1 0 | 0 0 | 1 0 | 0 0 | 1 0 | 1 A ₀ | Function Selection | A[0]=0b, Select external V _{DD} A[0]=1b, Enable internal V _{DD} regulator [reset] A[7:6]=00b, Select 8-bit parallel interface [reset] A[7:6]=01b, Select 16-bit parallel interface A[7:6]=11b, Select 18-bit parallel interface |
| 0 | AD | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | NOP | Command for no operation. |
| 0 | AE~AF | 1 | 0 | 1 | 0 | 1 | 1 | 1 | X ₀ | Set Sleep mode ON/OFF | A Eh = Sleep mode On (Display OFF) A Fh = Sleep mode OFF (Display ON) |
| 0 | B0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | NOP | Command for no operation. |
| 0 1 | B1 A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 1 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 1 A ₀ | Set Reset (Phase 1) / Pre-charge (Phase 2) period | A[3:0] Phase 1 period of 5~31 DCLK(s) clocks [reset=0010b] A[3:0]: 0-1 invalid 2 = 5 DCLKs 3 = 7 DCLKs : 15 = 31DCLKs A[7:4] Phase 2 period of 3~15 DCLK(s) clocks [reset=1000b] A[7:4]: 0-2 invalid 3 = 3 DCLKs 4 = 4 DCLKs : 15 = 15DCLKs Note (1) 0 DCLK is invalid in phase 1 & phase 2 (2) This command is locked by Command FDh by default. To unlock it, please refer to Command FDh. |

Fundamental Command Table

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|--|--|--------|--------|------|-------------|------|-------------|------|-------------|------|-------------|------|--------------|------|--------------|------|--------------|------|---------------|------|---------------|------|---------------|------|----------------|--------|---------|
| 0 1 1 1 | B2 A[7:0] B[7:0] C[7:0] | 1 A ₇ 0 0 | 0 A ₆ 0 0 | 1 A ₅ 0 0 | 1 A ₄ 0 0 | 0 A ₃ 0 0 | 0 A ₂ 0 0 | 1 A ₁ 0 0 | 0 A ₀ 0 0 | Display Enhancement | A[7:0] = 00h, B[7:0] = 00h, C[7:0] = 00h normal [reset] A[7:0] = A4h, B[7:0] = 00h, C[7:0] = 00h enhance display performance | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 1 | B3 A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 1 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 1 A ₀ | Front Clock Divider (DivSet)/ Oscillator Frequency | <p>A[3:0] [reset=0001], divide by DIVSET where</p> <table border="1"> <thead> <tr> <th>A[3:0]</th> <th>DIVSET</th> </tr> </thead> <tbody> <tr><td>0000</td><td>divide by 1</td></tr> <tr><td>0001</td><td>divide by 2</td></tr> <tr><td>0010</td><td>divide by 4</td></tr> <tr><td>0011</td><td>divide by 8</td></tr> <tr><td>0100</td><td>divide by 16</td></tr> <tr><td>0101</td><td>divide by 32</td></tr> <tr><td>0110</td><td>divide by 64</td></tr> <tr><td>0111</td><td>divide by 128</td></tr> <tr><td>1000</td><td>divide by 256</td></tr> <tr><td>1001</td><td>divide by 512</td></tr> <tr><td>1010</td><td>divide by 1024</td></tr> <tr><td>>=1011</td><td>invalid</td></tr> </tbody> </table> <p>A[7:4] Oscillator frequency, frequency increases as level increases [reset=1101b]</p> <p>Note (¹) This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.</p> | A[3:0] | DIVSET | 0000 | divide by 1 | 0001 | divide by 2 | 0010 | divide by 4 | 0011 | divide by 8 | 0100 | divide by 16 | 0101 | divide by 32 | 0110 | divide by 64 | 0111 | divide by 128 | 1000 | divide by 256 | 1001 | divide by 512 | 1010 | divide by 1024 | >=1011 | invalid |
| A[3:0] | DIVSET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0000 | divide by 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0001 | divide by 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0010 | divide by 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0011 | divide by 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0100 | divide by 16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0101 | divide by 32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0110 | divide by 64 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0111 | divide by 128 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1000 | divide by 256 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1001 | divide by 512 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1010 | divide by 1024 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| >=1011 | invalid | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 1 1 1 | B4 A[7:0] B[7:0] C[7:0] | 1 1 1 0 | 0 0 0 1 | 1 1 1 0 | 1 0 1 0 | 0 0 0 0 | 1 0 1 1 | 0 A ₁ 0 0 | 0 A ₀ 1 1 | Set Segment Low Voltage (VSL) | <p>A[1:0]=00 External VSL [reset] A[1:0]=01,10,11 are invalid</p> <p>Note (¹) When external VSL is enabled, in order to avoid distortion in display pattern, an external circuit is needed to connect between VSL and V_{SS} as shown in Figure 14-1.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 1 | B5 A[3:0] | 1 * | 0 * | 1 * | 1 * | 0 A ₃ | 1 A ₂ | 0 A ₁ | 1 A ₀ | Set GPIO | <p>A[1:0] GPIO0: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH</p> <p>A[3:2] GPIO1: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH</p> | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 1 | B6 A[3:0] | 1 * | 0 * | 1 * | 1 * | 0 A ₃ | 1 A ₂ | 0 A ₁ | 0 A ₀ | Set Second Pre-charge Period | <p>A[3:0] Set Second Pre-charge Period</p> <p>0000b invalid 0001b 1 DCLKS 0010b 2 DCLKS 1000 8 DCLKS [reset] 1111 15 DCLKS</p> | | | | | | | | | | | | | | | | | | | | | | | | | | |

Fundamental Command Table

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description | | | | | | | | | | | | | | | | | | |
|--------|----------|--------------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|--|---|--------|----------|--------------------|-------|-----|------------------------|---|---|---|-------|-----|--------------------------------|---|---|---|-----|-----|------------------------|
| 0 | B8 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | | The next 63 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, : A62[7:0]: Gamma Setting for GS62, A63[7:0]: Gamma Setting for GS63 Note (1) $0 \leq \text{Setting of GS1} < \text{Setting of GS2} < \text{Setting of GS3} \dots < \text{Setting of GS62} < \text{Setting of GS63}$ (2) GS0 has only pre-charge but no current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0. | | | | | | | | | | | | | | | | | | |
| 1 | A1[7:0] | A1 ₇ | A1 ₆ | A1 ₅ | A1 ₄ | A1 ₃ | A1 ₂ | A1 ₁ | A1 ₀ | | | | | | | | | | | | | | | | | | | | |
| 1 | A2[7:0] | A2 ₇ | A2 ₆ | A2 ₅ | A2 ₄ | A2 ₃ | A2 ₂ | A2 ₁ | A2 ₀ | | | | | | | | | | | | | | | | | | | | |
| 1 | . | . | . | . | . | . | . | . | . | | | | | | | | | | | | | | | | | | | | |
| 1 | . | . | . | . | . | . | . | . | . | | | | | | | | | | | | | | | | | | | | |
| 1 | . | . | . | . | . | . | . | . | . | | | | | | | | | | | | | | | | | | | | |
| 1 | A62[7:0] | A62 ₇ | A62 ₆ | A62 ₅ | A62 ₄ | A62 ₃ | A62 ₂ | A62 ₁ | A62 ₀ | | | | | | | | | | | | | | | | | | | | |
| 1 | A63[7:0] | A63 ₇ | A63 ₆ | A63 ₅ | A63 ₄ | A63 ₃ | A63 ₂ | A63 ₁ | A63 ₀ | Look Up Table for Gray Scale Pulse width | | | | | | | | | | | | | | | | | | | |
| 0 | B9 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | | Reset to default Look Up Table: GS1 = 0 DCLK GS2 = 2 DCLK GS3 = 4 DCLK GS4 = 6 DCLK ... GS62 = 122 DCLK GS63 = 124 DCLK | | | | | | | | | | | | | | | | | | |
| 0 | BB | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | | Set pre-charge voltage level.[reset = 17h] <table border="1"> <thead> <tr> <th>A[4:0]</th> <th>Hex code</th> <th>pre-charge voltage</th> </tr> </thead> <tbody> <tr> <td>00000</td> <td>00h</td> <td>0.20 x V_{CC}</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>11111</td> <td>1Fh</td> <td>0.60 x V_{CC}</td> </tr> </tbody> </table> | A[4:0] | Hex code | pre-charge voltage | 00000 | 00h | 0.20 x V _{CC} | : | : | : | 11111 | 1Fh | 0.60 x V _{CC} | | | | | | |
| A[4:0] | Hex code | pre-charge voltage | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00000 | 00h | 0.20 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11111 | 1Fh | 0.60 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | A[4:0] | 0 | 0 | 0 | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | Set Pre-charge voltage | | | | | | | | | | | | | | | | | | | |
| 0 | BE | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | | Set COM deselect voltage level [reset = 05h] <table border="1"> <thead> <tr> <th>A[2:0]</th> <th>Hex code</th> <th>V_{COMH}</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>00h</td> <td>0.72 x V_{CC}</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>101</td> <td>05h</td> <td>0.82 x V_{CC} [reset]</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>111</td> <td>07h</td> <td>0.86 x V_{CC}</td> </tr> </tbody> </table> | A[2:0] | Hex code | V _{COMH} | 000 | 00h | 0.72 x V _{CC} | : | : | : | 101 | 05h | 0.82 x V _{CC} [reset] | : | : | : | 111 | 07h | 0.86 x V _{CC} |
| A[2:0] | Hex code | V _{COMH} | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000 | 00h | 0.72 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 101 | 05h | 0.82 x V _{CC} [reset] | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 111 | 07h | 0.86 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | A[2:0] | 0 | 0 | 0 | 0 | 0 | A ₂ | A ₁ | A ₀ | Set V _{COMH} Voltage | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | Note (1) This command is locked by Command FDh by default. To unlock it, please refer to Command FDh. | | | | | | | | | | | | | | | | | | |

| Fundamental Command Table | | | | | | | | | | | |
|---------------------------|--------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--------------------------------------|---|
| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description |
| 0 | C1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | Set Contrast Current for Color A,B,C | A[7:0] Contrast Value Color A [reset=10001010b] |
| 1 | A[7:0] | A ₇ | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | B[7:0] Contrast Value Color B [reset=01010001b] |
| 1 | B[7:0] | B ₇ | B ₆ | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | | C[7:0] Contrast Value Color C [reset=10001010b] |
| 1 | C[7:0] | C ₇ | C ₆ | C ₅ | C ₄ | C ₃ | C ₂ | C ₁ | C ₀ | | |
| 0 | C7 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | Master Contrast Current Control | A[3:0] : |
| 1 | A[3:0] | * | * | * | * | A ₃ | A ₂ | A ₁ | A ₀ | | 0000b reduce output currents for all colors to 1/16 0001b reduce output currents for all colors to 2/16 1110b reduce output currents for all colors to 15/16 1111b no change [reset] |
| 0 | CA | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | Set MUX Ratio | A[6:0] MUX ratio 16MUX ~ 128MUX, [reset=127], (Range from 15 to 127) |
| 1 | A[6:0] | 0 | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | |
| 0 | D1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | NOP | Command for No Operation |
| 0 | E3 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | NOP | Command for No Operation |
| 0 | FD | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | Set Command Lock | A[7:0]: MCU protection status [reset = 12h] A[7:0] = 12b, Unlock OLED driver IC MCU interface from entering command [reset] A[7:0] = 16b, Lock OLED driver IC MCU interface from entering command |
| 1 | A[7:0] | A ₇ | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | A[7:0] = B0b, Command A2,B1,B3,BB,BE,C1 inaccessible in both lock and unlock state [reset] A[7:0] = B1b, Command A2,B1,B3,BB,BE,C1 accessible if in unlock state |
| | | | | | | | | | | | Note (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command. |

Note

(1) “*” stands for “Don’t care”.

Table 9-2: SSD1351 Graphic Acceleration Command List

Set (GAC) (D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated

Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

| Graphic acceleration command | | | | | | | | | | | |
|------------------------------|--------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-------------------|---|
| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
| 0 | 96 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | Horizontal Scroll | A[7:0] = 00000000b No scrolling |
| 1 | A[7:0] | A ₇ | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | A[7:0] = 00000001b to 00111111b Scroll towards SEG127 with 1 column offset |
| 1 | B[6:0] | 0 | B ₆ | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | | A[7:0] = 01000000b to 11111111b Scroll towards SEG0 with 1 column offset |
| 1 | C[7:0] | C ₇ | C ₆ | C ₅ | C ₄ | C ₃ | C ₂ | C ₁ | C ₀ | | |
| 1 | D[6:0] | 0 | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | | B[6:0] : start row address |
| 1 | E[1:0] | 0 | 0 | 0 | 0 | 0 | 0 | E ₁ | E ₀ | | C[7:0] : number of rows to be H-scrolled B+C <= 128 |
| | | | | | | | | | | | D[6:0] : Reserved (reset=00h) |
| | | | | | | | | | | | E[1:0] : scrolling time interval 00b test mode 01b normal 10b slow 11b slowest |
| | | | | | | | | | | | Note (1) Operates during display ON. |
| 0 | 9E | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | Stop Moving | Stop horizontal scroll |
| | | | | | | | | | | | Note (1) After sending 9Eh command to stop the scrolling action, the ram data needs to be rewritten |
| 0 | 9F | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | Start Moving | Start horizontal scroll |

Note

(1) After executed the graphic command, waiting time is required for update GDDRAM content.

V_{CI} = 2.4~3.5V, waiting time = 500ns/pixel.

(2) “*” stands for “Don’t care”.

10 COMMAND

10.1.1 Set Column Address (15h)

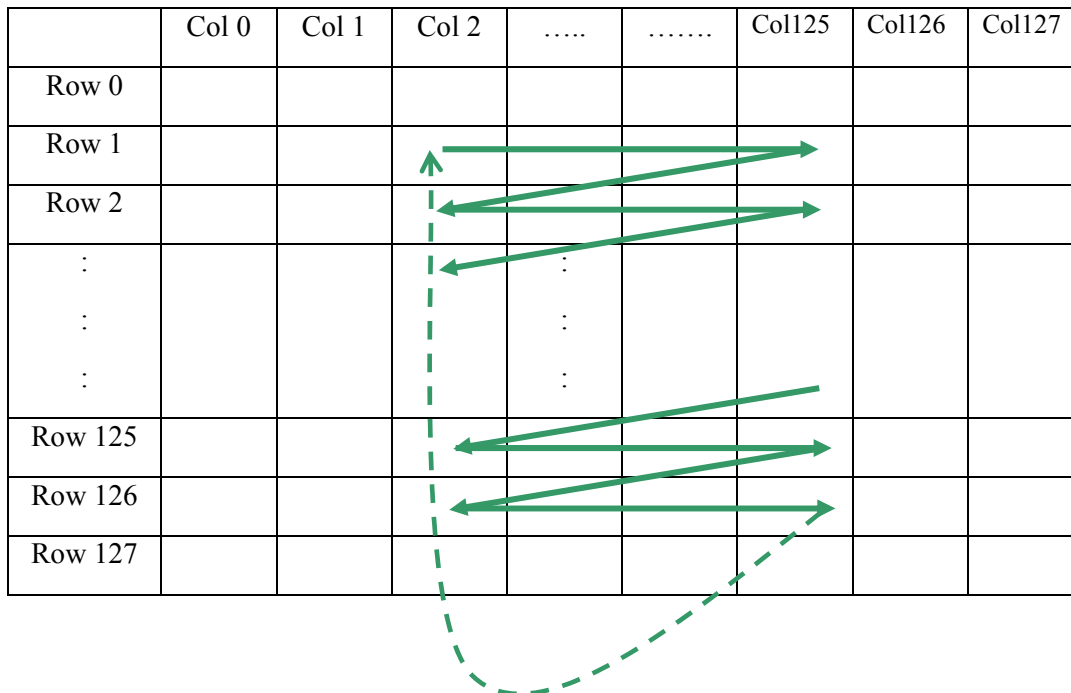
This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

10.1.2 Set Row Address (75h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

For example, column start address is set to 2 and column end address is set to 125, row start address is set to 1 and row end address is set to 126. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 125 and from row 1 to row 126 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (solid line in Figure 10-1). Whenever the column address pointer finishes accessing the end column 125, it is reset back to column 2 and row address is automatically increased by 1 (solid line in Figure 10-1). While the end row 126 and end column 125 RAM location is accessed, the row address is reset back to 1 and the column address is reset back to 2 (dotted line in Figure 10-1).

Figure 10-1 : Example of Column and Row Address Pointer Movement



10.1.3 Write RAM Command (5Ch)

After entering this single byte command, data entries will be written into the display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before write data into RAM.

10.1.4 Read RAM Command (5Dh)

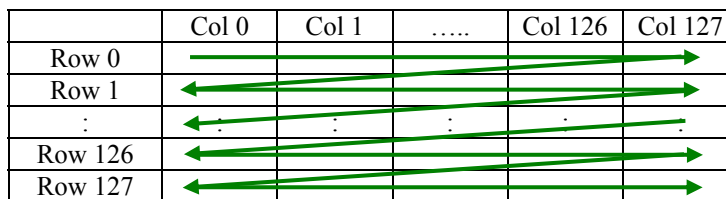
After entering this single byte command, data is read from display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before read data from RAM.

10.1.5 Set Re-map & Dual COM Line Mode (A0h)

This command has multiple configurations and each bit setting is described as follows:

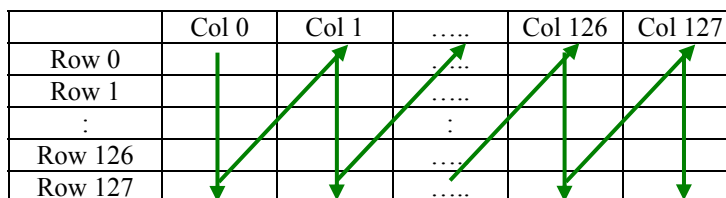
- Address increment mode (A[0])
When A[0] is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 10-2.

Figure 10-2 : Address Pointer Movement of Horizontal Address Increment Mode



When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read / written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 10-3.

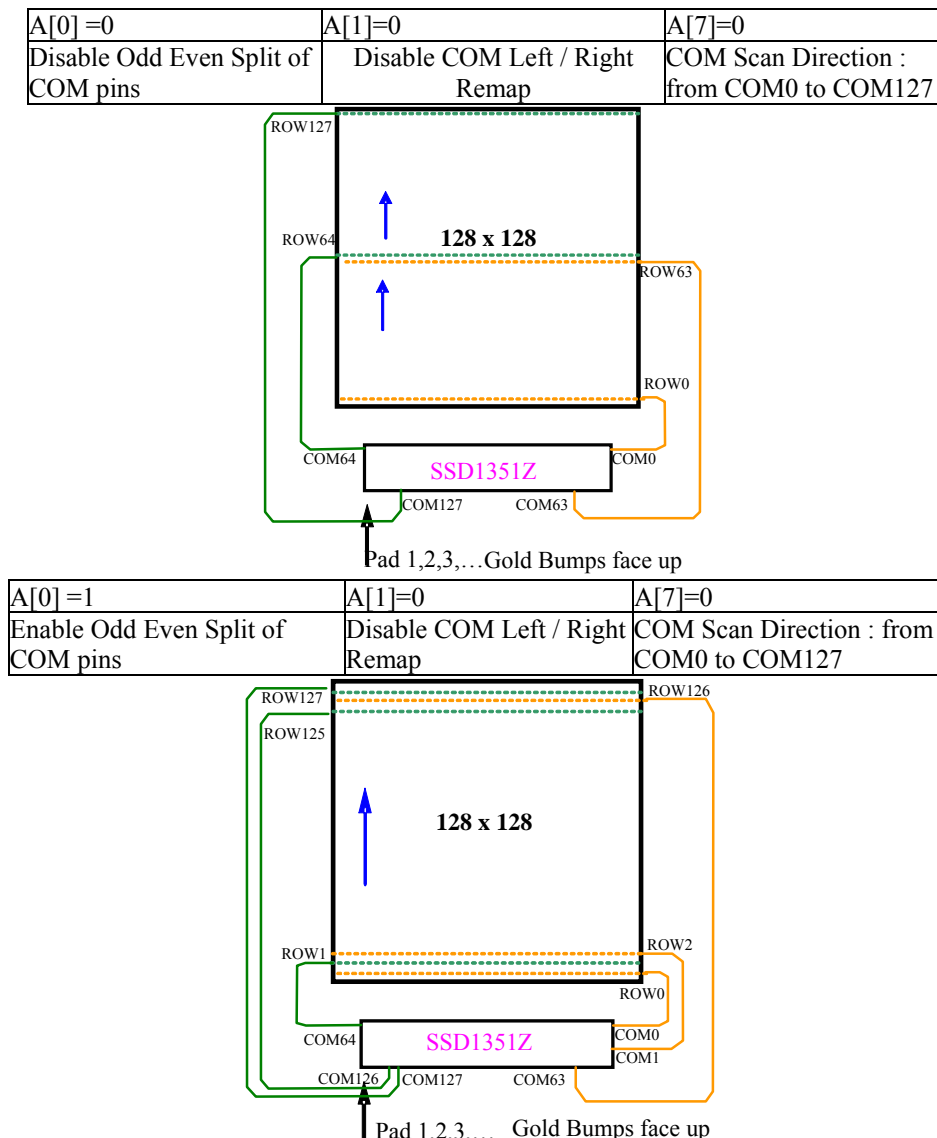
Figure 10-3: Address Pointer Movement of Vertical Address Increment Mode



- Column Address Remap (A[1])
This command bit is made for increasing the layout flexibility of segment signals in OLED module with segment arranged from left to right (when A[1] is set to 0) or vice versa (when A[1] is set to 1), as demonstrated in Figure 10-4.
A[1] = 0 (reset): RAM Column 0 ~ 127 maps to Col0~Col127
A[1] = 1: RAM Column 0 ~ 127 maps to Col127~Col0

- Color Remap (A[2])
A[2] = 0 (reset): color sequence A → B → C
A[2] = 1: color sequence C → B → A
- COM scan direction Remap (A[4])
This command bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa.
A[1] = 0 (reset): Scan from up to down
A[1] = 1: Scan from bottom to up
Details of pin arrangement can be found in Figure 10-4.
- Odd even split of COM pins (A[5])
This command bit can set the odd even arrangement of COM pins.
A[5] = 0 (reset): Disable COM split odd even, pin assignment of common is in sequential as
COM127 COM126...COM 65 COM64...SEG479...SEG0...COM0 COM1...COM62 COM63
A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
COM127 COM125...COM3 COM1...SEG479...SEG0...COM0 COM2...COM124 COM126
Details of pin arrangement can be found in Figure 10-4.

Figure 10-4 : COM Pins Hardware Configuration (MUX ratio: 128)








- Display color mode (A[7:6])
Select either 262k, 65k or 256 color mode.

10.1.6 Set Display Start Line (A1h)

This command is used to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 127. Figure 10-5 shows an example of using this command when MUX ratio = 128 and MUX ratio = 100 and Display Start Line = 28. In there, “Row” means the graphic display data RAM row.





Figure 10-5 : Example of Set Display Start Line with no Remap

| | 128 | 128 | 100 | 100 | MUX ratio (CAh) |
|-----------------|---|---|---|---|---|
| COM Pin | 0 | 28 | 0 | 28 | Display start line (A1h) |
| COM0 | Row0 | Row28 | Row0 | Row28 | |
| COM1 | Row1 | Row29 | Row1 | Row29 | |
| COM2 | Row2 | Row30 | Row2 | Row30 | |
| COM3 | Row3 | Row31 | Row3 | Row31 | |
| COM4 | Row4 | Row32 | Row4 | Row32 | |
| COM5 | Row5 | Row33 | Row5 | Row33 | |
| COM6 | Row6 | Row34 | Row6 | Row34 | |
| : | : | : | : | : | |
| : | : | : | : | : | |
| : | : | : | : | : | |
| : | : | : | : | : | |
| COM95 | Row95 | Row123 | Row95 | Row124 | |
| COM96 | Row96 | Row124 | Row96 | Row125 | |
| COM97 | Row97 | Row125 | Row97 | Row126 | |
| COM98 | Row98 | Row126 | Row98 | Row127 | |
| COM99 | Row99 | Row127 | Row99 | Row0 | |
| COM100 | Row100 | Row0 | - | - | |
| COM101 | Row101 | Row1 | - | - | |
| COM102 | Row102 | Row2 | - | - | |
| COM103 | Row103 | Row3 | - | - | |
| COM104 | Row104 | Row4 | - | - | |
| COM105 | Row105 | Row5 | - | - | |
| COM106 | Row106 | Row6 | - | - | |
| COM107 | Row107 | Row7 | - | - | |
| COM108 | Row108 | Row8 | - | - | |
| COM109 | Row109 | Row9 | - | - | |
| COM110 | Row110 | Row10 | - | - | |
| COM111 | Row111 | Row11 | - | - | |
| COM112 | Row112 | Row12 | - | - | |
| COM113 | Row113 | Row13 | - | - | |
| COM114 | Row114 | Row14 | - | - | |
| COM115 | Row115 | Row15 | - | - | |
| COM116 | Row116 | Row16 | - | - | |
| COM117 | Row117 | Row17 | - | - | |
| COM118 | Row118 | Row18 | - | - | |
| COM119 | Row119 | Row19 | - | - | |
| COM120 | Row120 | Row20 | - | - | |
| COM121 | Row121 | Row21 | - | - | |
| COM122 | Row122 | Row22 | - | - | |
| COM123 | Row123 | Row23 | - | - | |
| COM124 | Row124 | Row24 | - | - | |
| COM125 | Row125 | Row25 | - | - | |
| COM126 | Row126 | Row26 | - | - | |
| COM127 | Row127 | Row27 | - | - | |
| Display example |  |  |  |  |  |
| | (a) | (b) | (c) | (d) | (GDDARAM) |

10.1.7 Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-127. For example, to move the COM16 towards the COM0 direction for 16 lines, A[7:0] should be given by 00010000. The figure below shows an example of this command. In there, “Row” means the graphic display data RAM row.

Figure 10-6 : Example of Set Display Offset with no Remap

| | a | b | c | Case |
|-----------------|---|---|---|---|
| | 128 | 96 | 96 | MUX ratio (CAh) |
| | 0 | 0 | 32 | Display offset (A2h A[7:0]) |
| COM0 | Row0 | Row0 | Row32 | |
| COM1 | Row1 | Row1 | Row33 | |
| COM2 | Row2 | Row2 | Row34 | |
| . | . | . | . | |
| COM61 | Row61 | Row61 | Row93 | |
| COM62 | Row62 | Row62 | Row94 | |
| COM63 | Row63 | Row63 | Row95 | |
| COM64 | Row64 | Row64 | - | |
| COM65 | Row65 | Row65 | - | |
| COM66 | Row66 | Row66 | - | |
| . | . | . | . | |
| COM93 | Row93 | Row93 | - | |
| COM94 | Row94 | Row94 | - | |
| COM95 | Row95 | Row95 | - | |
| COM96 | Row96 | - | Row0 | |
| COM97 | Row97 | - | Row1 | |
| COM98 | Row98 | - | Row2 | |
| . | . | . | . | |
| COM125 | Row125 | - | Row29 | |
| COM126 | Row126 | - | Row30 | |
| COM127 | Row127 | - | Row31 | |
| Display example |  |  |  |  |
| | (a) | (c) | (d) | (GDDARAM) |

10.1.8 Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Normal Display, Entire Display ON, Entire Display OFF and Inverse Display.

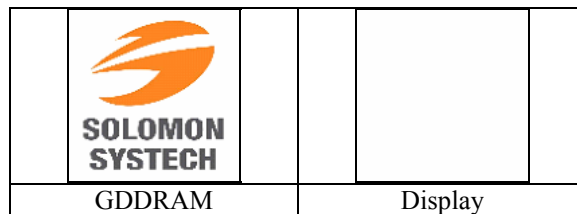
- All OFF (A4h)
Force the entire display to be at gray scale level “GS0” regardless of the contents of the display data RAM as shown in Figure.

Figure 10-7 : Example of Entire Display OFF



- Set Entire Display ON (A5h)
Force the entire display to be at gray scale “GS63” regardless of the contents of the display data RAM as shown in Figure 10-8.

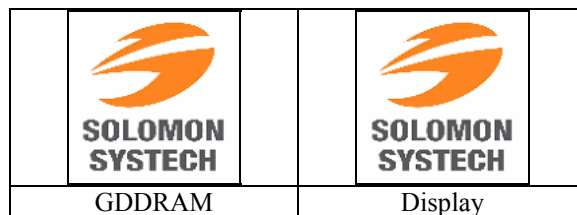
Figure 10-8 : Example of Entire Display ON



- Set Entire Display OFF (A6h)

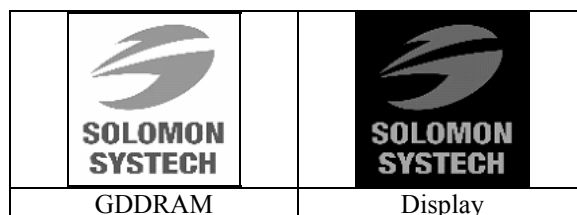
Reset the above effect and turn the data to ON at the corresponding gray level. Figure 10-9 shows an example of Normal Display.

Figure 10-9 : Example of Normal Display



- Inverse Display (A7h)
The gray level of display data are swapped such that “GS0” ↔ “GS63”, “GS1” ↔ “GS62”, ...
Figure 10-10 shows an example of inverse display.

Figure 10-10 : Example of Inverse Display



10.1.9 Set Function selection (ABh)

This double byte command is used to enable or disable the V_{DD} regulator.

Internal V_{DD} regulator is selected when the bit A[0] is set to 1b, while external V_{DD} is selected when A[0] is set to 0b.

10.1.10 Set Sleep mode ON/OFF (AEh / AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.

When the display is OFF (command AEh), the segment is in V_{SS} state and common is in high impedance state.

10.1.11 Set Phase Length (B1h)

This double byte command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 5 to 31 in the unit of 2 DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 3 to 15 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_p .

10.1.12 Display Enhancement (B2h)

This four byte command enhancement display performance.

10.1.13 Set Front Clock Divider / Oscillator Frequency (B3h)

This double byte command consists of two functions:

- Front Clock Divide Ratio (A[3:0])
Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to Section 8.5 for the detail relationship of DCLK and CLK.
- Oscillator Frequency (A[7:4])
Program the oscillator frequency F_{osc} which is the source of CLK if CLS pin is pulled HIGH. The 4-bit value results in 16 different frequency settings being available.

10.1.14 Set GPIO (B5h)

This double byte command is used to set the states of GPIO0 and GPIO1 pins. Refer to Table 9-1 for details.

10.1.15 Set Second Pre-charge period (B6h)

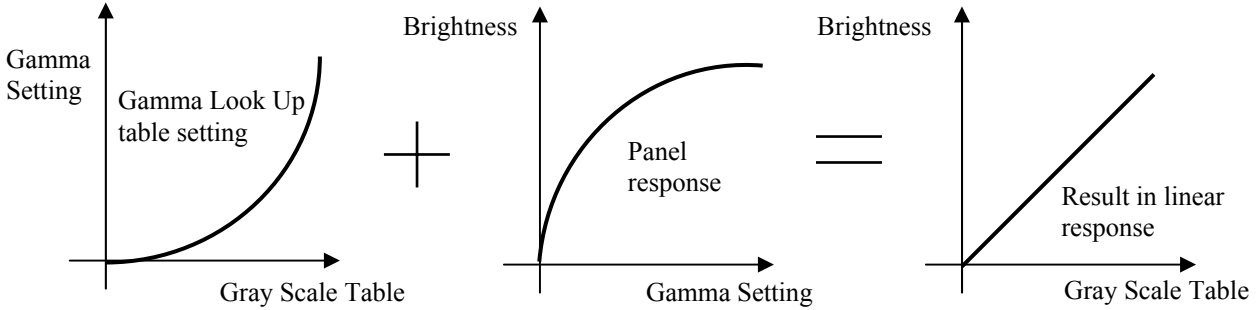
This double byte command is used to set the phase 3 second pre-charge period. The period of phase 3 can be programmed by command B6h and it is ranged from 1 to 15 DCLK's. Please refer to Table 9-1 for the detail information.

10.1.16 Look Up Table for Gray Scale Pulse width (B8h)

This command is used to set each individual gray scale level for the display. Except gray scale levels GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it's turned ON. Following the command B8h, the user has to set the gray scale setting for GS1, GS2, ..., GS62, GS63 one by one in sequence. GS1 can be set as gamma setting 0, which means there is only pre-charge phase but no current drive phase. Refer to Section 8.8 for details.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Since the perception of the brightness scale shall match the image data value in display data RAM, appropriate gray scale table setting like the example shown below (Figure 10-11) can compensate this effect.

Figure 10-11 : Example of Gamma correction by Gamma Look Up table setting



10.1.17 Use Built-in Linear LUT (B9h)

This single byte command reloads the preset linear Gray Scale table as GS0 =Gamma Setting 0, GS1 = Gamma Setting 0, GS2 = Gamma Setting 2, GS3 = Gamma Setting 4,... GS62 = Gamma Setting 122, GS63 = Gamma Setting 124. Refer to Section 8.8 for details.

10.1.18 Set Pre-charge voltage (BBh)

This double byte command sets the first pre-charge voltage (phase 2) level of segment pins. The level of pre-charge voltage is programmed with reference to V_{CC} . Refer to Table 9-1 for details.

10.1.19 Set V_{COMH} Voltage (BEh)

This double byte command sets the high voltage level of common pins, V_{COMH} . The level of V_{COMH} is programmed with reference to V_{CC} . Refer to Table 9-1 for details.

10.1.20 Set Contrast Current for Color A,B,C (C1h)

This command is used to set Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter display.

10.1.21 Master Contrast Current Control (C7h)

This double byte command is to control the segment output current by a scaling factor. The chip has 16 master control steps, with the factor ranges from 1 [0000b] to 16 [1111b – default]. The smaller the master current value, the dimmer the OLED panel display is set.

For example, if original segment output current is 160uA at scale factor = 16, setting scale factor to 8 would reduce the current to 80uA.

10.1.22 Set Multiplex Ratio (CAh)

This double byte command switches default 1:128 multiplex mode to any multiplex mode from 16 to 128. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of “Display Offset” register programmed by command A2h. Figure 10-5 and Figure 10-6 show examples of setting the multiplex ratio through command CAh.

10.1.23 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call “Lock” state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the “Lock” state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the “Lock” state. And the driver IC will then respond to the command and memory access.

11 MAXIMUM RATINGS

Table 11-1 : Maximum Ratings

(Voltage Reference to V_{SS})

| Symbol | Parameter | Value | Unit |
|------------|---------------------------|--------------------------------|------|
| V_{DD} | Supply Voltage | -0.5 to 2.75 | V |
| V_{CC} | | -0.5 to 19.0 | V |
| V_{DDIO} | | -0.5 to V_{CI} | V |
| V_{CI} | | -0.3 to 4.0 | V |
| V_{SEG} | SEG output voltage | 0 to V_{CC} | V |
| V_{COM} | COM output voltage | 0 to $0.9 \cdot V_{CC}$ | V |
| V_{in} | Input voltage | $V_{SS}-0.3$ to $V_{DDIO}+0.3$ | V |
| T_A | Operating Temperature | -40 to +85 | °C |
| T_{stg} | Storage Temperature Range | -65 to +150 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}

$V_{CI} = 2.4$ to $3.5V$ (V_{CI} must be larger than or equal to V_{DD})

$T_A = 25^\circ C$

Table 12-1 : DC Characteristics

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit | |
|------------------|---|--|--|-----|------------------|---------|---------|
| V_{CC} | Operating Voltage | - | 10 | 16 | 18 | V | |
| V_{DD} | Logic Supply Voltage | - | 2.4 | - | 2.6 | V | |
| V_{CI} | Low voltage power supply | - | 2.4 | - | 3.5 | V | |
| V_{DDIO} | Power Supply for I/O pins | - | 1.65 | - | V_{CI} | V | |
| V_{OH} | High Logic Output Level | $I_{out} = 100\mu A$ | $0.9 * V_{DDIO}$ | - | V_{DDIO} | V | |
| V_{OL} | Low Logic Output Level | $I_{out} = 100\mu A$ | 0 | - | $0.1 * V_{DDIO}$ | V | |
| V_{IH} | High Logic Input Level | - | $0.8 * V_{DDIO}$ | - | V_{DDIO} | V | |
| V_{IL} | Low Logic Input Level | - | 0 | - | $0.2 * V_{DDIO}$ | V | |
| I_{SLP_VDD} | V_{DD} Sleep mode Current | $V_{CI} = V_{DDIO} = 2.8V$, $V_{CC} = 16V$ $V_{DD}(\text{external}) = 2.5V$, Display OFF, No panel attached | - | - | 10 | μA | |
| I_{SLP_VDDIO} | V_{DDIO} Sleep mode Current | $V_{CI} = V_{DDIO} = 2.8V$, $V_{CC} = 16V$ Display OFF, No panel attached | External $V_{DD} = 2.5V$ | - | - | 10 | μA |
| | | | Internal V_{DD} | - | - | 10 | μA |
| I_{SLP_VCC} | V_{CC} Sleep mode Current | $V_{CI} = V_{DDIO} = 2.8V$, $V_{CC} = 16V$ Display OFF, No panel attached | External $V_{DD} = 2.5V$ | - | - | 10 | μA |
| | | | Internal V_{DD} | - | - | 10 | μA |
| I_{SLP_VCI} | V_{CI} Sleep mode Current | $V_{CI} = V_{DDIO} = 2.8V$, $V_{CC} = 16V$ Display OFF, No panel attached | External $V_{DD} = 2.5V$ | - | - | 10 | μA |
| | | | Enable Internal V_{DD} during Sleep mode | - | - | 50 | μA |
| | | | Disable Internal V_{DD} during Sleep mode | - | - | 10 | μA |
| I_{DD} | V_{DD} Supply Current | $V_{CI} = V_{DDIO} = 3.5V$, $V_{CC} = 16V$, External $V_{DD} = 2.6V$, Display ON, No panel attached, contrast = FF | - | 170 | 190 | μA | |
| I_{DDIO} | V_{DDIO} Supply Current | $V_{CI} = V_{DDIO} = 3.5V$, $V_{CC} = 16V$, Display ON, No panel attached, contrast = FF | External $V_{DD} = 2.6V$ | - | 0.5 | 10 | μA |
| | | | Internal V_{DD} | - | 0.5 | 10 | μA |
| I_{CI} | V_{CI} Supply Current | $V_{CI} = V_{DDIO} = 3.5V$, $V_{CC} = 16$, Display ON, No panel attached, contrast = FF | External $V_{DD} = 2.6V$ | - | 60 | 70 | μA |
| | | | Internal V_{DD} | - | 255 | 280 | μA |
| I_{CC} | V_{CC} Supply Current | $V_{CI} = V_{DDIO} = 3.5V$, $V_{CC} = 16$, Display ON, No panel attached, contrast = FF | External $V_{DD} = 2.6V$ | - | 1.15 | 1.26 | mA |
| | | | Internal V_{DD} | - | 1.15 | 1.26 | mA |
| I_{SEG} | Segment Output Current Setting $V_{CC} = 16$ at $I_{REF} = 12.5\mu A$ | Contrast = FFh | - | 200 | - | μA | |
| | | Contrast = 7Fh | - | 100 | - | μA | |
| | | Contrast = 3Fh | - | 50 | - | μA | |
| Dev | Segment (SA, SB, SC) output current uniformity (contrast = FF) | $Dev = (I_{Sn} - I_{MID}) / I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN}) / 2$ $I_{Sn} = \text{Segment } n \text{ current}$. e.g. For n=A, then $I_{Sn} = I_{SA} = SA \text{ current}$ | n = A | -3 | - | 3 | % |
| | | | n = B | -3 | - | 3 | |
| | | | n = C | -3 | - | 3 | |
| Adj. Dev | Adjacent pin output current uniformity (contrast = FF) | Adj Dev = $(I_{Sn[m]} - I_{Sn[m+1]}) / (I_{Sn[m]} + I_{Sn[m+1]})$ e.g. For n=A, m=3, then $I_{Sn[m]} = I_{SA[3]} = SA[3] \text{ current}$ | n = A | -2 | - | 2 | % |
| | | | n = B | -2 | - | 2 | |
| | | | n = C | -2 | - | 2 | |

13 AC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}

T_A = 25°C

Table 13-1 : AC Characteristics

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---------------------------------|---|---|------|---|-----|------|
| F _{OSC} ⁽¹⁾ | Oscillation Frequency of Display Timing Generator | V _{CI} = 2.8V | 2.5 | 2.8 | 3.1 | MHz |
| FFRM | Frame Frequency for 128 MUX Mode | 128x128 Graphic Display Mode, Display ON, Internal Oscillator Enabled | - | F _{OSC} * 1/(D*K*128) ⁽²⁾ | - | Hz |
| t _{RES} | Reset low pulse width (RES#) | - | 2000 | - | - | ns |

Note

⁽¹⁾ F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4] is in default value, and B3h A[3:0] is in [0001].

⁽²⁾ D: divide ratio set by command B3h A[3:0]

K: Phase 1 period +Phase 2 period + X

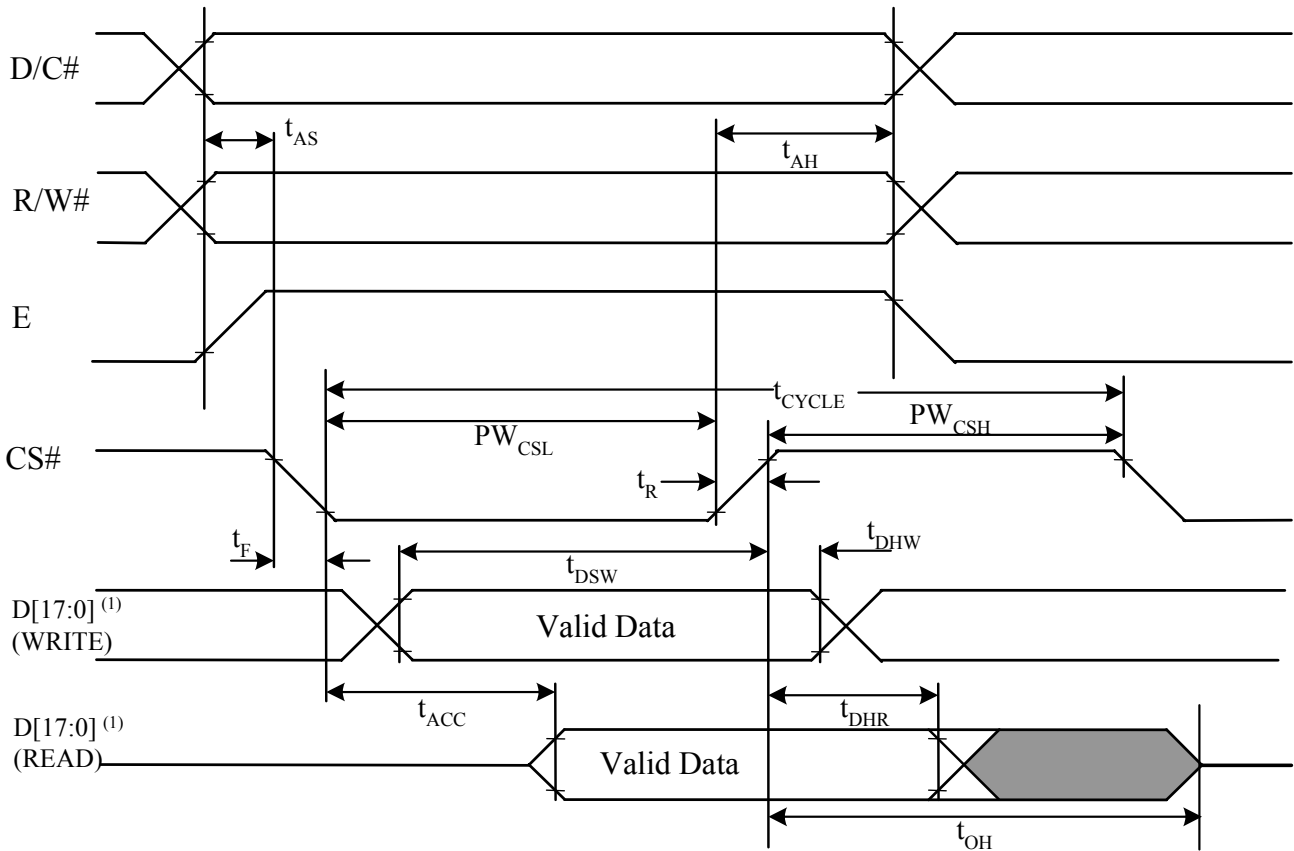
X: DCLKs in current drive period

Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

($V_{DDIO} - V_{SS} = 1.65V - V_{CI}$, $V_{CI} - V_{SS} = 2.4-3.5V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--------------------------------------|-----|-----|-----|------|
| t_{CYCLE} | Clock Cycle Time (read) | 320 | - | - | ns |
| | Clock Cycle Time (write) | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 24 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 7 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| PW_{CSL} | Chip Select Low Pulse Width (read) | 120 | - | - | ns |
| | Chip Select Low Pulse Width (write) | 60 | - | - | ns |
| PW_{CSH} | Chip Select High Pulse Width (read) | 60 | - | - | ns |
| | Chip Select High Pulse Width (write) | 60 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

Figure 13-1 : 6800-series MCU parallel interface characteristics



Note

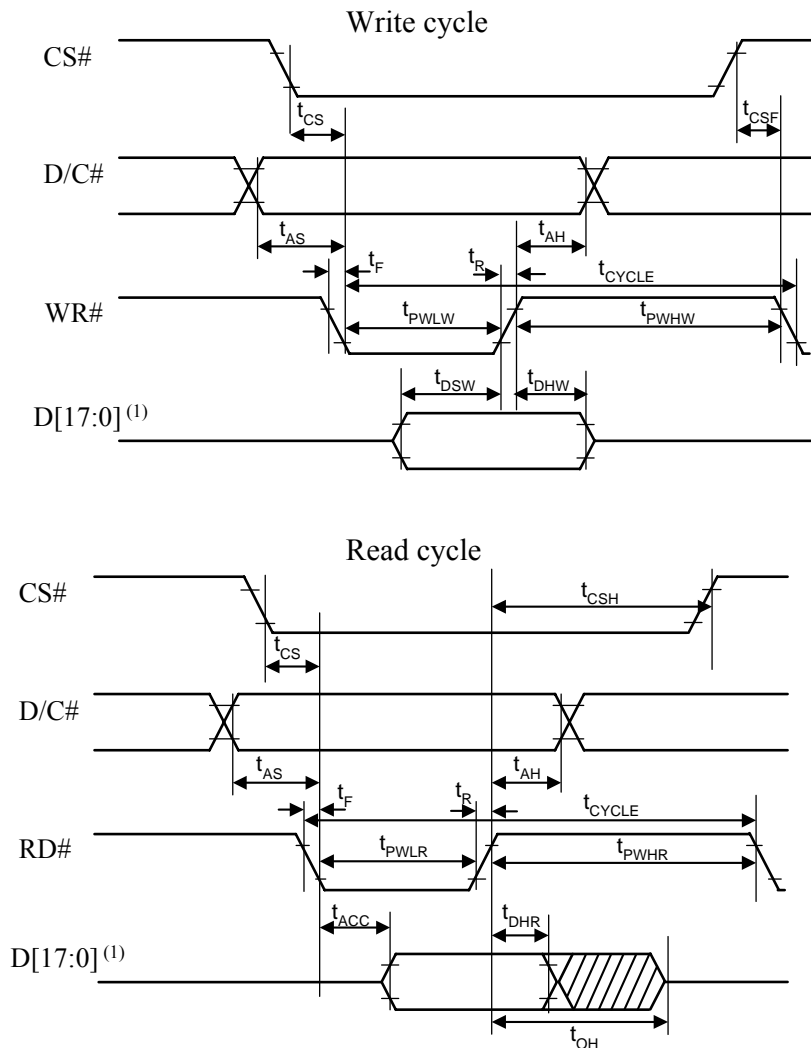
⁽¹⁾ when 8 bit used: D[7:0] instead; when 16 bit used: D[15:0] instead; when 18 bit used: D[17:0] instead.

Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics

($V_{DDIO} - V_{SS} = 1.65V - V_{CI}$, $V_{CI} - V_{SS} = 2.4-3.5V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--------------------------------------|-----|-----|-----|------|
| t_{CYCLE} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 10 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 7 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 46 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| t_{PWLR} | Read Low Time | 150 | - | - | ns |
| t_{PWLW} | Write Low Time | 60 | - | - | ns |
| t_{PWHR} | Read High Time | 60 | - | - | ns |
| t_{PWHW} | Write High Time | 60 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |
| t_{CS} | Chip select setup time | 0 | - | - | ns |
| t_{CSH} | Chip select hold time to read signal | 0 | - | - | ns |
| t_{CSF} | Chip select hold time | 20 | - | - | ns |

Figure 13-2 : 8080-series MCU parallel interface characteristics



Note

⁽¹⁾ when 8 bit used: D[7:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

Table 13-4 : Serial Interface Timing Characteristics (4-wire SPI)

($V_{DDIO} - V_{SS} = 1.65V - V_{CL}$, $V_{CI} - V_{SS} = 2.4-3.5V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 220 | - | - | ns |
| t_{AS} | Address Setup Time | 15 | - | - | ns |
| t_{AH} | Address Hold Time | 42 | - | - | ns |
| t_{CSS} | Chip Select Setup Time | 20 | - | - | ns |
| t_{CSH} | Chip Select Hold Time | 10 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 15 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 20 | - | - | ns |
| t_{CLKL} | Clock Low Time | 20 | - | - | ns |
| t_{CLKH} | Clock High Time | 20 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

Figure 13-3 : Serial interface characteristics (4-wire SPI)

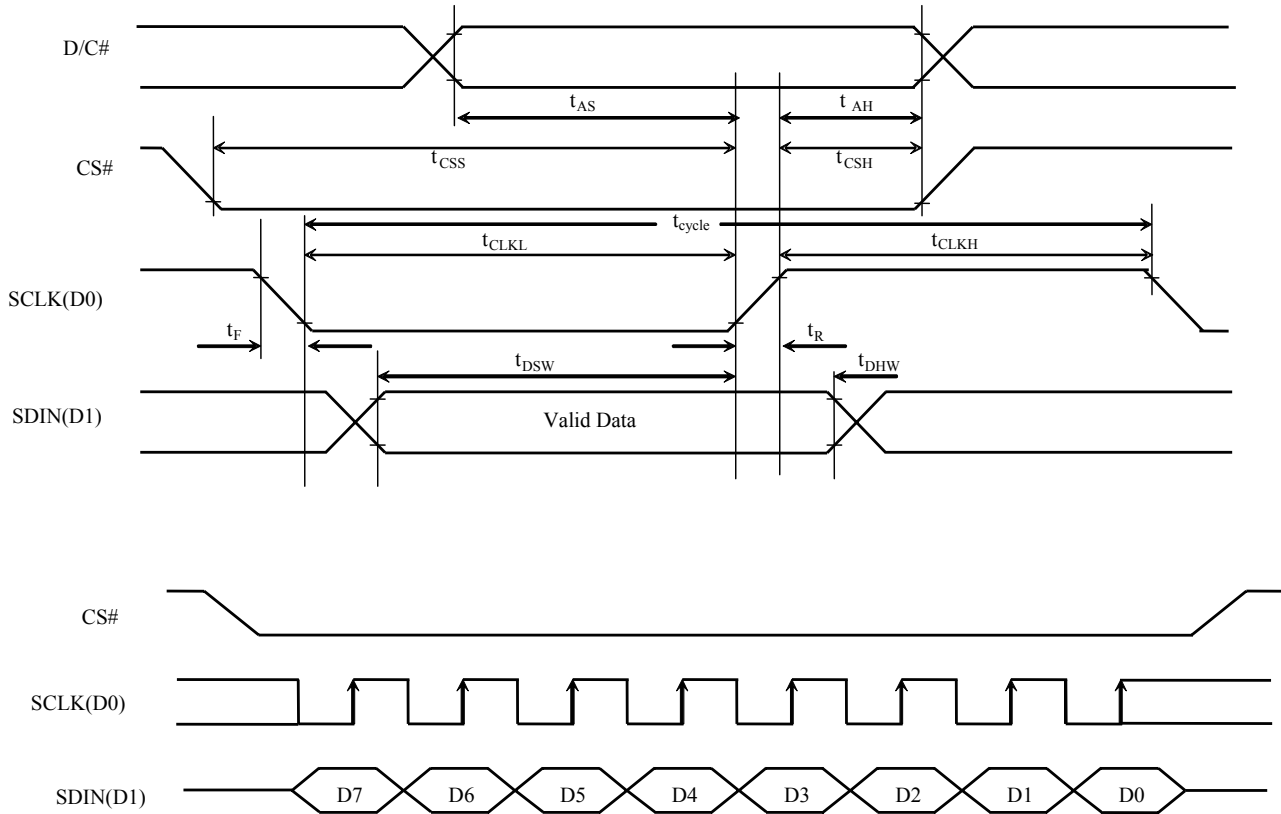
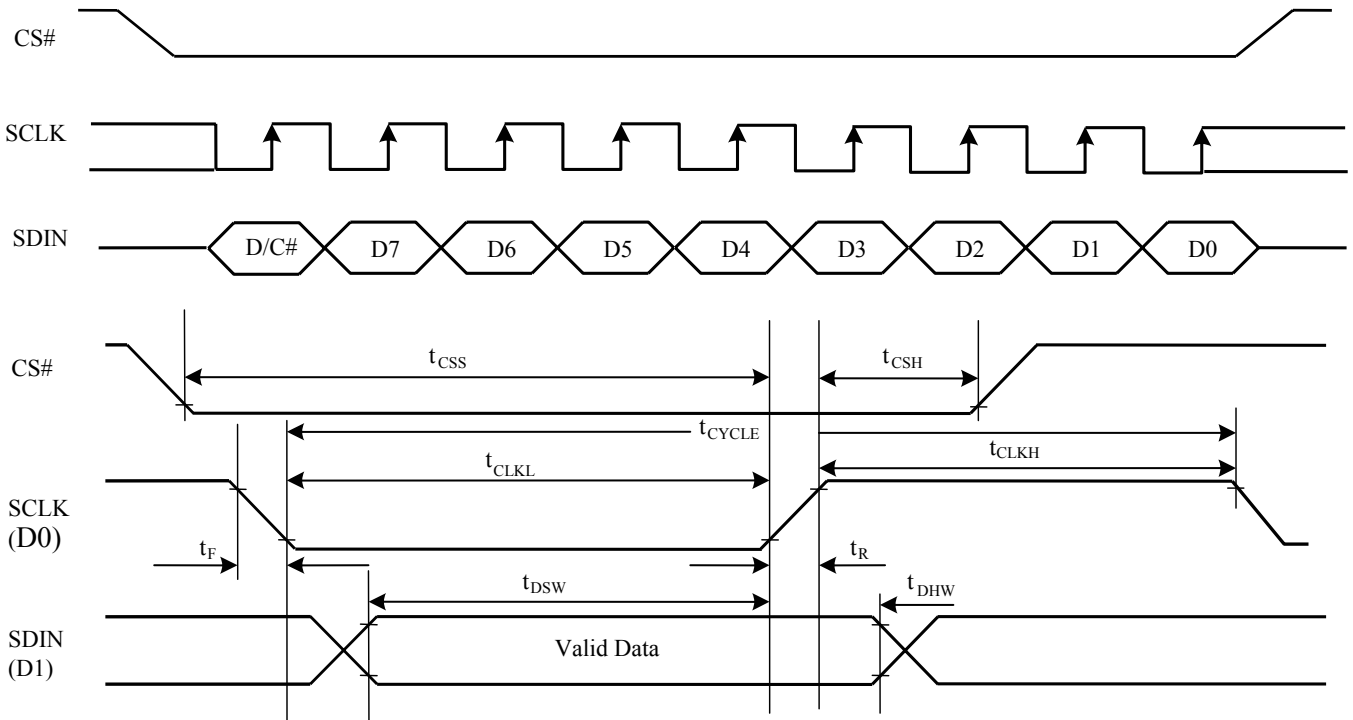


Table 13-5 : Serial Interface Timing Characteristics (3-wire SPI)

($V_{DDIO} - V_{SS} = 1.65V - V_{CL}$, $V_{CI} - V_{SS} = 2.4-3.5V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 220 | - | - | ns |
| t_{CSS} | Chip Select Setup Time | 20 | - | - | ns |
| t_{CSH} | Chip Select Hold Time | 44 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 15 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 20 | - | - | ns |
| t_{CLKL} | Clock Low Time | 20 | - | - | ns |
| t_{CLKH} | Clock High Time | 20 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

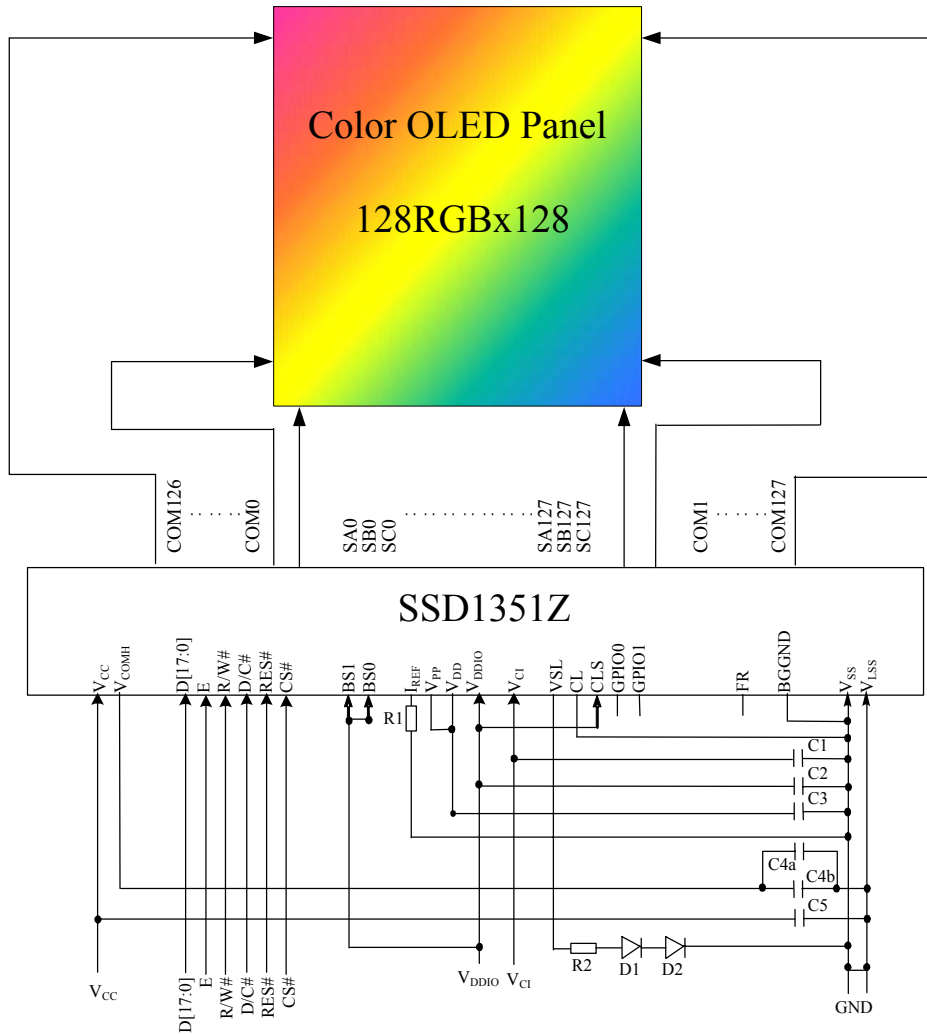
Figure 13-4 : Serial interface characteristics (3-wire SPI)



14 APPLICATION EXAMPLE

Figure 14-1 : SSD1351Z application example for 18-bit 6800-parallel interface mode (Internal regulated V_{DD})

The configuration for 18-bit 6800-parallel interface mode is shown in the following diagram:
 (V_{CI} = 3.3V (V_{CI} must be > 2.6V), Internal regulated V_{DD}, V_{DDIO} = 1.8V, external V_{CC} = 16V, I_{REF} = 12.5uA,
 BS[3:2] are set to 11b through command A0h)



Voltage at I_{REF} = V_{CC} - 6V. For V_{CC} = 16V, I_{REF} = 12.5uA:

$$R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF}$$

$$= (16-6) / 12.5\mu$$

$$= 800K\Omega$$

$$R2 = 50\Omega, 1/8W^{(1)}$$

$$D1 \sim D2: V_{th}=0.7V, 1N4148^{(1)}$$

$$C1 \sim C3: 1\mu F, C4a, C5: 4.7\mu F, C4b: 0.1\mu F^{(1)}$$

Note

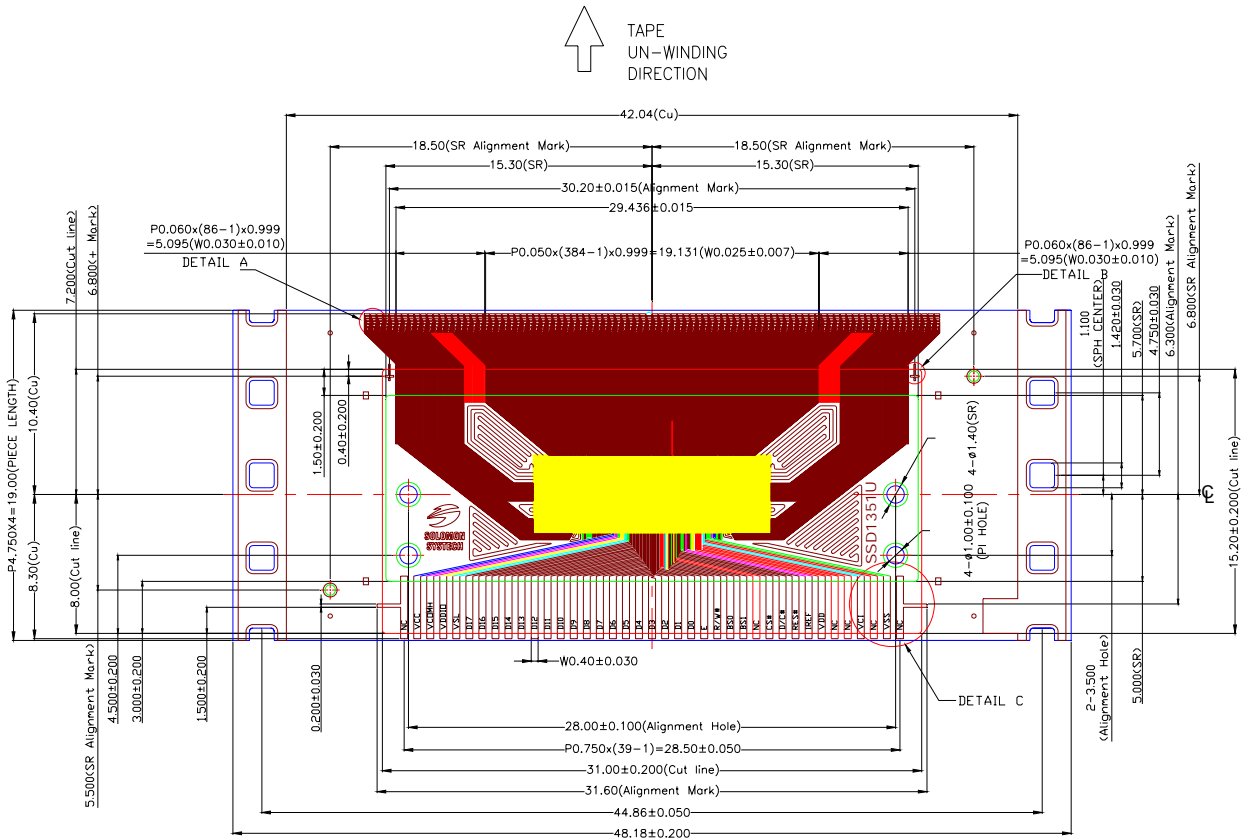
⁽¹⁾ The values are recommended value. Select appropriate value against module application.

⁽²⁾ It is recommended to tie V_{LSS} and V_{SS} at one common ground point to minimize circulating ground noise.

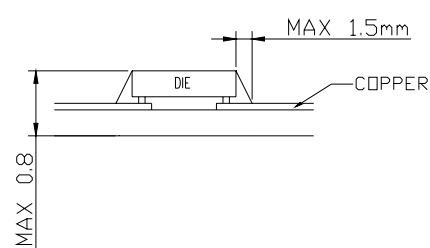
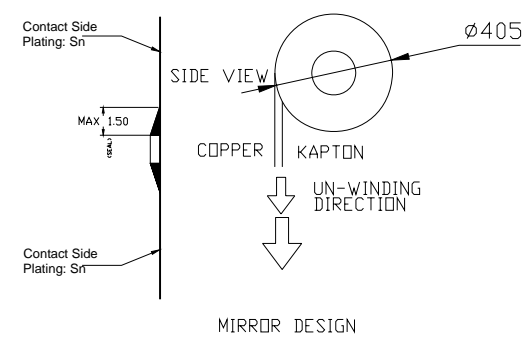
15 PACKAGE INFORMATION

15.1 SSD1351UR1 detail dimension

Figure 15-1: SSD1351UR1 Detail Dimension

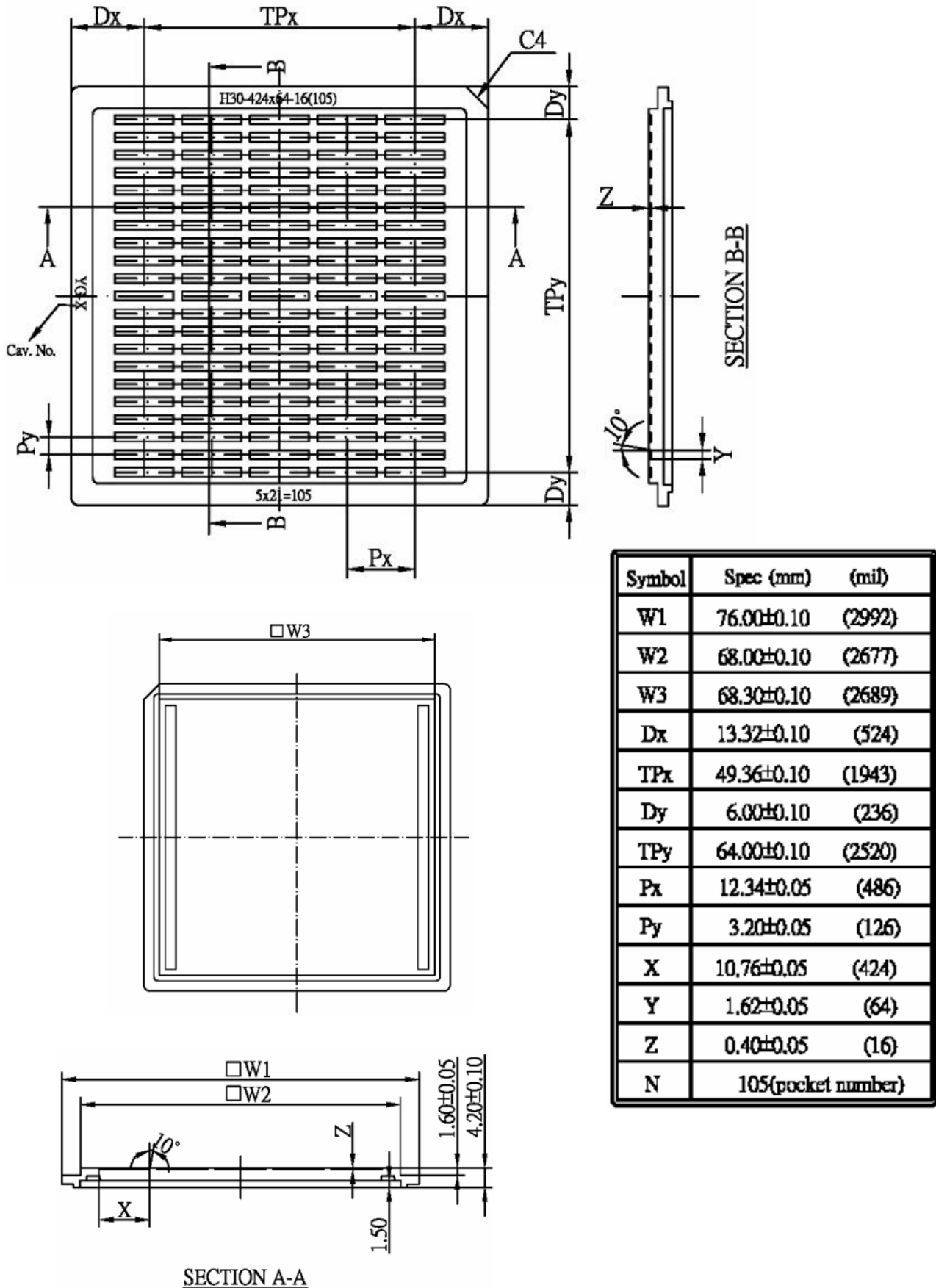


- NOTE:
1. GENERAL TOLERANCE: $\pm 0.050\text{mm}$
 2. MATERIAL
 PI: $38 \pm 4\mu\text{m}$
 CU: $8 \pm 2\mu\text{m}$
 SR: $15 \pm 10\mu\text{m}$
 (OTHER TOLERANCE: $\pm 0.200\text{mm}$)
 3. SN PLATING: $0.160 \pm 0.050\mu\text{m}$
 4. TAPESIZE: 4 SPH, 19.00mm



15.2 SSD1351Z Die Tray Information

Figure 15-2: SSD1351UR1 Die Tray Information



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