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人机界面整合者

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ST7102

Datasheet

V0.22

2024/10

Sitronix Technology Corporation

LIST OF CONTENT

1 GENERAL DESCRIPTION

The ST7102 is a System-on-Chip (SoC) driver LSI designed for TFT LCD controller with a build-in touch panel controller and suitable for small to medium size portable devices such as mobile phone or tablet. ST7102 can support up to 480RGBx1280 dots panel and support 16,777,216-color. There is no internal RAM in ST7102. The 1440-channel source driver has true 8-bit resolution, which generates 256 Gamma-corrected values by an internal D/A converter.

The ST7102 incorporates with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver. The built-in timing controller in ST7102 can support MIPI interface (included 4-lane/1-port) and RGB interface display serial interface with low EMI noise and touch protocol via standard integrated circuit bus(I^2C) or serial peripheral interface (SPI). The ST7102 also supports a standby mode for power control consideration. For further power control, the dynamic backlight control function basing on displaying image content is also supported.

2 FEATURES

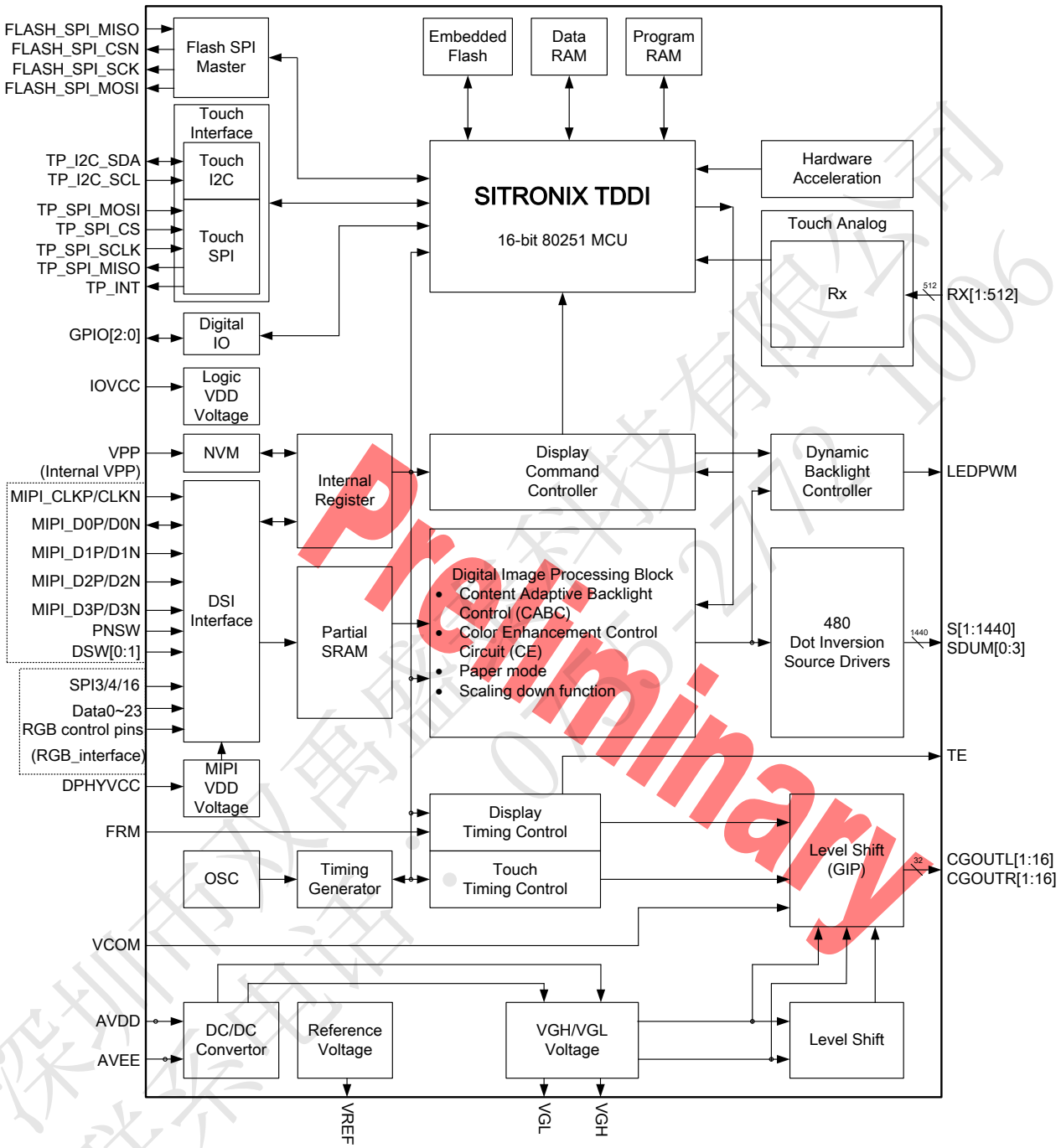
- Single-chip FWVGA Amorphous TFT Controller/Driver.
- Display Resolution
  - 480RGB(H) x 864(V) (WVGA)
  - 480RGB(H) x 960(V) (FWVGA)
  - 480RGB(H) x 1280(V)
- Display Modes (Color Mode)
  - Full Color: 16M, RGB=(888) max. Idle Mode Off
  - Color Reduce: 8-color, RGB=(111), Idle Mode On
- System Interfaces
  - MIPI DSI: MIPI DSI (DSI v1.01.00, D-PHY v1.00.00 and DCS v1.01)
  - 16/18/24 RGB interface (with 8bits / 9bits command interface)
- Display Features
  - Outputs 256γ-corrected values using an internal true 8-bit resolution D/A converter to achieve 16,777,216 colors
  - Supports CGOUTR[1:16]/CGOUTL[1:16] GIP control signal
  - Individual gamma correction setting for RGB dots (1 analog/ 3 digital gamma)
  - Supports column/1-dot/2-dot/4-dot inversion
  - Power saving mode (standby mode)
  - Supports low frame rate mode
- Built-in Color Image Processing Functions
  - Support WB function
  - Color enhance (CE 2.0)
  - Content adaptive brightness control (CABC 2.0)
- On Chip Function
  - Support VCOM ground level driving scheme
  - Internal oscillator for display clock generation
  - Timing controller
  - Built–in NVM to store VCOM/GVDD calibration and ID1~ID3
  - Built–in NVM to store analog gamma, digital gamma and color enhancement.
  - Built–in NVM to store panel timing, analog power setting, and etc.
- Supply Power Range
  - Logic power supply voltage (IOVCC): 1.65 ~ 3.3V
  - Positive analog power supply voltage (AVDD): 4.5 ~ 6.3V
  - Negative analog power supply voltage (AVEE): -4.5 ~ -6.3V
- Touch Feature

- 16-bits MCU optimized for capacitive sensing and other human interactions
- 64 analog front ends (AFEs) support up to 512 receiver pads
- Supports I2C and SPI protocol for communication with the host
- 64 analog front ends (AFEs) support up to 512 receiver pads
- 10 fingers support
- Support Long-V sensing mode
- Support noise detection and automatic frequency hopping
- Support passive stylus
- Support proximity
- Hopping frequency range from 50kHz to 120kHz to minimize noise interference
- High signal- to noise ratio (>50dB SNR) touch AFE enables
- Wake-up gesture
- Touch FW host download

- Optimized Layout for COG Assembly
- Operating Temperature Range: −30ºC to +75 ºC

3 BLOCK DIAGRAM

3.1 Function Block



4 PIN INFOMATION

4.1 Pad Arrangement

- **Chip Information**

Chip size	22500um x 918um
Chip height & width tolerance	20um
Chip thickness	250um
Pad Location	Pad center
Coordinate Origin	Chip center

Note:

Chip size do not include scribe line

4.2 Pin Definition

4.2.1 Voltage Pins

Name	I/O	PAD Type (Voltage Level)	Description
IOVCC	I	Power Supply	External power supply for internal logic circuit
AVDD	I	Power Supply	External positive power supply for analog circuit
AVEE	I	Power Supply	External negative power supply for analog circuit
AGND	-	GND	Analog ground, need to connect to GND from FPC
DGND	-	GND	Digital ground, need to connect to GND from FPC
VSS	--	GND	TP ground, need to connect to GND from FPC
DPHYGND	-	GND	Ground for MIPI DPHY circuit, need to connect to GND from FPC
VDD	O	Analog	Regulator output for logic, all pins need to connect together from FPC
VDDM	O	Analog	Regulator output for MIPI DSI,please keep it open
DPHYVCC	I	Analog	External power supply for MIPI PHY circuit This pin need connect to IOVCC from FPC
TVH	O	Analog	Touch output high voltage level, all pins need to connect together from FPC.
TVL	O	Analog	Touch output low voltage level, all pins need to connect together from FPC.
VAG	O	Analog	Active guard signal, all pins need to connect together from FPC. For IGZO panel, VGH/VGHO1/VGL need have capacitor to VAG
VGH	O	Analog	Step-up output voltage for panel, all pins need to connect together from FPC.
VGHO1	O	Analog	Step-up output voltage, all pins need to connect together from FPC.
VGL	O	Analog	Step-up output voltage for panel, all pins need to connect together from FPC.
VGLI	O	Analog	For Test used, please keep it open
GVDDP	O	Analog	Positive LDO output for gamma circuit. If not used, please keep it open.
GVDDN	O	Analog	Negative LDO output for gamma circuit. If not used, please keep it open.
VPP	I/O	Analog	Programming OTP Power. Internal power : keep it open. External power :supply voltage (8.5V); the current of Ivpp must be more than 10mA.

4.2.2 Control Pins

<table>
<tr><th>Name</th><th>I/O</th><th>PAD Type
(Voltage Level)</th><th>Description</th></tr>
<tr><td>RESX</td><td>I</td><td>Digital(IOVCC)</td><td>Global reset signal. Low active.</td></tr>
<tr><td>IM[2:0]</td><td>I</td><td>Digital(IOVCC)</td><td>Interface mode select pins
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface Selection</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>MIPI</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>RGB(video)+SPI9 control</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>RGB(video)+SPI8 control</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>RGB(video)+SPI16 (rise) control</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>RGB(video) +SPI16 (fall) control</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>LANSEL[1:0]</td><td>I</td><td>Digital(IOVCC)</td><td>Input pin to select 1 data lane to 4 data lanes in MIPI interface.
<table>
<tr><th>Lanesel 1</th><th>Lanesel 0</th><th>Interface Selection</th></tr>
<tr><td>0</td><td>0</td><td>1 Lane</td></tr>
<tr><td>0</td><td>1</td><td>2 Lanes</td></tr>
<tr><td>1</td><td>0</td><td>3 Lanes</td></tr>
<tr><td>1</td><td>1</td><td>4 Lanes</td></tr>
</table></td></tr>
<tr><td>TE</td><td>O</td><td>Digital(IOVCC)</td><td>Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command. When this pin is not activated (TE function OFF), this pin is GND level.</td></tr>
<tr><td>LEDPWM</td><td>O</td><td>Digital(IOVCC)</td><td>LCD backlight control PWM output pin</td></tr>
<tr><td>FRM</td><td>I</td><td>Digital(IOVCC)</td><td>Test pin, please connect to ground or floating.</td></tr>
<tr><td>PSWAP</td><td>I</td><td>Digital(IOVCC)</td><td>MIPI Lane polarity swap pin.</td></tr>
</table>

<table>
<tr><td>DSWAP[1:0]</td><td>I</td><td>Digital(IOVCC)</td><td>MIPI data lane swap and polarity swap table.
<table>
<tr><th>PNSWAP</th><th>DSWAP[1:0]</th><th>D2P</th><th>D2N</th><th>D1P</th><th>D1N</th><th>CLKP</th><th>CLKN</th><th>D0P</th><th>D0N</th><th>D3P</th><th>D3N</th></tr>
<tr><td rowspan="4">0</td><td>00</td><td>D3N</td><td>D3P</td><td>D2N</td><td>D2P</td><td>CLKN</td><td>CLKP</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td></tr>
<tr><td>01</td><td>D3N</td><td>D3P</td><td>D0N</td><td>D0P</td><td>CLKN</td><td>CLKP</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td></tr>
<tr><td>10</td><td>D0N</td><td>D0P</td><td>D1N</td><td>D1P</td><td>CLKN</td><td>CLKP</td><td>D2N</td><td>D2P</td><td>D3N</td><td>D3P</td></tr>
<tr><td>11</td><td>D2N</td><td>D2P</td><td>D1N</td><td>D1P</td><td>CLKN</td><td>CLKP</td><td>D0N</td><td>D0P</td><td>D3N</td><td>D3P</td></tr>
<tr><td rowspan="4">1</td><td>00</td><td>D3P</td><td>D3N</td><td>D2P</td><td>D2N</td><td>CLKP</td><td>CLKN</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td></tr>
<tr><td>01</td><td>D3P</td><td>D3N</td><td>D0P</td><td>D0N</td><td>CLKP</td><td>CLKN</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td></tr>
<tr><td>10</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>CLKP</td><td>CLKN</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td></tr>
<tr><td>11</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>CLKP</td><td>CLKN</td><td>D0P</td><td>D0N</td><td>D3P</td><td>D3N</td></tr>
</table></td></tr>
<tr><td>SDO</td><td>O</td><td>IOVCC</td><td>RGB/MIPI SPI9, RGB/MIPI SPI8, RGB/MIPI SP16 output data Pin.
-If not used, please floating</td></tr>
<tr><td>SDA</td><td>I</td><td>IOVCC</td><td>RGB/MIPI SPI9, RGB/MIPI SPI8, RGB/MIPI SP16 input data Pin.
-If not used, please fix this pin at GND or IOVCC.</td></tr>
<tr><td>DCX</td><td>I</td><td>IOVCC</td><td>- The 8 bit SPI interface (DCX): The signal for command or parameter select. Low: Command High: Parameter
-If not used, please fix this pin at IOVCC or GND.</td></tr>
<tr><td>CSX</td><td>I</td><td>IOVCC</td><td>RGB/MIPI SPI9, RGB/MIPI SPI8, RGB/MIPI SP16 Chip select pin.
CSX=’0’ : Low enable.
CSX=’1’ : High disable
-If not used, please fix this pin at IOVCC.</td></tr>
<tr><td>SCL</td><td>I</td><td>IOVCC</td><td>RGB/MIPI SPI9, RGB/MIPI SPI8, RGB/MIPI SP16 CLK Pin.
-If not used, please fix this pin at IOVCC.</td></tr>
</table>

4.2.3 MIPI Interface Pins

Name	I/O	PAD Type (Voltage Level)	Description
CLKP	I	MIPI	MIPI-DSI clock lane positive-end input pin
CLKN	I	MIPI	MIPI-DSI clock lane negative-end input pin
DATA0P	I/O	MIPI	MIPI-DSI data lane 0 positive-end input/output pin * Please connected to GND if not used
DATA0N	I/O	MIPI	MIPI-DSI data lane 0 negative-end input/output pin * Please connected to GND if not used
DATA1P	I	MIPI	MIPI-DSI data lane 1 positive-end input pin * Please connected to GND if not used
DATA1N	I	MIPI	MIPI-DSI data lane 1 negative-end input pin * Please connected to GND if not used.
DATA 2P	I	MIPI	MIPI-DSI data lane 2 positive-end input pin * Please connected to GND if not used
DATA 2N	I	MIPI	MIPI-DSI data lane 2 negative-end input pin * Please connected to GND if not used
DATA 3P	I	MIPI	MIPI-DSI data lane 3 positive-end input pin * Please connected to GND if not used
DATA 3N	I	MIPI	MIPI-DSI data lane 3 negative-end input pin * Please connected to GND if not used

4.2.4 RGB Interface Pins

Name	I/O	PAD Type (Voltage Level)	Description
D0~D23	I	IOVCC	RGB interface data bus. -If not used, please fix this pin at GND or IOVCC.
ENABLE	I	IOVCC	Data enable signal in RGB interface. -If not used, please fix this pin at IOVCC or Gnd.
PCLK	I	IOVCC	Dot clock signal in RGB interface. (DOTCLK) -If not used, please fix this pin at IOVCC or Gnd
HSYNC	I	IOVCC	-Horizontal (Line) synchronizing input signal in RGB interface. -If not used, please fix to the IOVCC or Gnd.
VSYNC	I	IOVCC	Vertical (Frame) synchronizing input signal in RGB interface. -If not used, please fix to the IOVCC. or Gnd

4.2.5 Driver Panel Related Pins

Name	I/O	PAD Type (Voltage Level)	Description
CGOUTL[16:1]	O	Analog	Panel control signal output pads for left side GIP.
CGOUTR[16:1]	O	Analog	Panel control signal output pads for right side GIP.
S1:S1440	O	Analog	Output source driver signals. The D/A converted 256-gray-scale analog voltage is output.
VCOM	O	Analog	VCOM voltage output, for monitor
COGTEST12 COGTEST34	O	No level	For ITO resistance trace, if not use please floating
VCOM_PASS_R VCOM_PASS_L	-	No level	Pass line for VCOM_OPT If use, connect to VCOM_OPT
VCOM_OPT_R VCOM_OPT_L	O	Analog	VCOM optional buffer output. (Connect to Panel Vcom)

4.2.6 Touch Related Pins

Name	I/O	PAD Type (Voltage Level)	Description
TP_RESX	I	Digital(IOVCC)	External reset for TP
TP_UART_TX	I/O	Digital(IOVCC)	-UART TX pad. -If not used, please let this pin open.
TP_INT	O	Digital(IOVCC)	-Touch screen interrupt. -If not used, please let this pin open.
TP_I2C_SDA	I/O	Digital(IOVCC)	-I2C interface data pin. -If not used, please let this pin open.
TP_I2C_SCL	I	Digital(IOVCC)	-I2C interface clock pin. -If not used, please let this pin open.
TP_SPI_CS	I	Digital(IOVCC)	Slave chip select pin in SPI interface -If not used, please fix this pin at IOVCC
TP_SPI_MISO	O	Digital(IOVCC)	Slave input data pin in SPI interface -If not used, please let this pin open.
TP_SPI_MOSI	I	Digital(IOVCC)	Slave output data pin in SPI interface -If not used, please let this pin open.
TP_SPI_SCL	I	Digital(IOVCC)	Slave clock pin in SPI interface -If not used, please let this pin open.

FLASH_HOLD	O	Digital(IOVCC)	Hold signal to flash. -If not used, please let this pin open.
FLASH_WP	O	Digital(IOVCC)	Write protect signal to flash. -If not used, please let this pin open.
FLASH_CS	O	Digital(IOVCC)	Master chip select in SPI interface -If not used, please let this pin open.
FLASH_MISO	I	Digital(IOVCC)	Master input data in SPI interface, If not used, please let this pin open
FLASH_MOSI	O	Digital(IOVCC)	Master output data in SPI interface, If not used, please let this pin open
FLASH_SCL	I	Digital(IOVCC)	Master clock signal in SPI interface, If not used, please let this pin open
RX[512:1]	O	Analog	Output RX signals.
TP_OPT_1	I	Digital(IOVCC)	-Boot From Flash Pin , TP_OPT_1P ='0' : Host download. TP_OPT_1P ='1' : Flash Boot.
IM_SPI	I	Digital(IOVCC)	IM_SPI: "0" SPI mode 0/3 (normal using , SCK rising edge trigger) IM_SPI: "1" SPI mode 1/2 (SCK falling edge trigger)

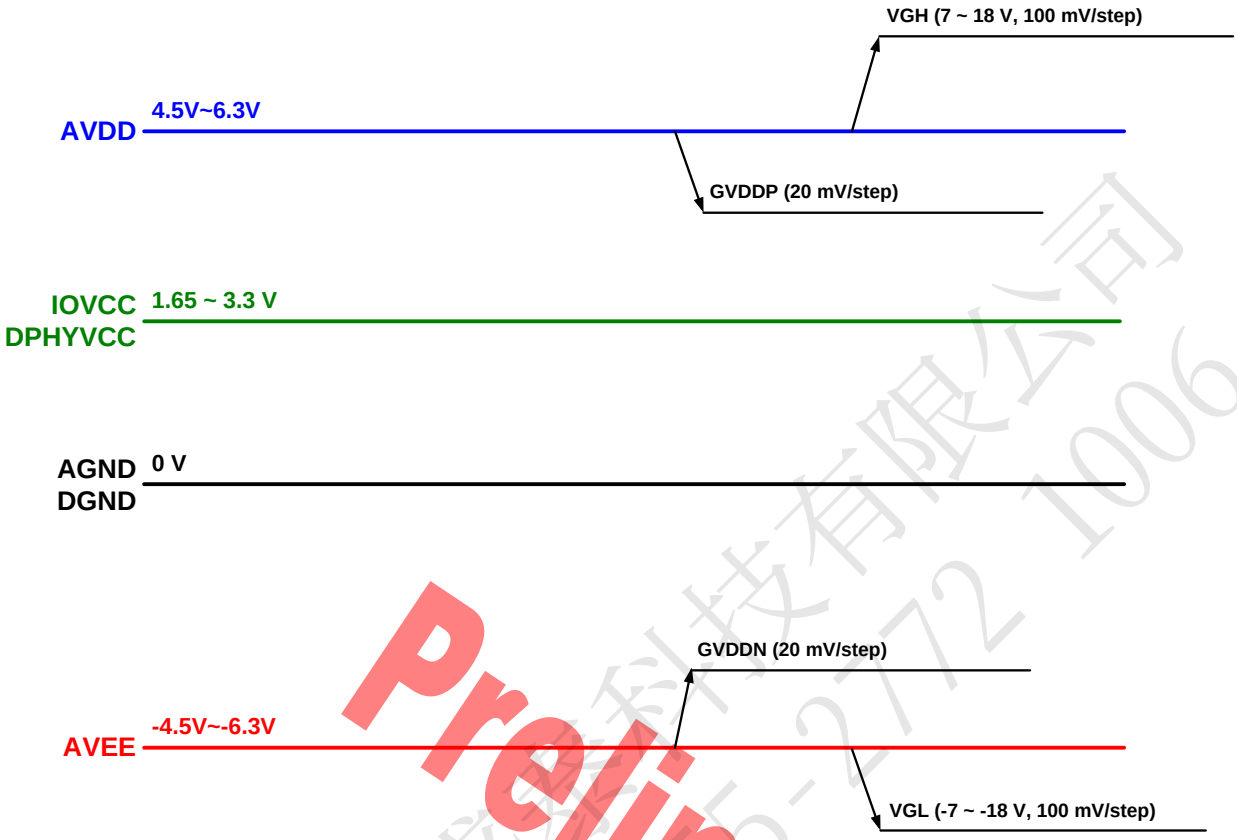
4.2.7 External power Supply Pins

Nami	I/O	PAD Type (Voltage Level)	Description
VCI	I	Power Suppl)	Connect to external power IC level (VCSW1 & VCSW2 output level)
PWR_MODE	I	VCI	-Power Mode Selectn Normal:"1" IOVCC External :"0" GND (when used VCSW1& VCSW2)
VCSW1/VCSW2	O	VCI	VCSW1/VCSW2 CLK Out Pin, connect to external power IC

4.2.8 Other

Name	I/O	PAD Type (Voltage Level)	Description
RST_OR_ENB	I	IOVCC	For text, connect to IOVCC or Floating.
SWIRE	O	IOVCC	Let it open.

4.3 Power Supply Configuration



5 FUNCTION DESCRIPTION

5.1 Frame Tearing Effect Interface

The Tearing Effect output can be show the synchronize status with MPU (Host). This signal can be enabled or disabled by the TE off & on commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command.

Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only (Figure 1):

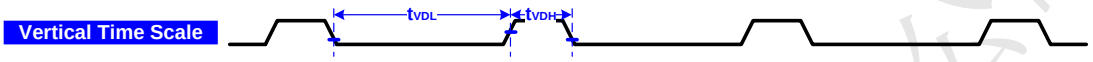


Figure 1 Mode1

tVDH= The LCD display is not updated video signal.

tVDL= The LCD display is updated video signal

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 800 H-sync pulses per field. (Figure 2)

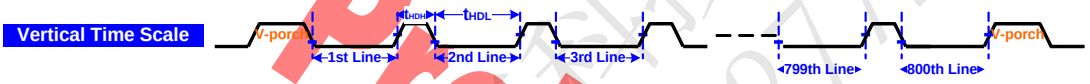


Figure 2 Mode2

tHDH= The LCD display is not updated video signal.

tHDL= The LCD display is updated f video signal.

Mode3, in this mode, the tearing effect output when the display reaches line N. The output signal length of the high level is one line period. In below figure, it shows the TE pulse that can be select from 1st line to 800th line by CMD44h.P1 and CMD44.P2 (Figure 3)

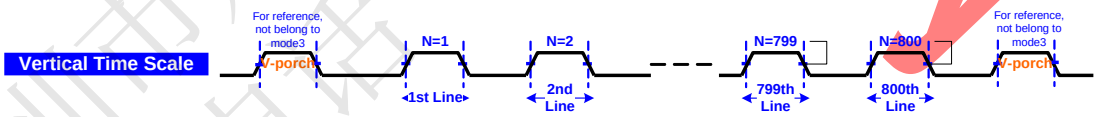


Figure 3 Mode3

CMD 35h	CMD 44h	TE output
TEM	TESN	
0	0	TE high in V-porch region (mode1)
1	0	TE high in all V-porch and H-porch region (mode2)
0	≠0	TE high at N-th line (mode3)
1	≠0	Same as mode2

Where mode1, mode2 and mode3 timing chart is shown in below (Figure 4):

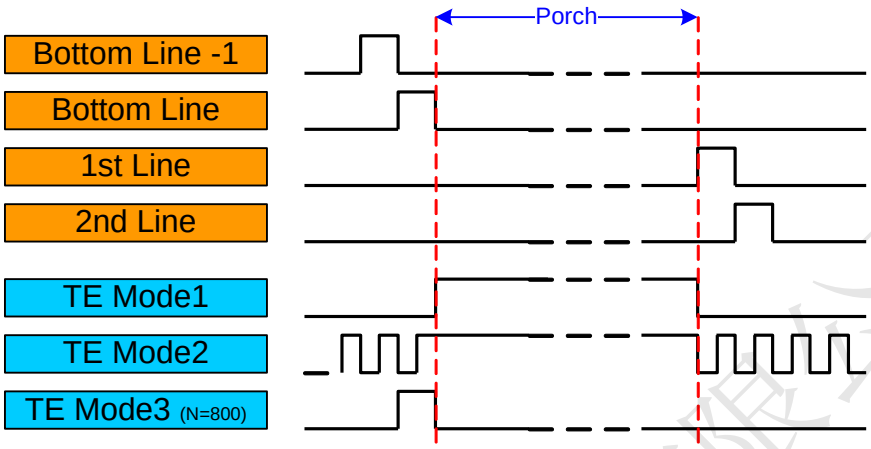


Figure 4 TE Mode

Note: during sleep in mode, the Tearing output pin is active low.l

5.2 Content Adaptive Backlight Control (CABC2.0)

5.2.1 Definition of CABC

A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content gray level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted gray level scale and thus the power consumption reduction

Definition of Modes and target power reduction ratio:

Off mode: Content Adaptive Brightness Control functionality is totally off.

UI [User Interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less.

Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%.

Moving image mode: Optimized for moving image. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%.

	Off ode	UI image mode	Still picture mode	Moving image mode
Power Reduction	0%	10% or Less	More than 30%	More than 30%
Image Quality	Best	Approaching Best	Some image degradation	Some image degradation

Note 1: Updating partial area of the image data should be supported by CABC functionality.
Note 2: Processing power consumption of CABC should be minimized.
Note 3: Customer need program NVM GAMMA when using CABC.

The transition time for dimming function is illustrated below.

- Content Adaptive Brightness Control

Display brightness is changed, according to the image contents. The following graph mentions the case of displaying three different images.

- Image A: -20% brightness reduction
- Image B: -30% brightness reduction
- Image C: -10% brightness reduction

Transition time from the previous image to the current displayed image is “transition time A”.

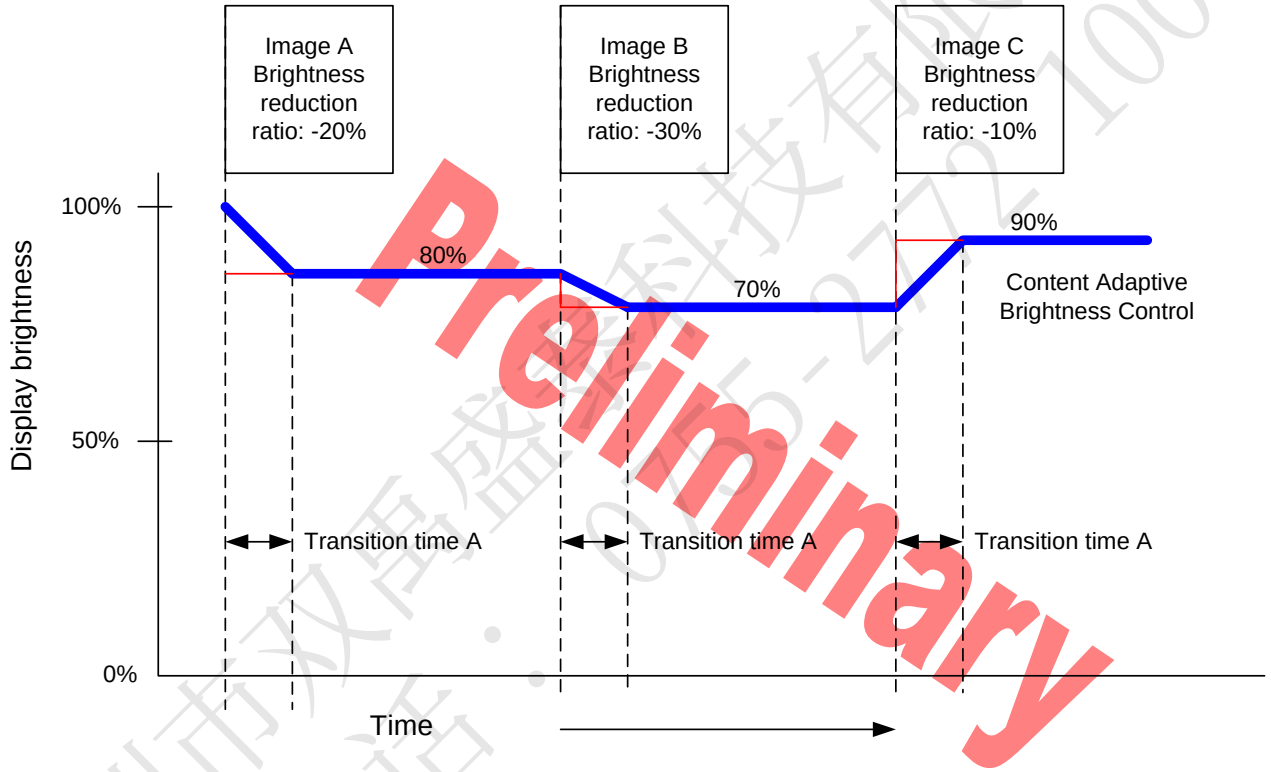


Figure 5 Transition time A

- Manual brightness setting and Dimming function

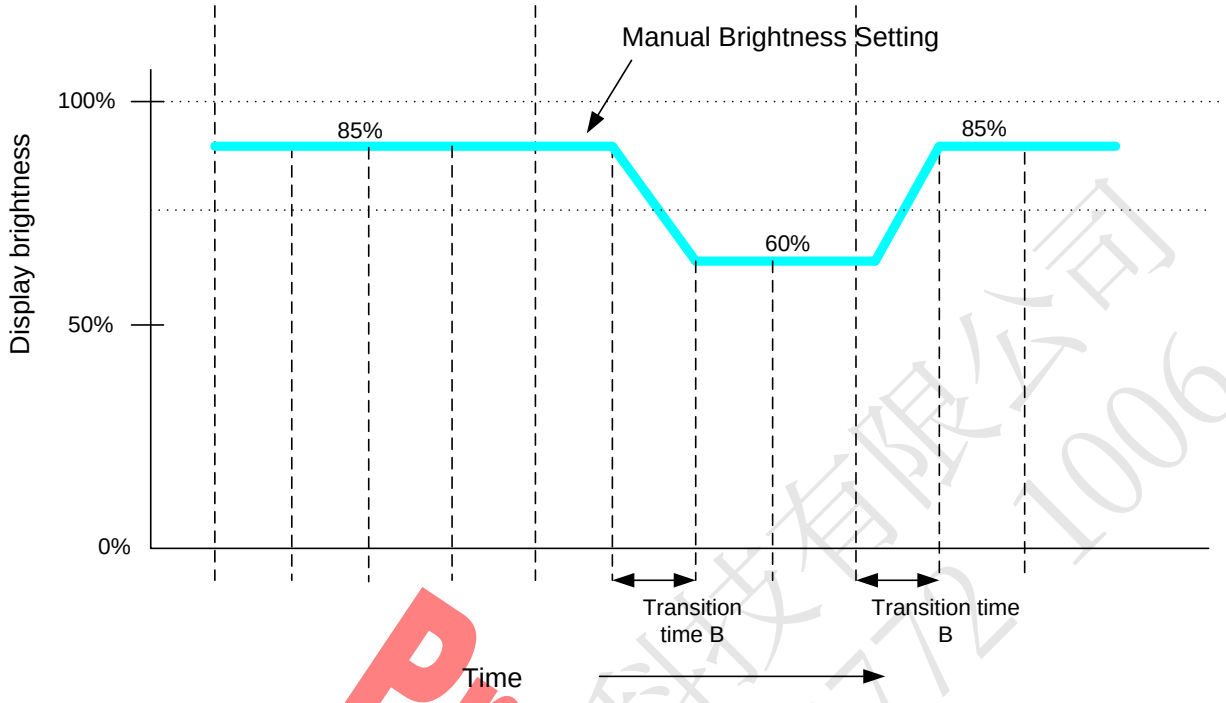


Figure 6 Manual brightness setting and Dimming function

- Combine Display brightness

Green line in the following graph is for the output brightness of display. It is combined with both display brightness, which are defined in the above graphs.

Maximum transition time is transition time A+B.

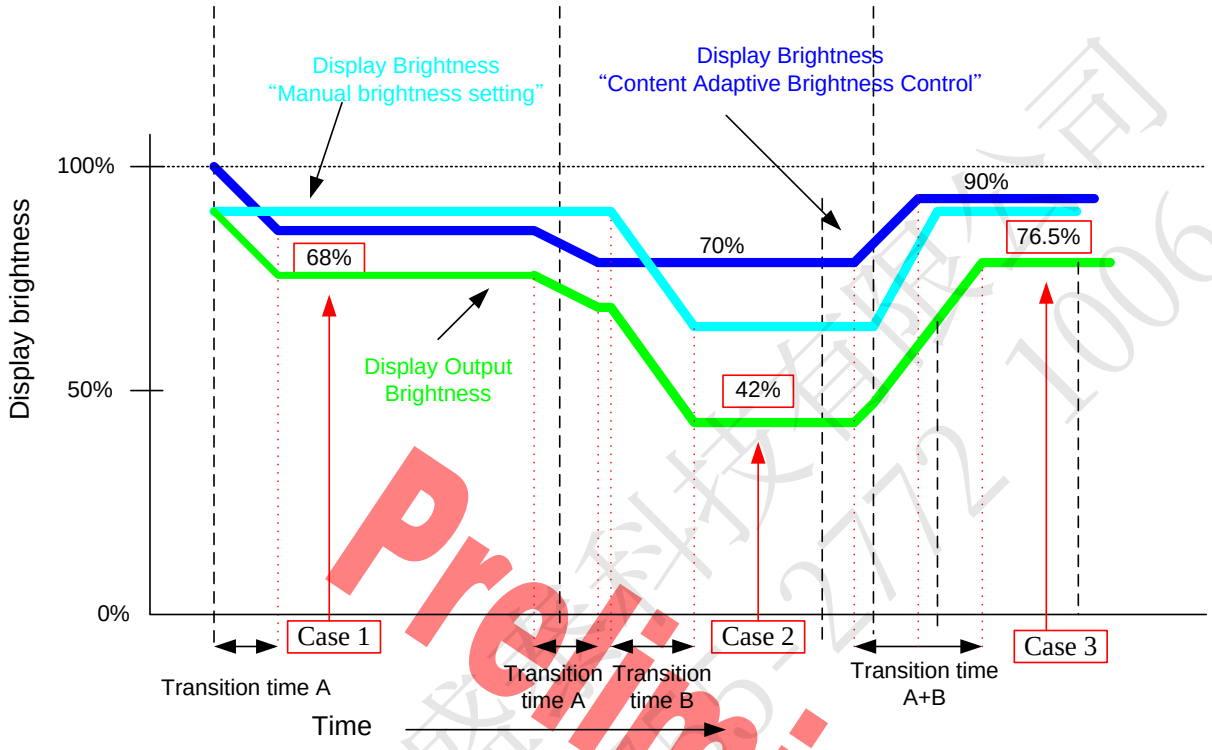


Figure 7 Maximum transition time is transition time A+B

Brightness level calculates with the following formula.

Display Output brightness = Manual Brightness setting * CABC brightness ratio

	Manual Brightness setting	Brightness ratio [CABC]	Display Output brightness
Case 1	85%	80%	68%
Case 2	60%	70%	42%
Case 3	85%	90%	76.5%

Transition time from the current brightness to target brightness is A+B in the worst case.

5.2.2 Minimum Brightness Setting of CABC Function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the LABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting is to avoid too much brightness reduction. When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. If CABC algorithm works without any abnormal visual effect, image processing function can operate even when the brightness cannot be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of “Write CTRL Display (53h)”), CABC minimum brightness setting is ignored. “Read CABC minimum brightness (5Fh)” always read the setting value of “Write CABC minimum brightness (5Eh)”.

	WRCABC (55h)	Function	RDCABCMB (5Fh)	Image
Sleep-in		NA	WRCABCMB (5Eh)	
CABC off	00b	Disable	WRCABCMB (5Eh)	Original
CABC on	01b/10b/11b	Enable	WRCABCMB (5Eh)	CABC modified

Brightness level calculates with the following formula.

Display Output Brightness = Manual brightness setting * CABC brightness ratio

Below drawing is for the explanation of the CABC minimum brightness setting.

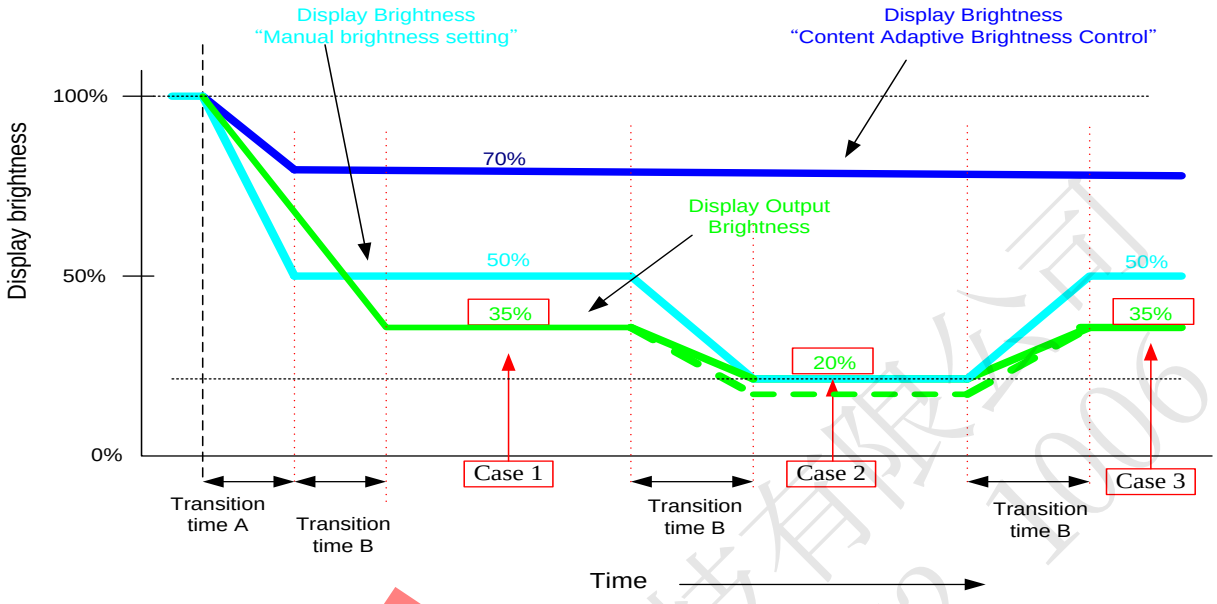


Figure 8 CABC minimum brightness setting

CABC minimum brightness value = 51 (33h: 20% display brightness)

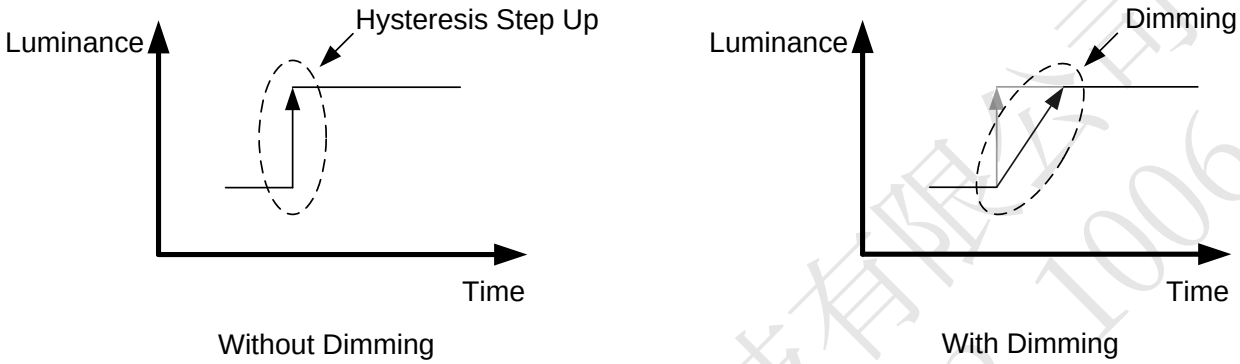
	Display Brightness [manual setting]	Brightness ratio [CABC]	Calculation result of the display brightness formula	Display Output Brightness	Image
Case 1	50%	70%	35%	35%	CABC modified
Case 2	20%	70%	14%	20%	CABC modified
Case 3	50%	70%	35%	35%	CABC modified

At the case 2, the calculation result of the display brightness is 14%. CABC minimum brightness value is set to 20% brightness. Actual display brightness is 20% as the CABC minimum brightness setting.

5.2.3 Display Dimming

5.2.3.1 General Description

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. This dimming function curve is the same in increment and decrement. The basic idea is described below.



Dimming function can be enable and disable. See “Write CTRL Display (53h)” (bit DD) for more information.

5.2.3.2 Dimming Requirement

Dimming function in the display module should be implemented so that 400-600ms is used for the transition between the original brightness value and the target brightness value. The transferring time steps between these two brightness values are equal making the transition linear.

The dimming function is working similarly in both upward and downward directions.

An upward example is illustrating below

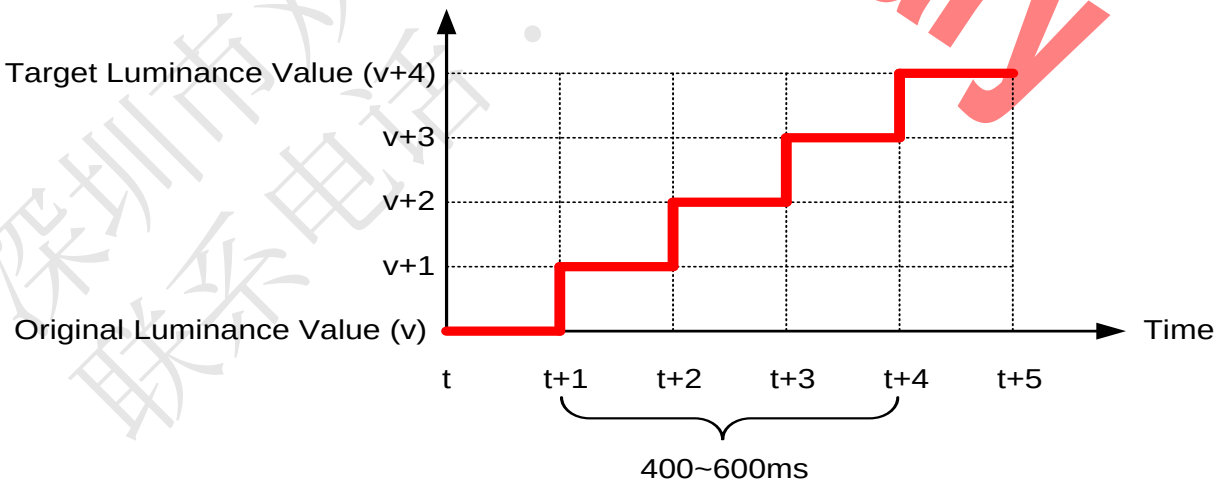


Figure 9 Dimming Requirement

5.2.4 Definition of Brightness Transition Time

- Shorter transition time than 500ms.

There is some stable time between transitions. Below drawing is for transition time: 400ms.

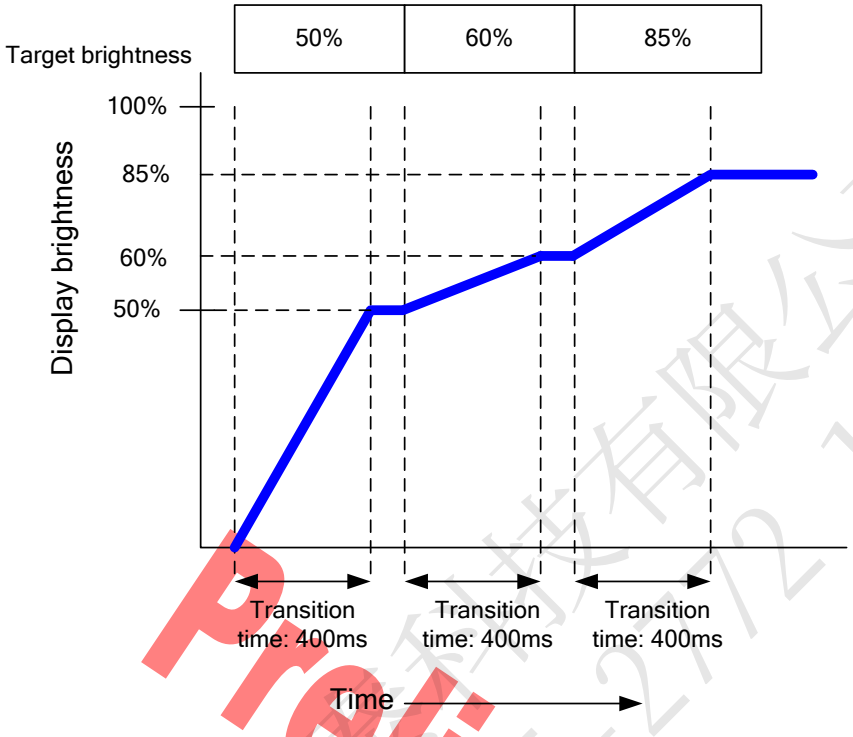


Figure 10 Shorter Transition time than 500ms

- Longer transition time than 500ms

There is no any stable time between transitions. Below drawing is for transition time: 600ms.

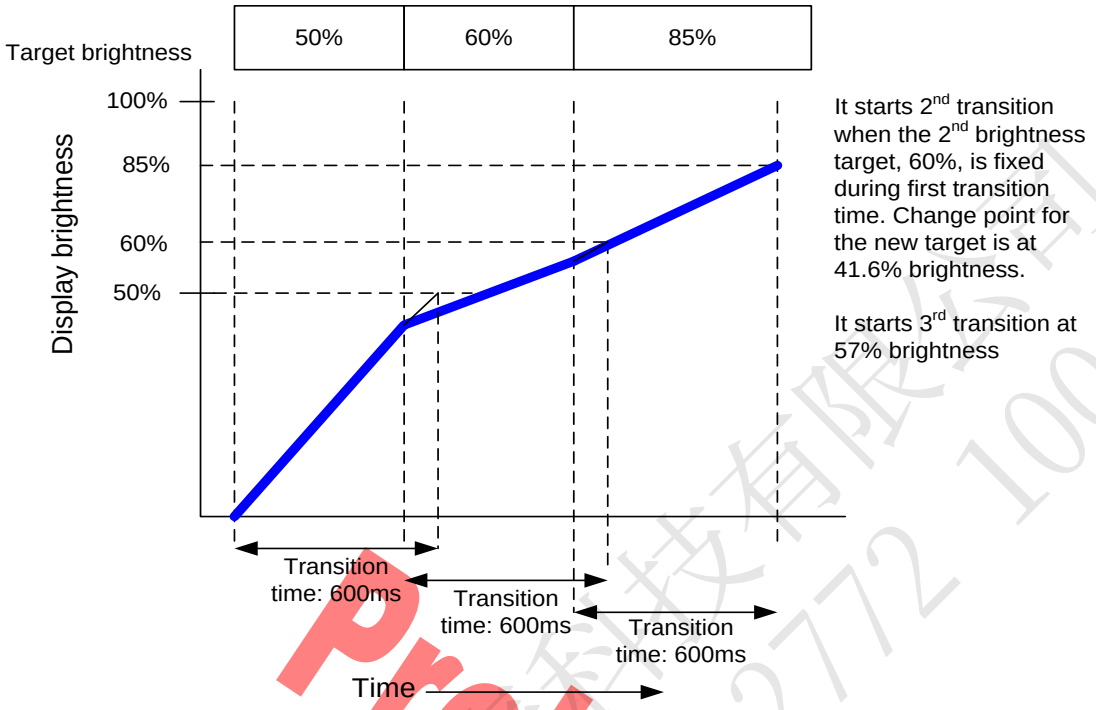


Figure 11 Longer Transition time than 500ms

5.3 Color Enhancement (CE2.0)

Color enhancement function enhances the color saturation by gamut expansion.

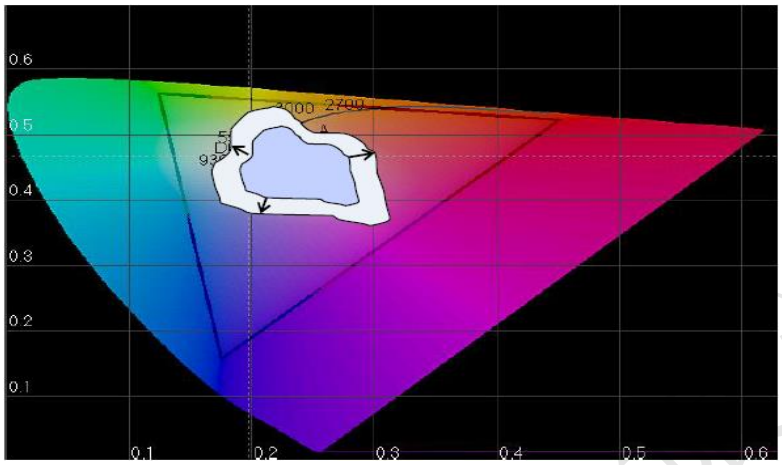
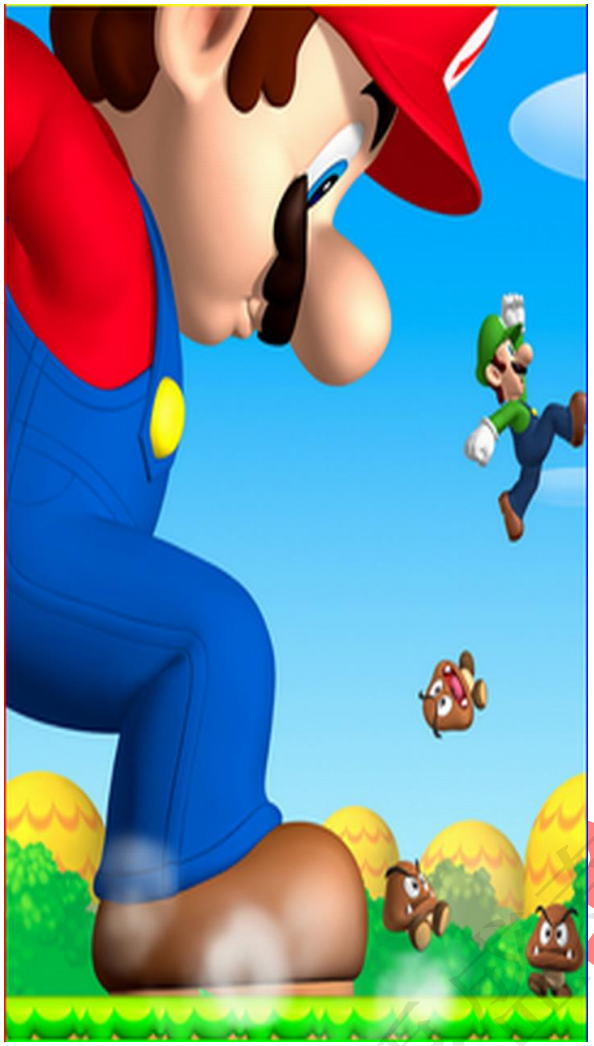


Figure 12 Color Gamut Expansion

An example of the color enhancement function is illustrated below:

Color Enhancement Off	Color Enhancement On



5.4 MIPI-DSI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

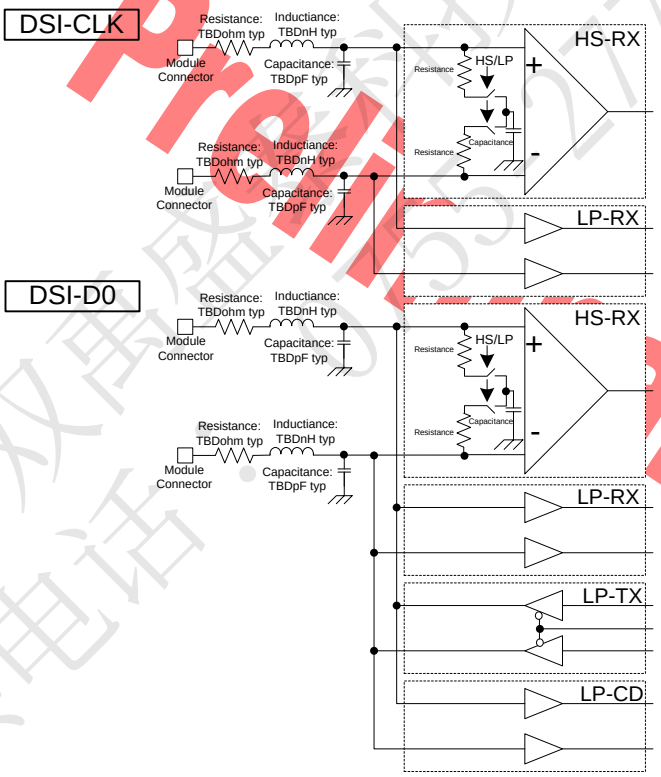
DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

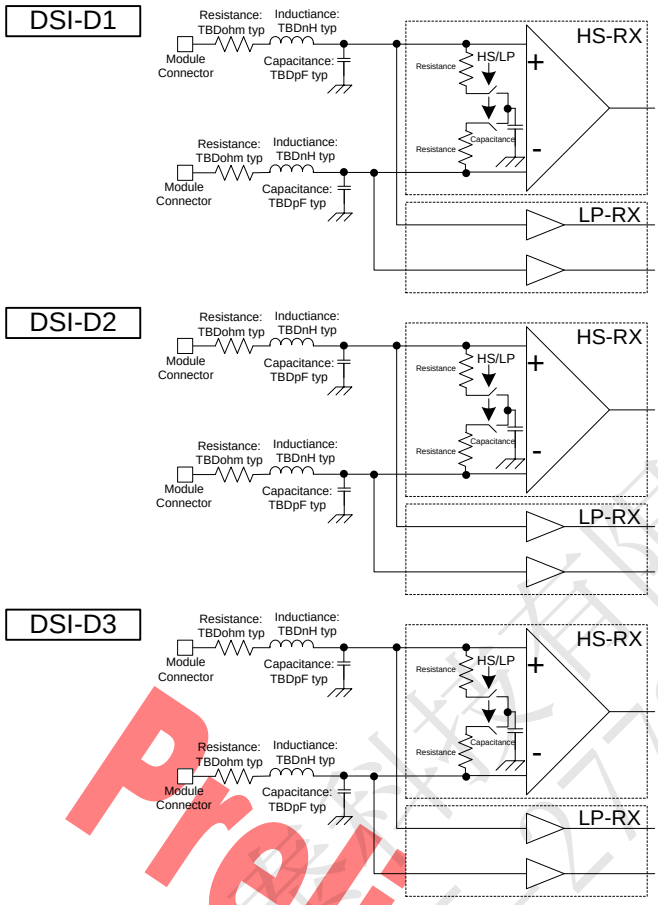
Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode refers to operation in which transactions primarily take the form of sending commands to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High-Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low-Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

5.4.1 Display Module Pin Configuration for DSI





5.4.2 Display Serial Interface (DSI)

5.4.2.1 General description

The communication can be separated 2 different levels between the MCU and the display module:

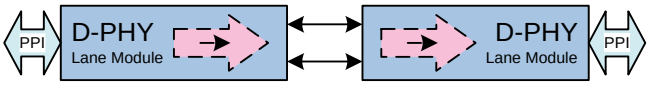
- Interface level : Low level communication

- Packet level : High level communication

5.4.2.2 Interface level communication

5.4.2.2.1 General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane0 can be driven Low-Power (LP) or High-Speed (HS) mode. Data lane1, data lane2 and data lane3 can be driven High-Speed mode only.

	Lane support mode	
Clock Lane	Unidirectional lane High-Speed Clock only Simplified Escape Mode (ULPS Only)	

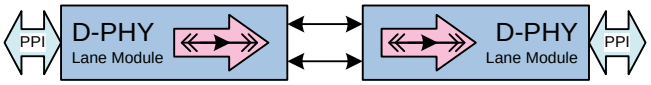
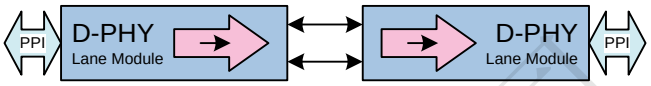
Data Lane0	Bi-directional lane Forward high-speed only Bi-directional Escape Mode Bi-direction LPDT	
Data Lane1/2/3	Unidirectional lane Forward high-speed only Simplified Escape Mode(ULPS Only)	

Figure 13 The Interface Color Lane Types and Support Mode

Low-Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a Low-Power mode.

High-Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High-Speed (HS) and Low-Power (LP) lane pair are defined below.

Lane Pair State Code	Line Voltage Levels		High-Speed(HS)	Low-Power(LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A, Note 1	N/A, Note 1
HS-1	HS High	HS Low	Differential-1	N/A, Note 1	N/A, Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Request	Mark-0
LP-10	LP High	LP Low	N/A	LP-Request	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A, Note 2

High-Speed and Low-Power Lane Pair State Descriptions

Notes:

1. During High-Speed transmission the Low-Power observe LP-00 on the Lines.

2. If LP-11 occurs during Escape mode the Lane returns to Stop state.

5.4.2.2.2 DSI-CLOCK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low-Power Mode (LPM LP-11), Ultra-Low Power Mode (ULPM) or High-Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low-Power) when there is entering or leaving Low-Power Mode (LPM) or Ultra-Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low-Power) when there is entering in or leaving out High-Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

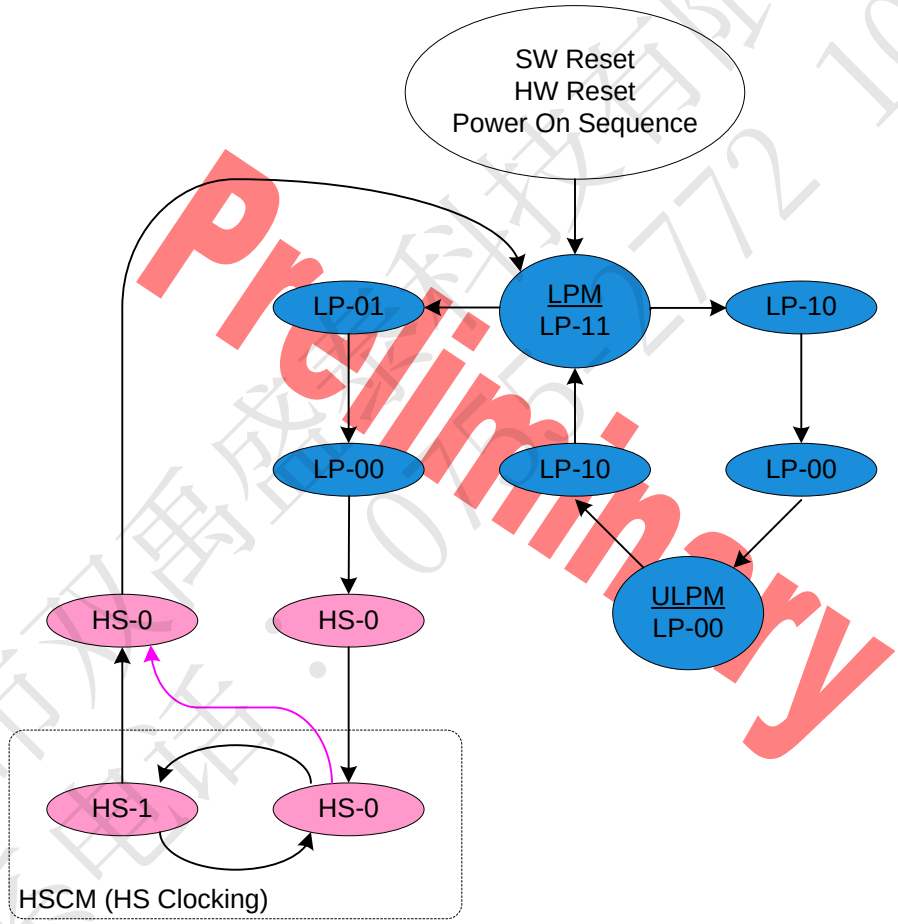


Figure 14 Clock Lanes Power Modes

5.4.2.2.1 Low-Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low-Power Mode (LPM),when DSI-CLK lanes are entering LP-11 State Code , in three different ways:

After SW Reset, HW Reset or Power On Sequence=>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP10=>LP-11(LPM).

This sequence is illustrated below.

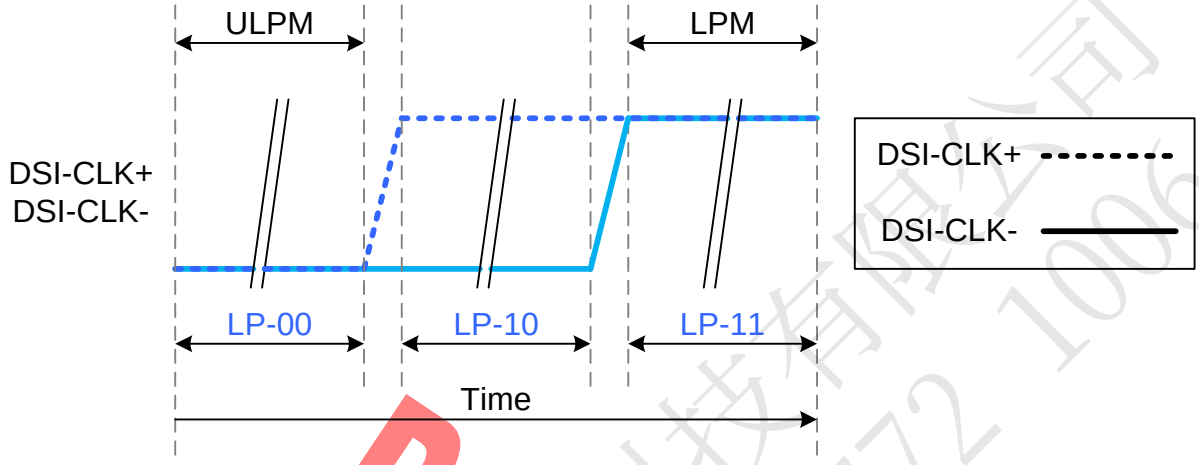


Figure 15 From ULPM to LPM

After DSI-CLK+/- lanes are leaving High-Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM).

This sequence is illustrated below.

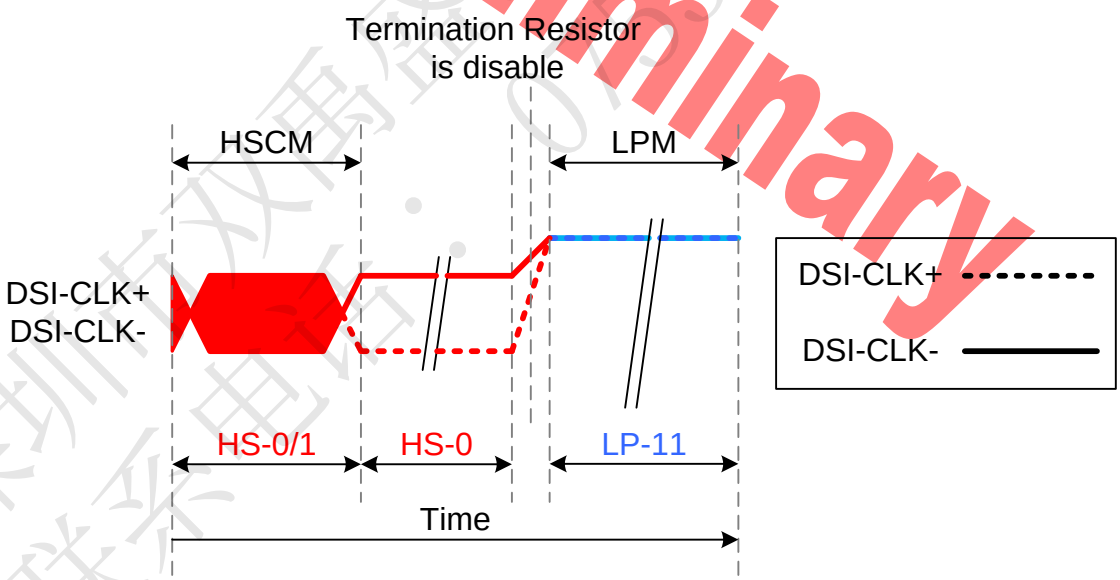


Figure 16 From HSCM to LPM

All three mode changes are illustrated a flow chart below.

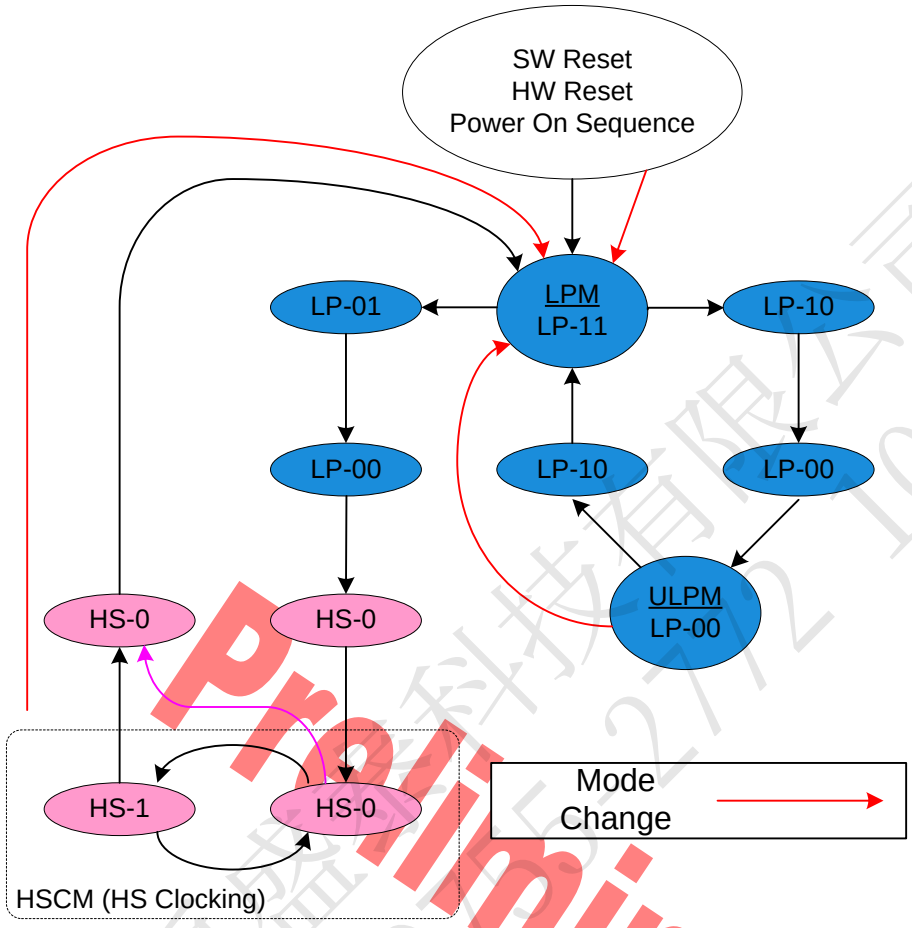


Figure 17 All three mode changes to LPM

5.4.2.2.2.2 Ultra-Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra-Low Power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility if from the Low-Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM).

This sequence is illustrated below:

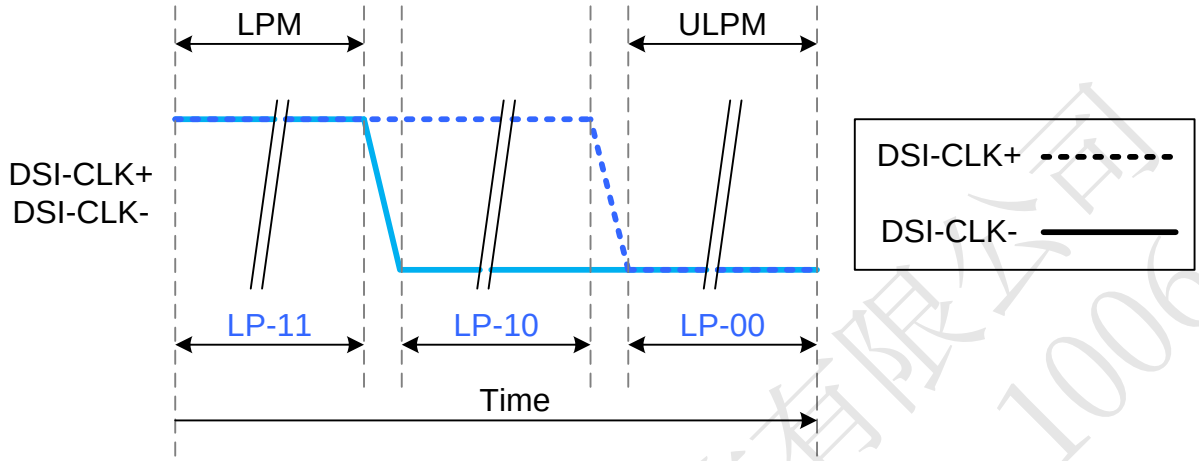


Figure 18 From LPM to UPLM

The mode change is also illustrated below:

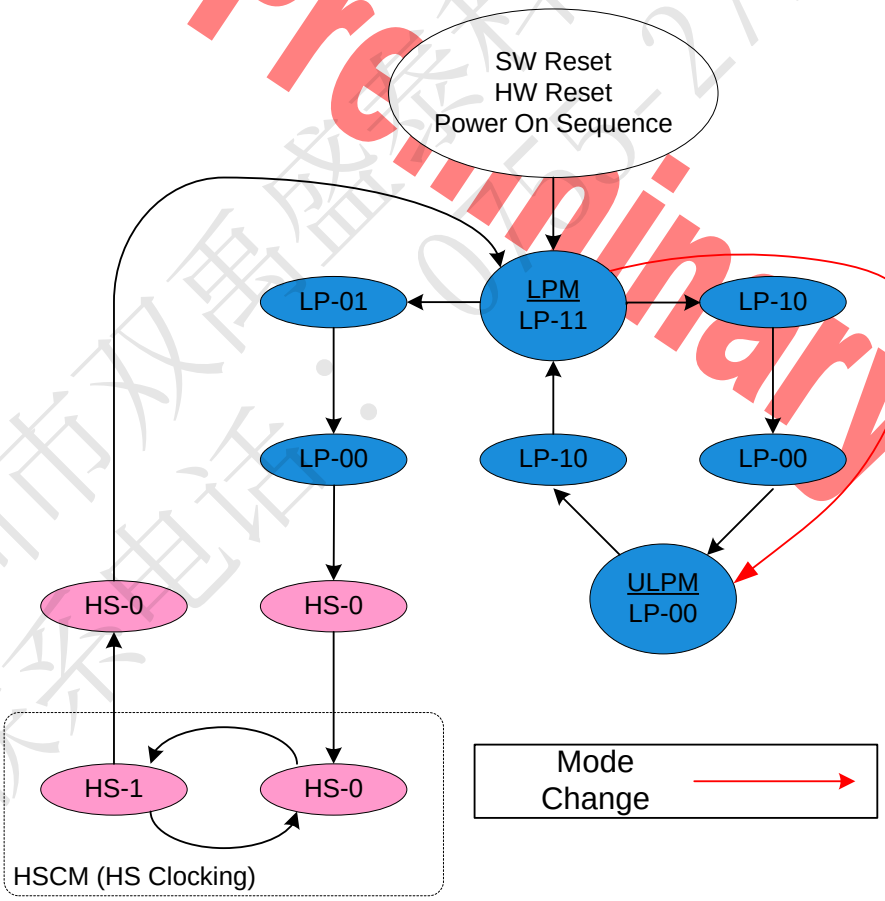


Figure 19 The mode change from LPM to UPLM

5.4.2.2.2.3 High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High-Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes. The only entering possibility is from the Low-Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

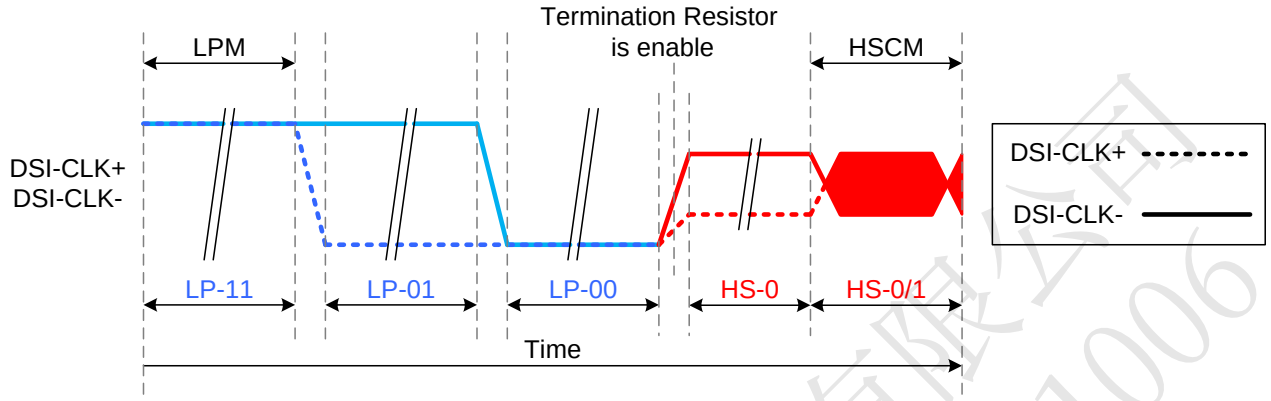


Figure 20 From LPM to HSCM

The mode change is also illustrated below:

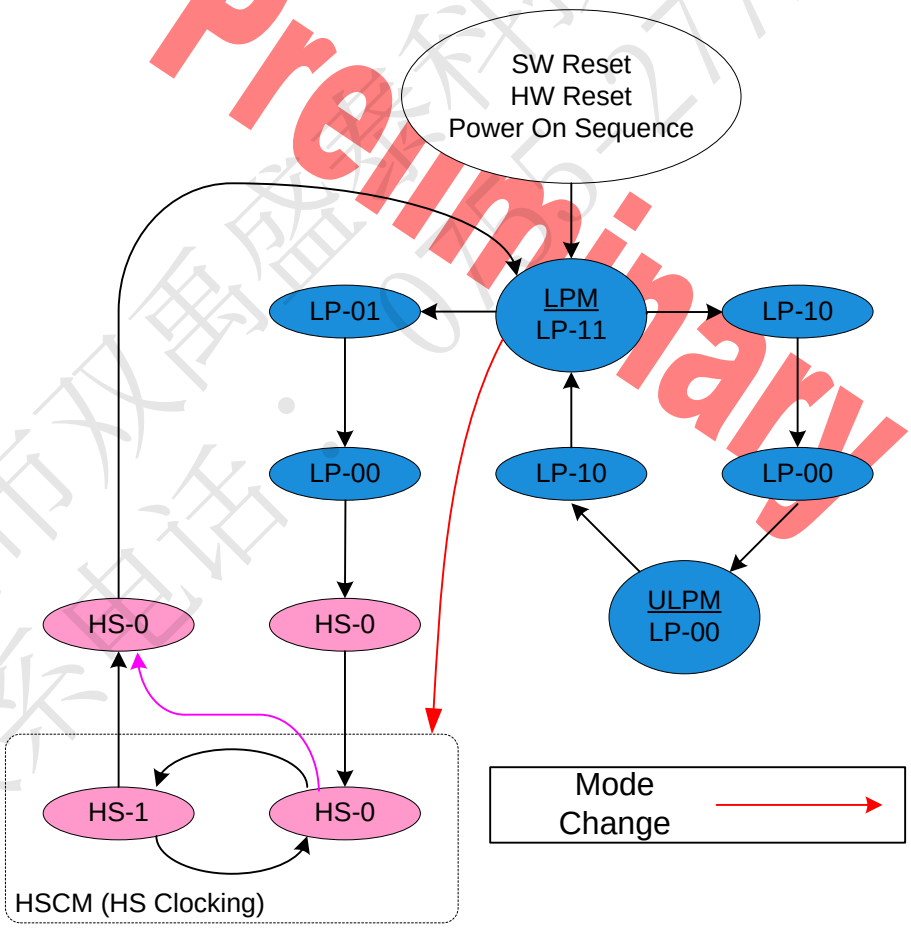


Figure 21 Mode Change from LPM to HSCM on the Flow Chart

The High-Speed clock (DSI-CLK+/-) is started before High-Speed data is sent via DSI-Dn+/- lanes. The High-Speed clock continues clocking after the High-Speed data sending has been stopped.

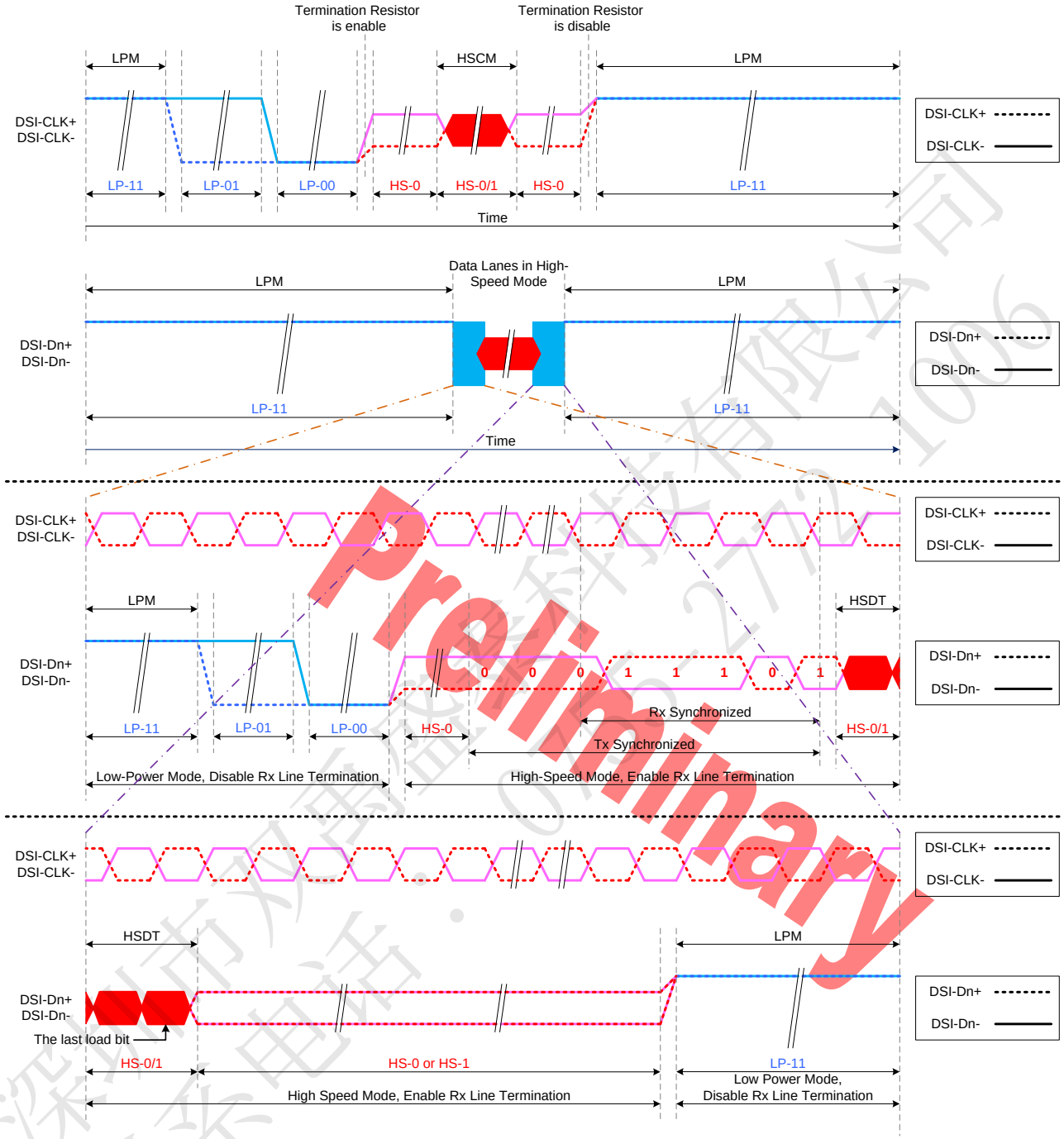


Figure 22 High-Speed Clock Burst

Note:

If the last load bits is HS-0, the transmitter changes form HS-0 to HS-1.

If the last load bits is HS-1, the transmitter changes form HS-1 to HS-0.

5.4.2.2.3 DSI-DATA Lanes

5.4.2.2.3.1 General

DSI-D0+/- data lanes can be driven in different modes which are:

• Escape Mode (Only DSI-D0+/- data lane is used)

• High-Speed Data Transmission (DSI-D0+/-, DSI-D1+/-, DSI-D2+/- and DSI-D3+/- data lanes are used)

• Bus Turnaround Request (Only DSI-D0+/- data lane is used)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP11(Mark1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z

Entering and leaving sequence

5.4.2.2.3.2 ESCAPE MODE

Data lane0 (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low-Power (LP) mode.

These Escape Modes are used to:

• Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module

• Drive data lanes to “Ultra-Low Power State” (ULPS)

• Indicate “Remote Application Reset” (RAR), which is reset the display module

• Indicate “Tearing Effect” (TEE), which is used for a TE trigger event from the display module to the MCU

• Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.

• A load if it is needed

• Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

• End: LP-11

This basic construction is illustrated below:

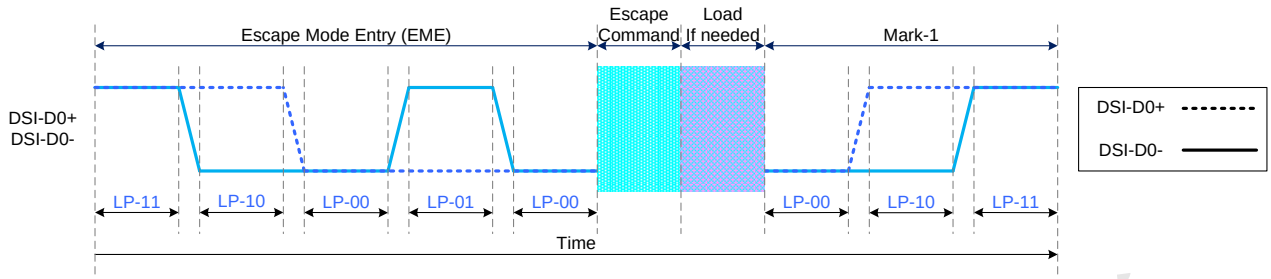


Figure 23 General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the Low-Power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Escape commands are defined on the next table.

This basic construction is illustrated below:

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit➔Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 bin	-	○
Ultra-Low Power Mode	Mode	0001 1110 bin	○	○
Underfined-1, Note 1	Mode	1001 1111 bin	-	-
Underfined-2, Note 1	Mode	1101 1110 bin	-	-
Remote Application Reset	Trigger	0110 0010 bin	-	○
Tearing Effect	Trigger	0101 1101 bin	-	-
Acknowledge	Trigger	0010 0001 bin	-	○
Unknow-5, Note 1	Trigger	1010 0000 bin	-	-

Notes:

1. This Escape command support has not been implemented on the display module.

2. n=1.

3. "○"=Supported

4. "-"=Not Supported

5. Tearing Effect Trigger cannot be used in MIPI Video mode.

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low-Power Data Transmission (LPDT) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

• Load (Data):

One or more bytes (8 bits)

Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

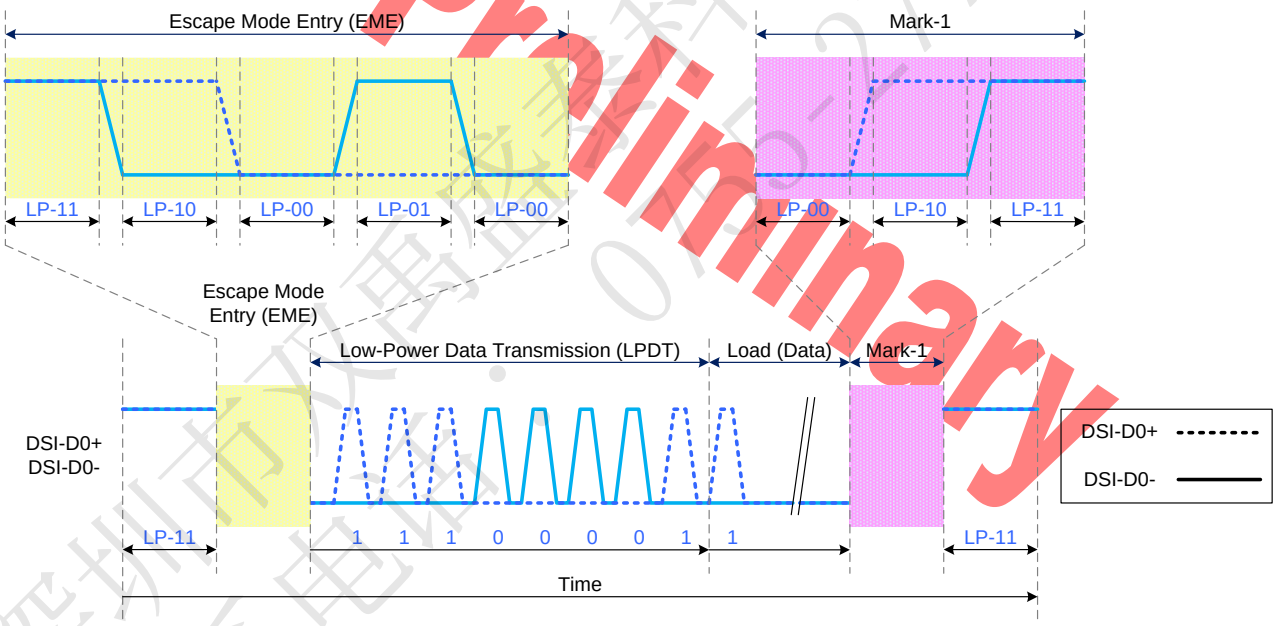


Figure 24 Low-Power Data Transmission (LPDT)

Note:

Load(Data) is presenting that the first bit is logical '1' in this example

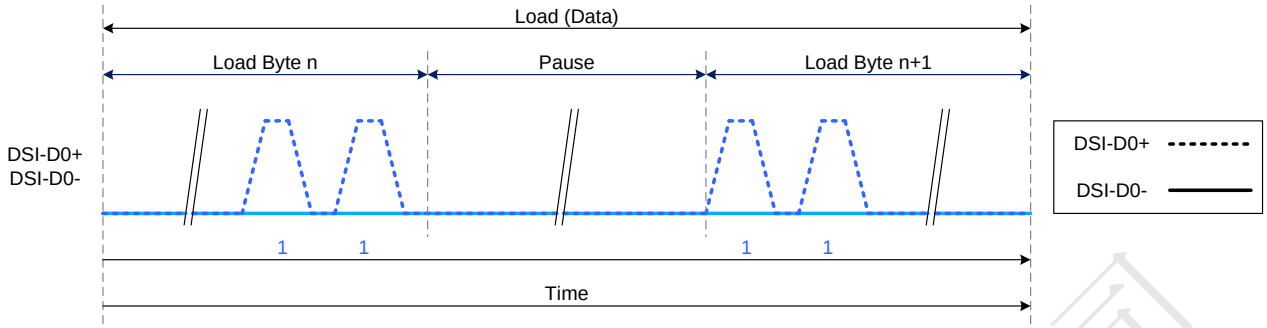


Figure 25 Pause (Example)

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

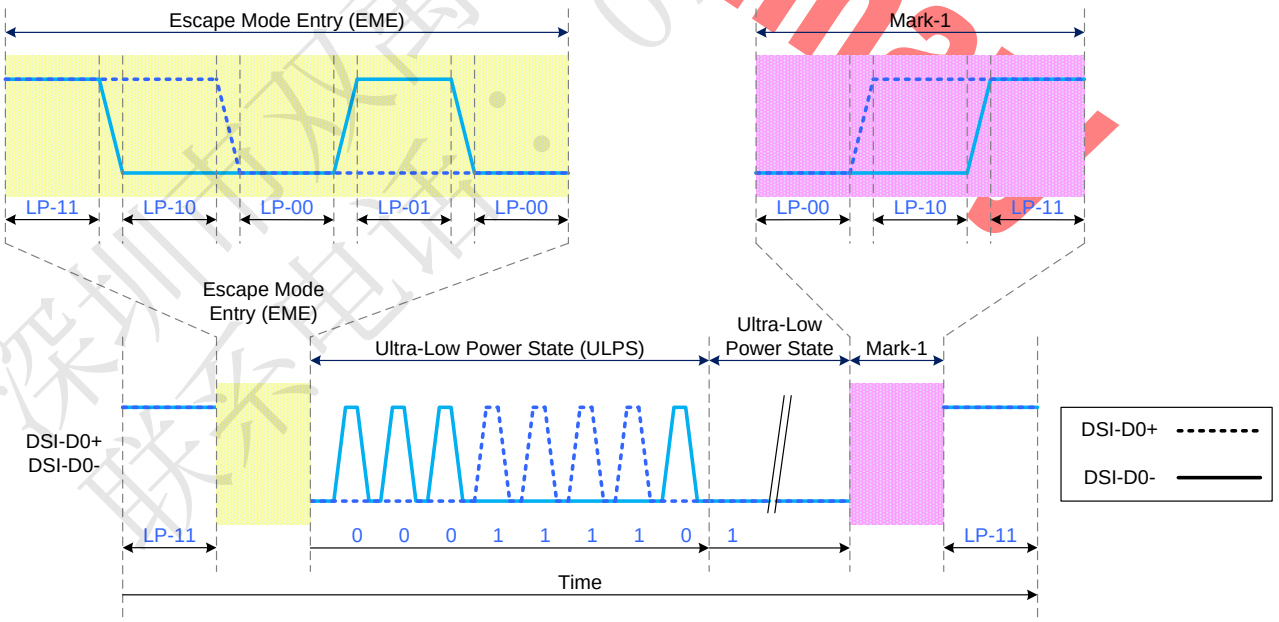


Figure 26 Ultra-Low Power State (ULPS)

Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

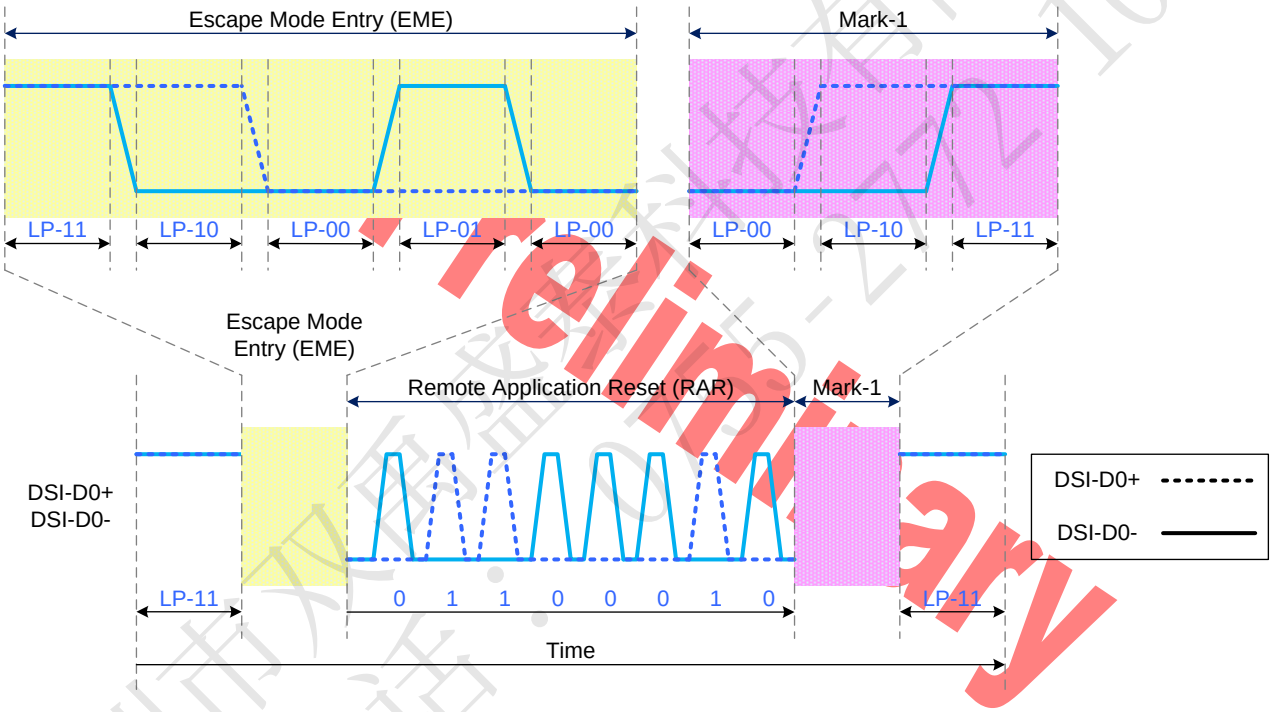


Figure 27 Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

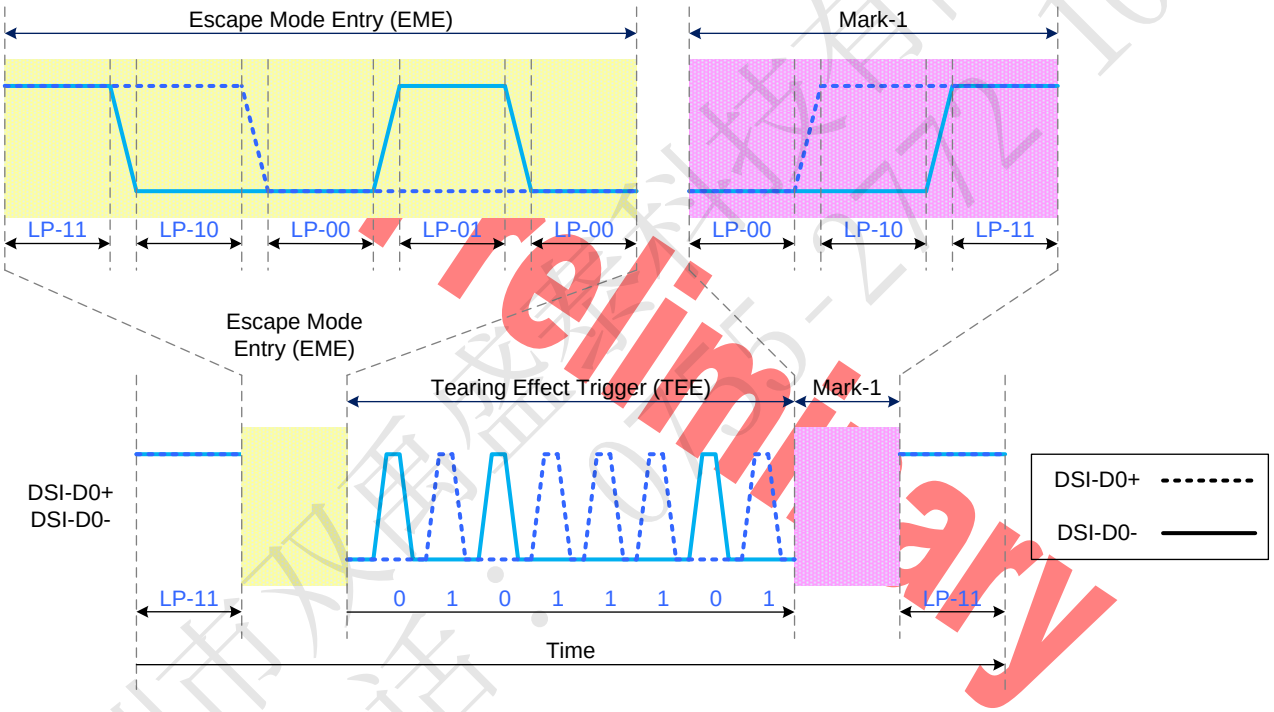


Figure 28 Tearing Effect (TEE)

Note: Tearing Effect (TEE) can not be used in MIPI Video Mode

Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

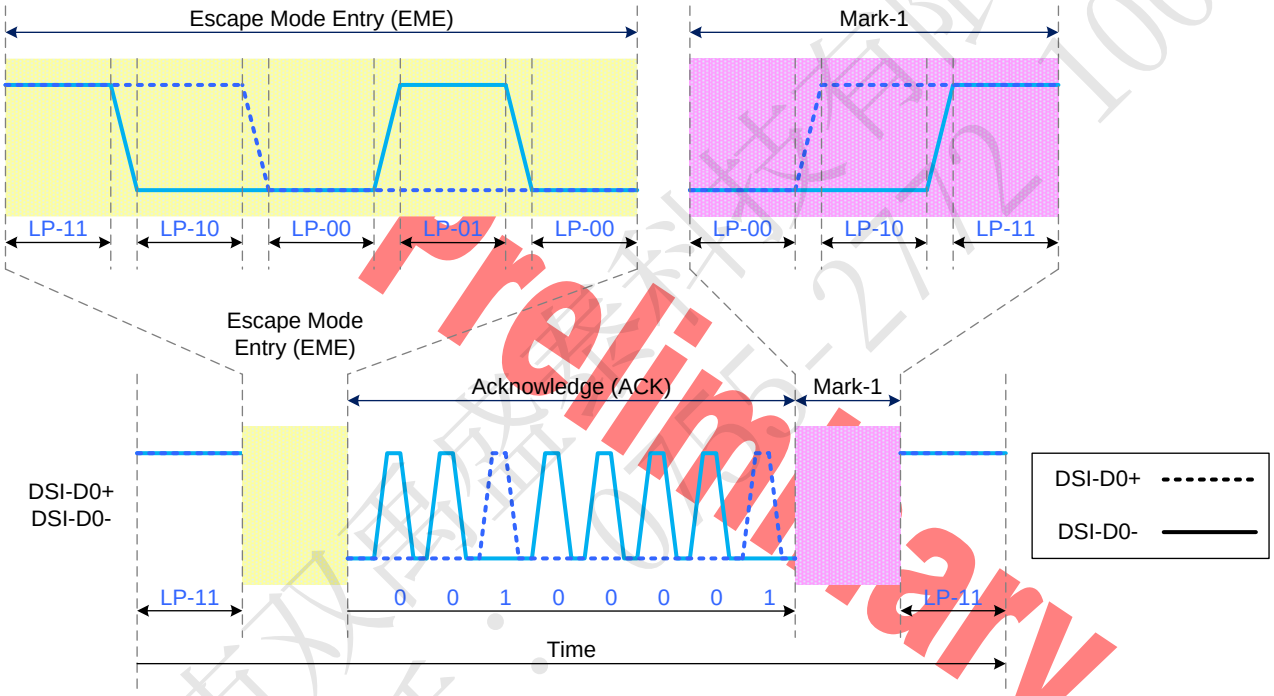


Figure 29 Acknowledge (ACK)

5.4.2.2.3.3 High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below

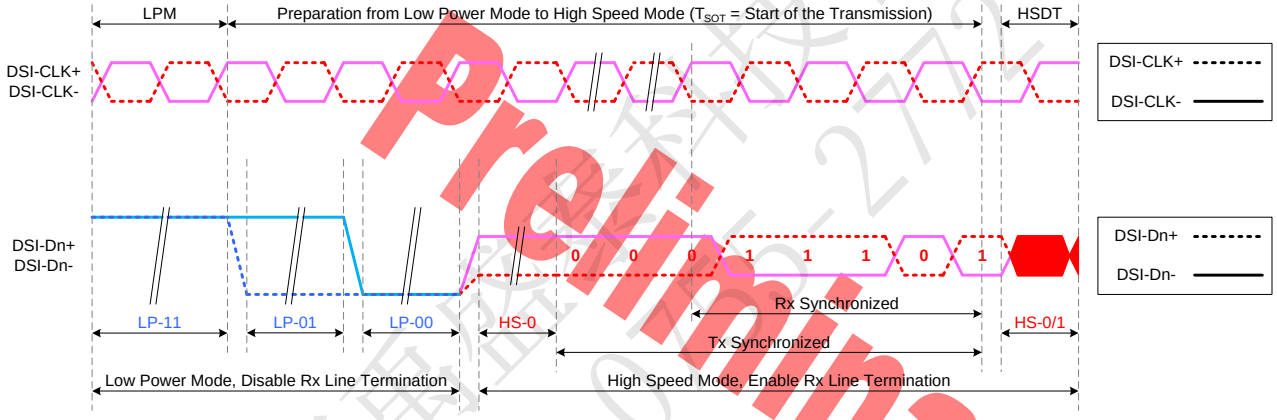


Figure 30 Entering High-Speed Data transmission (T_{SOT} of HSDT)

Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

• Start: High-Speed Data Transmission (HSDT)

• Stops High-Speed Data Transmission

MCU changes to HS-1, if the last load bit is HS-0

MCU changes to HS-0, if the last load bit is HS-1

• End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

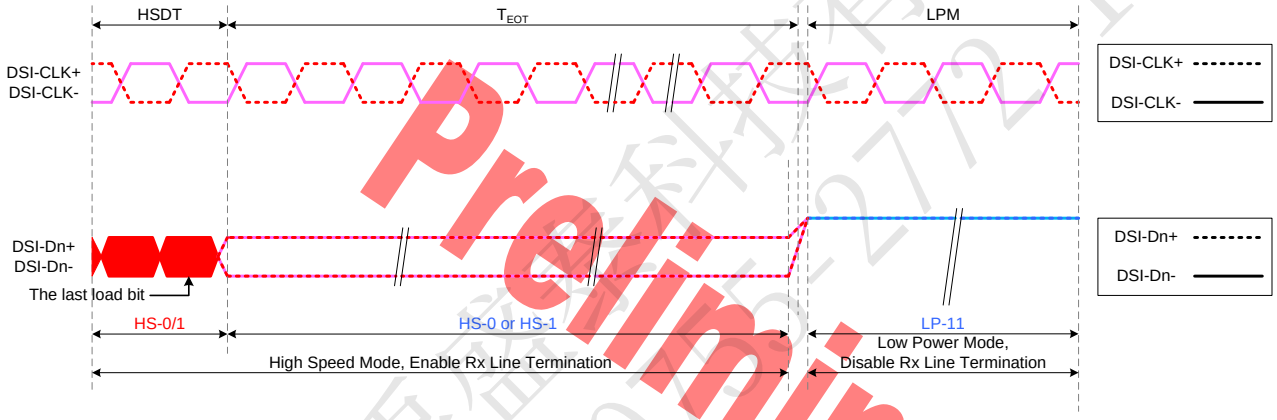


Figure 31 Leaving High-Speed data Transmission (T_{EOT} of HSDT)

Burst of the High-Speed Data Transmission (HSDT)

The burst of the High-Speed Data Transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

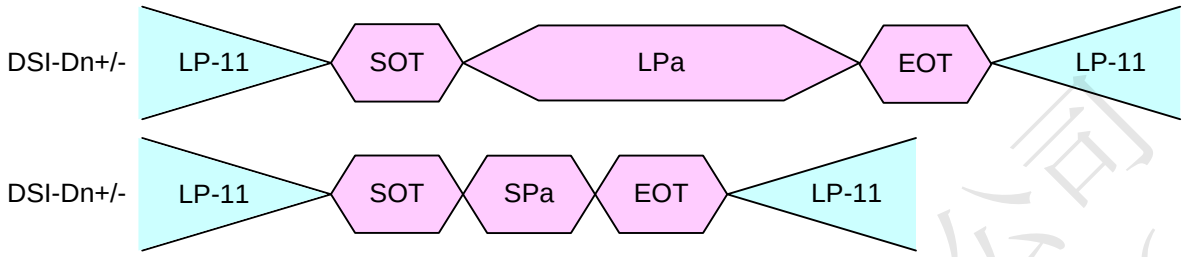


Figure 32 Single Packet in High-Speed Data Transmission with EoT packet disabled

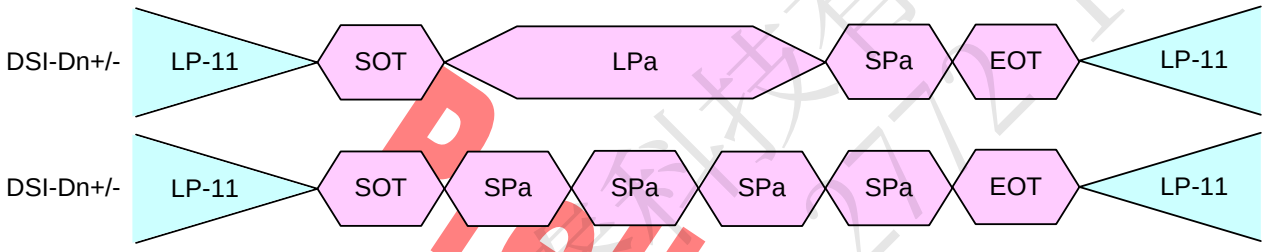


Figure 33 Multiple Packets in High-Speed Data Transmission with EoT packet disabled

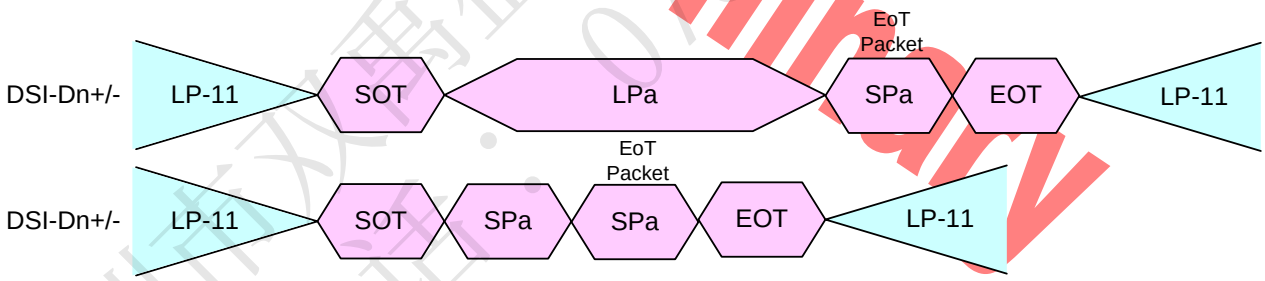


Figure 34 Single Packet in High-Speed Data Transmission with EoT packet enable

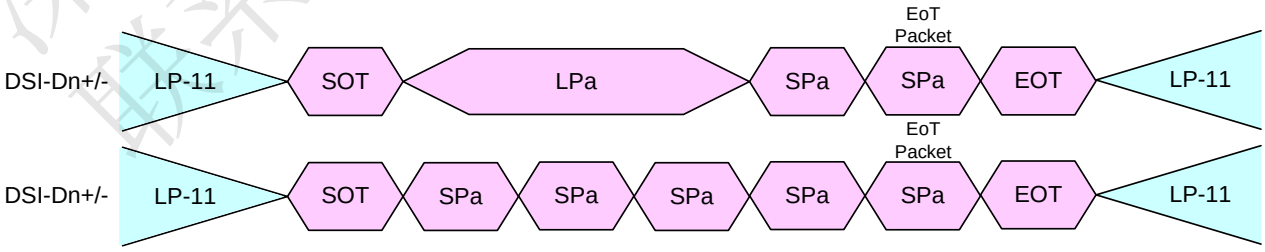


Figure 35 Multiple Packets in High-Speed Data Transmission with EoT packet enable

Abbreviation	Explanation
EoT	End of the Transmission
LPa	Long Packet
LP-11	Low-Power Mode, Data lanes are'1's (Stop Mode)
SPa	Short Packet
SoT	Start of the Transmission

5.4.2.2.3.4 Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module is using the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

• Start (MCU): LP-11

• Turnaround Request (MCU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00

• The MCU wait until the display module is starting to control DSI-D0+/- data lanes and the MCU stop to control DSI-D0+/- data lanes (=High-Z)

• The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The same bus turnaround .procedure (From the MCU to the display module) is illustrated below.

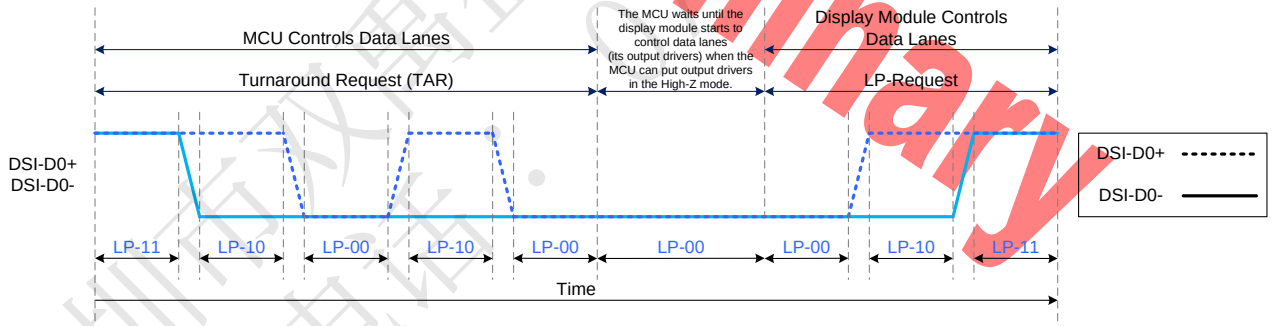


Figure 36 Bus Turnaround Procedure

MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU..

5.4.2.3 Packer Level Communication

5.4.2.3.1 Short Packet (SPa) and Long Packet (LPa) Structure

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low-Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

• Short Packet (SPa): 4 bytes

• Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

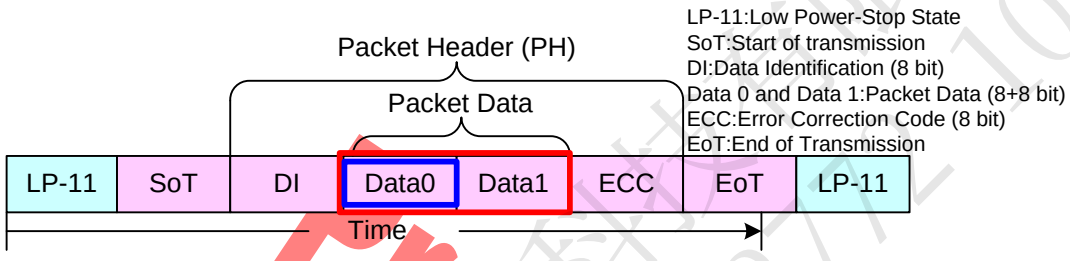


Figure 37 Short Packet (SPa) Structure

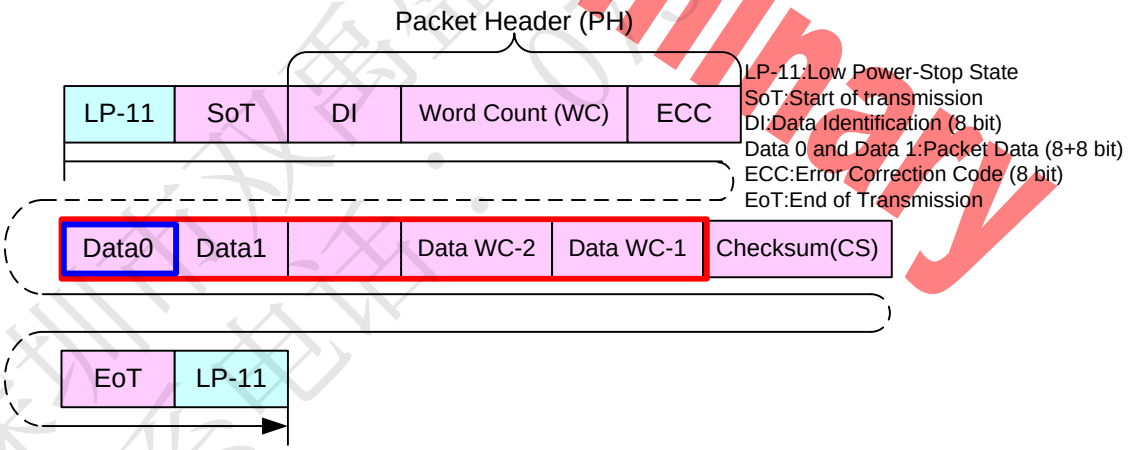


Figure 38 Long Packet (LPa) Structure

Note:

Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple

packet format e.g.

** LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11*

** LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11*

** LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11*

5.4.2.3.1.1 Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.

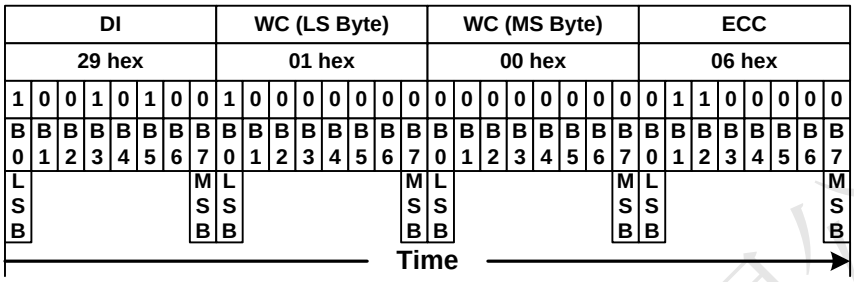


Figure 39 Bit Order of Byte on Packets

5.4.2.3.1.2 Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

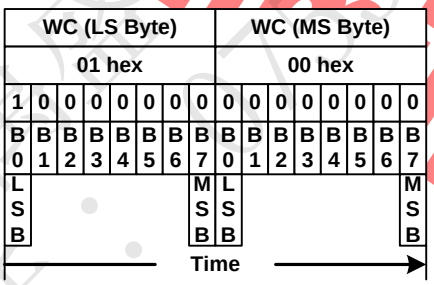


Figure 40 Byte Order of the Multiple Byte on Packets

5.4.2.3.1.3 Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

• 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)

• 2nd and 3rd bytes: Packet Data (PD), Data 0 and Data 1

• 4th byte: Error Correction Code (ECC)

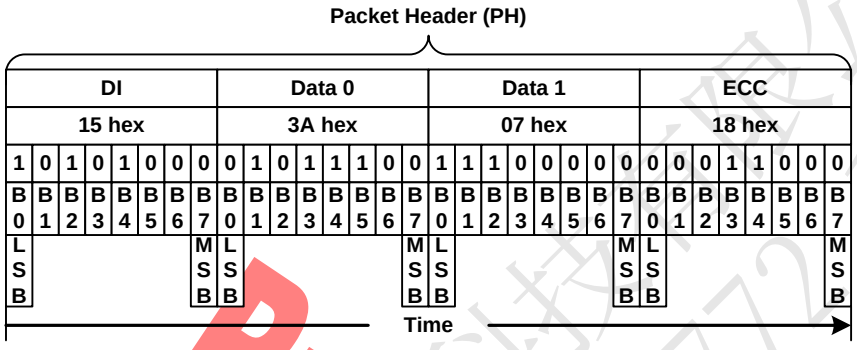


Figure 41 Packet Header (PH) on the Short Packet(SPa)

Long Packet (LPa):

• 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

• 2nd and 3rd bytes: Word Count (WC)

• 4th byte: Error Correction Code (ECC)

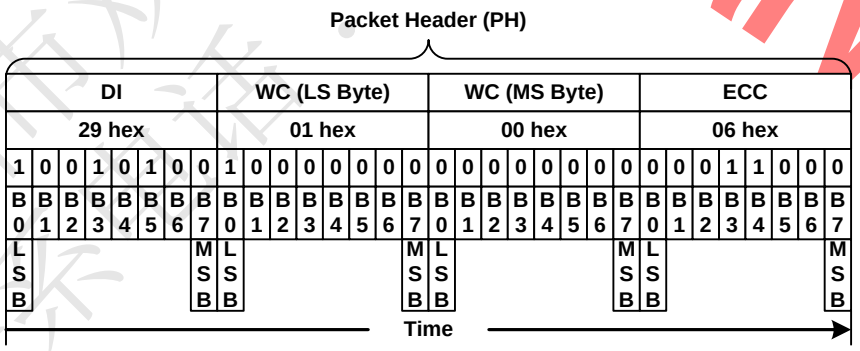


Figure 42 Packet Header (PH) on the Long Packet (LPa)

- **Data Identification (DI)**

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

• Virtual Channel (VC), 2 bits, DI[7...6]

• Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Figure 43 Data Identification (DI) Structure

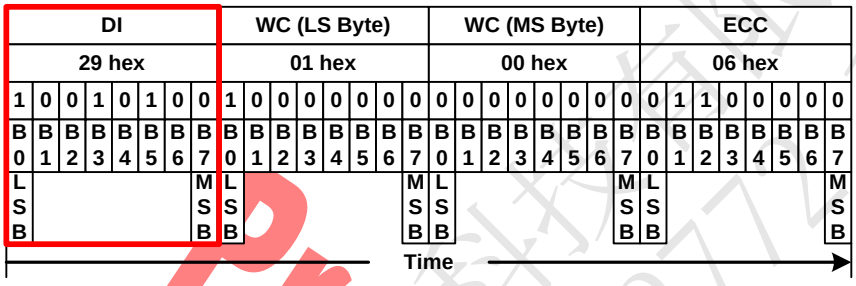


Figure 44 Data Identification (DI) on the Packet Header(PH)

- **Virtual Channel (VC)**

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

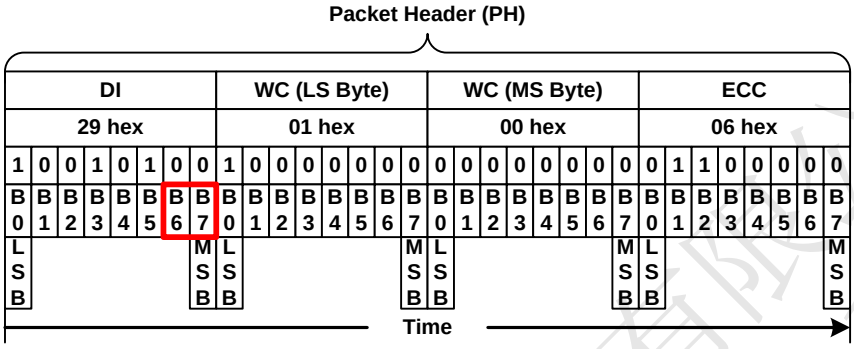


Figure 45 Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

• The MCU is using the virtual channel 0 when it sends packets to this display module

• This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.

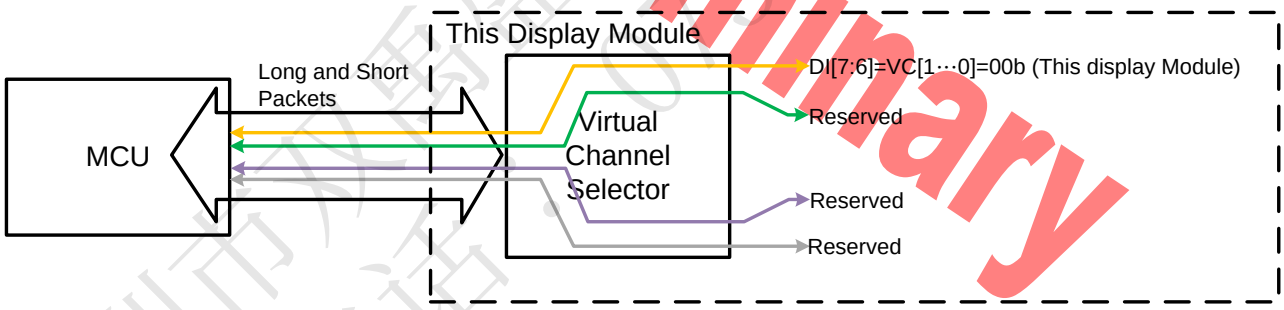


Figure 46 Virtual Channel (VC) Configuration

- **Data Type (DT)**

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

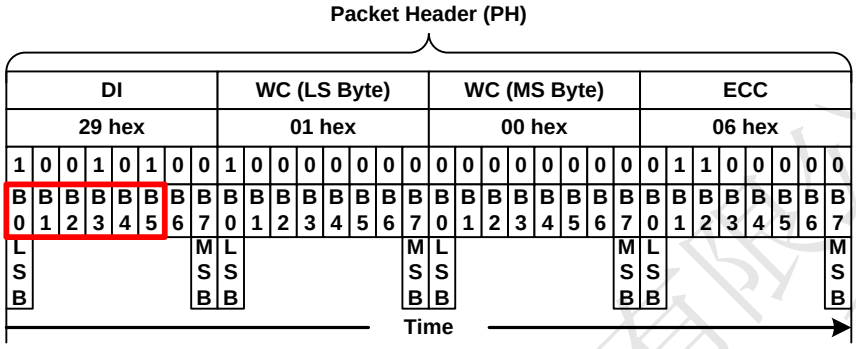


Figure 47 Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Data Type Hex	Data Type Binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start.	Short
21h	10 0001	Sync Event, H Sync Start.	Short
08h	00 1000	End of Transmission (EoT) packet.	Short
02h	00 0010	Color Mode (CM) Off Command.	Short
12h	01 0010	Color Mode (CM) On Command.	Short
hh22h	10 0010	Shut Down Peripheral Command.	Short
32h	11 0010	Turn On Peripheral Command.	Short
13h	01 0011	Generic Short WRITE, 1 parameter.	Short
23h	10 0011	Generic Short WRITE, 2 parameters.	Short
14h	01 0100	Generic READ, 1 parameter.	Short
24h	10 0100	Generic READ, 2 parameters.	Short
05h	00 0101	DCS WRITE, no parameter.	Short
15h	01 0101	DCS WRITE, 1 parameter.	Short
06h	00 0110	DCS READ, no parameter.	Short
37h	11 0111	Set Maximum Return Packet Size.	Short
09h	00 1001	Null Packet, no data.	Long
19h	01 1001	Blanking Packet, no data.	Long
29h	10 1001	Generic Long Write.	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet.	Long
3Eh	11 1110	Packed Pixel Stream,24-bit RGB,8-8-8 Format.	Long

Data Type (DT) from MCU to the Display Module (or Other Devices)

From the Display Module (or Other Devices) to the MCU									
Data Type Hex	B 5	B 4	B 3	B 2	B 1	B 0	Description	Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge and Error Report	Short	AwER
11h	0	1	0	0	0	1	Generic Short READ Response,1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Short READ Response,2 bytes returned	Short	GENRR2-S
1Ah	0	1	1	0	1	0	Generic Long READ Response	Short	GENRR-L
1Ch	0	1	1	1	0	0	DCS Long READ Response	Short	DCSRR_L
21h	1	0	0	0	0	1	DCS Short READ Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Short READ Response, 2 bytes returned	Short	DCSRR2_S

Data Type (DT) from the Display Module (or Other Devices) to the MCU

The receiver will ignore other Data Type (DT) if they are not defined on tables: “Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “ Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

- **Packet Data (PD) on the Short Packet (SPa)**

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet of Packet Data (PD) send after the Packet Header.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

• Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS's parameter)

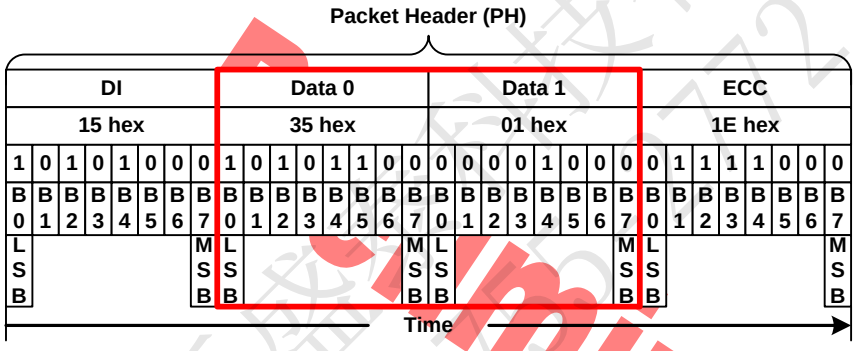


Figure 48 Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)

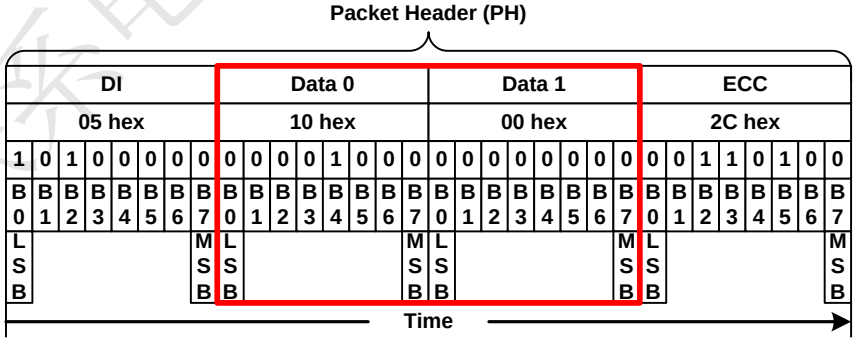


Figure 49 Packet Data (PD) for Short Packet (SPa), 1 Bytes Information

- **Word Count (WC) on the Long Packet (LPa)**

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

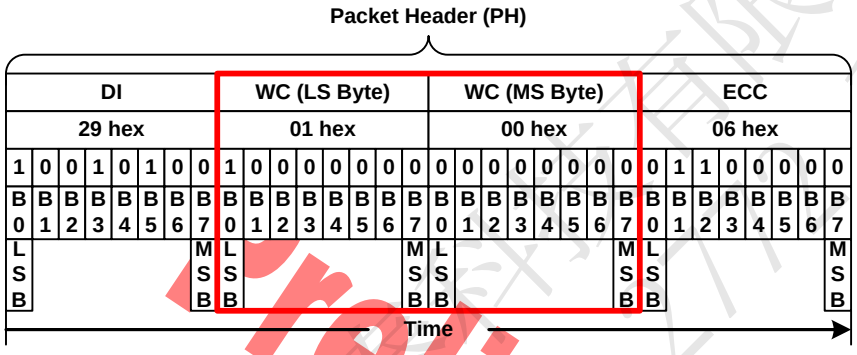


Figure 50 Word Count (WC) on the Long Packet (LPa)

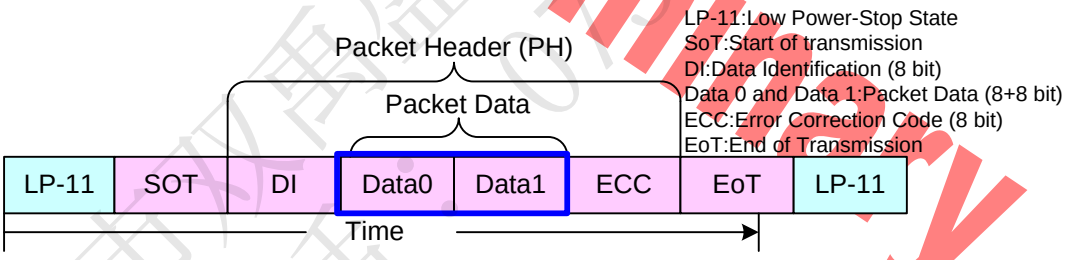


Figure 51 Packet Data (PD) on the Short Packet (SPa)

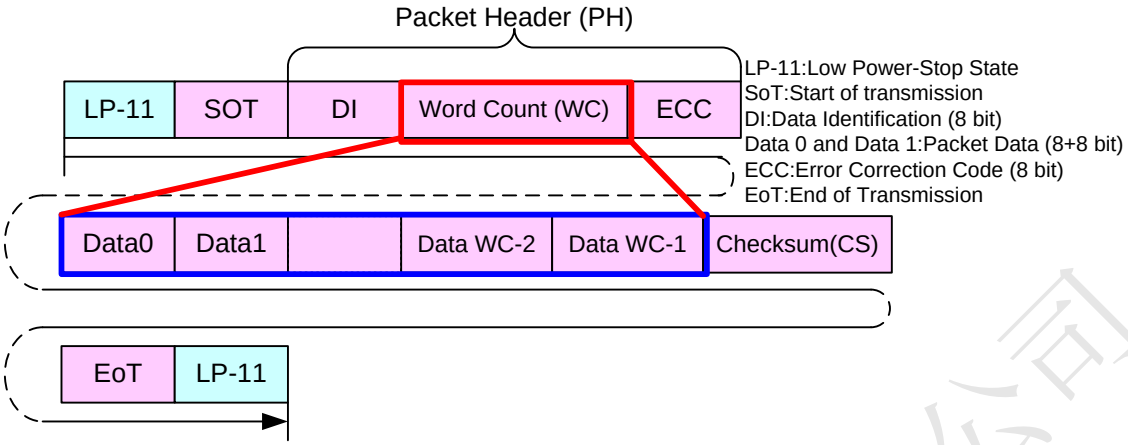


Figure 52 Packet Data (PD) on the Long Packet (LPa)

- **Error Correction Code (ECC)**

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH):

The ECC protects the following field”

• Short Packet (SPa): Data Identification (DI) byte (8 bits, D[0...7]), Packet Data (PD) bytes (16 bits, D[8...23]) and ECC(8 bits: P[0…7])

• Long Packet (LPa): Data Identification (DI) byte (8 bits, D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits, P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.

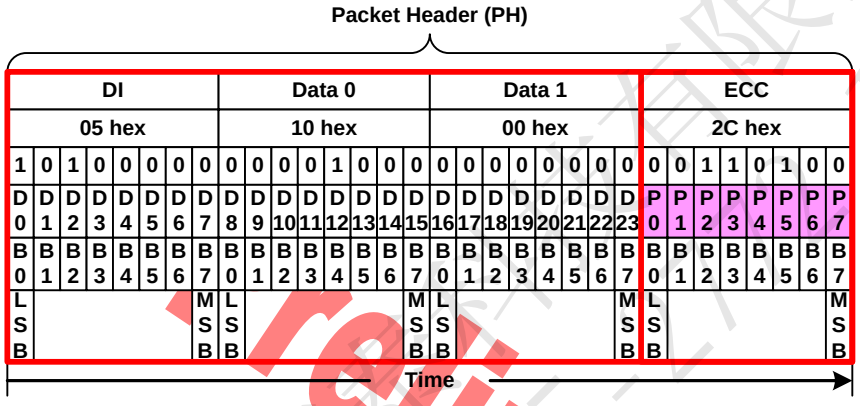


Figure 53 D[23..0] and P[7…0] on the Short Packet (SPa)

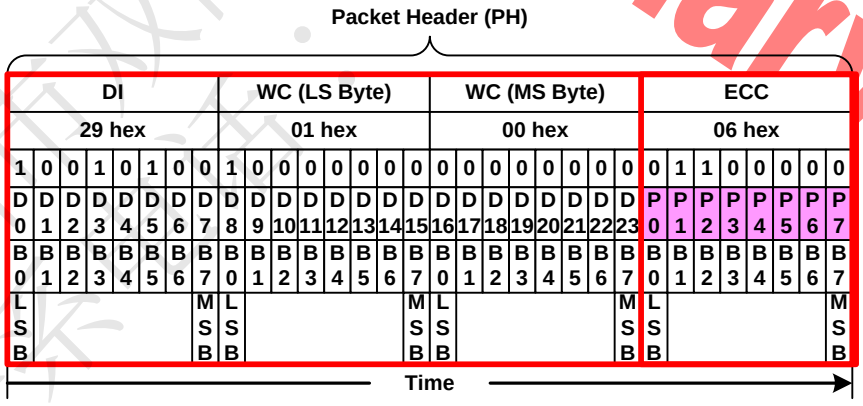


Figure 54 D[23…0] and P[7…0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol ‘^’ is presenting XOR function

(Pn is ‘1’ if there is odd number of ‘1’s and Pn is ‘0’ if there is even number of ‘1’s), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to ‘0’ because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

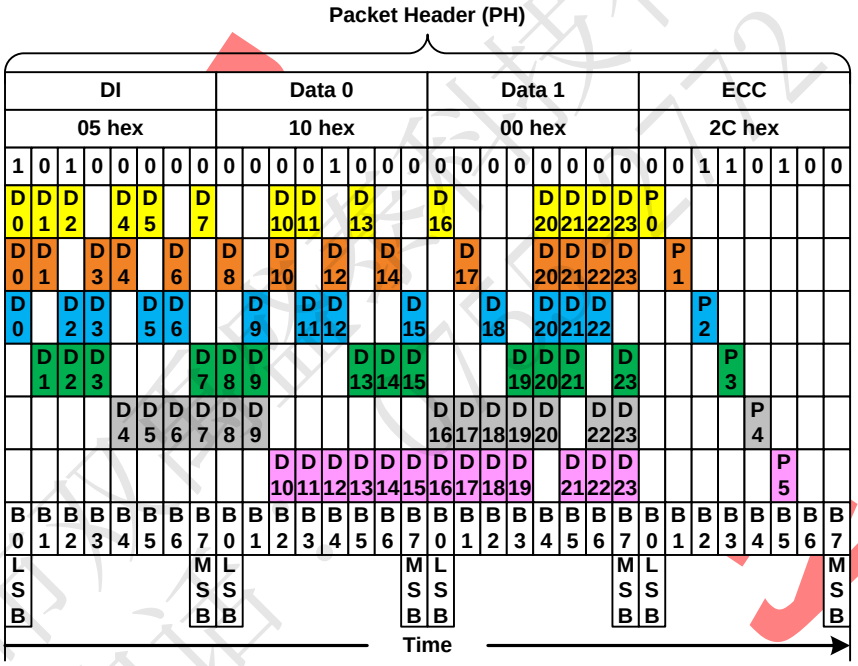


Figure 55 XOR Functionality on the Short Packet (SPa)

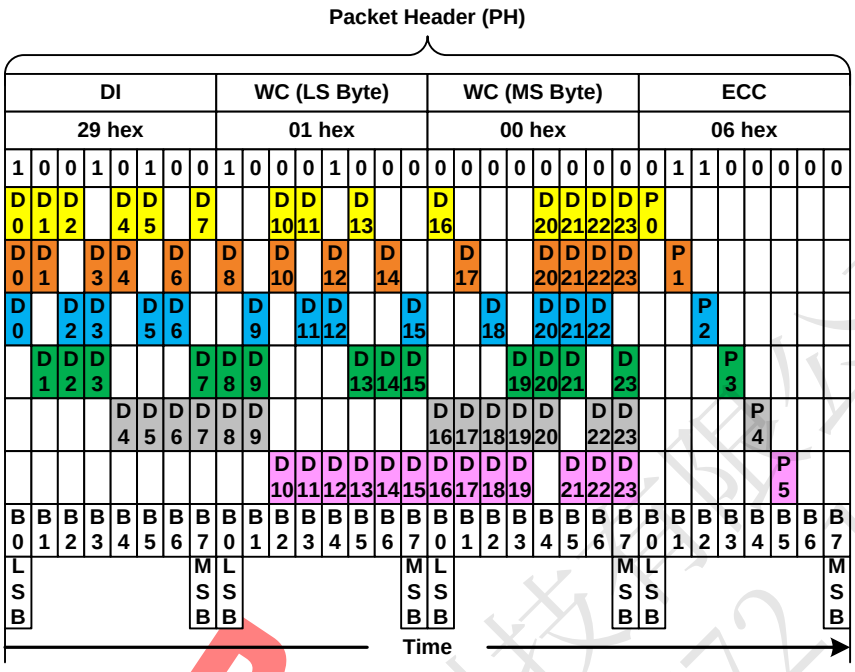


Figure 56 XOR Functionality on the Long Packet (LPa)

The transmitter (The MCU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

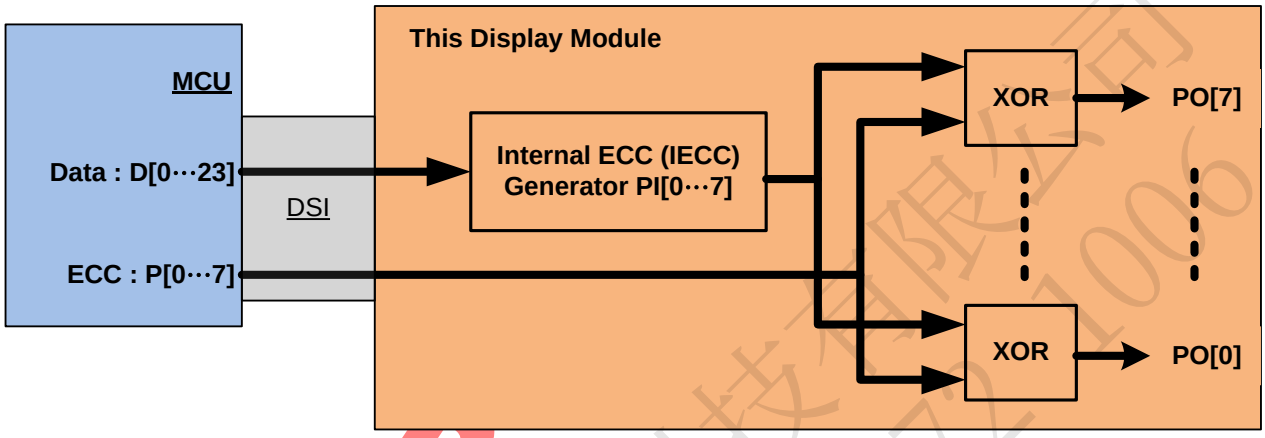


Figure 57 Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 0 0h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC) =>PO[7…0]	0	0	0	0	0	0	0	0	=00h=>No Error
	L S B							M S B	

Internal XOR Calculation between ECC and IECC Values-No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC) =>PO[7…0]	0	0	1	1	0	0	0	0	=0Ch=> Error
	L S B							M S B	

Internal XOR Calculation between ECC and IECC Values- Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7…0] is on : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

• PO[7…0] = 0Eh

• The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

5.4.2.3.1.4 Packet Date (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

5.4.2.3.1.5 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

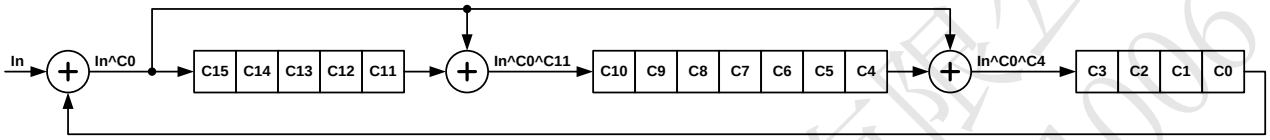


Figure 58 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.

Step	In	In^C0	C15	C14	C13	C12	C11	In^C0^C11	C10	C9	C8	C7	C6	C5	C4	In^C0^C4	C3	C2	C1	C0
0	1(LSB)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1
5	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
6	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
7	0(MSB)	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
8	X	X	0	0	0	1	1	X	1	1	0	0	0	0	0	X	1	1	1	0
CRC Result:			0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0
			MSB																	LSB

Figure 59 CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is Illustrated below.

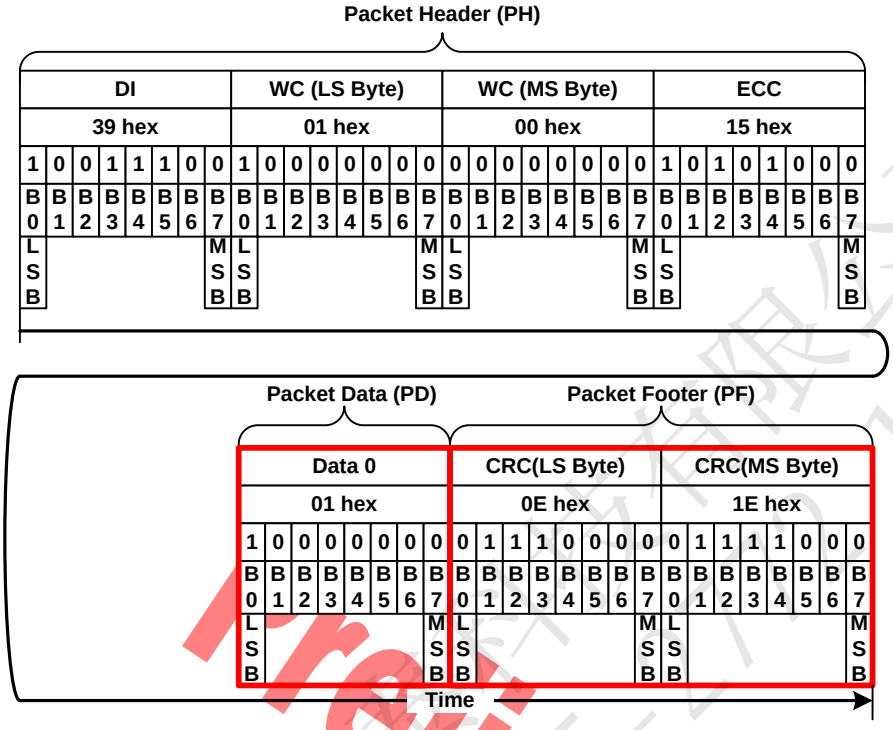


Figure 60 Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.4.2.3.2 Packet Transmissions

5.4.2.3.2.1 Packet from the MCU to the Display Module

- **Display Command Set (DCS)**

Display Command Set (DCS), which is defined on chapter “Command Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD),which is included in Short Packet (SPa) and Long Packet (LPa) as these are illustrated below.

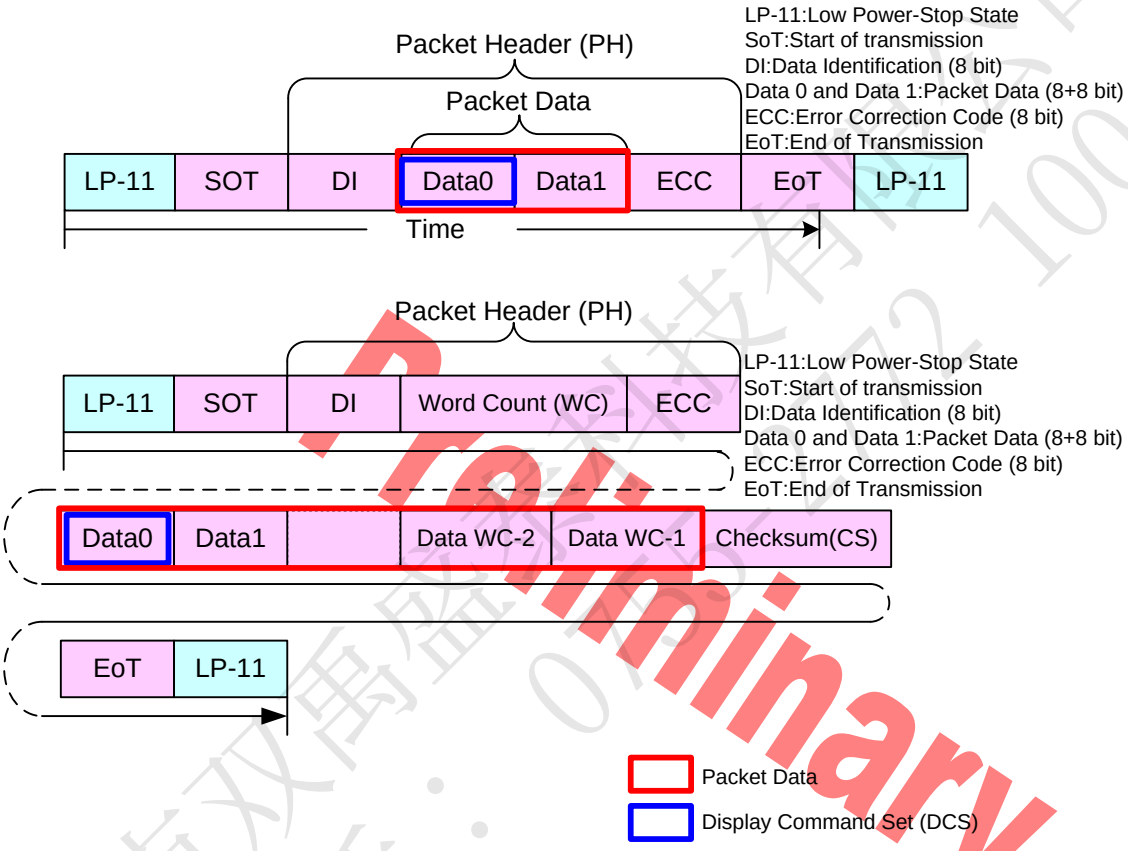


Figure 61 Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

5.4.2.3.2.2 Packet from the Display Module to the MCU

- **Used Packet Types**

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) or an Acknowledge with Error Report.

The used packet type is defined on Data Type (DT).

A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

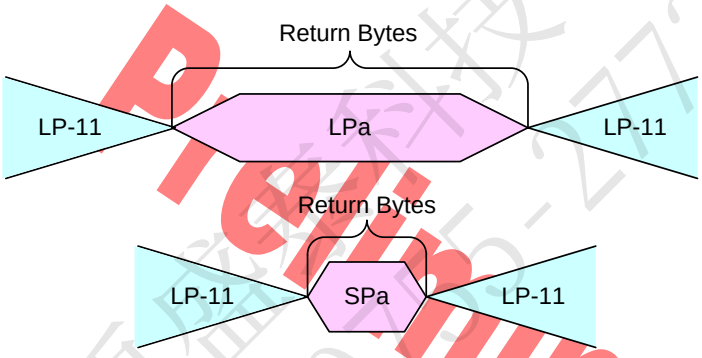


Figure 62 Return Bytes on Signal Packet

From the Display Module (or Other Devices) to the MCU									
Data Type Hex	B 5	B 4	B 3	B 2	B 1	B 0	Description	Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge and Error Report	Short	AwER
11h	0	1	0	0	0	1	Generic Short READ Response,1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Short READ Response,2 bytes returned	Short	GENRR2-S
1Ah	0	1	1	0	1	0	Generic Long READ Response	Short	GENRR-L
1Ch	0	1	1	1	0	0	DCS Long READ Response	Short	DCSRR_L
21h	1	0	0	0	0	1	DCS Short READ Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Short READ Response, 2 bytes returned	Short	DCSRR2_S

Data Type for Display Module-sourced Packets

The display module is return 2 packets (1st packet: Data, 2nd packet: Acknowledge with Error Report) to the MCU when the display module has received a read command. These return packets are illustrated for reference purpose below.

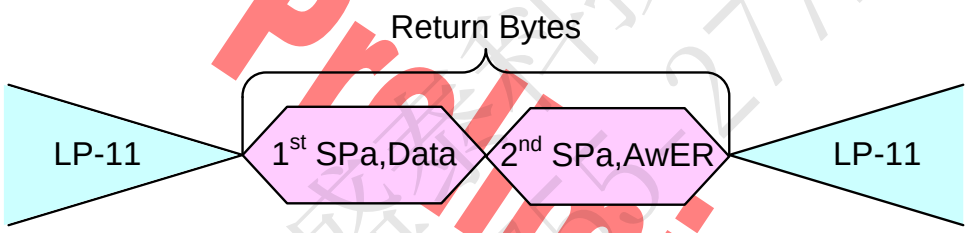


Figure 63 Exception When Return Bytes on Several Packet

Note:

1. AwER=Acknowledge with Error Report

- **Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)**

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT,00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

Bit	Description	Sitronix LCD Driver Implementation
0	SoT Error	NO
1	SoT Sync Error	NO
2	EoT Sync Error	NO
3	Escape Mode Entry Command Error	YES
4	Low-Power Transmit Sync Error	YES
5	Any Protocol Timer Time-Out	NO
6	False Control Error	YES
7	Contention is Detected on the Display Module	NO
8	ECC Error, single-bit (detected and corrected)	YES
9	ECC Error, multi-bit (detected, not corrected)	YES
10	Set to "0" internally (Only for Long Packet (LP))	YES
11	DSI Data Type (DT) Not Recognized	YES
12	DSI Virtual Channel (VC) ID Invalid	YES
13	Invalid Transmission Length	NO
14	Reserved, Set to '0' internally	NO
15	DSI Protocol Violation	NO

Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

Note

AwER will return1-bit zero if the item is no implementation.

These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

• Data Identification (DI)

Virtual Channel (VC, DI[7…6]): 00b

Data Type (DT, DI[5…0]): 00 0010b

• Packet Data (PD):

Bit 8: ECC Error, single-bit (detected and corrected)

AwER: 0100h

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

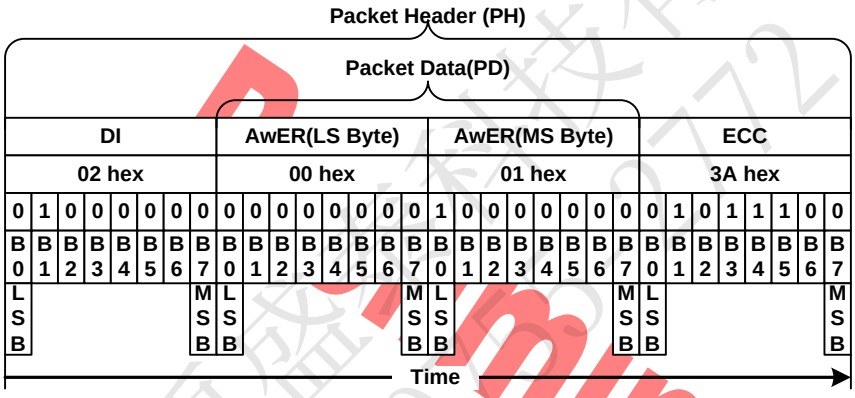


Figure 64 Acknowledge with Error Report (AwER)-Example

It is possible that the display module receivers several packets, which include error, from the MPU before the MPU performs the Bus Turnaround (BTA).Some examples are illustrated below for reference purpose.

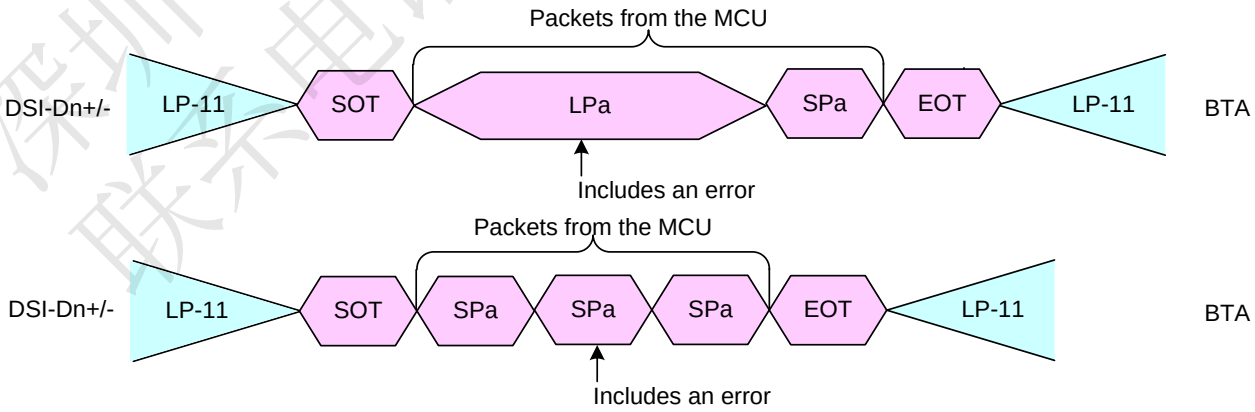


Figure 65 Error Packet

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Number of the Errors on DSI (05h)" command.

The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h after the MCU has read the RDNUMED register from the display module.

5.5 Serial Interface_ Control Bus (RGB_video / MIPI video)

The serial interface is either SPI9, SPI16 or SPI4/8-bits interface for communication between the micro controller and the LCD driver. The SPI9,SPI16 serial interface use: CSX (chip enable), SCL (serial clock) , SDA (serial data input) and SDO(serial data output), and the SPI8 serial interface use: CSX (chip enable), D/CX (data/ command flag), SCL (serial clock) , SDA (serial data input) and SDO(serial data output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

Pin description

SPI9_3-line serial interface (9 bits) & SPI16_3-line serial interface (16 bits)

Pin Name	Description
CSX	Chip selection signal
SCL	Serial input CLK
SDA	Serial input data
SDO	Serial output data

SPI8_4-line serial interface (8 bits)

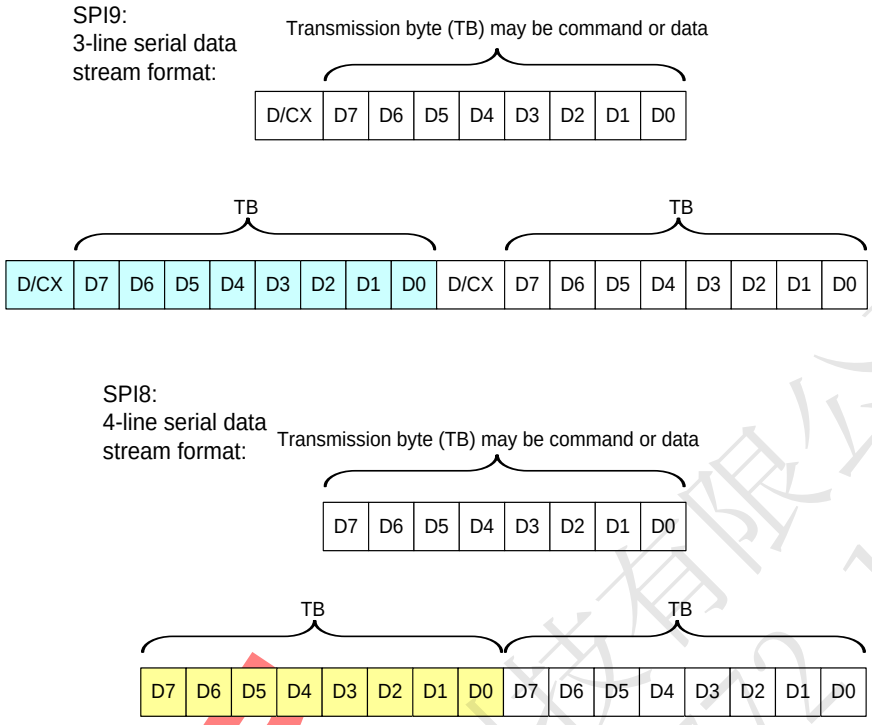
Pin Name	Description
CSX	Chip selection signal
DCX	Data is regarded as a command when SCL is low Data is regarded as a parameter or data when SCL is high
SCL	Clock signal
SDA	Serial input data
SDO	Serial output data

5.5.1 SPI Write mode

5.5.1.1 SPI8 & SPI9

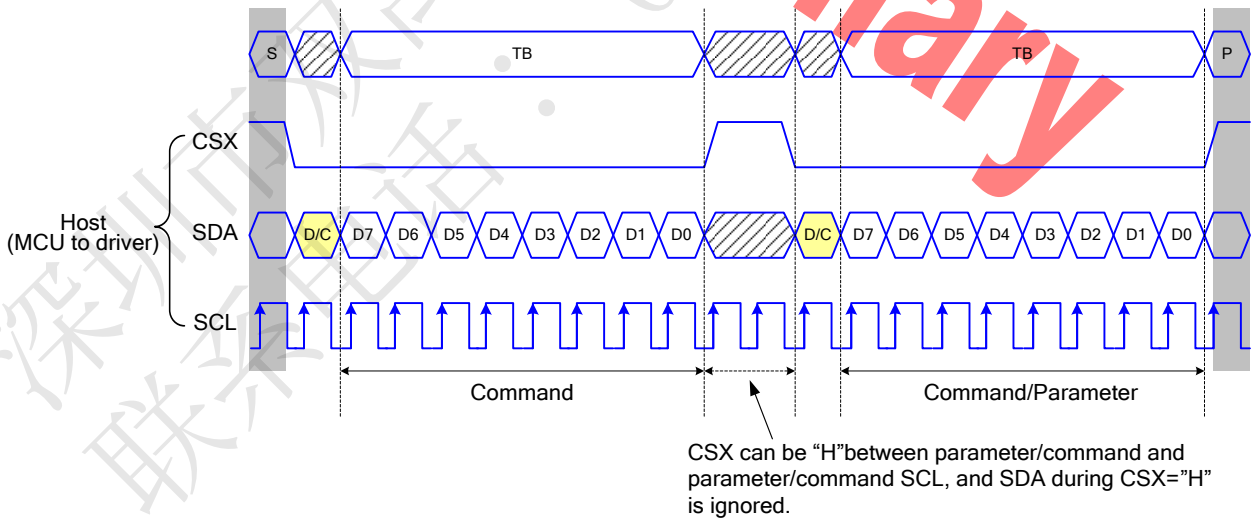
The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. In 4-lines serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

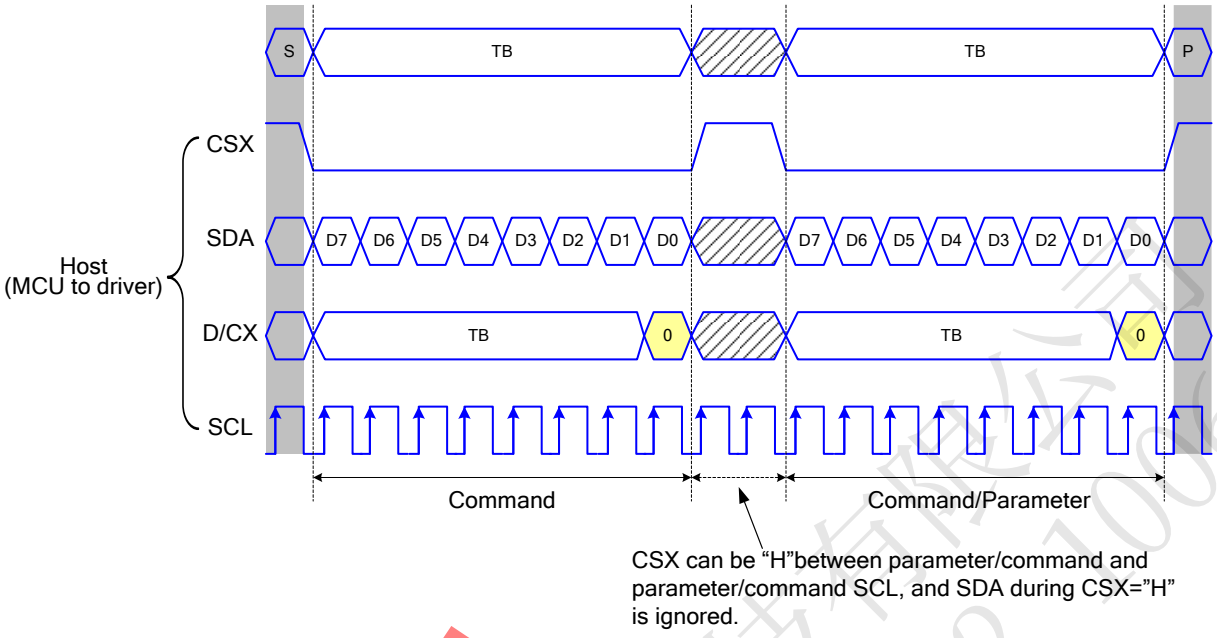


Serial interface data stream format

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX=’0’) or parameter data (D/CX=’1’). D/CX is sampled when first rising edge of SCL (SPI9:3-line serial interface) or 8th rising edge of SCL (SPI8:4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (SPI9:3-line serial interface) or D7 (SPI8:4-line serial interface) of the next byte at the next rising edge of SCL..



SPI9:3-line serial interface write protocol (write to register with control bit in transmission)

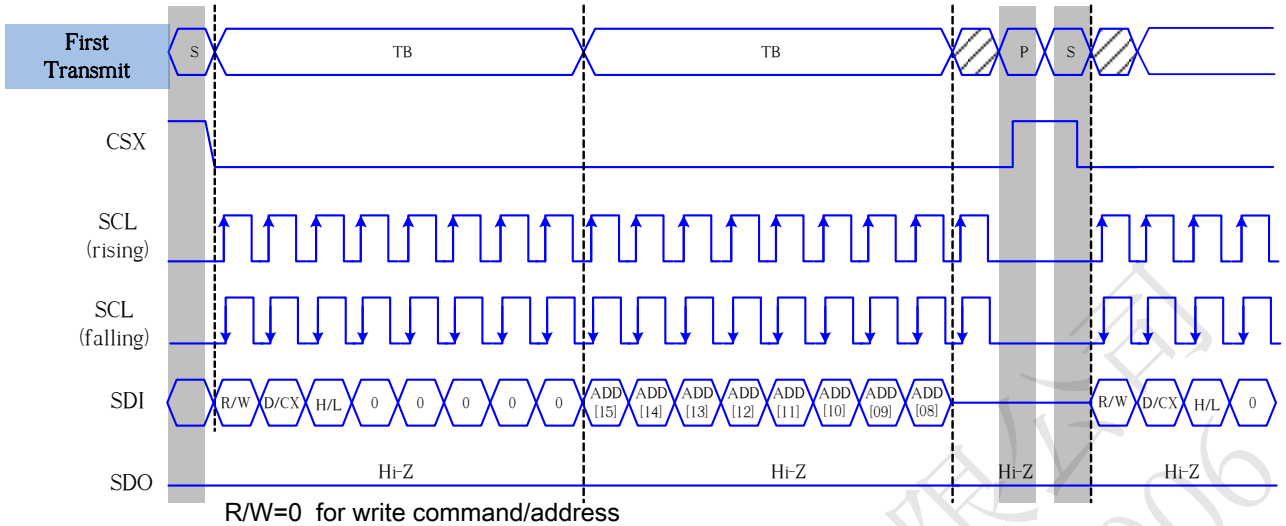


SPI8:4-line serial interface write protocol (write to register with control bit in transmission)

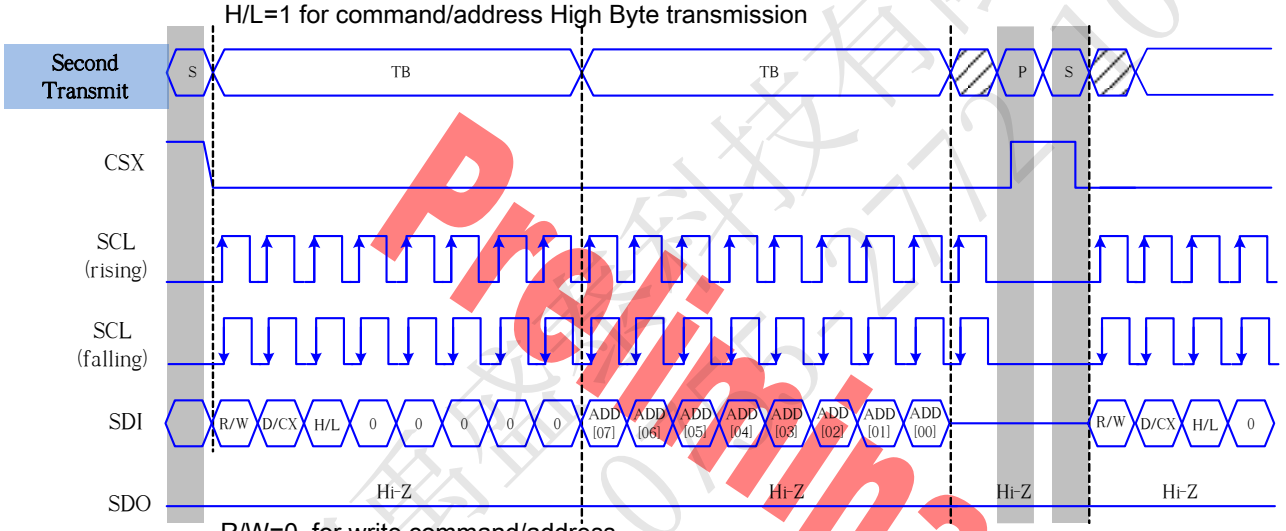
5.5.1.2 SPI16

The write mode of the interface means the micro controller writes commands and data to the ST7102. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

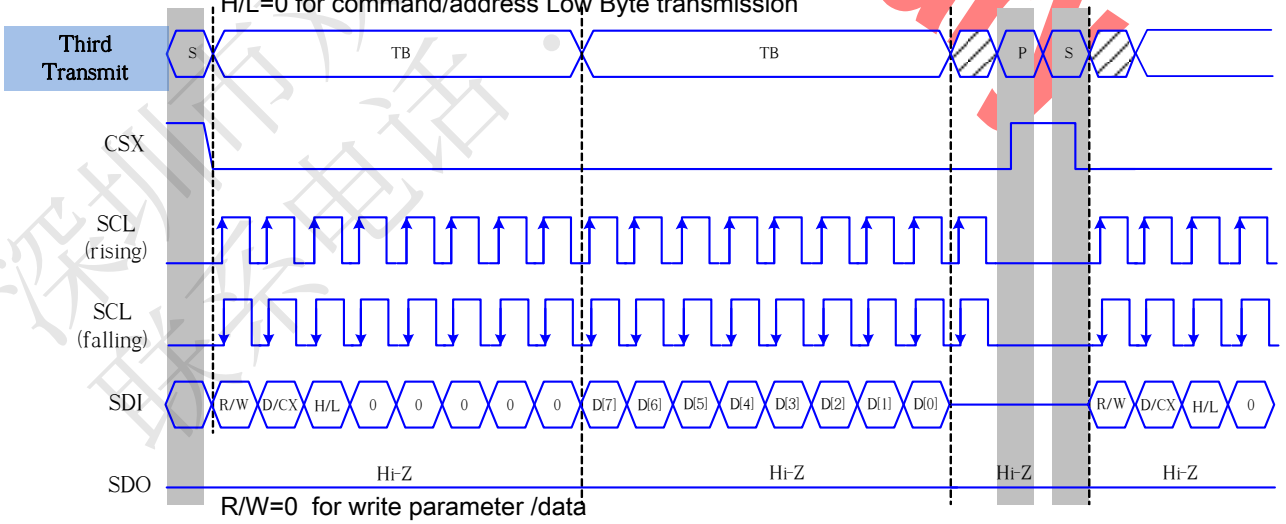
When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low. SDI/SDO are sampled at the rising edge of SCL. R/W indicates, whether the byte is read command (R/W = '1') or write command (R/W = '0'). It is sampled when first rising SCL edge. If CSX stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising edge of SCL



R/W=0 for write command/address
D/CX=0 for command /address transmission
H/L=1 for command/address High Byte transmission



R/W=0 for write command/address
D/CX=0 for command /address transmission
H/L=0 for command/address Low Byte transmission



R/W=0 for write parameter /data
D/CX=1 for parameter /data transmission
H/L=0 for parameter /data Low Byte transmission

serial 16 bit interface write mode

5.5.2 SPI Read mode

5.5.2.1 SPI8 & SPI9

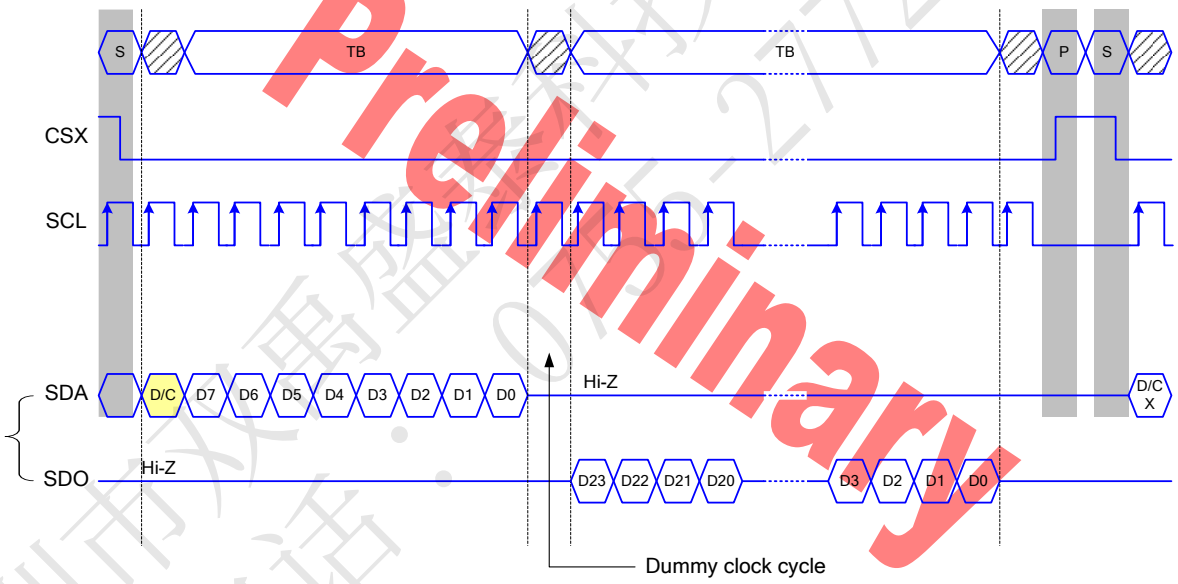
The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDO (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

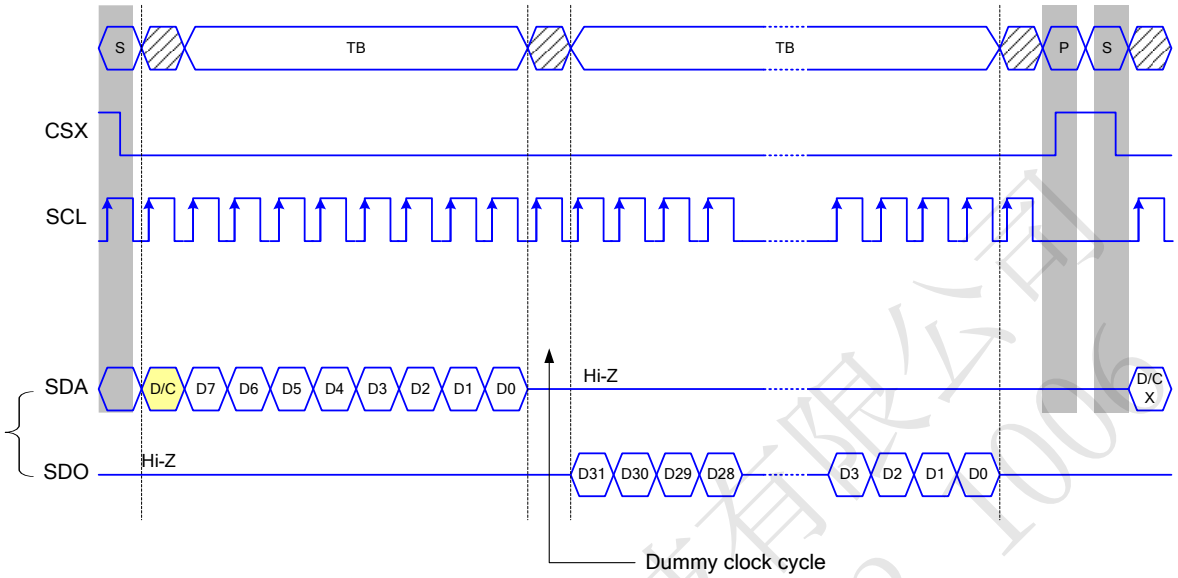
SPI9:3-line serial interface protocol

SPI9:3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):

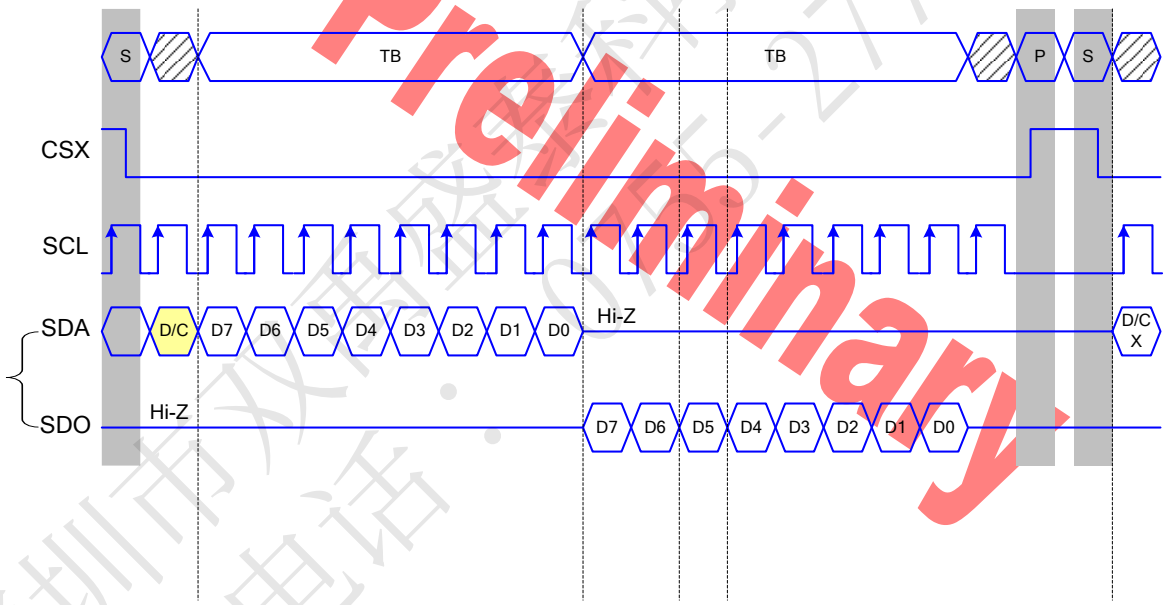
SPI9:3-line serial protocol (for RDDID command: 24-bit read)



SPI9:3-line Serial Protocol (for RDDST command: 32-bit read)

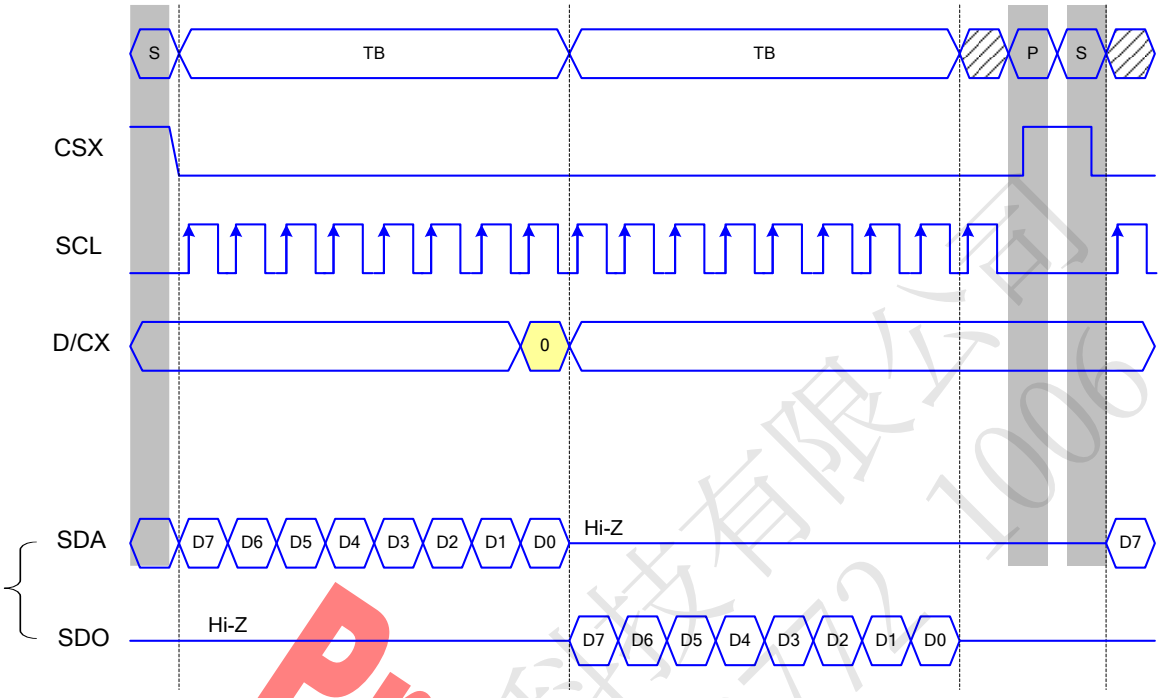


SPI9:3-line serial interface read protocol

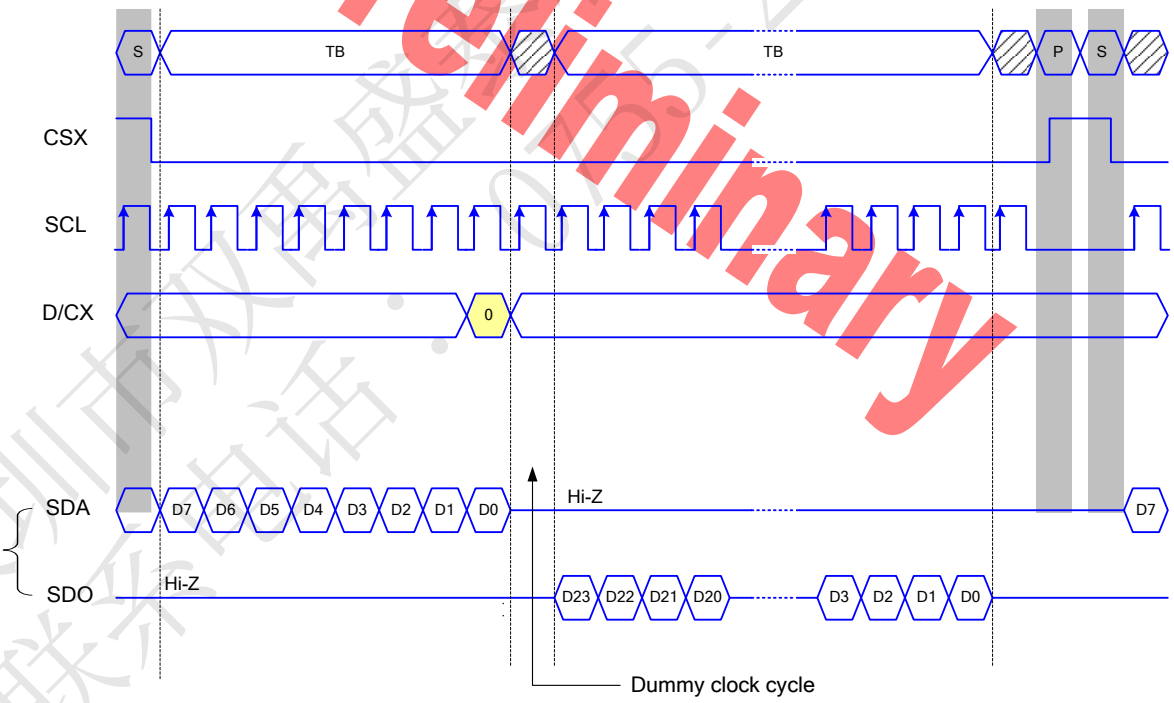


SPI8:4-line serial protocol

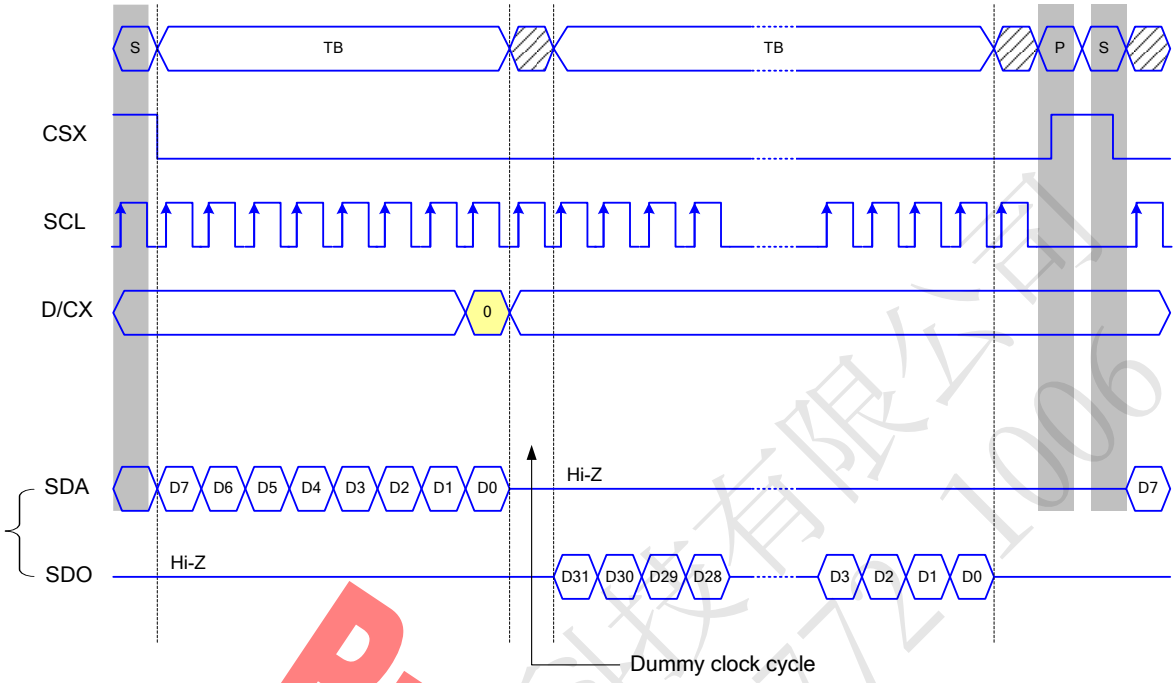
SPI8:4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



SPI8:4-line serial protocol (for RDDID command: 24-bit read)



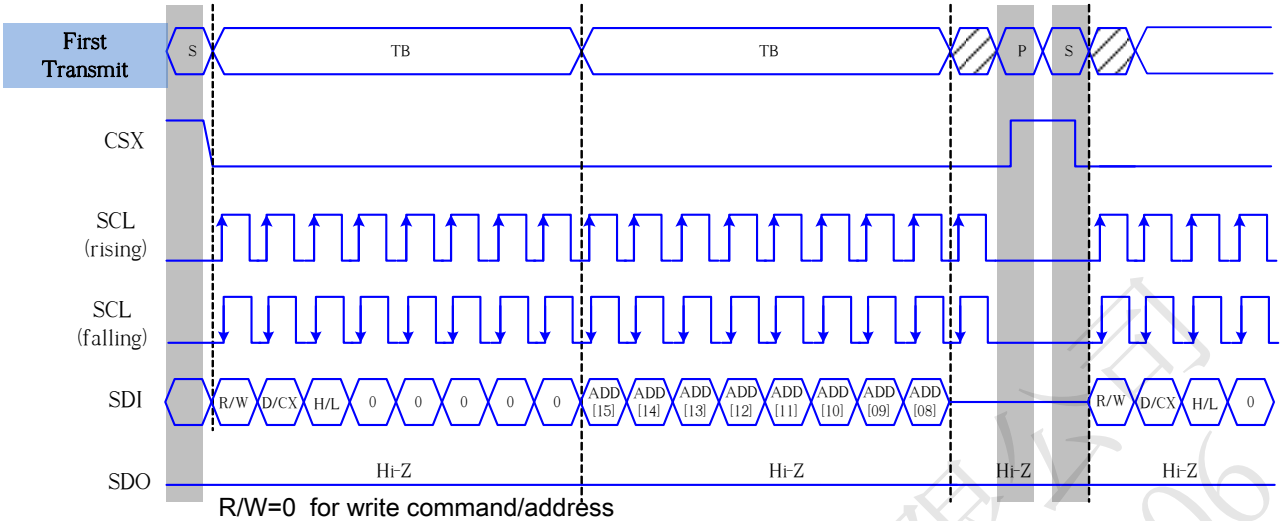
SPI8:4-line Serial Protocol (for RDDST command: 32-bit read)



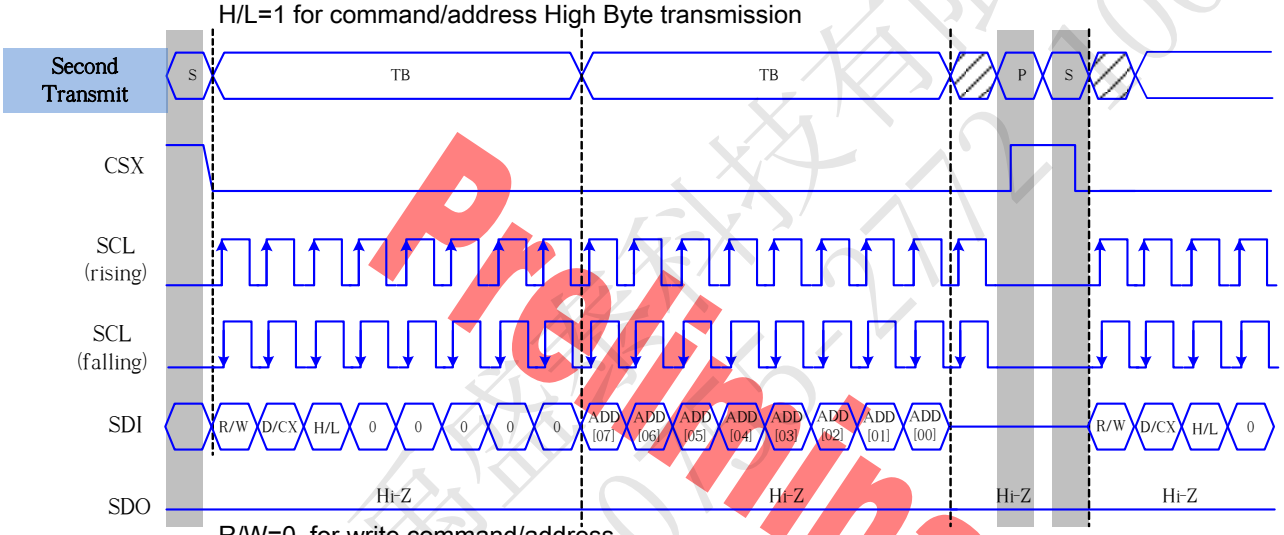
SPI8:4-line serial interface read protocol

5.5.2.1 SPI16

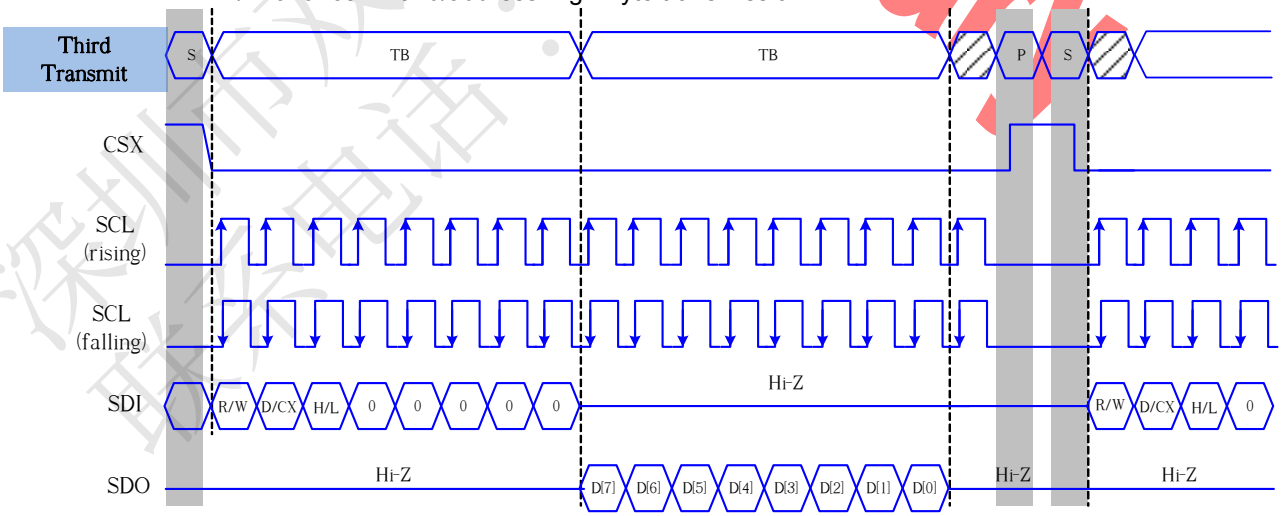
The read mode of the interface means that the micro controller reads register value from the IC. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send. The IC samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. It doesn't need any dummy clock when execute the command data read.



R/W=0 for write command/address
D/CX=0 for command /address transmission
H/L=1 for command/address High Byte transmission



R/W=0 for write command/address
D/CX=0 for command /address transmission
H/L=0 for command/address High Byte transmission



R/W=1 for read command/address
D/CX=0 for command /address transmission
H/L=0 for command/address High Byte transmission

5.6 RGB Interface

The ST7102 support RGB interface Mode 1 and Mode 2. The interface signals as shown in following table.

The Mode 1 and Mode 2 function is select by setting in the Command 2, please reference application note.

In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D[23:0]), when Enable is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to ST7102.

In RGB Mode 2, back porch of Vsync is defined by VBP_HVRGB [7:0] of RGBCTR command. And back porch of Hsync is defined by HBP_HVRGB [7:0] of RGBCTR command. Front porch of Vsync are not setting by this mode

RGB I/F Mode	PCLK	DE	VS	HS	DB[23:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Symbol	Name	Description
PCLK	Pixel clock	Pixel clock for capturing pixels at display interface
HS	Horizontal sync	Horizontal synchronization timing signal
VS	Vertical sync	Vertical synchronization timing signal
DE	Data enable	Data enable signal (assertion indicates valid pixels)
DB[23:0]	Pixel data	Pixel data in 16-bit,18-bit and 24-bit format

The interface signals of RGB interface

5.6.1 RGB Color Format

ST7102 supports two kinds of RGB interface, DE mode (mode 1) and HV mode (mode 2), and 16bit/18bit and 24 bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, ENABLE, D[23:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, PCLK, D[23:0] pins can be used. When using RGB interface, only serial interface can be selected.

Pad name	24 bits configuration VIPF[3:0]=0111	18 bits configuration VIPF[3:0]=0110		16 bits configuration VIPF[3:0]=0101
		MDT=0	MDT=1	
DB[23]	R7	Not used	Not used	Not used
DB[22]	R6	Not used	Not used	Not used
DB[21]	R5	R5	Not used	Not used
DB[20]	R4	R4	Not used	R4
DB[19]	R3	R3	Not used	R3
DB[18]	R2	R2	Not used	R2
DB[17]	R1	R1	R5	R1
DB[16]	R0	R0	R4	R0
DB[15]	G7	Not used	R3	Not used
DB[14]	G6	Not used	R2	Not used
DB[13]	G5	G5	R1	G5
DB[12]	G4	G4	R0	G4
DB[11]	G3	G3	G5	G3
DB[10]	G2	G2	G4	G2
DB[09]	G1	G1	G3	G1
DB[08]	G0	G0	G2	G0
DB[07]	B7	Not used	G1	Not used
DB[06]	B6	Not used	G0	Not used
DB[05]	B5	B5	B5	Not used
DB[04]	B4	B4	B4	B4
DB[03]	B3	B3	B3	B3
DB[02]	B2	B2	B2	B2
DB[01]	B1	B1	B1	B1
DB[00]	B0	B0	B0	B0

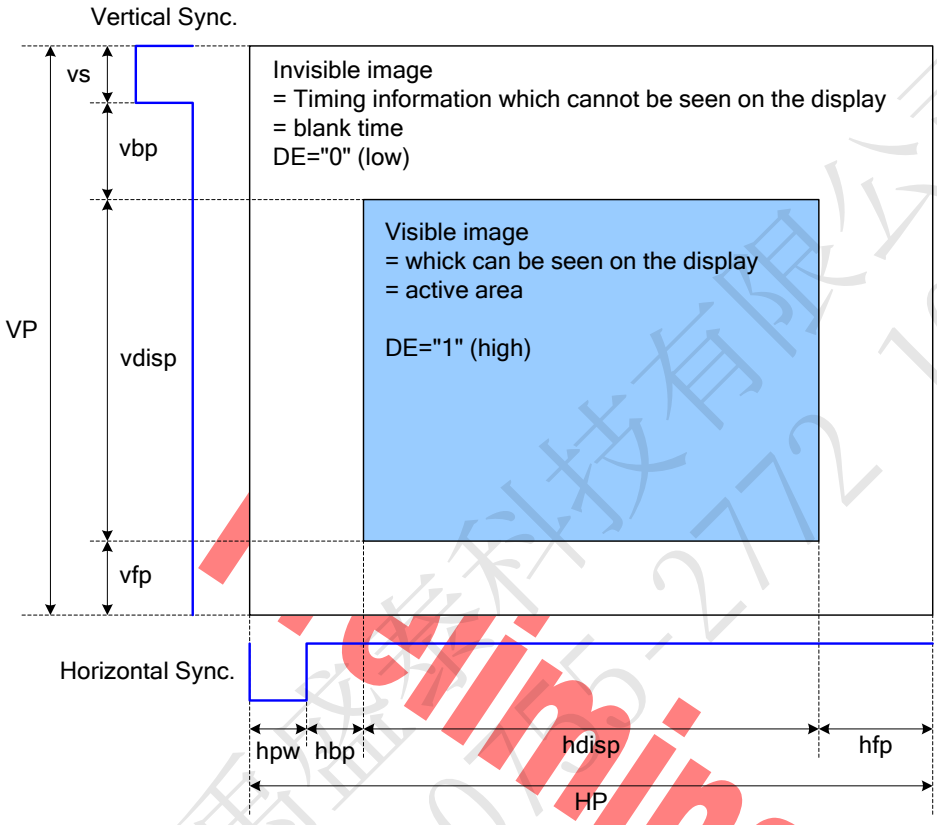
The interface color mapping of RGB interface

Other Application TABLE

Pad name	24 bits configuration VIPF[3:0]=0111		
	For 24 Bit	For 18 Bit	For 16 Bit
DB[23]	R7	R5	R4
DB[22]	R6	R4	R3
DB[21]	R5	R3	R2
DB[20]	R4	R2	R1
DB[19]	R3	R1	R0
DB[18]	R2	R0	R4
DB[17]	R1	R5	R3
DB[16]	R0	R4	R2
DB[15]	G7	G5	G5
DB[14]	G6	G4	G4
DB[13]	G5	G3	G3
DB[12]	G4	G2	G2
DB[11]	G3	G1	G1
DB[10]	G2	G0	G0
DB[09]	G1	G5	G5
DB[08]	G0	G4	G4
DB[07]	B7	B5	B4
DB[06]	B6	B4	B3
DB[05]	B5	B3	B2
DB[04]	B4	B2	B1
DB[03]	B3	B1	B0
DB[02]	B2	B0	B4
DB[01]	B1	B5	B3
DB[00]	B0	B4	B2

5.6.2 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and PCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.



Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	2	-	TBD	Clock
Horizontal Sync. Back Porch	hbp	2	--	TBD	Clock
Horizontal Sync. Front Porch	hfp	2	--	-	Clock
Vertical Sync. Width	vs	2	--	TBD	Line
Vertical Sync. Back Porch	vbp	2	--	TBD	Line
Vertical Sync. Front Porch	vfp	2	--	--	Line

Note:

1、Typical value are related to the setting frame rate is 60Hz..

2、VS+VBP<= TBD, *HPW+HBP<=* TBD

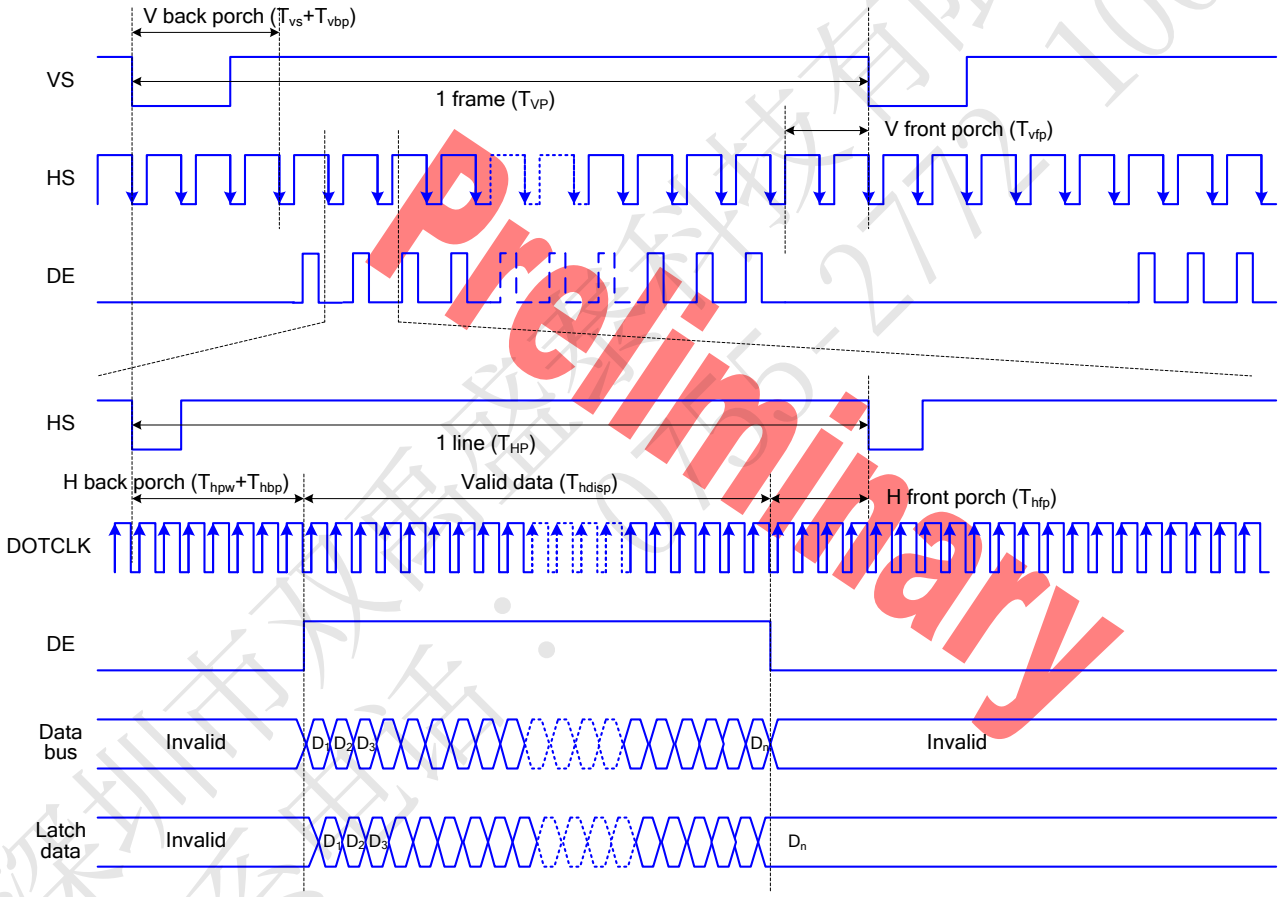
5.6.1 RGB Interface Mode Selection

ST7102 supports two kinds of RGB interface, DE mode and HV mode. The table shown below uses command C3h to select RGB interface mode.

DE/HV(Sync)	RGB Mode
0	DE mode
1	HV mode

RGB Interface Timing

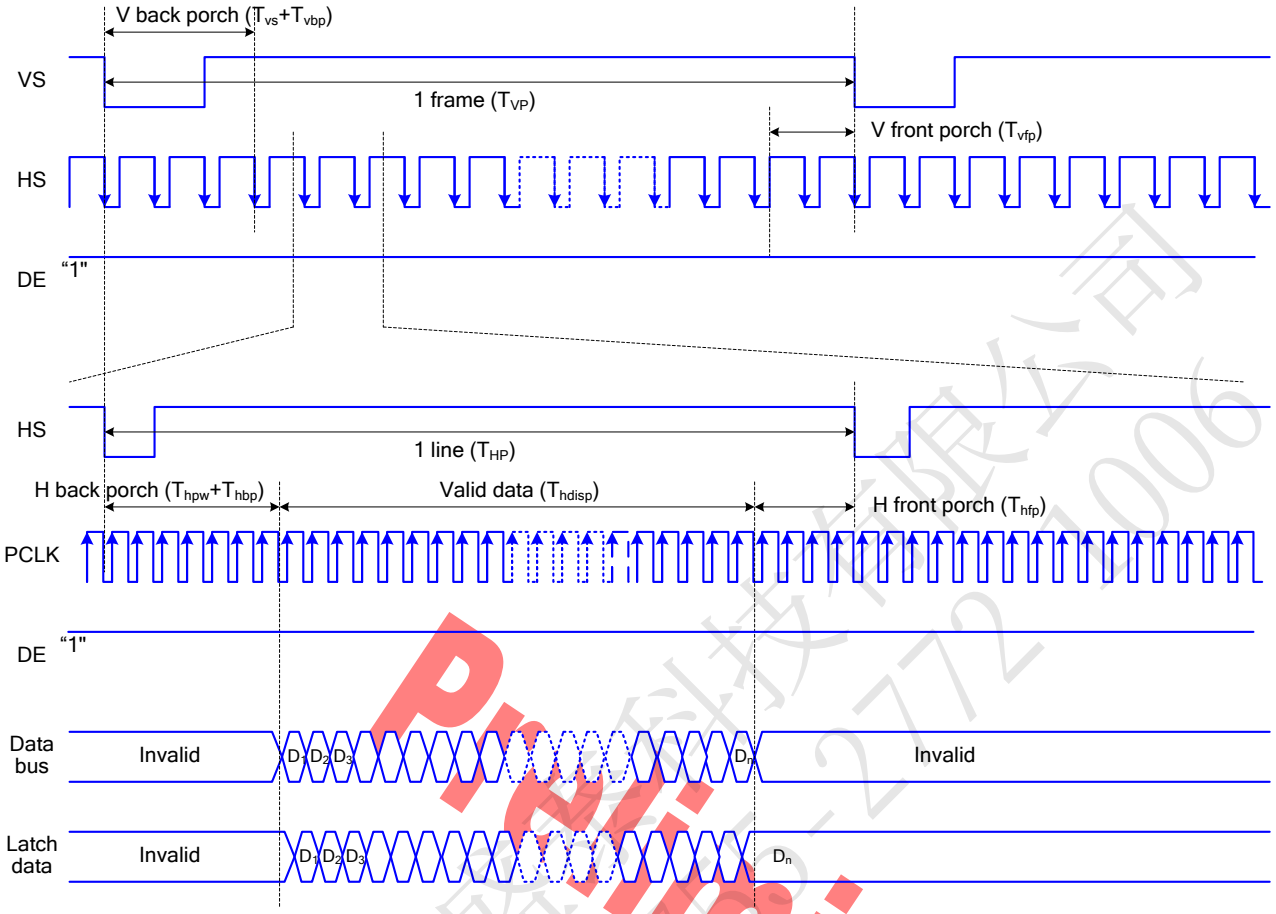
The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.

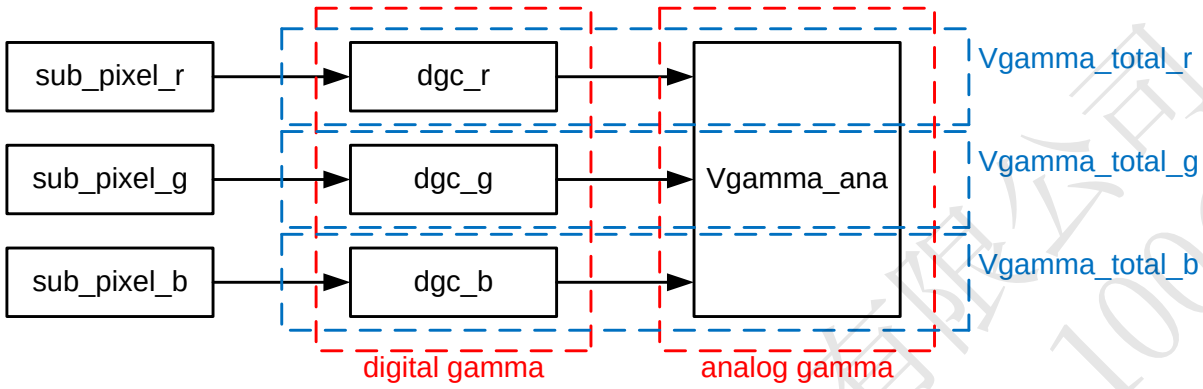


Timing chart of RGB interface HV mode

5.7 Digital Gamma

Digital gamma correct makes three sub-pixel (Red, Green, Blue) gamma curve by using one analog gamma curve.

By setting the digital gamma correction registers we can make three equivalent gamma curve Vgamma_total_r, Vgamma_total_g, Vgamma_total_b as desired.



5.8 Gamma Correction Function

ST7102 incorporates the gamma correction function to display 16,777,216 colors for the LCD panel. There is a analog gamma correction is performed with 2 registers to set both positive and negative polarity voltage for gamma curve.

5.8.1 Gamma Correction Registers

The all of grayscale reference levels are shown blow.

Register Groups	Gamma Polarity		Description
	Positive	Negative	
Grayscale adjustment	VGMP0[9:0]	VGMN0[9:0]	1023-to-1 selector (voltage level of R grayscale 0)
	VGMP1[9:0]	VGMN1[9:0]	1023-to-1 selector (voltage level of R grayscale 1)
	VGMP2[9:0]	VGMN2[9:0]	1023-to-1 selector (voltage level of R grayscale 2)
	VGMP3[9:0]	VGMN3[9:0]	1023-to-1 selector (voltage level of R grayscale 4)
	VGMP4[9:0]	VGMN4[9:0]	1023-to-1 selector (voltage level of R grayscale 8)
	VGMP5[5:0]	VGMN5[5:0]	1023-to-1 selector (voltage level of R grayscale 12)
	VGMP6[9:0]	VGMN6[9:0]	1023-to-1 selector (voltage level of R grayscale 16)
	VGMP7[5:0]	VGMN7[5:0]	1023-to-1 selector (voltage level of R grayscale 24)
	VGMP8[9:0]	VGMN8[9:0]	1023-to-1 selector (voltage level of R grayscale 32)
	VGMP9[5:0]	VGMN9[5:0]	1023-to-1 selector (voltage level of R grayscale 48)
	VGMP10[9:0]	VGMN10[9:0]	1023-to-1 selector (voltage level of R grayscale 64)
	VGMP11[3:0]	VGMN11[3:0]	1023-to-1 selector (voltage level of R grayscale 80)
	VGMP12[9:0]	VGMN12[9:0]	1023-to-1 selector (voltage level of R grayscale 96)
	VGMP13[3:0]	VGMN13[3:0]	1023-to-1 selector (voltage level of R grayscale 112)
	VGMP14[9:0]	VGMN14[9:0]	1023-to-1 selector (voltage level of R grayscale 128)
	VGMP15[3:0]	VGMN15[3:0]	1023-to-1 selector (voltage level of R grayscale 144)
	VGMP16[9:0]	VGMN16[9:0]	1023-to-1 selector (voltage level of R grayscale 160)
	VGMP17[3:0]	VGMN17[3:0]	1023-to-1 selector (voltage level of R grayscale 176)
	VGMP18[9:0]	VGMN18[9:0]	1023-to-1 selector (voltage level of R grayscale 192)
	VGMP19[3:0]	VGMN19[3:0]	1023-to-1 selector (voltage level of R grayscale 208)
	VGMP20[9:0]	VGMN20[9:0]	1023-to-1 selector (voltage level of R grayscale 224)
	VGMP21[3:0]	VGMN21[3:0]	1023-to-1 selector (voltage level of R grayscale 232)
	VGMP22[9:0]	VGMN22[9:0]	1023-to-1 selector (voltage level of R grayscale 240)
	VGMP23[3:0]	VGMN23[3:0]	1023-to-1 selector (voltage level of R grayscale 244)
	VGMP24[9:0]	VGMN24[9:0]	1023-to-1 selector (voltage level of R grayscale 248)
	VGMP25[3:0]	VGMN25[3:0]	1023-to-1 selector (voltage level of R grayscale 250)

	VGMP26[9:0]	VGMN26[9:0]	1023-to-1 selector (voltage level of R grayscale 252)
	VGMP27[9:0]	VGMN27[9:0]	1023-to-1 selector (voltage level of R grayscale 254)
	VGMP28[9:0]	VGMN28[9:0]	1023-to-1 selector (voltage level of R grayscale 255)

5.8.2 Gamma function architecture

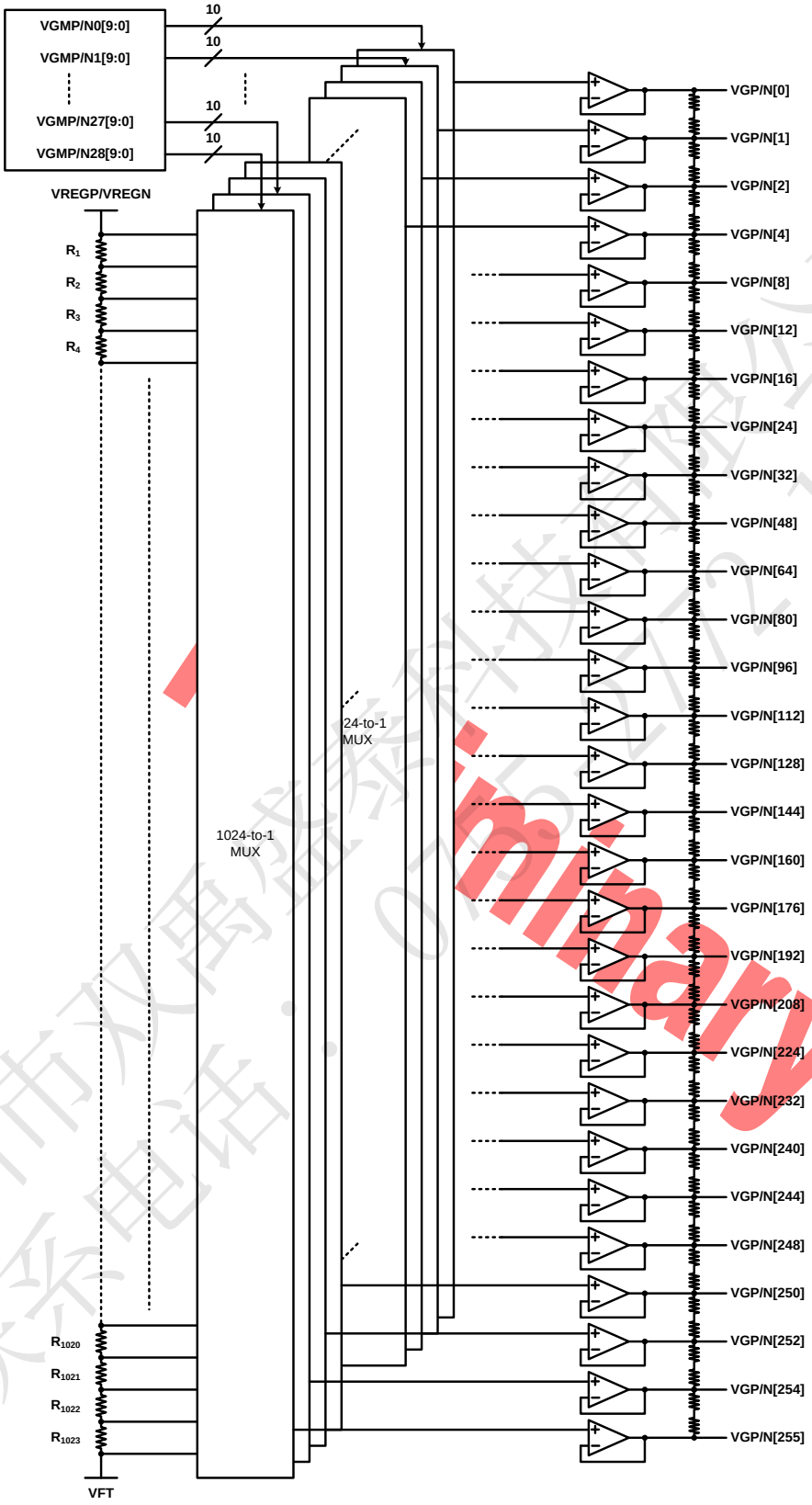


Figure 66 positive and Negative grayscale voltage generation

Note1. VFT: Feed through voltage

Note2.VREGP: VFT+VGPAMP=feed through voltage + positive gamma amplitude.

Note3.VREGN: VFT+VGNAMP=feed through voltage + negative gamma amplitude.

5.8.3 Grayscale voltage formula

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	VGP/N0	V64	VGP/N10
V1	VGP/N1	V65	15/16 * VGP/N10 + 1/16 * VGP/N11
V2	VGP/N2	V66	14/16 * VGP/N10 + 2/16 * VGP/N11
V3	1/2 * VGP/N2 + 1/2* VGP/N3	V67	13/16 * VGP/N10 + 3/16 * VGP/N11
V4	VGP/N3	V68	12/16 * VGP/N10 + 4/16 * VGP/N11
V5	3/4 * VGP/N3 + 1/4* VGP/N4	V69	11/16 * VGP/N10 + 5/16 * VGP/N11
V6	2/4 * VGP/N3 + 2/4* VGP/N4	V70	10/16 * VGP/N10 + 6/16 * VGP/N11
V7	1/4 * VGP/N3 + 3/4* VGP/N4	V71	9/16 * VGP/N10 + 7/16 * VGP/N11
V8	VGP/N4	V72	8/16 * VGP/N10 + 8/16 * VGP/N11
V9	3/4 * VGP/N4 + 1/4* VGP/N5	V73	7/16 * VGP/N10 + 9/16 * VGP/N11
V10	2/4 * VGP/N4 + 2/4* VGP/N5	V74	6/16 * VGP/N10 + 10/16 * VGP/N11
V11	1/4 * VGP/N4 + 3/4* VGP/N5	V75	5/16 * VGP/N10 + 11/16 * VGP/N11
V12	VGP/N5	V76	4/16 * VGP/N10 + 12/16 * VGP/N11
V13	3/4 * VGP/N5 + 1/4* VGP/N6	V77	3/16 * VGP/N10 + 13/16 * VGP/N11
V14	2/4 * VGP/N5 + 2/4* VGP/N6	V78	2/16 * VGP/N10 + 14/16 * VGP/N11
V15	1/4 * VGP/N5 + 3/4* VGP/N6	V79	1/16 * VGP/N10 + 15/16 * VGP/N11
V16	VGP/N6	V80	VGP/N11
V17	7/8 * VGP/N6 + 1/8 * VGP/N7	V81	15/16 * VGP/N11 + 1/16 * VGP/N12
V18	6/8 * VGP/N6 + 2/8 * VGP/N7	V82	14/16 * VGP/N11 + 2/16 * VGP/N12
V19	5/8 * VGP/N6 + 3/8 * VGP/N7	V83	13/16 * VGP/N11 + 3/16 * VGP/N12
V20	4/8 * VGP/N6 + 4/8 * VGP/N7	V84	12/16 * VGP/N11 + 4/16 * VGP/N12
V21	3/8 * VGP/N6 + 5/8 * VGP/N7	V85	11/16 * VGP/N11 + 5/16 * VGP/N12
V22	2/8 * VGP/N6 + 6/8 * VGP/N7	V86	10/16 * VGP/N11 + 6/16 * VGP/N12
V23	1/8 * VGP/N6 + 7/8 * VGP/N7	V87	9/16 * VGP/N11 + 7/16 * VGP/N12
V24	VGP/N7	V88	8/16 * VGP/N11 + 8/16 * VGP/N12
V25	7/8 * VGP/N7 + 1/8 * VGP/N8	V89	7/16 * VGP/N11 + 9/16 * VGP/N12
V26	6/8 * VGP/N7 + 2/8 * VGP/N8	V90	6/16 * VGP/N11 + 10/16 * VGP/N12

V27	5/8 * VGP/N7 + 3/8 * VGP/N8	V91	5/16 * VGP/N11 + 11/16 * VGP/N12
V28	4/8 * VGP/N7 + 4/8 * VGP/N8	V92	4/16 * VGP/N11 + 12/16 * VGP/N12
V29	3/8 * VGP/N7 + 5/8 * VGP/N8	V93	3/16 * VGP/N11 + 13/16 * VGP/N12
V30	2/8 * VGP/N7 + 6/8 * VGP/N8	V94	2/16 * VGP/N11 + 14/16 * VGP/N12
V31	1/8 * VGP/N7 + 7/8 * VGP/N8	V95	1/16 * VGP/N11 + 15/16 * VGP/N12
V32	VGP/N8	V96	VGP/N12
V33	15/16 * VGP/N8 + 1/16 * VGP/N9	V97	15/16 * VGP/N12 + 1/16 * VGP/N13
V34	14/16 * VGP/N8 + 2/16 * VGP/N9	V98	14/16 * VGP/N12 + 2/16 * VGP/N13
V35	13/16 * VGP/N8 + 3/16 * VGP/N9	V99	13/16 * VGP/N12 + 3/16 * VGP/N13
V36	12/16 * VGP/N8 + 4/16 * VGP/N9	V100	12/16 * VGP/N12 + 4/16 * VGP/N13
V37	11/16 * VGP/N8 + 5/16 * VGP/N9	V101	11/16 * VGP/N12 + 5/16 * VGP/N13
V38	10/16 * VGP/N8 + 6/16 * VGP/N9	V102	10/16 * VGP/N12 + 6/16 * VGP/N13
V39	9/16 * VGP/N8 + 7/16 * VGP/N9	V103	9/16 * VGP/N12 + 7/16 * VGP/N13
V40	8/16 * VGP/N8 + 8/16 * VGP/N9	V104	8/16 * VGP/N12 + 8/16 * VGP/N13
V41	7/16 * VGP/N8 + 9/16 * VGP/N9	V105	7/16 * VGP/N12 + 9/16 * VGP/N13
V42	6/16 * VGP/N8 + 10/16 * VGP/N9	V106	6/16 * VGP/N12 + 10/16 * VGP/N13
V43	5/16 * VGP/N8 + 11/16 * VGP/N9	V107	5/16 * VGP/N12 + 11/16 * VGP/N13
V44	4/16 * VGP/N8 + 12/16 * VGP/N9	V108	4/16 * VGP/N12 + 12/16 * VGP/N13
V45	3/16 * VGP/N8 + 13/16 * VGP/N9	V109	3/16 * VGP/N12 + 13/16 * VGP/N13
V46	2/16 * VGP/N8 + 14/16 * VGP/N9	V110	2/16 * VGP/N12 + 14/16 * VGP/N13
V47	1/16 * VGP/N8 + 15/16 * VGP/N9	V111	1/16 * VGP/N12 + 15/16 * VGP/N13
V48	VGP/N9	V112	VGP/N13
V49	15/16 * VGP/N9 + 1/16 * VGP/N10	V113	15/16 * VGP/N13 + 1/16 * VGP/N14
V50	14/16 * VGP/N9 + 2/16 * VGP/N10	V114	14/16 * VGP/N13 + 2/16 * VGP/N14
V51	13/16 * VGP/N9 + 3/16 * VGP/N10	V115	13/16 * VGP/N13 + 3/16 * VGP/N14
V52	12/16 * VGP/N9 + 4/16 * VGP/N10	V116	12/16 * VGP/N13 + 4/16 * VGP/N14
V53	11/16 * VGP/N9 + 5/16 * VGP/N10	V117	11/16 * VGP/N13 + 5/16 * VGP/N14
V54	10/16 * VGP/N9 + 6/16 * VGP/N10	V118	10/16 * VGP/N13 + 6/16 * VGP/N14
V55	9/16 * VGP/N9 + 7/16 * VGP/N10	V119	9/16 * VGP/N13 + 7/16 * VGP/N14
V56	8/16 * VGP/N9 + 8/16 * VGP/N10	V120	8/16 * VGP/N13 + 8/16 * VGP/N14
V57	7/16 * VGP/N9 + 9/16 * VGP/N10	V121	7/16 * VGP/N13 + 9/16 * VGP/N14
V58	6/16 * VGP/N9 + 10/16 * VGP/N10	V122	6/16 * VGP/N13 + 10/16 * VGP/N14
V59	5/16 * VGP/N9 + 11/16 * VGP/N10	V123	5/16 * VGP/N13 + 11/16 * VGP/N14
V60	4/16 * VGP/N9 + 12/16 * VGP/N10	V124	4/16 * VGP/N13 + 12/16 * VGP/N14
V61	3/16 * VGP/N9 + 13/16 * VGP/N10	V125	3/16 * VGP/N13 + 13/16 * VGP/N14
V62	2/16 * VGP/N9 + 14/16 * VGP/N10	V126	2/16 * VGP/N13 + 14/16 * VGP/N14

V63	1/16 * VGP/N9 + 15/16 * VGP/N10	V127	1/16 * VGP/N13 + 15/16 * VGP/N14

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V128	VGP/N14	V192	VGP/N18
V129	15/16 * VGP/N14 + 1/16 * VGP/N15	V193	15/16 * VGP/N18 + 1/16 * VGP/N19
V130	14/16 * VGP/N14 + 2/16 * VGP/N15	V194	14/16 * VGP/N18 + 2/16 * VGP/N19
V131	13/16 * VGP/N14 + 3/16 * VGP/N15	V195	13/16 * VGP/N18 + 3/16 * VGP/N19
V132	12/16 * VGP/N14 + 4/16 * VGP/N15	V196	12/16 * VGP/N18 + 4/16 * VGP/N19
V133	11/16 * VGP/N14 + 5/16 * VGP/N15	V197	11/16 * VGP/N18 + 5/16 * VGP/N19
V134	10/16 * VGP/N14 + 6/16 * VGP/N15	V198	10/16 * VGP/N18 + 6/16 * VGP/N19
V135	9/16 * VGP/N14 + 7/16 * VGP/N15	V199	9/16 * VGP/N18 + 7/16 * VGP/N19
V136	8/16 * VGP/N14 + 8/16 * VGP/N15	V200	8/16 * VGP/N18 + 8/16 * VGP/N19
V137	7/16 * VGP/N14 + 9/16 * VGP/N15	V201	7/16 * VGP/N18 + 9/16 * VGP/N19
V138	6/16 * VGP/N14 + 10/16 * VGP/N15	V202	6/16 * VGP/N18 + 10/16 * VGP/N19
V139	5/16 * VGP/N14 + 11/16 * VGP/N15	V203	5/16 * VGP/N18 + 11/16 * VGP/N19
V140	4/16 * VGP/N14 + 12/16 * VGP/N15	V204	4/16 * VGP/N18 + 12/16 * VGP/N19
V141	3/16 * VGP/N14 + 13/16 * VGP/N15	V205	3/16 * VGP/N18 + 13/16 * VGP/N19
V142	2/16 * VGP/N14 + 14/16 * VGP/N15	V206	2/16 * VGP/N18 + 14/16 * VGP/N19
V143	1/16 * VGP/N14 + 15/16 * VGP/N15	V207	1/16 * VGP/N18 + 15/16 * VGP/N19
V144	VGP/N15	V208	VGP/N19
V145	15/16 * VGP/N15 + 1/16 * VGP/N16	V209	15/16 * VGP/N19 + 1/16 * VGP/N20
V146	14/16 * VGP/N15 + 2/16 * VGP/N16	V210	14/16 * VGP/N19 + 2/16 * VGP/N20
V147	13/16 * VGP/N15 + 3/16 * VGP/N16	V211	13/16 * VGP/N19 + 3/16 * VGP/N20
V148	12/16 * VGP/N15 + 4/16 * VGP/N16	V212	12/16 * VGP/N19 + 4/16 * VGP/N20
V149	11/16 * VGP/N15 + 5/16 * VGP/N16	V213	11/16 * VGP/N19 + 5/16 * VGP/N20
V150	10/16 * VGP/N15 + 6/16 * VGP/N16	V214	10/16 * VGP/N19 + 6/16 * VGP/N20
V151	9/16 * VGP/N15 + 7/16 * VGP/N16	V215	9/16 * VGP/N19 + 7/16 * VGP/N20
V152	8/16 * VGP/N15 + 8/16 * VGP/N16	V216	8/16 * VGP/N19 + 8/16 * VGP/N20
V153	7/16 * VGP/N15 + 9/16 * VGP/N16	V217	7/16 * VGP/N19 + 9/16 * VGP/N20
V154	6/16 * VGP/N15 + 10/16 * VGP/N16	V218	6/16 * VGP/N19 + 10/16 * VGP/N20
V155	5/16 * VGP/N15 + 11/16 * VGP/N16	V219	5/16 * VGP/N19 + 11/16 * VGP/N20
V156	4/16 * VGP/N15 + 12/16 * VGP/N16	V220	4/16 * VGP/N19 + 12/16 * VGP/N20
V157	3/16 * VGP/N15 + 13/16 * VGP/N16	V221	3/16 * VGP/N19 + 13/16 * VGP/N20
V158	2/16 * VGP/N15 + 14/16 * VGP/N16	V222	2/16 * VGP/N19 + 14/16 * VGP/N20
V159	1/16 * VGP/N15 + 15/16 * VGP/N16	V223	1/16 * VGP/N19 + 15/16 * VGP/N20
V160	VGP/N16	V224	VGP/N20

V161	15/16 * VGP/N16 + 1/16 * VGP/N17	V225	7/8 * VGP/N20 + 1/8 * VGP/N21
V162	14/16 * VGP/N16 + 2/16 * VGP/N17	V226	6/8 * VGP/N20 + 2/8 * VGP/N21
V163	13/16 * VGP/N16 + 3/16 * VGP/N17	V227	5/8 * VGP/N20 + 3/8 * VGP/N21
V164	12/16 * VGP/N16 + 4/16 * VGP/N17	V228	4/8 * VGP/N20 + 4/8 * VGP/N21
V165	11/16 * VGP/N16 + 5/16 * VGP/N17	V229	3/8 * VGP/N20 + 5/8 * VGP/N21
V166	10/16 * VGP/N16 + 6/16 * VGP/N17	V230	2/8 * VGP/N20 + 6/8 * VGP/N21
V167	9/16 * VGP/N16 + 7/16 * VGP/N17	V231	1/8 * VGP/N20 + 7/8 * VGP/N21
V168	8/16 * VGP/N16 + 8/16 * VGP/N17	V232	VGP/N21
V169	7/16 * VGP/N16 + 9/16 * VGP/N17	V233	7/8 * VGP/N21 + 1/8 * VGP/N22
V170	6/16 * VGP/N16 + 10/16 * VGP/N17	V234	6/8 * VGP/N21 + 2/8 * VGP/N22
V171	5/16 * VGP/N16 + 11/16 * VGP/N17	V235	5/8 * VGP/N21 + 3/8 * VGP/N22
V172	4/16 * VGP/N16 + 12/16 * VGP/N17	V236	4/8 * VGP/N21 + 4/8 * VGP/N22
V173	3/16 * VGP/N16 + 13/16 * VGP/N17	V237	3/8 * VGP/N21 + 5/8 * VGP/N22
V174	2/16 * VGP/N16 + 14/16 * VGP/N17	V238	2/8 * VGP/N21 + 6/8 * VGP/N22
V175	1/16 * VGP/N16 + 15/16 * VGP/N17	V239	1/8 * VGP/N21 + 7/8 * VGP/N22
V176	VGP/N17	V240	VGP/N22
V177	15/16 * VGP/N17 + 1/16 * VGP/N18	V241	3/4 * VGP/N22 + 1/4* VGP/N23
V178	14/16 * VGP/N17 + 2/16 * VGP/N18	V242	2/4 * VGP/N22 + 2/4* VGP/N23
V179	13/16 * VGP/N17 + 3/16 * VGP/N18	V243	1/4 * VGP/N22 + 3/4* VGP/N23
V180	12/16 * VGP/N17 + 4/16 * VGP/N18	V244	VGP/N23
V181	11/16 * VGP/N17 + 5/16 * VGP/N18	V245	3/4 * VGP/N23 + 1/4* VGP/N24
V182	10/16 * VGP/N17 + 6/16 * VGP/N18	V246	2/4 * VGP/N23 + 2/4* VGP/N24
V183	9/16 * VGP/N17 + 7/16 * VGP/N18	V247	1/4 * VGP/N23 + 3/4* VGP/N24
V184	8/16 * VGP/N17 + 8/16 * VGP/N18	V248	VGP/N24
V185	7/16 * VGP/N17 + 9/16 * VGP/N18	V249	1/2 * VGP/N24 + 1/2* VGP/N25
V186	6/16 * VGP/N17 + 10/16 * VGP/N18	V250	VGP/N25
V187	5/16 * VGP/N17 + 11/16 * VGP/N18	V251	1/2 * VGP/N25 + 1/2* VGP/N26
V188	4/16 * VGP/N17 + 12/16 * VGP/N18	V252	VGP/N26
V189	3/16 * VGP/N17 + 13/16 * VGP/N18	V253	1/2 * VGP/N26 + 1/2* VGP/N27
V190	2/16 * VGP/N17 + 14/16 * VGP/N18	V254	VGP/N27
V191	1/16 * VGP/N17 + 15/16 * VGP/N18	V255	VGP/N28

5.9 Reset function

The Reset function of ST7102 is triggered by RESX input. After reset function is triggered, the ST7102 is into a reset period, and the duration of this period must be at least 1ms. During this period, the ST7102 and its power circuit is initialized.

Initial State Of Output Pins

Output Pins Name	Initial State
S[480:1] (source output)	GND
VGH	GND
VGL	GND
VCOM	GND
CGOUTL_R[16:1](GIP signal)	GND

5.9.1 Reset Timing Diagram

ST7102 provides Power On Reset and HWRST pin (RESX) for IC initialization and exit Deep Standby Mode (DSTB). For exiting DSTB Mode, HWRST pin should be tied to high at least 10ms. The timing diagram is located at below.

5.9.1.1 Power On Reset & HWRST Reset

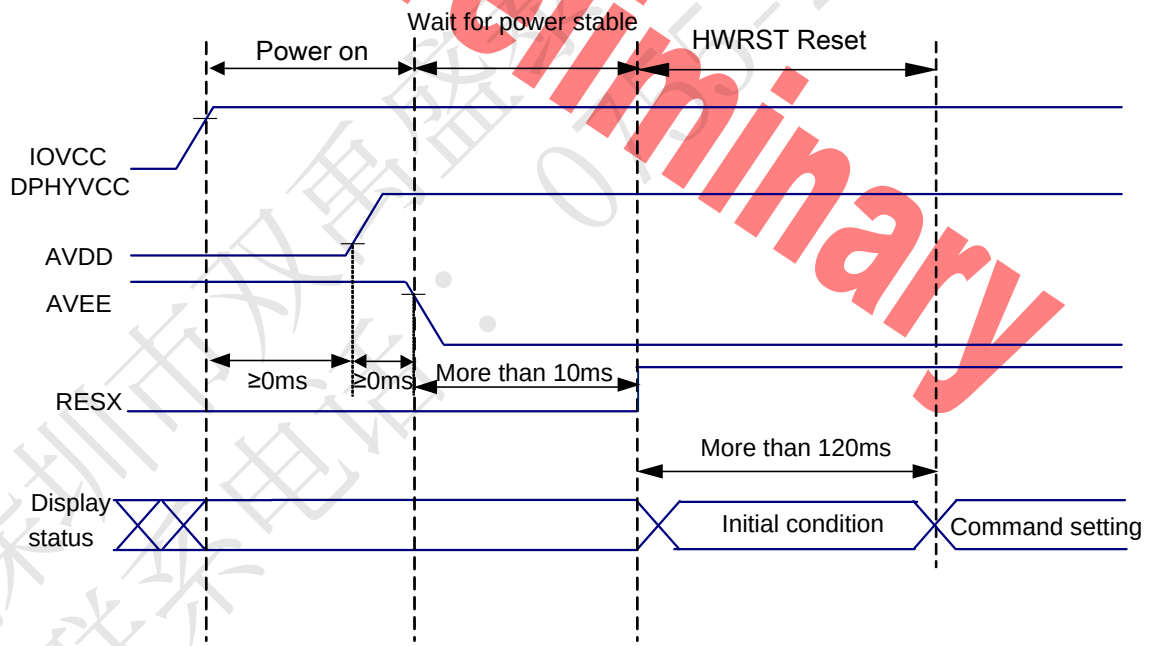


Figure 67 Power on Reset and HWRST reset

Note: RESX should be tied from low to high when exiting DSTB Mode.

5.10 Abnormal Power off Function

ST7102 provides Power Drop detection. If external power drops lower than circuit detection voltage, then the system will enter into Sleep In Mode.

5.10.1 Abnormal Power Off

Abnormal Power Off circuit can detect external voltage source IOVCC, AVDD, AVEE, if one of them is below detection voltage, then the system will be into Sleep In Mode. The following schematic is to show how the detection circuit produces abnormal signal.

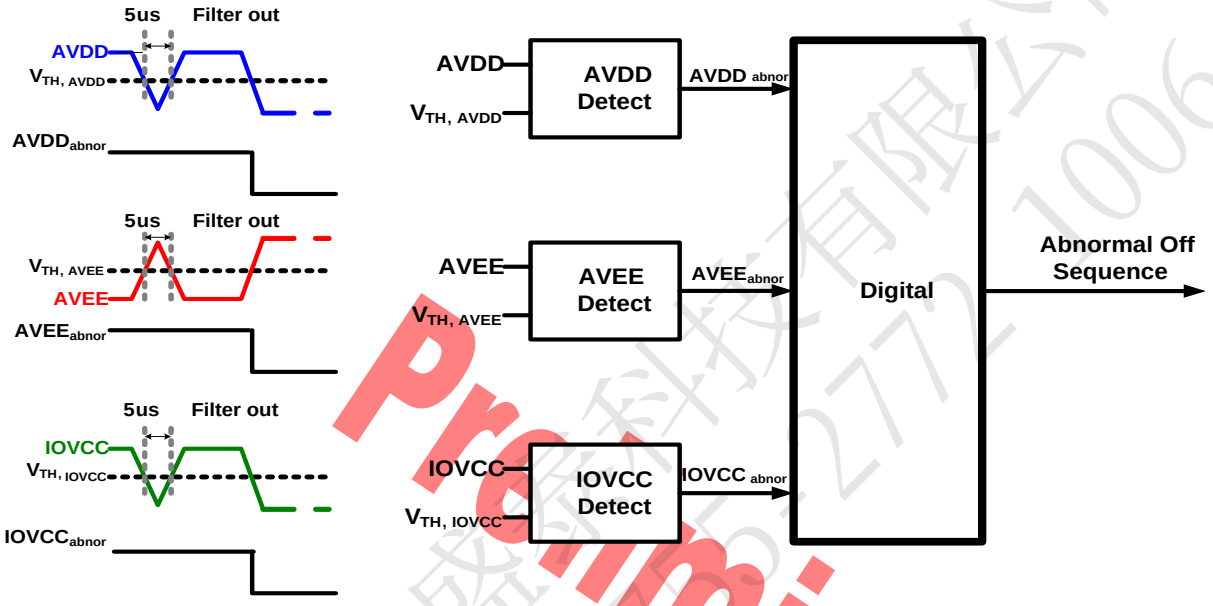


Figure 68 Abnormal Off Function Block Diagram

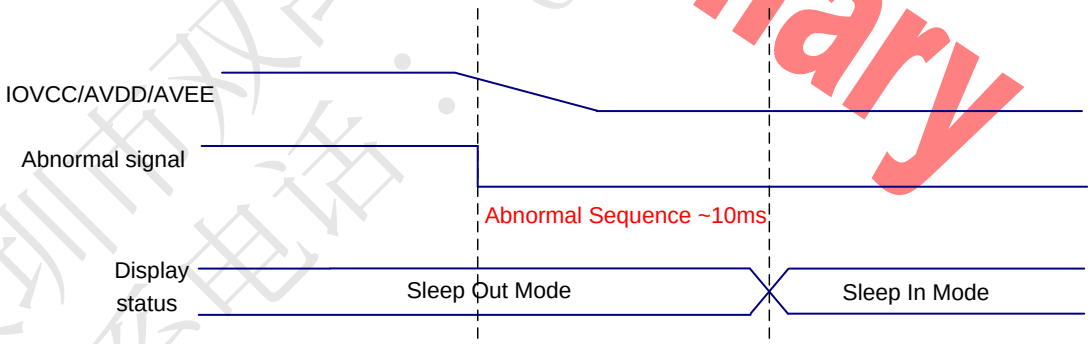


Figure 69 Abnormal Off Sequence Diagram

Note1: Abnormal function is working only in Sleep Out Mode

5.11 Basic Operation Mode

The basic operation mode of ST7102 is illustrated below. When changing from one mode to another, make sure to follow the sequence indicated in below figure.

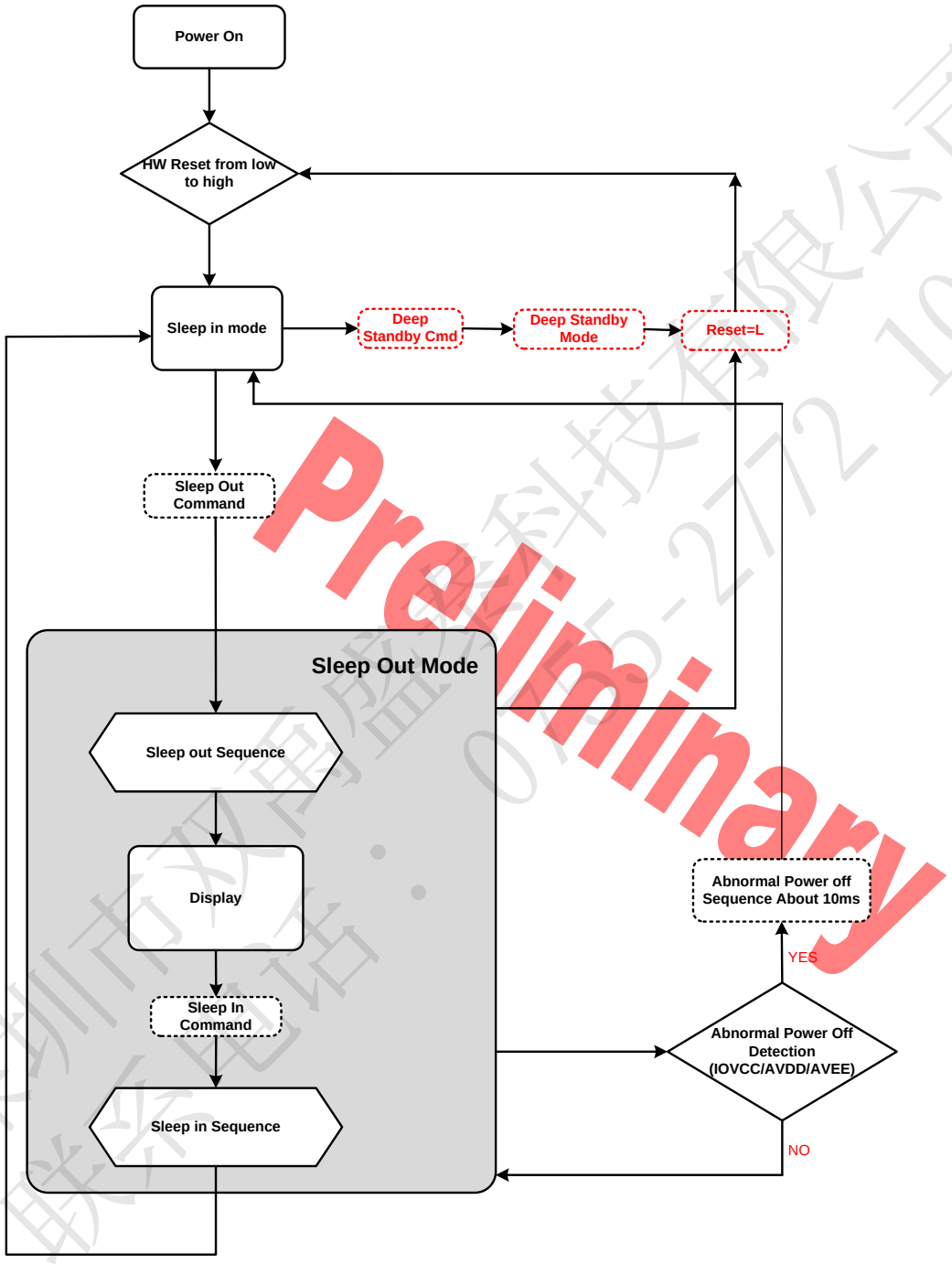


Figure 70 Basic Operation Mode

5.12 Power On/Off Sequence

The power On/Off sequence is illustrated below.

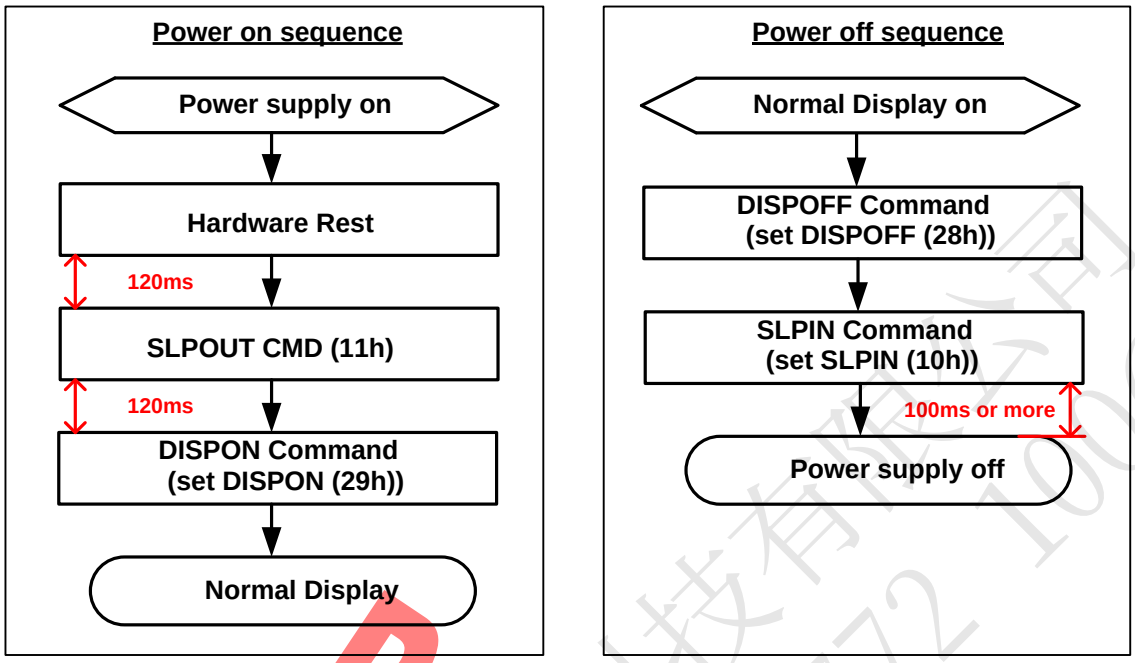


Figure 71 The power On/Off sequence block diagram

5.12.1 Power On/Off Timing

The power On/Off timing diagram is illustrated below.

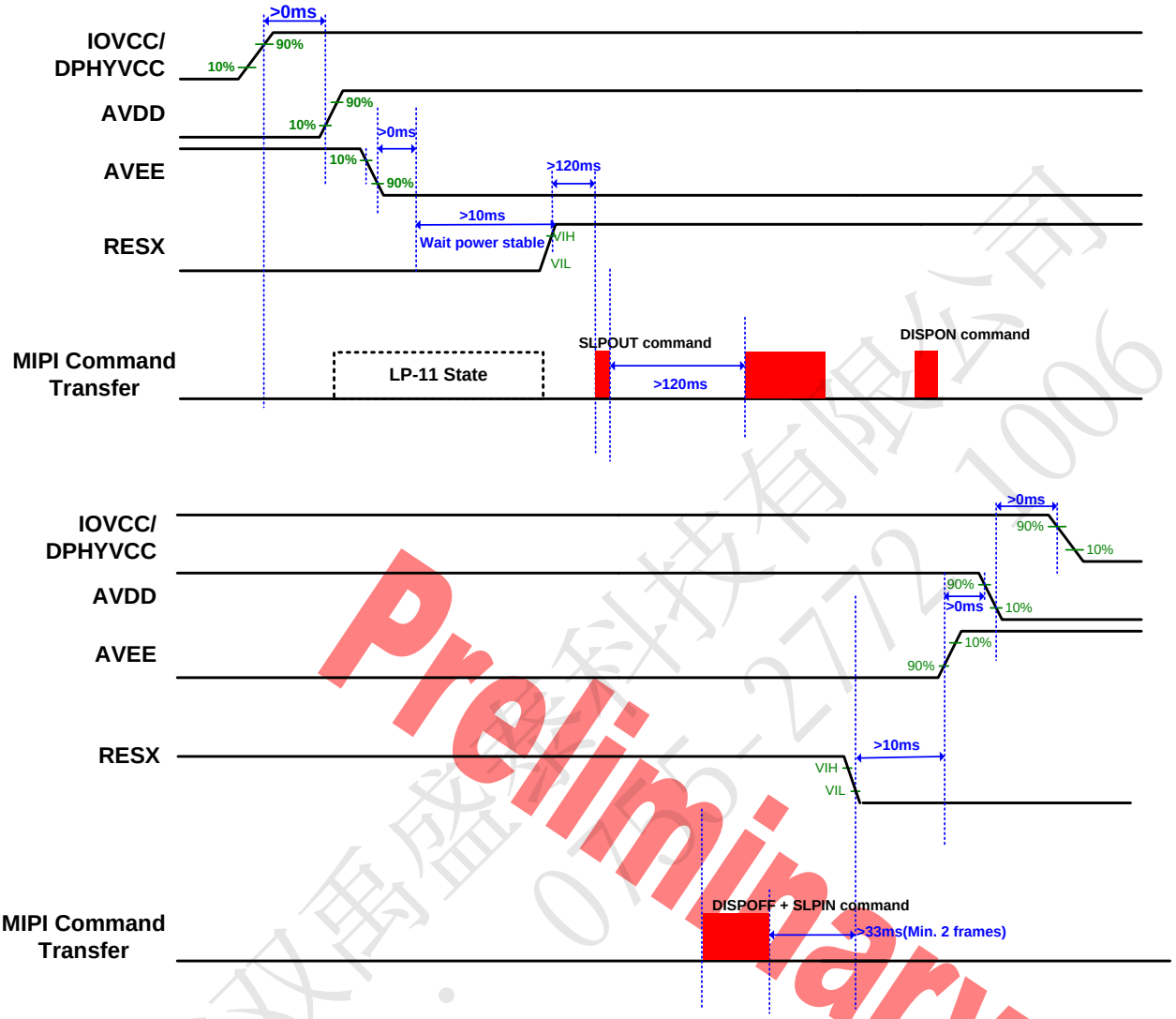


Figure 72 The power on sequence timing

Note 1: MIPI lanes must go to LP11 after Power IOVCC/DPHYVCC is ready

Note 2: After SLPOUT command, driver IC will start internal power on action. Any other settings should be set after SLPOUT command with a minimum of 120mS.

Note 3: DISPOFF and SLPIN command should be set after SLPOUT command with a minimum delay time of 120mS.

Note 4: RESX tied low into deep standby mode with a minimum time of 10ms.

5.12.2 Power Ramp Up/Down Specifications

The power ramp up/down specifications are illustrate below

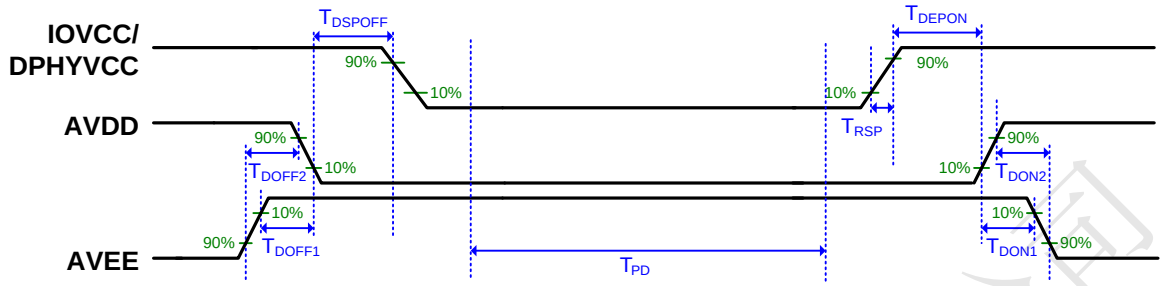


Figure 73 The power ramp up/down timing

Item	Symbol	Unit	Min.	Max.
System power (IOVCC) rise time (10% to 90%)	T_{RSP}	ms	-	2
System power (IOVCC) on to AVDD on time	T_{DEPON}	ms	0	-
AVDD-AVEE on delay time (10% to 10%)	T_{DON1}	ms	0	-
AVDD-AVEE on delay time (90% to 90%)	T_{DON2}	ms	0	-
AVEE-AVDD off delay time (10% to 10%)	T_{DOFF1}	ms	0	-
AVEE-AVDD off delay time (90% to 90%)	T_{DOFF2}	ms	0	-
AVDD off to system power off time	T_{DSPOFF}	ms	0	-
Power down time	T_{PD}	ms	10	

5.13 Instruction Setting Sequence

5.13.1 Sleep Enter/Exit Sequences

When setting instruction to the ST7102, the sequence shown in below figure must be followed to complete the instruction setting.

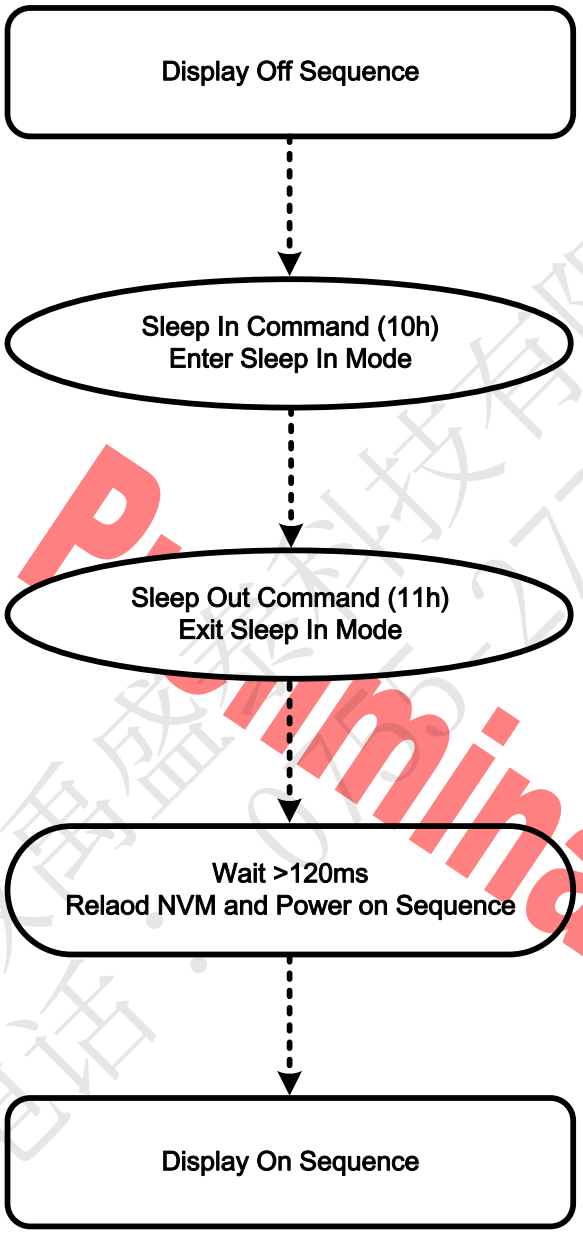


Figure 74 Sleep Enter/Exit Setting Sequence

5.13.2 Deep Standby Mode Enter/Exit Sequences

When setting instruction to the ST7102, the sequence shown in below figure must be followed to complete the instruction setting.

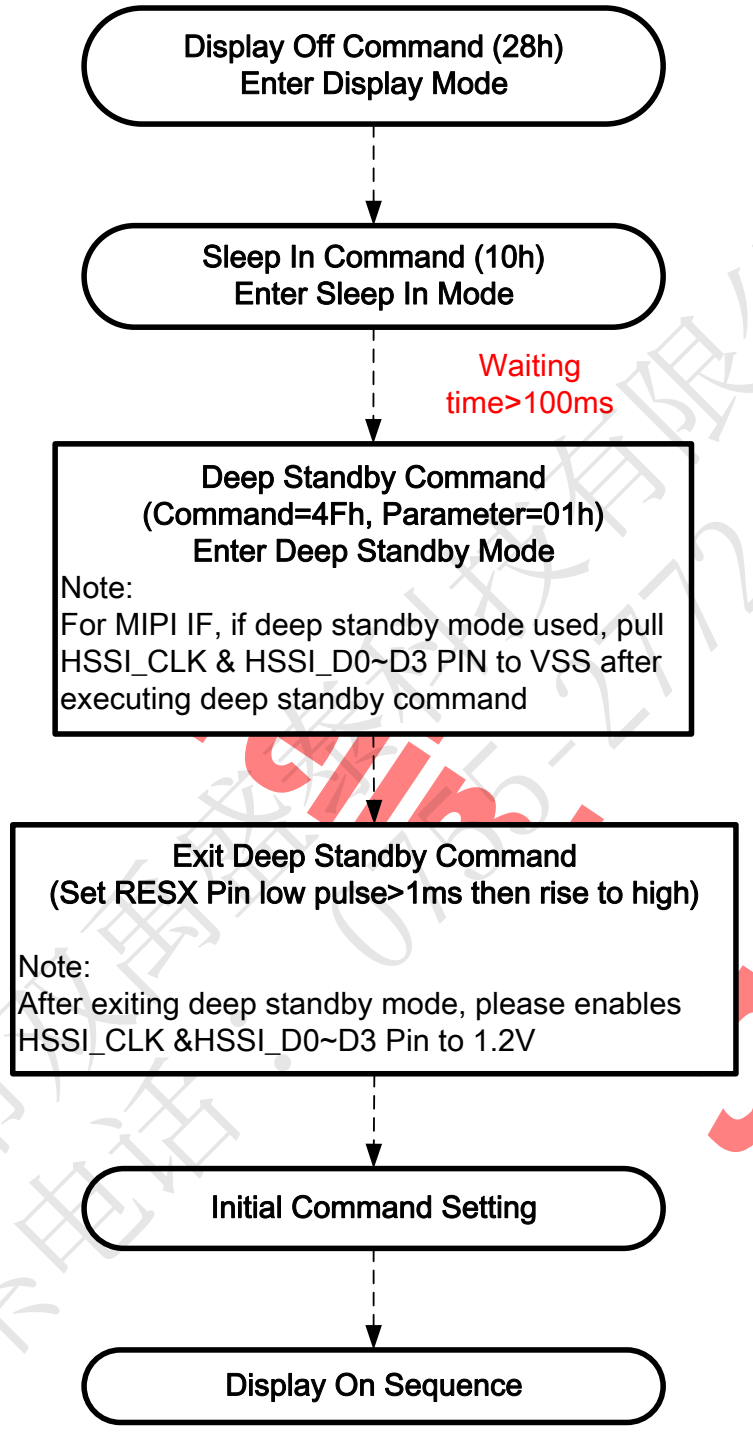


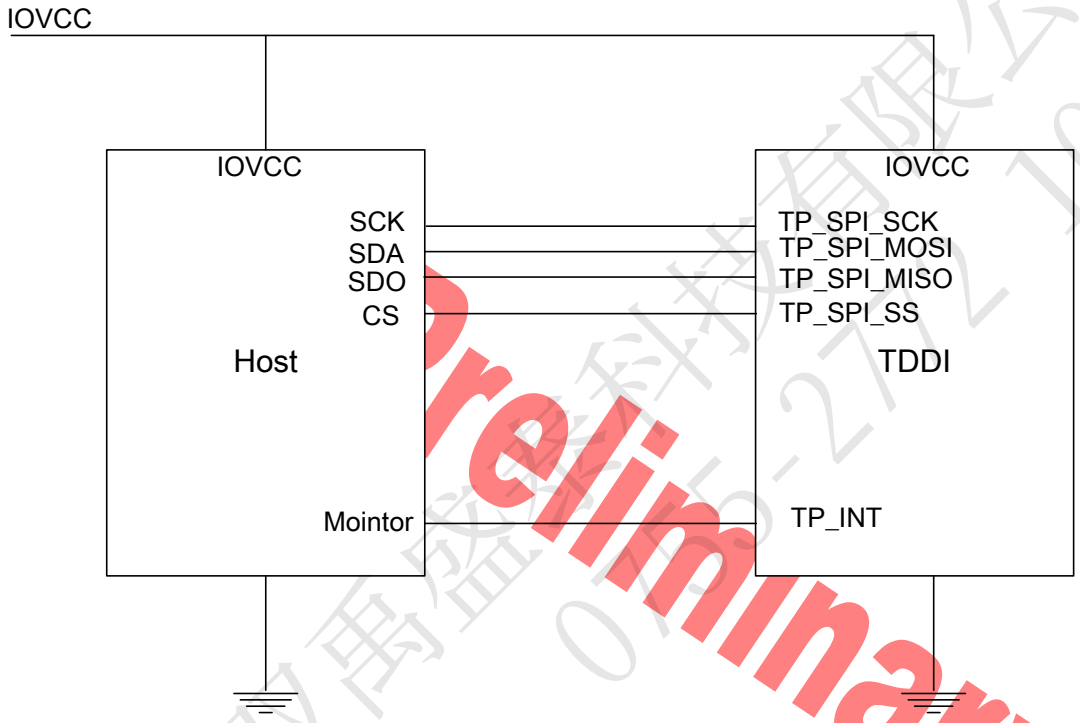
Figure 75 Deep Standby Mode Enter/Exit Setting Sequence

5.14 Touch interface protocol

ST7102 supports SPI and I2C interface, which allows full-duplex, synchronous, serial communications with host controllers. ST7102 SPI equips four serial signals, SS, SCK, MISO and MOSI.

5.14.1 SPI interface

ST7102 operates as a SPI slave device and data length is 16-bit. TP_SPI_SS, TP_SPI_SCK and TP_SPI_MOSI are Schmitt trigger inputs. The data on TP_SPI_MOSI is latched on rising edge of TP_SPI_SCK and the data on TP_SPI_MISO output on falling edge of TP_SPI_SCK. The maximum SPI clock rate is 16 MHz.

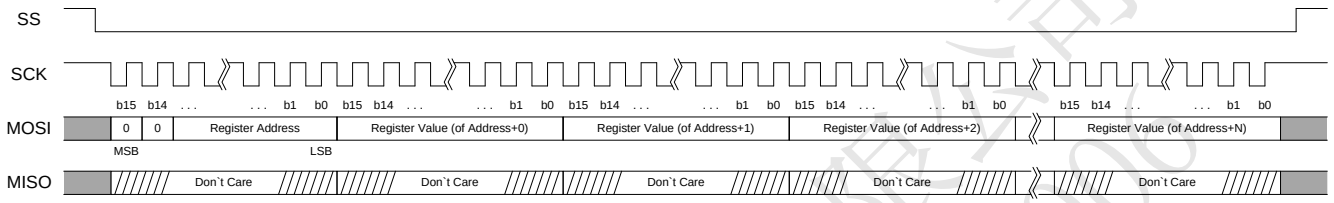


The information transmitted by SPI can be divided into command packet and data packet. Command packet can access register and data packet can access internal RAM. The most significant bit, called ID bit, after TP_SPI_SS falling edge is used to identify command or data packet. And the following bit, called R/W bit, is used to identify write or read operation.

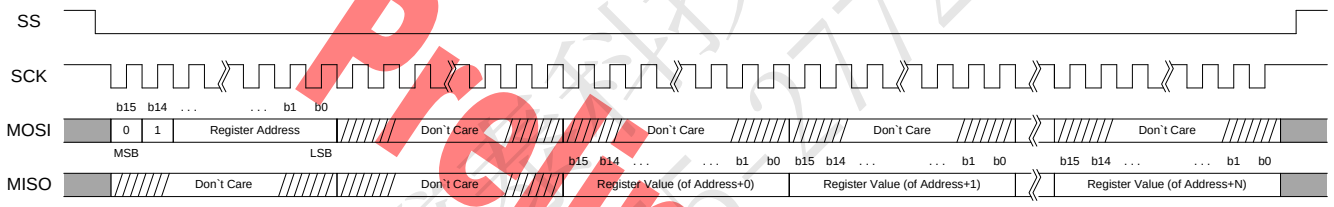
5.14.1.1 Command Protocol

In command protocol, ID bit of 1st word after TP_SPI_SS falling edge is “0” to indicate register access. R/W bit is “0” to indicate write operation and “1” to indicate read operation. Bit13 to bit0 of 1st word, called ADD bits, are address of register to be accessed. If at write operation, the 2nd word on TP_SPI_MOSI will update the register which is addressed

by ADD and afterward ADD will increase one automatically. If at read operation, the 2nd word on TP_SPI_MOSI is dummy word (value doesn't care). The 3rd word on TP_SPI_MISO will be outputted from register addressed by ADD and similarly ADD is increment afterwards. Keep writing and reading words can access the consecutive registers during one SPI transmission. If accessing non-consecutive register is happened, SS should return to "1" to end current transmission and start another SPI command protocol to assign new register address.



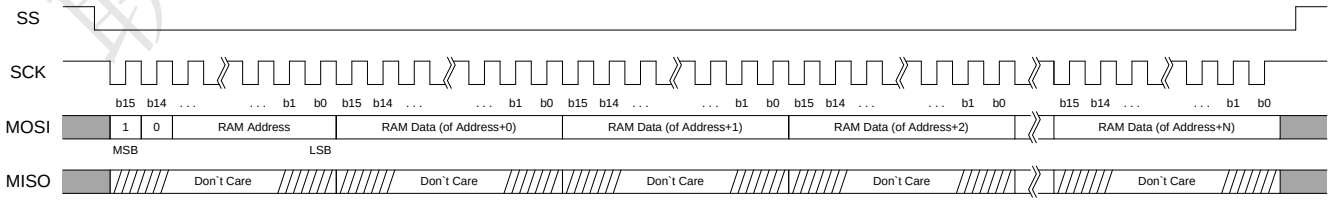
Host write register command



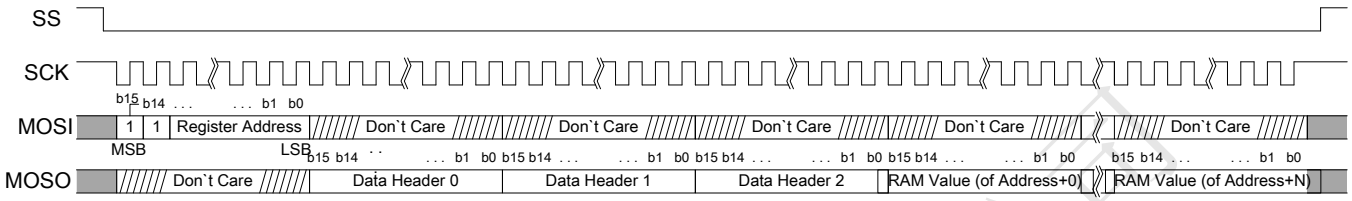
Host read register command

5.14.1.2 Data Protocol

In data protocol, ID bit of 1st word after SS falling edge is "1" to indicate RAM access. R/W bit is "0" to indicate write operation and "1" to indicate read operation. Bit13 to bit0 of 1st word, called ADD bits, are address of RAM to be accessed. If at write operation, the 2nd word on MOSI will update RAM which is addressed by ADD and afterward ADD will increase one automatically. If at read operation, the 2nd word on MISO is 16-bit header. The 3rd word on MISO will be outputted from RAM addressed by ADD and similarly ADD is increment afterwards. Keep writing and reading words can access the consecutive RAM addresses during one SPI transmission. If accessing non-consecutive RAM address is happened, SS should return to "1" to end current transmission and start another SPI data protocol to assign new RAM address.



Host write RAM data

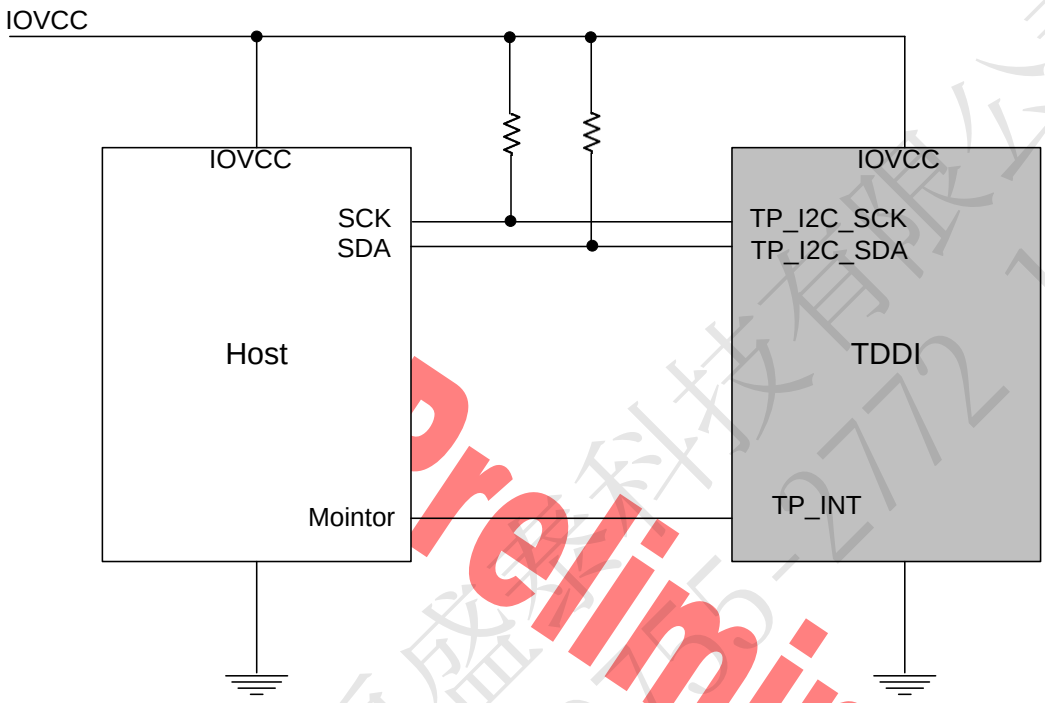


Host read RAM data

5.14.2 I2C

ST7102 protocol supports operating speeds up to 400 kb/s with 7-bit addressing and 8-bit data bytes. The TP_I2C_SCK, TP_I2C_SDA, and TP_TSIX pins are typically used in an I2C interface.

The values of the pull-up resistors should be chosen to ensure that the rise times of the TP_I2C_SDA and TP_I2C_SCK signals are within the limits set by the I2C specification. These values depend on what other devices, if any, are on the I2C bus. Typical values fall within the range of 2 kΩ to 10 kΩ.



- **I2C Pin Definition**

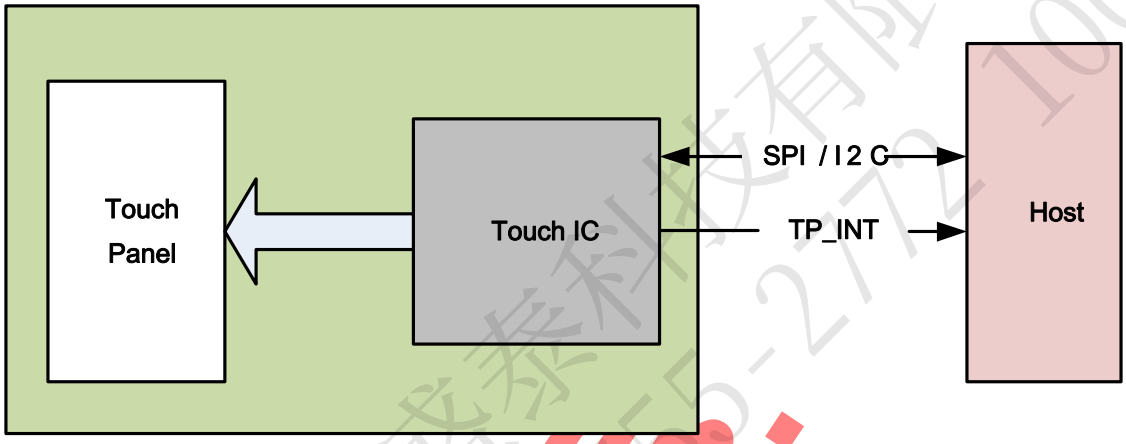
Name	I/O	Description	Connect Pin
IOVCC	I	Power supply for I/O system	IOVCC
SCK	I	I2C clock pin	TP_I2C_SCK
SDA	I/O	I2C data pin	TP_I2C_SDA
IRQ	O	Data ready interrupt pin	TP_INT

- **I2C clock timing**

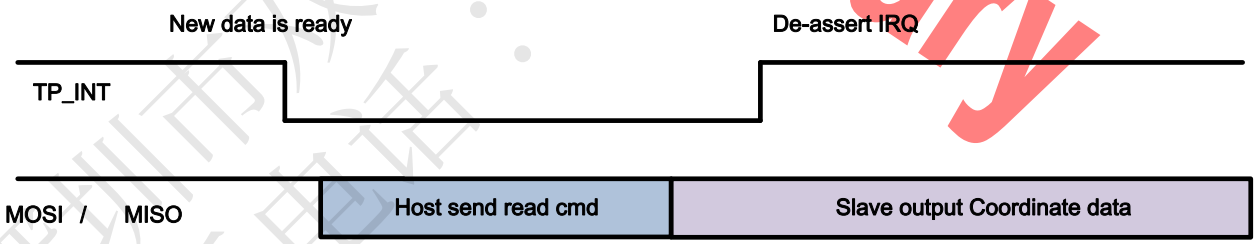
When a transaction contains the slave address and R/W bit (start condition), the sensor can hold SCL low and checks that the slave address matches. If the slave address fails to match, the sensor no longer clock stretches on subsequent byte transmission until it detects the next start condition. When the slave address matches, the sensor acknowledges and can continue to clock stretch at the end of subsequent bytes within the same transaction.

5.14.3 IRQ

ST7102 provides an interrupt pin(TP_TSIX) that is asserted to indicate that new data is available for reading by the host. The TP_TSIX signal is intended to be used as interrupt source to a host. IRQ functionality is added by MCU firmware. The IRQ to host connection as below.



The TP_INT pin behavior



6 COMMAND DESCRIPTION

6.1 User Command Set (UCS) List

Command	(Hex)	Write/Read /Command	NVM option	Function	Parameter Number	MIPI Transmission
NOP	00	C	No	No Operation	0	LPDT/HSDT
SWRESET	01	C	No	Software Reset	0	LPDT/HSDT
RDDID	04	R	No	Read Display Identification Information	3	LPDT/HSDT
RDNUMED	05	R	No	Read Number of Errors on DSI	1	LPDT/HSDT
RDDST	09	R	No	Read Display Status	4	LPDT/HSDT
RDDPM	0A	R	No	Read Display Power Mode	1	LPDT/HSDT
RDDMADCTL	0B	R	No	Read Display MADCTL	1	LPDT/HSDT
RDDIM	0D	R	No	Read Display Image Mode	1	LPDT/HSDT
RDDSM	0E	R	No	Read Display Signal Mode	1	LPDT/HSDT
RDDSDR	0F	R	No	Read Display Self-Diagnostic Result	1	LPDT/HSDT
SLPIN	10	C	No	Enter Sleep In mode	0	LPDT/HSDT
SLPOUT	11	C	No	Enter Sleep Out mode	0	LPDT/HSDT
NORON	13	C	No	Enter Normal Display mode	0	LPDT/HSDT
INVOFF	20	C	No	Display Inversion Off	0	LPDT/HSDT
INVON	21	C	No	Display Inversion On	0	LPDT/HSDT
ALLPOFF	22	C	No	All pixel off	0	LPDT/HSDT
ALLPON	23	C	No	All pixel on	0	LPDT/HSDT
GAMSEL	26	C	No	Gamma curve select	1	LPDT/HSDT
DISPOFF	28	C	No	Display off	0	LPDT/HSDT
DISPON	29	C	No	Display on	0	LPDT/HSDT
TEOFF	34	C	No	Tearing Effect Line Off	0	LPDT/HSDT
TEEON	35	W	No	Tearing Effect Line On	1	LPDT/HSDT
MADCTL	36	W	Yes	Memory Access Direction Control	1	LPDT/HSDT
IDMOFF	38	W	No	Idle Mode OFF	0	LPDT/HSDT
IDMON	39	W	No	Idle Mode ON	0	LPDT/HSDT
TESLWR	44	W	No	Write TE Scan Line	2	LPDT/HSDT
TESLRD	45	R	No	Read Scan Line	2	LPDT/HSDT
DSTB	4F	W	No	Deep standby mode on	1	LPDT/HSDT
WRDISBV	51	W	No	Write Display Brightness	1	LPDT/HSDT
RDDISBV	52	R	No	Read Display Brightness Value	1	LPDT/HSDT
WRCTRLD	53	W	No	Write CTRL Display	1	LPDT/HSDT

RDCTRLD	54	R	No	Read CTRL Display	1	LPDT/HSDT
WRCABC	55	W	No	Write Content Adaptive Brightness Control	1	LPDT/HSDT
RDCABC	56	R	No	Read Content Adaptive Brightness Control	1	LPDT/HSDT
WRCABCMB	5E	W	No	Write CABC Minimum Brightness	1	LPDT/HSDT
RDCABCMB	5F	R	No	Read CABC Minimum Brightness	1	LPDT/HSDT
RDID1	DA	R	Yes	Read ID1	1	LPDT/HSDT
RDID2	DB	R	Yes	Read ID2	1	LPDT/HSDT
RDID3	DC	R	Yes	Read ID3	1	LPDT/HSDT
RDDDBS	A1	R	No	Read DDB Start	8	LPDT/HSDT
RDDDBC	A8	R	Yes	Read DDB Continue	8	LPDT/HSDT
RDFCS	AA	R	No	Read First Checksum	1	LPDT/HSDT
RDCCS	AF	R	No	Read Continue Checksum	1	LPDT/HSDT
RDICCD	F4	R	No	Read Sitronix IC ID	2	LPDT/HSDT
MIPIEXTFMAT	F9	W/R	YES	MIPI Extension Format	1	LPDT/HSDT

Note: LPDT (Low Power Mode), HSDT (High Speed Mode)

6.2 User Command Set (UCS) DESCRIPTION

6.2.1 NOP (00H) : No Operation

00H	NOP (No Operation)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
NOP	Write	0	0	0	0	0	0	0	0	(00H)
Parameter	No Parameter									-
Description	- This command is empty command. It does not have effect on the display module.									
Restriction	-									

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.2 SWRESET (01H): Software Reset

01H	SWRESET (Software Reset)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
SWRESET	Write	0	0	0	0	0	0	0	1	(01H)
Parameter	No Parameter									-
Description	- When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to VSS (display off).									
Restriction	-									

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.3 RDDID (04H) Read Display Identification Information

04H	RDDID (Read Display Identification Information)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDID	Write	0	0	0	0	0	1	0	0	(04H)
1st Parameter	Read	ID1[7:0]								FFh
2nd Parameter	Read	ID2[7:0]								FFh
3rd Parameter	Read	ID3[7:0]								FFh
Description	- Read Display Identification Information -ID1 : LCD module's manufacturer ID (FFh: not programmed) -ID2 : LCD module/driver version ID (FFh: not programmed) -ID3 : LCD module/driver ID (FFh: not programmed)									
Restriction	-									

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.4 RDNUMED (05H) Read Number of Errors on DSI

05H	RDNUMED									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDNUMED	Write	0	0	0	0	0	1	0	1	(05H)
1st Parameter	Read	DSI_NUMBER[7:0]								00h
Description	- Read Number of Errors on DSI, DSI_NUMBER[7:0] is a number of the errors on DSI.									
Restriction	-									

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.5 RDDST (09H) Read Display Status

09H	RDNUMED(Read Display Status)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDST	Write	0	0	0	0	1	0	0	1	(09H)
1st Parameter	Read	Booster_on	0	0	0	0	BGR	0	CA	00h
2nd Parameter	Read	LA	0	0	0	IDMON	0	SLPOUT	NORON	00h
3rd Parameter	Read	0	0	INVON	ALLPON	ALLPOFF	DSPON	TEON	GAMM_SEL[2]	00h
4th Parameter	Read	GAMMA_SEL[1]	GAMMA_SEL[0]	TEMOD	0	0	0	0	EOD	00h

Description

- This command indicates the current status of the display as described in the table below :

Bit	Description	Value
Booster_on	Booster status	'1' = Booster on. '0' = Booster off
CA	Column Address Order (CA)	'1' = Decrement, (Right to Left, when MADCTL (36h) CA='1') '0' = Increment, (Left to Right, when MADCTL (36h) CA='0')
LA	Row Address Order (LA)	'1' = Row/column exchange, (when MADCTL (36h) LA='1') '0' = Normal, (when MADCTL (36h) LA='0'
BGR	RGB/ BGR Order	'1' = BGR Order, (When MADCTL (36h) BGR='1') '0' = RGB Order, (When MADCTL (36h) BGR='0')
IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
SLPOUT	Sleep In/Out Mode	'1' = Sleep Out Mode '0' = Sleep In Mode
NORON	Normal mode	'1' = Normal Mode on '0' = Normal Mode off
DSPON	Display On/Off Mode	'1' = Display On Mode '0' = Display Off Mode
INVON	Inversion On/Off Mode	'1' = Inversion On Mode '0' = Inversion Off Mode
ALLPON	All pixel on	'1' = All pixel on '0' = Normal mode
ALLPOFF	All pixel off	'1' = All pixel off '0' = Normal mode
TEON	Tearing effect line on/off	'1' = Inversion On Mode '0' = Inversion Off Mode
GAMMA_SEL[2:0]	Gamma curve selection	'000' = Gamma curve 1(gamma 2.2) 'others' = reserved

	TEMOD	Tearing effect line mode	'1' = V- blanking and H-blanking '0' = V-blanking only
	EOD	Error on DSI	'1' = Error '0' = No Error
Restriction	-		

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.6 RDDPM (0AH): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDPM	Write	0	0	0	0	1	0	1	0	(0AH)
1st Parameter	Read	Booster_on	IDMON	0	SLPOUT	NORON	DSPON	0	0	00h

Description

- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
Booster_on	Booster status	'1' = Booster on. '0' = Booster off
IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
SLPOUT	Sleep In/Out Mode	'1' = Sleep Out Mode '0' = Sleep In Mode
NORON	Normal mode	'1' = Normal Mode on '0' = Normal Mode off
DSPON	Display On/Off Mode	'1' = Display On Mode '0' = Display Off Mode

Restriction

-

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.7 RDDMADCTR (0BH): Read Display MADCTR

0BH	RDDMADCTR (Read Display MADCTR)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDMADCTR	Write	0	0	0	0	1	0	1	1	(0BH)
1st Parameter	Read	0	0	0	0	BGR	0	CA	LA	00h

Description

- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
CA	Column Address Order (CA)	'1' = Decrement, (Right to Left, when MADCTL (36h) CA='1') '0' = Increment, (Left to Right, when MADCTL (36h) CA='0')
LA	Row Address Order (LA)	'1' = Row/column exchange, (when MADCTL (36h) LA='1') '0' = Normal, (when MADCTL (36h) LA='0'
BGR	RGB/ BGR Order	'1' = BGR Order, (When MADCTL (36h) BGR='1') '0' = RGB Order, (When MADCTL (36h) BGR='0')

Restriction

-

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.8 RDDCOLM (0CH): Read Display Color Mode

0DH	RDDIM (Read Display Image Mode)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDIM	Write	0	0	0	0	1	1	0	1	(0CH)
1st Parameter	Read	0	0	0	0	0	DBI[2:0]			00h

Description

- This command indicates the current status of the display as described in the table.

DBI[2:0]	Color Format
0h~4h	Reserved
5h	16-bit/pixel
6h	18-bit/pixel
7h	24-bit/pixel

Note: For DBI[2:0] definition refer to interface Pixel Format (3Ah)

Restriction

-

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.9 RDDIM (0DH): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDIM	Write	0	0	0	0	1	1	0	1	(0DH)
1st Parameter	Read	0	0	INVON	ALLPON	ALLPOFF	GAMMA_SEL[2:0]			00h

Description

- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
INVON	Inversion On/Off Mode	'1' = Inversion On Mode '0' = Inversion Off Mode
ALLPON	All pixel on	'1' = All pixel on '0' = Normal display
ALLPOFF	All pixel off	'1' = All pixel off '0' = Normal display
GAMMA_SEL[2:0]	Gamma curve selection	'000' = Gamma curve 1(gamma 2.2) 'others' = Reserved

Restriction

-

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.10 RDDSM (0EH): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Mode)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDSM	Write	0	0	0	0	1	1	0	1	(0EH)
1st Parameter	Read	TEON	TEM	0	0	0	0	0	EOD	00h

Description

- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing effect line on/off	'1' = Inversion On Mode '0' = Inversion Off Mode
TEM	Tearing effect line mode	'1' = V- blanking and H-blanking '0' = V-blanking only
EOD	Error on DSI	'1' = Error '0' = No Error

Restriction

-

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.11 RDDSDR(0FH): Read Display Self-Diagnostic Result

0FH	RDDSM (Read Display Signal Mode)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDSDR	Write	0	0	0	0	1	1	1	1	(0FH)
1st Parameter	Read	RLD	FD	0	0	0	0	0	CCR	00h

Description	- This command indicates the current status of the display as described in the below: -RLD: This bit is the Register Loading Detection -FD: This bit is the Functionality Detection -CCR: The checksum compare result. 0 = Checksum is the same. 1 = Checksum is not the same
Restriction	-
Register Availability	

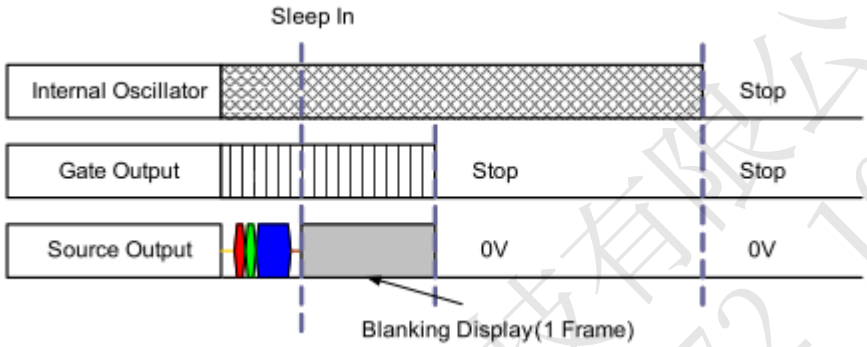
Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.12 SLPIN (10H): Sleep In

10H	SLPIN (Sleep In)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
SLPIN	Write	0	0	0	1	0	0	0	0	(10H)
Parameter	No Parameter									-

Description

- This command causes the LCD module to enter the minimum power consumption mode.
- In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



Restriction

- This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11H).
- It will be necessary to wait 5ms before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.
- It will be necessary to wait 120ms after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

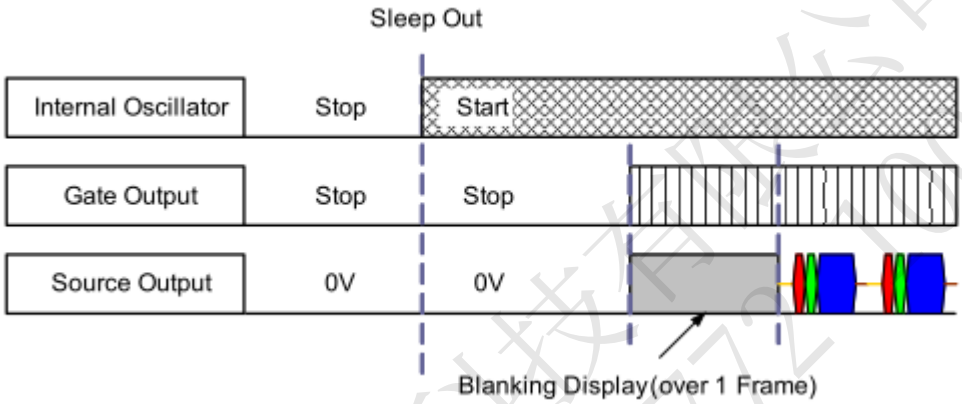
Status	Availability
Sleep Out, Display On	Yes
Sleep In	No

6.2.13 SLPOUT (11H): Sleep Out

11H	SLPOUT (Sleep Out)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
SLPOUT	Write	0	0	0	1	0	0	0	1	(11H)
Parameter	No Parameter									-

Description

- This command turns off sleep mode.
- In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



Restriction

- This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10H).
- It will be necessary to wait 5ms before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.
- DRIVER loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the DRIVER is already Sleep Out mode.
- It will be necessary to wait 120ms after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent

Register Availability

Status	Availability
Sleep Out, Display On	No
Sleep In	Yes

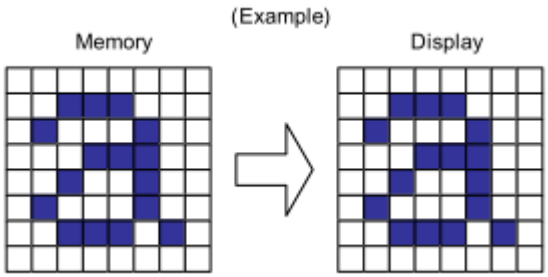
6.2.14 NORON (13H): Normal display mode On

13H	NORON (Normal Display Mode On)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
INVOFF	Write	0	0	0	1	0	0	1	1	(13H)
Parameter	No Parameter									-

Description	- This command is used to return display to normal display mode. -.This command can exit all pixel on/off mode to normal display mode.
Restriction	
Register Availability	

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.15 INVOFF (20H) : Display Inversion Off

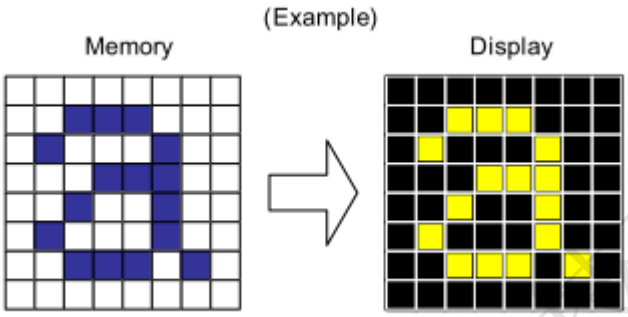
20H	INVOFF (Display Inversion Off)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
INVOFF	Write	0	0	1	0	0	0	0	0	(20H)
Parameter	No Parameter									-
Description	- This command is used to recover from display inversion mode. - This command makes no change of contents of frame memory. - This command does not change any other status. 									
Restriction	- This command has no effect when module is already in inversion off mode.									
Register Availability	**Status** / **Availability** Sleep Out, Display On / Yes Sleep In / Yes									

6.2.16 INVON (21H) : Display Inversion On

21H	INVON (Display Inversion On)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
INVON	Write	0	0	1	0	0	0	0	1	(21H)
Parameter	No Parameter									-

Description

- This command is used to enter into display inversion mode.
- This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.
- This command does not change any other status.



Restriction

- This command has no effect when module is already in inversion off mode.

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.17 ALLPOFF (22H): All pixel off

22H	ALLPOFF (All pixel off)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
ALLPOFF	Write	0	0	1	0	0	0	1	0	(22H)
Parameter	No Parameter									-
Description	- This command is used to black display In sleep out mode. - Exit from this command by All pixel on(23H) or Normal display mode(13H)									
Restriction										

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	No

6.2.18 ALLPON (23H): All pixel on

23H	ALLPOFF (All pixel off)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
ALLPON	Write	0	0	1	0	0	0	1	1	(23H)
Parameter	No Parameter									-
Description	- This command is used to white display In sleep out mode. - Exit from this command by All pixel off(22H) or Normal display mode(13H)									
Restriction										
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	No

6.2.19 GAMSEL (26H): Gamma Curve Select

26H	(Gamma Curve Select)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
GAMSEL	Write	0	0	1	0	0	1	1	0	(26H)
Parameter	Write	0	0	0	0	GC[3:0]				

Description

- This command is used to select gamma curve, and only 1 curve (gamma 2.2) can be selected.

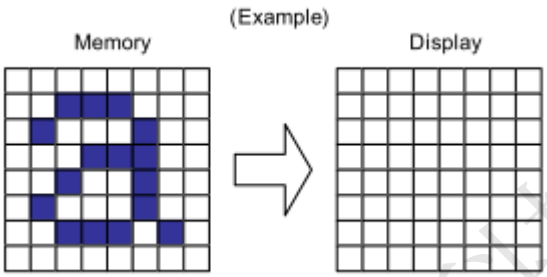
GC[3:0]	Gamma Curve
1	Gamma 2.2
others	Reserved

Restriction

Register Availability

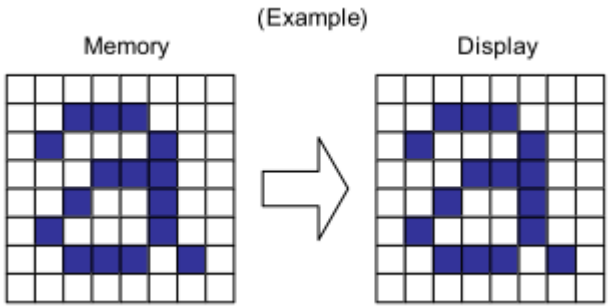
Status	Availability
Sleep Out, Display On	Yes
Sleep In	No

6.2.20 DISPOFF (28H): Display Off

28H	DISPOFF (Display Off)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
DISPOFF	Write	0	0	1	0	1	0	0	0	(28H)
Parameter	No Parameter									-
Description	- This command is used to enter into DISPLAY OFF mode. In this mode. - This command makes no change of contents of frame memory. - This command does not change any other status. - There will be no abnormal visible effect on the display. - Exit from this command by Display On (29H) 									
Restriction	-This command has no effect when module is already in Display Off mode.									
Register Availability	**Status** / **Availability** Sleep Out, Display On: Yes Sleep In: No									

6.2.21 DISPON (29H): Display On

29H	DISPON (Display On)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
DISPON	Write	0	0	1	0	1	0	0	1	(29H)
Parameter	No Parameter									-
Description	- This command is used to recover from DISPLAY OFF mode. - This command makes no change of contents of frame memory. - This command does not change any other status.									

<table>
<tr><td></td><td> 
</td></tr>
<tr><td>Restriction</td><td>-This command has no effect when module is already in Display Off mode.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Sleep Out, Display On</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

6.2.22 TEOFF (34H): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
TEOFF	Write	0	0	1	1	0	1	0	0	(34H)
Parameter	No Parameter									-
Description	- This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	- This command has no effect when Tearing Effect output is already OFF.									

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

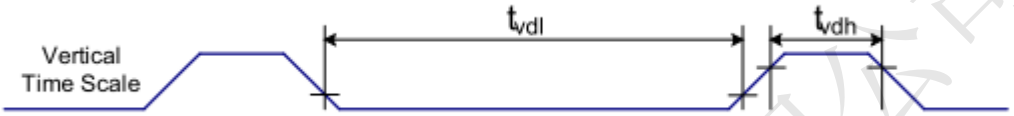
6.2.23 TEON (35H): Tearing Effect Line ON

35H	TEON (Tearing Effect Line ON)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
TEON	Write	0	0	1	1	0	1	0	1	(35H)
1st Parameter	Write	0	0	0	0	0	0	0	TEM	00h

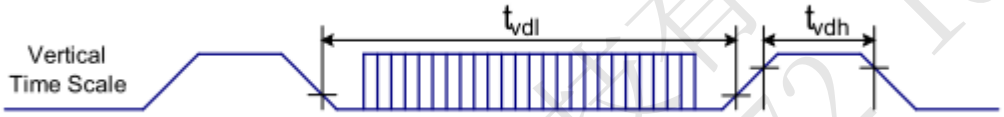
Description

-Tearing Effect Mode ON

- Mode 1: When TEM = '0', The tearing effect output line consists of V-blanking information only.



- Mode 2: When TEM = '1': The tearing effect output line consists of both V-blanking and H-blanking information.



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

- This command has no effect when Tearing Effect output is already ON.

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.24 MADCTR (36H): Memory Data Access Control

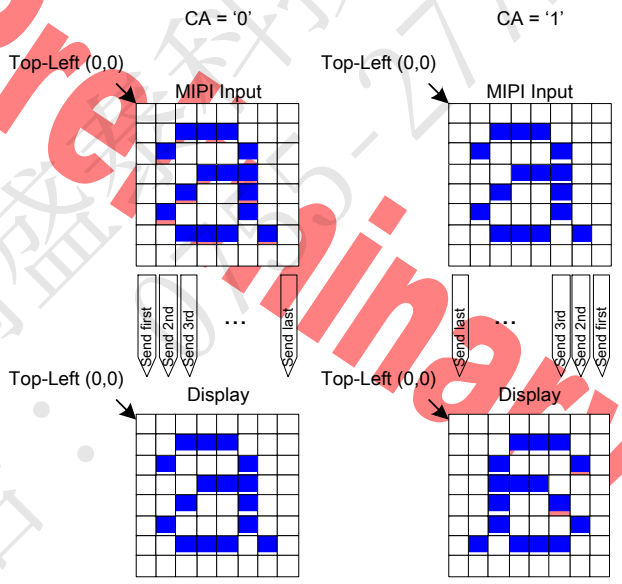
36H	MADCTR (Memory Data Access Control)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
MADCTR	Write	0	0	1	1	0	1	1	0	(36H)
1st Parameter	Read	0	0	0	0	BGR	0	CA	LA	00h

Description

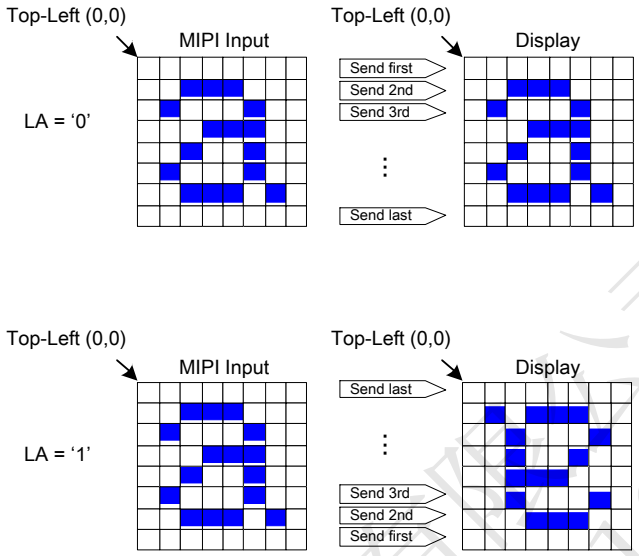
- Bit Assignment

Bit	Description	Value
CA	Column Address Order (CA)	'1' = Decrement, (Right to Left, when MADCTL (36h) CA='1') '0' = Increment, (Left to Right, when MADCTL (36h) CA='0')
LA	Row Address Order (LA)	'1' = Row/column exchange, (when MADCTL (36h) LA='1') '0' = Normal, (when MADCTL (36h) LA='0'
BGR	RGB/ BGR Order	'1' = BGR Order, (When MADCTL (36h) BGR='1') '0' = RGB Order, (When MADCTL (36h) BGR='0')

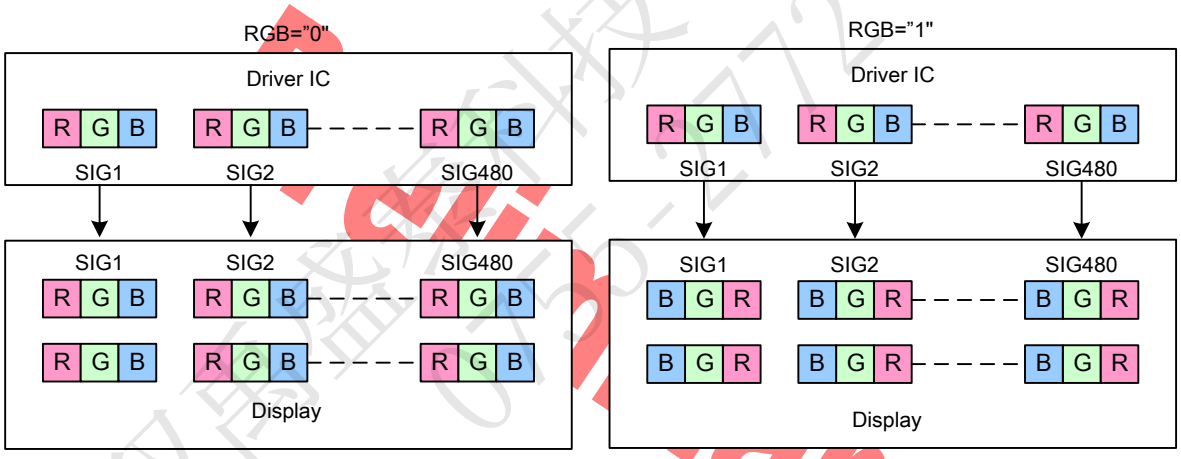
-CA :



LA :



BGR :



Restriction -

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.25 IDMOFF (38H): Idle Mode Off

38H	IDMOFF (Idle Mode Off)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
IDMOFF	Write	0	0	1	1	1	0	0	0	(38H)
Parameter	No Parameter	No Parameter								-
Description	-This command is used to recover from Idle mode on.									
Restriction	-This command has no effect when module is already in idle off mode									
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.26 IDMON (39H): Idle Mode On

38H	IDMOFF (Idle Mode Off)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
IDMON	Write	0	0	1	1	1	0	0	1	(39H)
Parameter	No Parameter	No Parameter								-

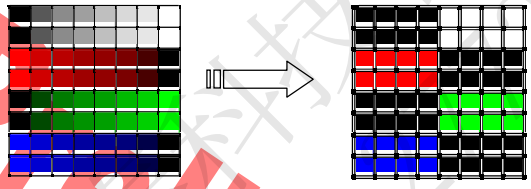
Description

-This command is used to enter into Idle mode on.

-There will be no abnormal visible effect on the display mode change transition.

-In the idle on mode,

1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command



Color	R[7:0]	G[7:0]	B[7:0]
Blank	0xxxxxxx	0xxxxxxx	0xxxxxxx
Blue	0xxxxxxx	0xxxxxxx	1xxxxxxx
Red	1xxxxxxx	0xxxxxxx	0xxxxxxx
Magenta	1xxxxxxx	0xxxxxxx	1xxxxxxx
Green	0xxxxxxx	1xxxxxxx	0xxxxxxx
Cyan	0xxxxxxx	1xxxxxxx	1xxxxxxx
Yellow	1xxxxxxx	1xxxxxxx	0xxxxxxx
White	1xxxxxxx	1xxxxxxx	1xxxxxxx

Restriction

-This command has no effect when module is already in idle on mode

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.27 TESLWR (44H): Write TE Scan Line

44H	WRTESCN (Write TE Scan Line)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
TESLWR	Write	0	1	0	0	0	1	0	0	(44H)
1st Parameter	Write	-	-	-	-	TESN[11:8]				00h
2nd Parameter	Write	TESN[7:0]								00h

Description	- This command turns on the display module's TE signal when the display module reaches line TESN.
Restriction	- The command takes affect with the end of one frame.

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.28 RDSCNL (45H): Read Scan Line

45H	RDSCNL (Read Scan Line)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDSCNL	Write	0	1	0	0	0	1	0	1	(45H)
1st Parameter	Read	-	-	-	-	TESN[11:8]				00h
2nd Parameter	Read	TESN[7:0]								00h

Description	- This read byte returns the current scan line.
Restriction	- The command takes affect with the end of one frame.

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.29 DSTB (4FH): Deep Standby Mode ON

4FH	DSTB (Deep Standby Mode ON)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
DSTB	Write	0	1	0	0	1	1	1	1	(4FH)
Parameter	Write	0	0	0	0	0	0	0	DSTB	00H

Description	- When DSTB = 1 :Deep Standby Mode ON Exit deep standby mode by pulling low "RESX" pin at least 1ms
Restriction	- Only effect at Sleep In mode.
Register Availability	

Status	Availability
Sleep Out, Display On	No
Sleep In	Yes

6.2.30 WRDISBV (51H) Write Display Brightness

51H	WRDISBV (Write Display Brightness)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDSCNL	Write	0	1	0	1	0	0	0	1	(51h)
1st Parameter	Write	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00h

Description	- This command is used to adjust the brightness value of the display. - It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. - In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.
Restriction	-
Register Availability	

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.31 RDDISBV (52H) Read Display Brightness Value

52H	RDDISBV (Read Display Brightness Value)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDISBV	Write	0	1	0	1	0	0	1	0	(52h)
1st Parameter	Read	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00h

Description	- This command returns the brightness value of the display. - It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. - In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. - See command “Write Display Brightness (51H)”. - This command can be used to read the brightness value of the display also when Display brightness control is in automatic mode. - DBV [7:0] is reset when display is in sleep-in mode. - DBV [7:0] is ‘0’ when bit BCTRL of “Write CTRL Display (53H)” command is ‘0’. - DBV[7:0] is manual set brightness specified with “Write CTRL Display (53H)” command when bit BCTRL is ‘1’
Restriction	-
Register Availability	

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.32 WRCTRLD (53H) Write CTRL Display

53H	WRCTRLD (Write CTRL Display)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
WRCTRLD	Write	0	1	0	1	0	0	1	1	(53h)
1st Parameter	Write	0	0	BCTRL	0	DD	BL	0	0	00h

Description

- This command is used to control ambient light, brightness and gamma settings.

-BCTRL：Brightness Control Block On/Off. This bit is always used to switch brightness for display and keyboard.

'0' = Off (Brightness registers are 00h)

'1' = On (Brightness registers are active, according to the other parameters.)

-DD：Display Dimming

'0' = Display Dimming is off

'1' = Display Dimming is on

-BL：Backlight On/Off

'0' = Off (Completely turn off backlight circuit. Control lines must be low.)

'1' = On

-Dimming function is adapted to the brightness registers for display and keyboard when bit BCTRL is changed at dimming-on (DD=1).

-When BL bit changed from 'on' to 'off', backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.

Restriction

-

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.33 RDCTRLD (54H) Read CTRL Display

54H	RDCTRLD (Read CTRL Display)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDCTRLD	Write	0	1	0	1	0	1	0	0	(54h)
1st Parameter	Read	0	0	BCTRL	0	DD	BL	0	0	00h

Description

-This command returns ambient light and brightness control values.

-BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

'0' = Off

'1' = On

-DD: Display Dimming On/Off (Only for manual brightness setting)

'0' = Off

'1' = On

-BL: Backlight Control On/Off

'0' = Off

'1' = On

Restriction

-

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.34 WRCABC (55H) Write Content Adaptive Brightness Control

55H	WRCABC (Write Content Adaptive Brightness Control)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
WRCABD	Write	0	1	0	1	0	1	0	1	(55h)
1st Parameter	Write	CEON	SREON	EN_LEVEL[1:0]		0	0	CABC_MODE[1:0]		00h

Description

- CEON: Color and Skin Enhancement ON/OFF.

  '0' = OFF

  '1' = ON

- SREON: Sunlight Readability Enhancement ON/OFF

  '0' = OFF

  '1' = ON

-EN_LEVEL: Enhancement mode Selection

CEON	SREON	EN_LEVEL[1:0]		Function
0	0	0	0	Enhancement OFF
1	0	0	0	CE LOW
1	0	0	1	CE MIDDLE
1	0	1	1	CE HIGH
0	1	0	0	SRE LOW
0	1	0	1	SRE MIDDLE
0	1	1	0	SRE HIGH
0	1	1	1	SRE USER DEFINE
1	1	0	0	CE / SRE LOW
1	1	0	1	CE / SRE MIDDLE
1	1	1	X	CE / SRE HIGH

Note: "X" is don't care

-CABC_MODE: CABC mode selection

CABC_MODE	Function
0	Off
1	User Interface Mode
2	Still Picture
3	Moving Image

Restriction -

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.35 RDCABC (56H) Read Content Adaptive Brightness Control

56H	WRCABC (Write Content Adaptive Brightness Control)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDCABD	Write	0	1	0	1	0	1	1	0	(56h)
1st Parameter	Read	CEON	SREON	EN_LEVEL[1:0]		0	0	CABC_MODE[1:0]		00h

Description

- CEON: Color and Skin Enhancement ON/OFF.

  '0' = OFF

  '1' = ON

- SREON: Sunlight Readability Enhancement ON/OFF

  '0' = OFF

  '1' = ON

-EN_LEVEL: Enhancement mode Selection

CEON	SREON	EN_LEVEL[1:0]		Function
0	0	0	0	Enhancement OFF
1	0	0	0	CE LOW
1	0	0	1	CE MIDDLE
1	0	1	1	CE HIGH
0	1	0	0	SRE LOW
0	1	0	1	SRE MIDDLE
0	1	1	0	SRE HIGH
0	1	1	1	SRE USER DEFINE

Note: "X" is don't care.

-CABC_MODE: CABC mode selection

CABC_MODE[1:0]	Function
00b	Off
01b	User Interface Mode
10b	Still Picture
11b	Moving Image

Restriction -

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.36 WRCABCMB (5EH) Write CABC Minimum Brightness

5EH	WRCABCMB (Write CABC Minimum Brightness)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
WRCABCMB	Write	0	1	0	1	1	1	1	0	(5Eh)
1st Parameter	Write	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	00h
Description	- This command is used to set the minimum brightness value of the display for CABC function. - In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.									
Restriction	-									

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.37 RDCABCMB (5FH) Read CABC Minimum Brightness

5FH	RDCABCMB (Read CABC Minimum Brightness)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDCABCMB	Write	0	1	0	1	1	1	1	1	(5Fh)
1st Parameter	Read	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	00h
Description	- This command returns the minimum brightness value of CABC function. - In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. - See command “Write CABC Minimum Brightness (5EH)”.									
Restriction	-									

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.38 RDDID1 (DAH) Read Display Identification Information

DAH	RDDID1 (Read Display Identification Information 1)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDID1	Write	0	0	0	0	0	1	0	1	(DAH)
1st Parameter	Read	ID1[7:0]								FFh
Description	- Read Display Identification Information ID1:LCD module's manufacturer ID (FFh: not programmed)									
Restriction	-									
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.39 RDDID2 (DBH) Read Display Identification Information

DBH	RDDID2 (Read Display Identification Information 2)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDID2	Write	0	0	0	0	0	1	0	1	(DBH)
1st Parameter	Read	ID2[7:0]								FFh
Description	- Read Display Identification Information ID2:LCD module/driver version ID (FFh: not programmed)									
Restriction	-									

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.40 RDDID3 (DCH) Read Display Identification Information

DCH	RDDID 3 (Read Display Identification Information 3)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDID3	Write	0	0	0	0	0	1	0	1	(DCH)
1st Parameter	Read	ID3[7:0]								FFh
Description	- Read Display Identification Information ID3:LCD module/driver ID (FFh: not programmed)									
Restriction	-									
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.41 RDDDBS (A1H) : Read DDB Start

A1H	RDDDBS (Read DDB Start)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDDBS	Write	1	0	1	0	0	0	0	1	(A1H)
1st Parameter	Read	SID[7:0]								FFh
2nd Parameter	Read	SID[15:8]								FFh
3rd Parameter	Read	MID[7:0]								FFh
4th Parameter	Read	MID[15:8]								FFh
5th parameter	Read	RID[7:0]								FFh
6th Parameter	Read	RID[15:8]								FFh
7th Parameter	Read	DDB_ID_1[7:0]								FFh
8th Parameter	Read	DDB_ID_2[7:0]								FFh
9th Parameter	Read	DDB_ID_3[7:0]								FFh
10th Parameter	Read	DDB_ID_4[7:0]								FFh

Description

- This command returns supplier identification and display module / revision information.

Note:

1. This information is not the same what DAh/DBh/DCh commands are returning.
2. Parameter 8th is an “Exit code”, this means that there is no more data in the DDB block.

This read sequence can be interrupted by any command and it can be continued by “Read DDB Continue(A8h)” command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1st parameter has been sent => 2nd parameter has been sent => interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.

Restriction

-

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.42 RDDDBC (A8H) : Read DDB Continue

A8H	RDDDBC (Read DDB Continue)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDDBC	Write	1	0	1	0	1	0	0	0	(A8H)
1st Parameter	Read	DDB1[7:0]								FFh
2nd Parameter	Read	DDB2[7:0]								FFh
3rd Parameter	Read	DDB3[7:0]								FFh
4th Parameter	Read	DDB4[7:0]								FFh
5th parameter	Read	DDB5[7:0]								FFh
6th Parameter	Read	DDB6[7:0]								FFh
7th Parameter	Read	DDB7[7:0]								FFh

Description	- This command returns supplier's identification and display module model/revision information from the point where RDDDBS command was interrupt by an other command e.g. RDDDBS was interrupt after 3rd parameter (DDB3). The first parameter (DDB1), what RDDDBC is returning, is DDB4[7:0]. See also section "6.2.36 Read DDB Start (A1h)".
Restriction	-
Register Availability	Status / Availability Sleep Out, Display On / Yes Sleep In / Yes

6.2.43 RDFCS (AAH) : Read First Checksum

AAH	RDFCS (Read First Checksum)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDFCS	Write	1	0	1	0	1	0	1	0	(AAH)
1st Parameter	Read	FCS[7:0]								00h

Description	- Read the first checksum that has been calculated from user commands after write access to these commands has been done.
Restriction	-only in sleep out mode
Register Availability	

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.44 RDCCS (AFH) : Read Continue Checksum

AFH	RDCCS (Read Continue Checksum)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDCCS	Write	1	0	1	0	1	1	1	1	(AFH)
1st Parameter	Read	CCS[7:0]								00h

Description	-Read the continue checksum that has been calculated continuously after the first checksum has calculated from user commands after write access to these commands has been done.
Restriction	-
Register Availability	

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.45 RDICID (F4H) : Read Sitronix IC ID

F4H	RDICID (Read Sitronix IC ID Code)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDICID	Write	1	1	1	1	0	1	0	0	(F4H)
1st Parameter	Read	0	1	1	1	0	0	0	1	71h
2nd Parameter	Read	0	0	1	0	0	0	1	1	23h

Description	- Read Sitronix IC ID Code
Restriction	-
Register Availability	

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.46 MIPIEXTFMAT (F9H) : MIPI Extension Format

F9H	MIPIEXTFMAT (MIPI Extension Format)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
MIPIEXTFMAT	Write	1	1	1	1	1	0	0	1	(F9H)
1st Parameter	Write	0	0	0	0	0	0	PIXEL_EXTEN[1:0]		00h

Description

-The PIXEL_EXTEN is used for pixel extension format.

PIXEL_EXTEN[1:0]	5-6-5 Format	6-6-6 Format	8-8-8 Format
00	R[7:0] = {R[4:0] , 000b } G[7:0] = {G[5:0] , 00b } B[7:0] = {B[4:0] , 000b }	R[7:0] = {R[5:0] , 00b } G[7:0] = {G[5:0] , 00b } B[7:0] = {B[5:0] , 00b }	R[7:0] = R[7:0] G[7:0] = G[7:0] B[7:0] = B[7:0]
01	R[7:0] = {R[4:0] , 111b} G[7:0] = {G[5:0] , 11b} B[7:0] = {B[4:0] , 111b}	R[7:0] = {R[5:0] , 11b} G[7:0] = {G[5:0] , 11b} B[7:0] = {B[5:0] , 11b}	R[7:0] = R[7:0] G[7:0] = G[7:0] B[7:0] = B[7:0]
10	R[7:0] = {R[4:0] ,R[4:2]} G[7:0] = {G[5:0] , G[5:4]} B[7:0] = {B[4:0] , B[4:2]}	R[7:0] = {R[5:0] ,R[5:4]} G[7:0] = {G[5:0] , G[5:4]} B[7:0] = {B[5:0] , B[5:4]}	R[7:0] = R[7:0] G[7:0] = G[7:0] B[7:0] = B[7:0]
11	R[7:0] = {R[4:0] , G[5:3]} G[7:0] = {G[5:0] , G[5:4]} B[7:0] = {B[4:0] , G[5:3]}	R[7:0] = {R[5:0] , G[5:4]} G[7:0] = {G[5:0] , G[5:4]} B[7:0] = {B[5:0] , G[5:4]}	R[7:0] = R[7:0] G[7:0] = G[7:0] B[7:0] = B[7:0]

Restriction

-

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Item	Symbol	Range	Unit
Supply Voltage (Analog)	IOVCC	- 0.3 ~ +2.1	V
Supply Voltage (I/O)	DPHYVCC	- 0.3 ~ +2.1	V
Driver Supply Voltage	AVDD-VSS	-0.3 ~ +6.6	V
Driver Supply Voltage	AVEE-VSS	- 6.6 ~ +0.3	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	-0.3 ~ DPHYVCC + 0.3	V
Logic Output Voltage Range	VO	-0.3 ~ DPHYVCC + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +75	℃
Storage Temperature Range	TSTG	-40 ~ +110	℃

7.2 DC Characteristics

7.2.1 Basic Characteristics

Parameter	Symbol	Condition	Specification	Unit			Note
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
Power supply Voltage	IOVCC		1.65	1.8	3.3	V	
	DPHYVCC		1.65	1.8	3.3	V	
	AVDD		4.5	5.5	6.3	V	
	AVEE		4.5	5.5	6.3	V	
Gate Driver High Voltage	VGH		7		18	V	Note 2
Gate Driver Low Voltage	VGL		-7		-18	V	
Input / Output							
Logic-High Input Voltage	VIH		0.7 IOVCC		IOVCC	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3IOVCC	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8 IOVCC		IOVCC	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2 IOVCC	V	Note 1
Input Leakage Current	IIL	VIN=IOVCC/VSS	-1		+1	uA	Note 1
VCOM Voltage							
VCOM amplitude	VCOM		-2.75		-0.2	V	
Source Driver							
Gamma Amplitude (Positive)	VGPAMP		3		6	V	
Gamma Amplitude (Negative)	VGNAMP		-6		-3	V	

Notes:

1. TA= -30 to 70℃ (to +75℃ no damage).

2. When evaluating the maximum and minimum of VGH/VGL. IOVCC/AVDD/AVEE is typical value.

3. VGH-VGL<28V.

4 . AVDD-VGPAMP>300mV AVEE-VGNAMP>-300mV

7.2.2 Current Consumption

(Ta = 25℃)

Parameter	Symbol	Test Condition	Specification			Unit
			MIN.	TYP.	MAX.	
Power supply voltage	IOVCC = 1.8	Deep standby mode No load on panel	-	TBD		uA
	AVDD = 5.9		-	TBD		uA
	AVEE = -5.9		-	TBD		uA
	IOVCC = 1.8	Sleep in mode No load on panel	-	TBD		mA
	AVDD = 5.9		-	TBD		mA
	AVEE = -5.9		-	TBD		mA

7.2.3 MIPI DC Characteristic

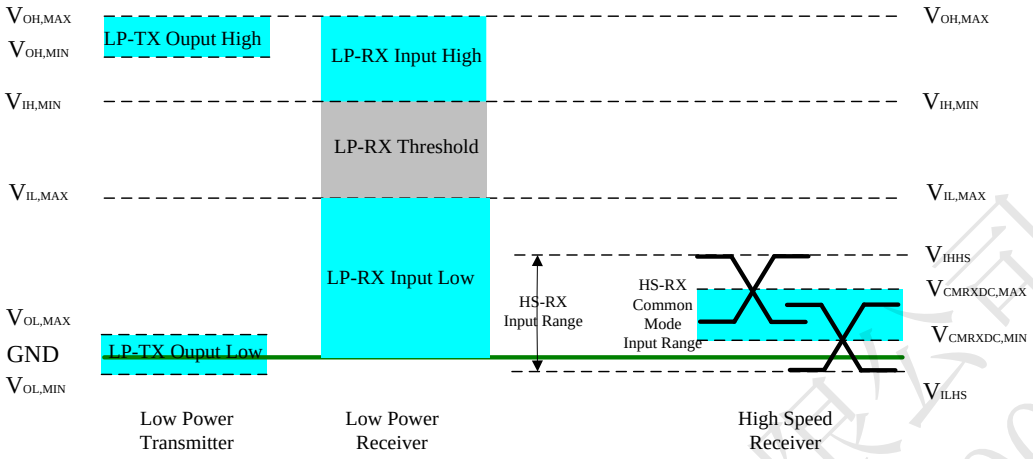


Figure 76 MIPI Signaling Voltage Levels

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	VLPH	-	TBD	-	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	VILHS	TBD	-	-	mV
Single-ended input high voltage	VIHHS	-	-	TBD	mV
Common-mode voltage	VCMRXDC	TBD	-	TBD	mV
Differential input impedance	ZID	TBD	TBD	TBD	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	VI	TBD	-	TBD	mV
Logic 0 input threshold	VIL	TBD	-	TBD	mV
Logic 1 input threshold	VIH	TBD	-	-	mV
Output low level	VOL	TBD	-	TBD	mV
Output high level	VOH	TBD	TBD	TBD	V

7.3 AC Characteristics

7.3.1 MIPI Timing

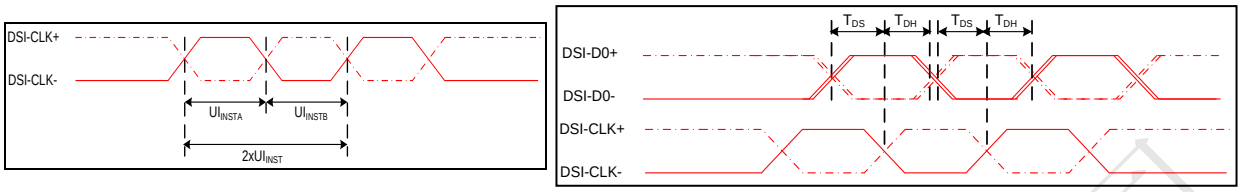


Figure 77 High Speed Mode – Clock Channel Timing

Signal	Symbol	Parameter	Specification			Unit	Description
			MIN	TYP	MAX		
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	TBD	-	TBD	ns	
DSI-CLK+/-	UI_{INSTA} ,UI_{INSTB}	UI instantaneous half	TBD	-	TBD	ns	
fDSI-CLK+/-	F_{DSICLK}	DSI-CLK+/- frequency	TBD	-	TBD	MHz	
DSI-Dn+/-	T_{DS}	Data to clock setup time	TBD	-	-	UI	
DSI-Dn+/-	T_{DH}	Data to clock hold time	TBD	-	-	UI	

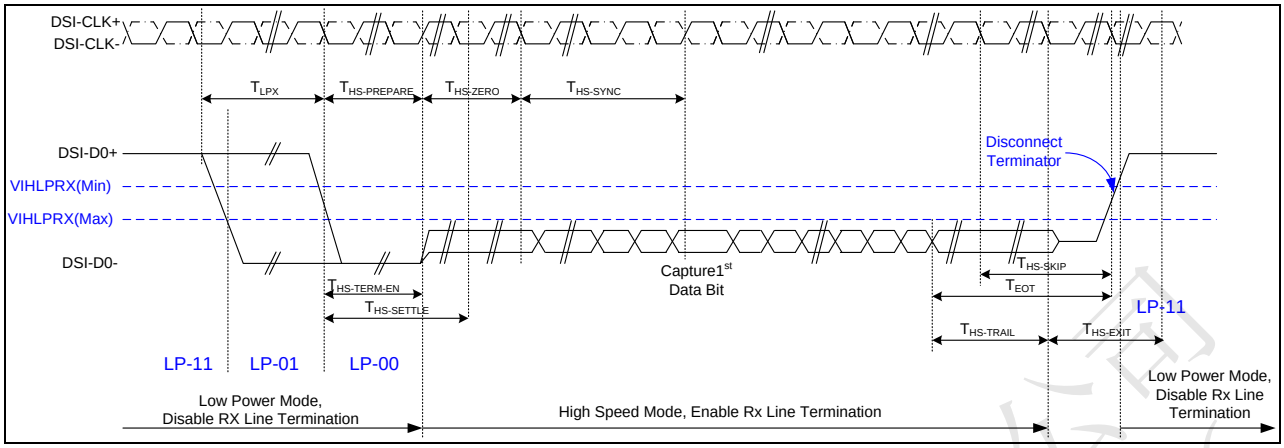


Figure 78 High-Speed Data Transmission

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	TBD	-	TBD	ns
Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state	T_{EOT}	-	-	TBD	ns
Time to enable data receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$	-	-	TBD	ns
Time to drive flipped differential state after last payload data bit of a HS transmission	$T_{HS-TRAIL}$	TBD	-	-	ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	TBD	-	TBD	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	TBD	-	-	ns
Length of any Low-Power state period	T_{LPX}	TBD	-	-	ns
Sync sequence period	$T_{HS-SYNC}$	-	TBD	-	ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	TBD	-	-	ns
Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPAR}$	$T_{CLK-SETTLE}$	TBD	-	TBD	ns
Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPAR}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	$T_{HS-SETTLE}$	TBD	-	TBD	ns

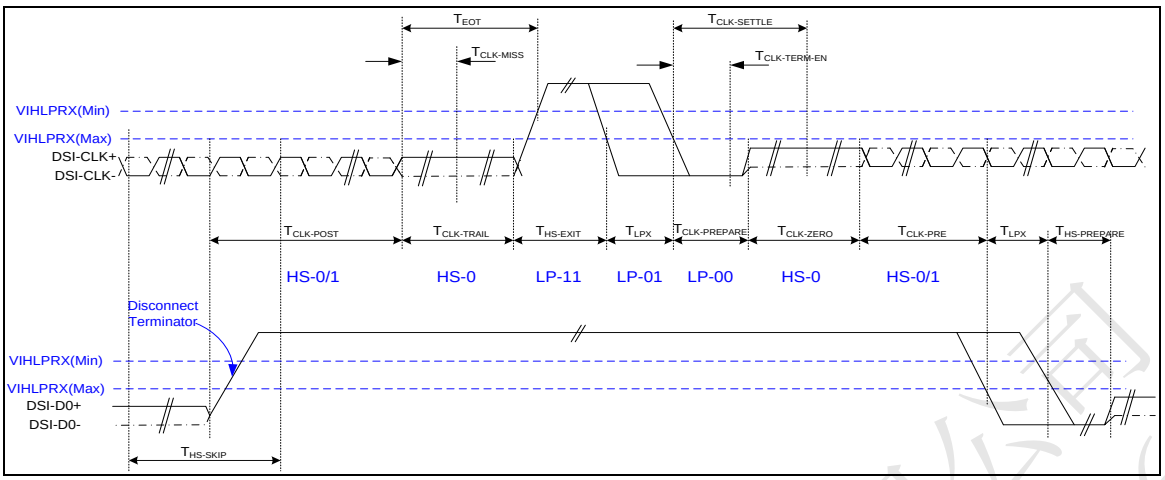


Figure 79 Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	TBD	-	-	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	-	-	TBD	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	TBD	-	TBD	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	TBD	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{CLK-TERM-EN}$	-	-	TBD	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	TBD	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	TBD	-	-	ns

*Note: 3-Lane = (1000 / f_{mipi} * 8 * 52 -T_{HS_TRAIL}- 60) / (1000/f_{mipi})*

*4-Lane = (1000 / f_{mipi} * 8 * 39 -T_{HS_TRAIL}- 60) / (1000/f_{mipi})*

*Example: 3-Lane, 600Mbps : n = (1000 / 600 * 8 * 52 - T_{HS_TRAIL}- 60) / (1000/600) = 340*

*4-Lane, 600Mbps : n = (1000 / 600 * 8 * 39 - T_{HS_TRAIL}- 60) / (1000/600) = 236*

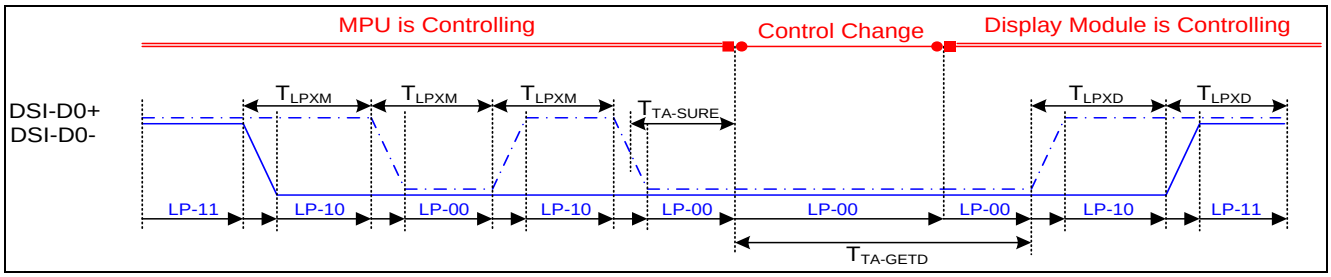


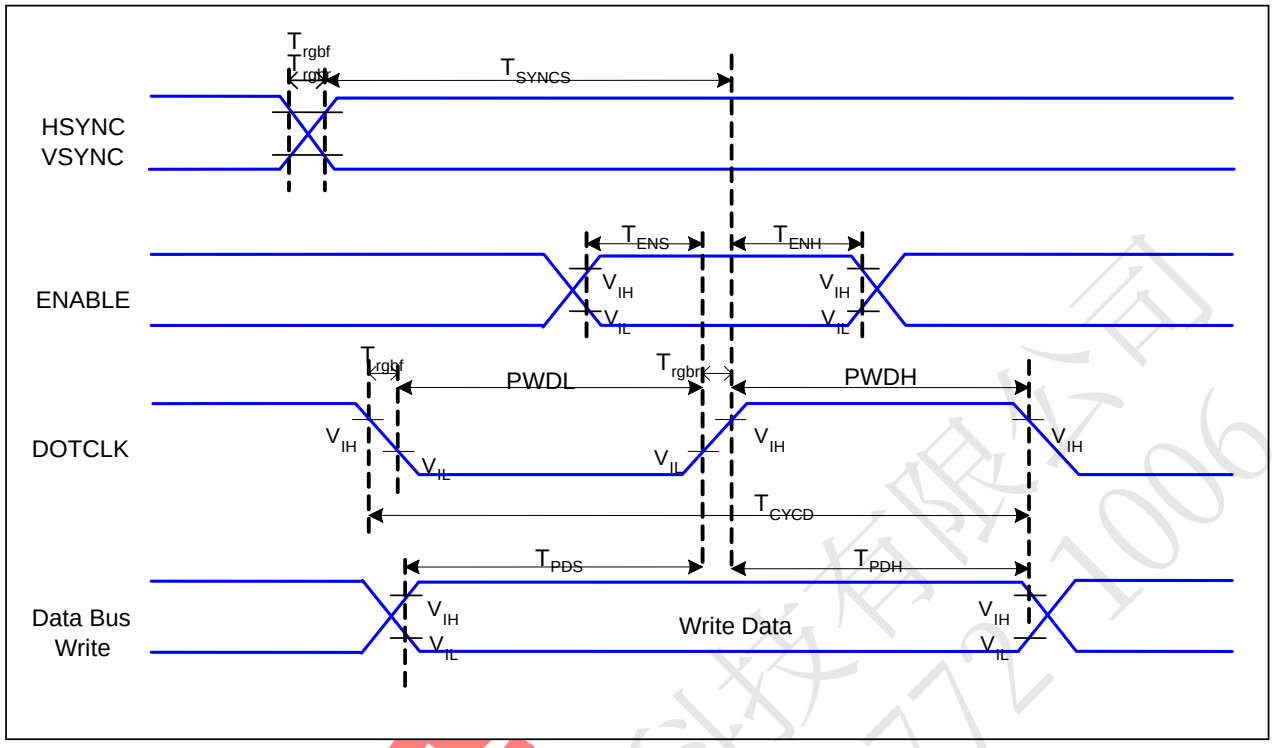
Figure 80 Bus Turn-around Procedure

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Length of any Low-Power state period : Master side	T_{LPX}	TBD	-	TBD	ns
Length of any Low-Power state period : Slave side	T_{LPX}	TBD	-	TBD	ns
Ratio of T_{LPX} (MASTER)/ T_{LPX} (SLAVE) between Master and Slave side	Ratio T_{LPX}	TBD	-	TBD	
Time-out before new TX side start driving	$T_{TA-SURE}$	TBD	-	TBD	ns
Time to drive LP-00 by new TX	T_{TA-GET}	-	TBD	-	ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}	-	TBD	-	ns

7.3.2 MIPI Interface Timing

Parameter	Symbol	Min.	Typ..	Max.	Unit
Horizontal Sync. Width	HPW	TBD	-	-	Byte Clock
Horizontal Sync. Back Porch	HBP	TBD	-	-	Byte Clock
Horizontal Sync. Front Porch	HFP	TBD	-	-	Byte Clock
Vertical Sync. Width	VSW	TBD	-	-	Line
Vertical Sync. Back Porch	VBP	TBD	-	-	Line
Vertical Sync. Front Porch	VFP	TBD	-	-	Line
Vertical Frequency		-	TBD	-	Hz

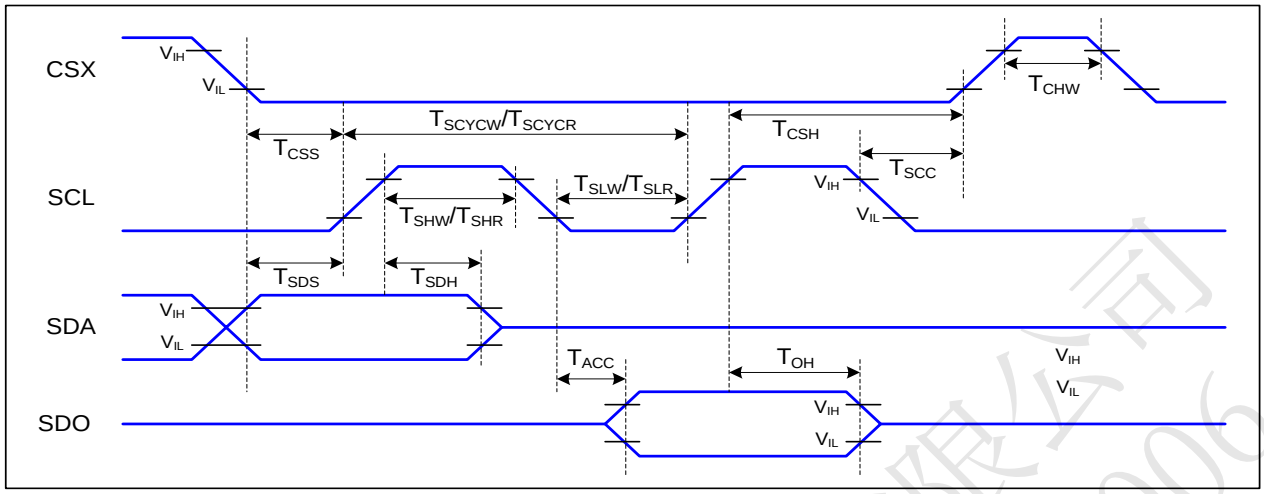
7.3.3 RGB timing



IOVCC=1.8V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	TBD	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	TBD	-	ns	
	T_{ENH}	Enable Hold Time	TBD	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	TBD	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	TBD	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	TBD	-	ns	
DB	T_{PDS}	PD Data Setup Time	TBD	-	ns	
	T_{PDH}	PD Data Hold Time	TBD	-	ns	

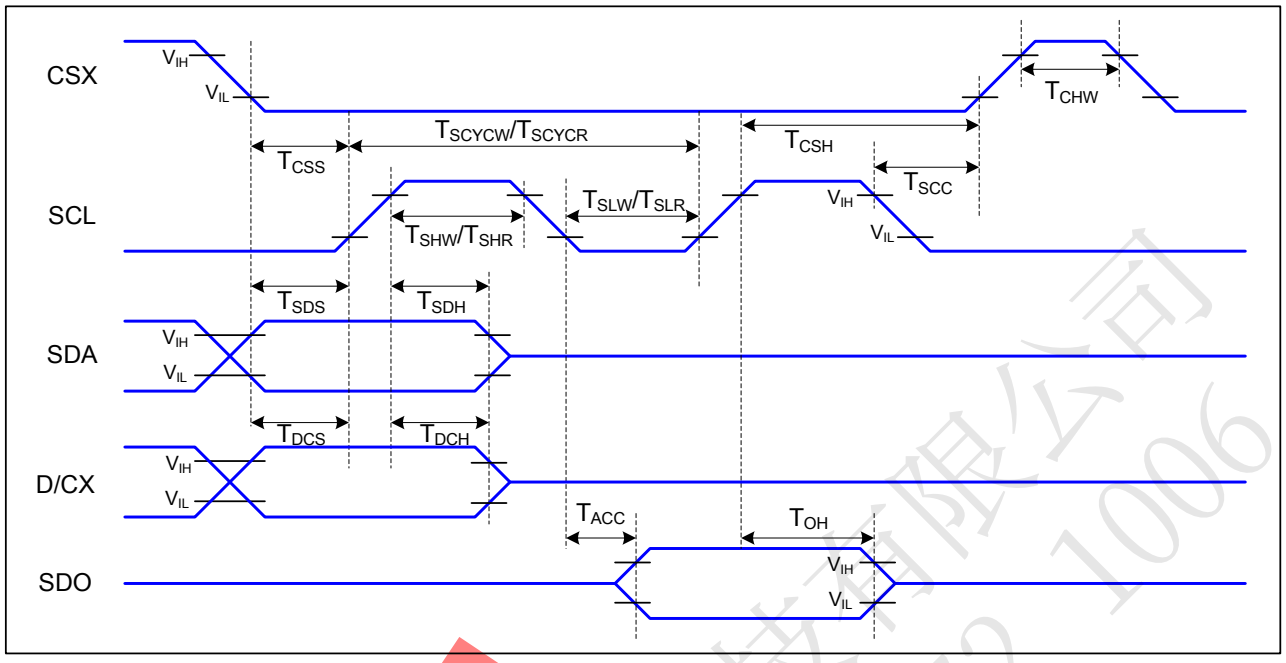
7.3.4 SPI9 & SPI16 Timing



IOVCC=1.8V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD		ns	
	T_{CSH}	Chip select hold time (write)	TBD		ns	
	T_{CSS}	Chip select setup time (read)	TBD		ns	
	T_{SCC}	Chip select hold time (read)	TBD		ns	
	T_{CHW}	Chip select “H” pulse width	TBD		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD		ns	
	T_{SHW}	SCL “H” pulse width (Write)	TBD		ns	
	T_{SLW}	SCL “L” pulse width (Write)	TBD		ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD		ns	
	T_{SHR}	SCL “H” pulse width (Read)	TBD		ns	
	T_{SLR}	SCL “L” pulse width (Read)	TBD		ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD		ns	
	T_{SDH}	Data hold time	TBD		ns	
DOUT	T_{ACC}	Access time	TBD	TBD	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

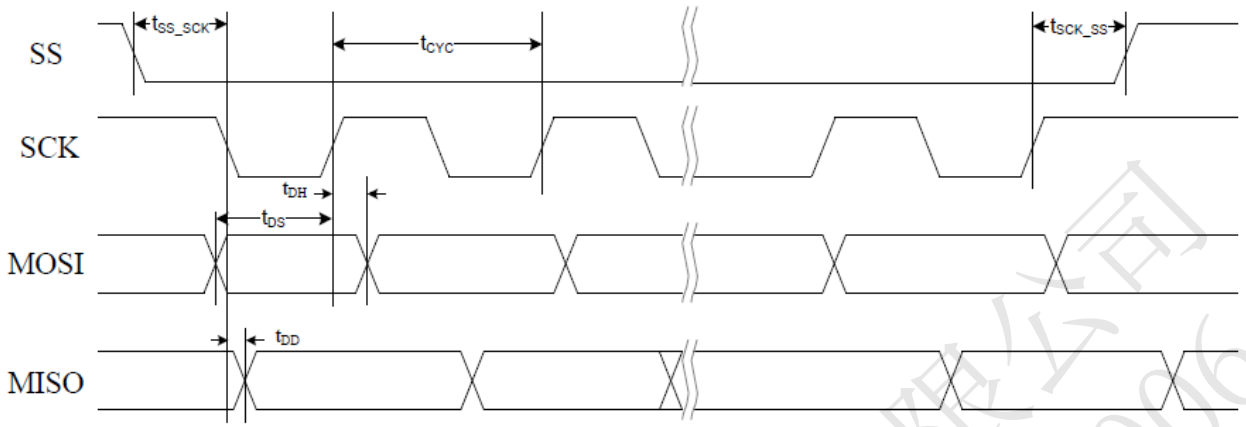
7.3.5 SPI8 (4 line) Timing



IOVCC=1.8V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD		ns	
	T_{CSH}	Chip select hold time (write)	TBD		ns	
	T_{CSS}	Chip select setup time (read)	TBD		ns	
	T_{SCC}	Chip select hold time (read)	TBD		ns	
	T_{CHW}	Chip select “H” pulse width	TBD		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	TBD		ns	
	T_{SLW}	SCL “L” pulse width (Write)	TBD		ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	TBD		ns	
	T_{SLR}	SCL “L” pulse width (Read)	TBD		ns	
D/CX	T_{DCS}	D/CX setup time	TBD		ns	
	T_{DCH}	D/CX hold time	TBD		ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD		ns	
	T_{SDH}	Data hold time	TBD		ns	
DOUT	T_{ACC}	Access time	TBD	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	50	ns	For minimum CL=8pF

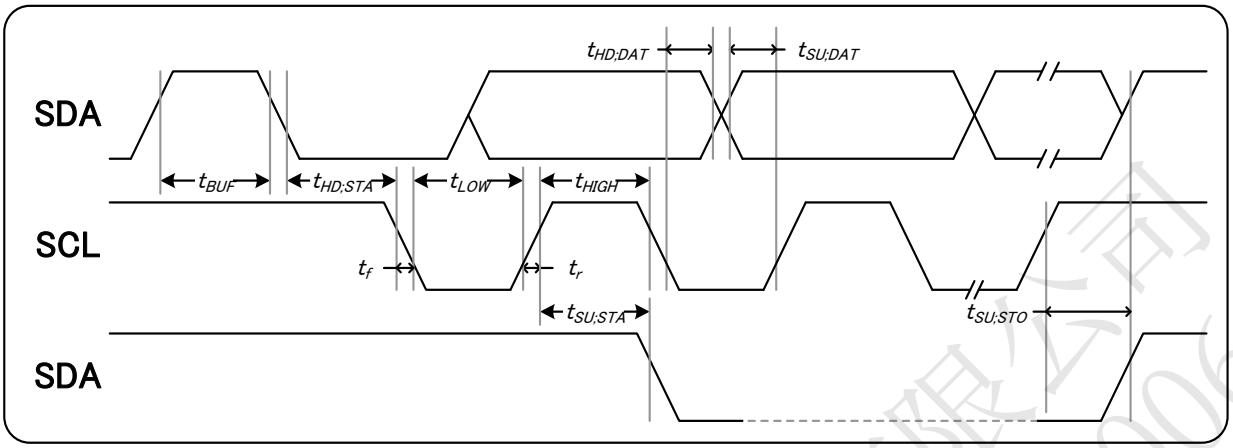
7.3.6 Touch SPI Timing



IOVCC=1.8V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCK	f_{SCK}	SCK frequency	-	TBD	Mhz	
SCK	t_{CYC}	SCK cycle time	TBD	-	ns	
MOSI	t_{DS}	Data setup time prior SCK rising	TBD	-	ns	
	t_{DH}	Data hold time after SCK rising	TBD	-	ns	
MISO	t_{DD}	MISO data output delay from SCK falling	-	TBD	ns	
SS	t_{SS}_SCK	SS falling to 1st SCK falling	TBD	-	ns	
	t_{SCK}_SS	SCK rising to SS rising	TBD	-	ns	
	t_R	CS recovery time	TBD	-	us	

7.3.7 Touch I2C timing



IOVCC=1.8V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	f_{SCL}	SCL clock frequency	-	TBD	kHz	
	t_{LOW}	SCL clock low period	TBD	-	ns	
	t_{HIGH}	SCL clock high period	TBD	-	ns	
SDA	t_{SU};Data	Data set-up time	TBD	-	ns	
	t_{HD};Data	Data hold time	TBD	-	ns	
SDA	t_{SU};STA	Setup time for a repeated START condition	TBD	-	ns	
	t_{HD};STA	Start condition hold time	TBD	-	ns	
	t_{SU};STO	Setup time for STOP condition	TBD	-	ns	
	t_{BUF}	Bus free time between a STOP and START	TBD	-	us	

7.3.8 Reset Timing

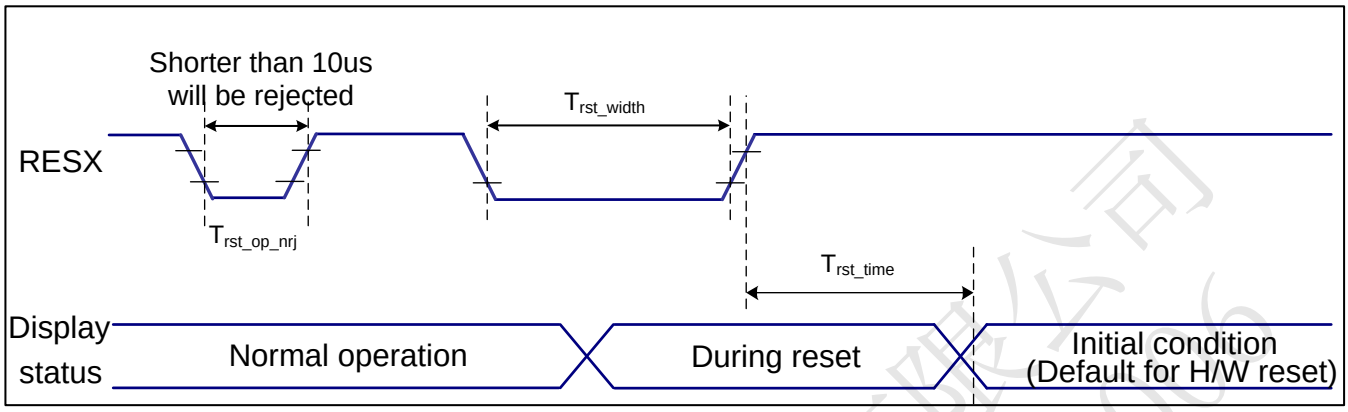


Figure 81 Reset Operation

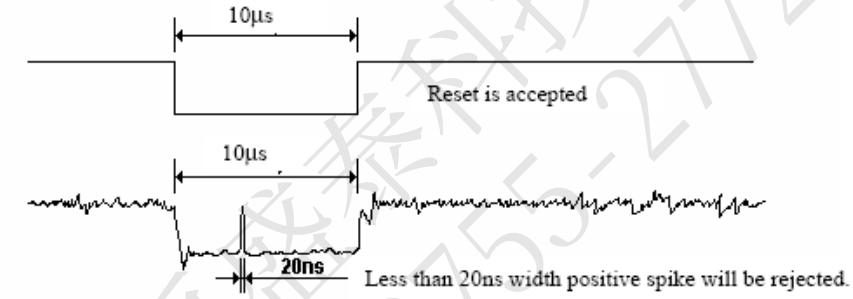


Figure 82 Reset Noise Rejected Diagram

Reset Timing Characteristics IOVCC=1.8v Ta=25℃

Parameter	Symbol	Specification			Unit
		Min.	Typ.	Max.	
Reset low width	Trst_width	TBD	-	-	ms
Reset time	Trst_time	TBD	-	-	ms
OP noise reject	Trst_op_nrj	-	-	TBD	us

- During the reset period, the display will be blanked, then return to default condition for IC initialization

7.3.9 Abnormal Timing:

ST7102 provides abnormal power drop detection function, but there has a premise that external power must drop at low ramp, or the discharge function will not work. The following diagram is show how much time that external power drop from 90% to 10% is suitable.

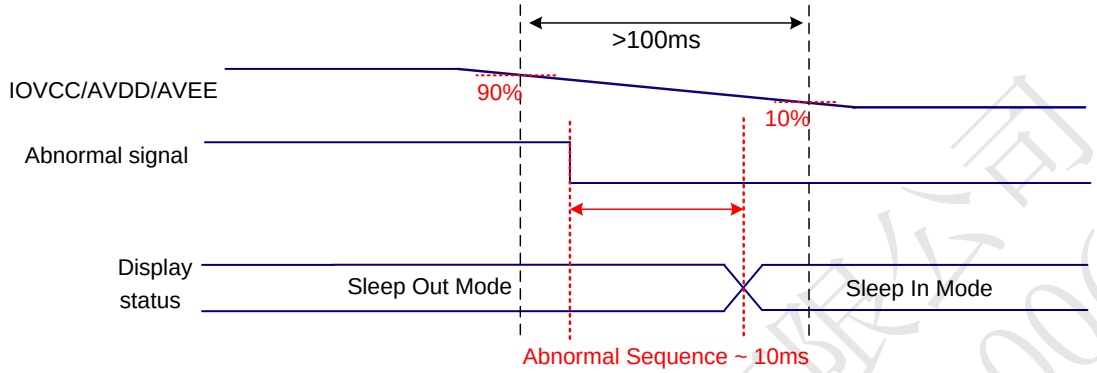


Figure 83 Reset Noise Rejected Diagram

Reset Timing Characteristics IOVCC=1.8v, AVDD=5.8v, AVEE=-5.8v Ta=25℃

External power	Power drop time from 90% to 10%			Unit
	Min.	Typ.	Max.	
IOVCC	100			ms
AVDD	100			ms
AVEE	100			ms

Note: Due to IOVCC is critical for whole chip, keep IOVCC as stable as possible

8 REVISION HISTORY

Version	Date	Description
V0.0	2023/10	**First issue**
V0.1	2024/01	**Modify Interface Select P13**
V0.21	2024/10	**Addition Some PAD description. P12~P17** **Addition RGB application2 Table P93**