Sitronix

ST7262

1200CH System-On-Chip Driver for 800RGBx480 TFT LCD

Datasheet

Version 1.0
2020/10

Hazardous Substance Free
RoHS/ REACH Compliant

Sitronix Technology Corporation

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1. GENERAL DESCRIPTION

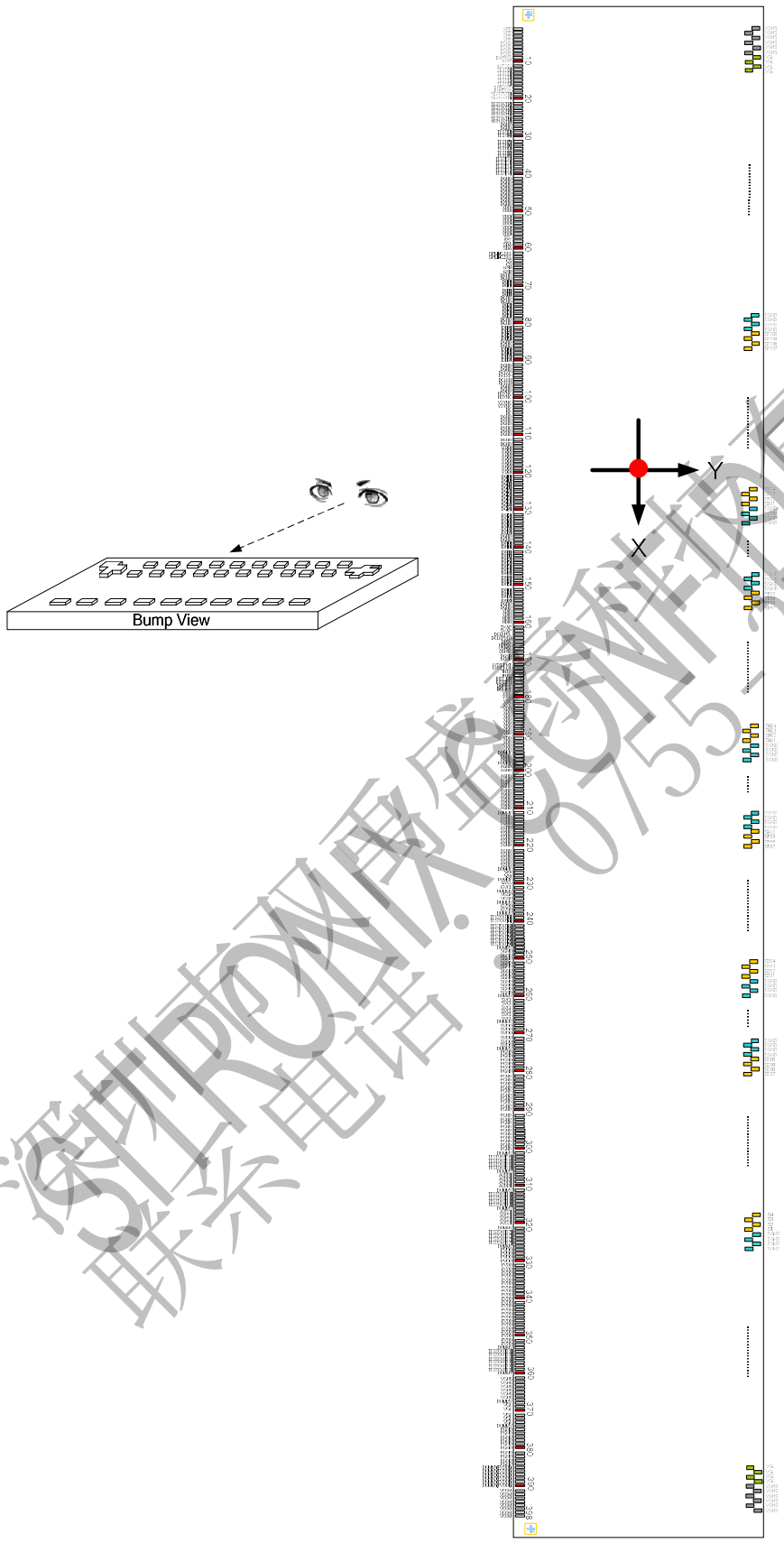
IC offers all-in-one chip solution of 800RGBx480 for color dual gate TFT-LCD panel. The driver IC output ports consists of 1200 source channels and 20 gate control channels for panel application. This chip incorporated with digital timing generator, source and gate driver, power supply circuit and embedded 3-wire SPI and I^2C interfaces for function setting. The display data bits sent from MCU via LVDS interface or RGB interface directly related to the pixels of LCD panel. The source output supports 256 gray scale with real 8-bit DAC to get a small output deviation for high color resolution. The power supply circuit incorporated with step-up circuit, regulators and operational amplifiers to generate power supply voltages to drive TFT LCD.

2. FEATURES

- Display Resolution: arbitrary resolution up to 800*RGB (H) * 480(V)
  -256 Gray Scale with True 8-bit DAC
  -full color mode: 16.7M, RGB(888) max
- LCD Driver Output Circuits
  - source outputs: 1200channels
  - gate outputs: 20 GIP control signals
  - common electrode output
- Microprocessor Interface
- - 3 lane and 4 lane LVDS interface
  - 24-bit RGB interface support: SYNC, SYNC-DE and DE mode
  - 3-wire SPI and I^2C interface
- On Chip Build-In Circuits
  - DC/DC converter
  - Multi-OTP circuit
  - Timing controller
- Wide Supply Voltage Range
  - I/O voltage (VDDI to DGND): 3.1V ~3.6V
  - analog voltage (VDD to AGND): 3.1V ~3.6V
  - charge pump voltage (PVDD to PGND): 3.1V ~3.6V
  - enhance charge pump voltage (DUMMY(PVDD1) to PGND): 3.1V ~3.6V
- On-Chip Power System
  - GVDD: 4.960V ~ 5.968V
  - GVCL: -2.960V ~ -4.480V
  - VCOM: GND (Including built-in circuit for compensating feed-through voltage)
  - Maximum Vop : Vop(Max.) ≤ GVDD-VCOM" = VCOM"-GVCL
- Optimized Layout for COG Assembly
- Built-in Multi-OTP Programming Circuit
  - Internal VPP power supply
- Multi-OTP Adjustable Parameters
- - 7-bit for VCOM offset adjustment
- - 7-bit ID1/ID2/ID3 OTP for end user use
- - 7-bit I2C I/F ID OTP for end user use
- - Command2 OTP for end user use
- - Gamma OTP for end user use
- Temperature Range: −30°C ~ 85°C
- **Design for consumer applications; this product is not designed for use in cars, motorcycles, marine equipment, aircraft equipment, military equipment and other applications in extreme environment.**

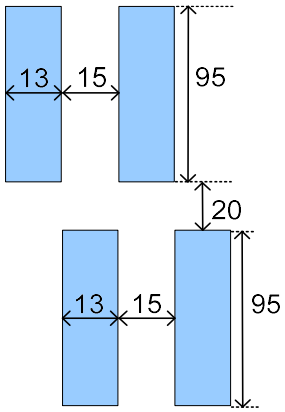
3. PAD ARRANGEMENT

3.1 Output Bump Dimension

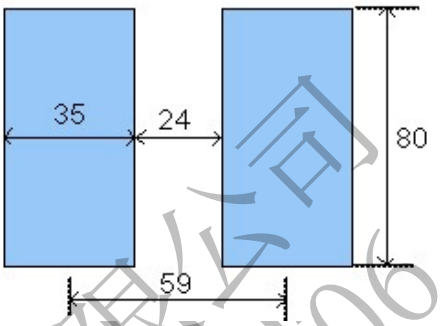


3.2 Bump Dimension

- (Pad NO. 399~1990)

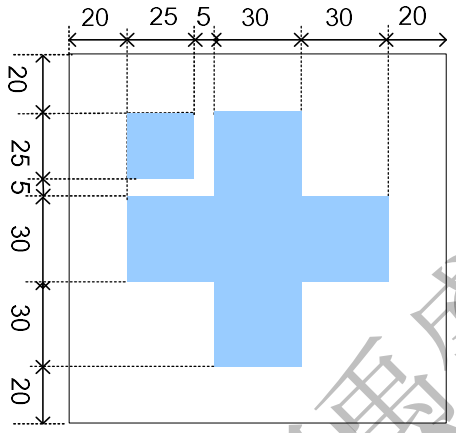


(Pad NO. 1~398)

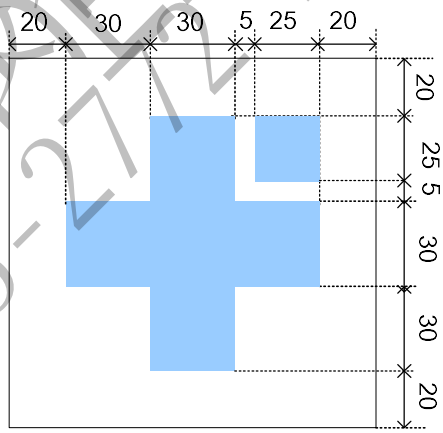


3.3 Alignment Mark Dimension

Alignment Mark: A1(X,Y)=(-11812,-337)



Alignment Mark: A2(X,Y)=(11812,-337)



4. PAD CENTER COORDINATES

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	VPP	-11712	-340	34	TESTI[8]	-9765	-340
2	VPP	-11653	-340	35	TESTI[9]	-9706	-340
3	VPP	-11594	-340	36	TESTI[10]	-9647	-340
4	VPP	-11535	-340	37	TESTI[11]	-9588	-340
5	PGND	-11476	-340	38	TESTI[12]	-9529	-340
6	PGND	-11417	-340	39	TESTI[13]	-9470	-340
7	PGND	-11358	-340	40	TESTI[14]	-9411	-340
8	PGND	-11299	-340	41	DGND	-9352	-340
9	ENPROG	-11240	-340	42	DGND	-9293	-340
10	DISP	-11181	-340	43	DGND	-9234	-340
11	AUTODL	-11122	-340	44	DGND	-9175	-340
12	TESTI[0]	-11063	-340	45	DGND	-9116	-340
13	TESTI[1]	-11004	-340	46	DGND	-9057	-340
14	TESTI[1]	-10945	-340	47	DGND	-8998	-340
15	TESTI[2]	-10886	-340	48	DGND	-8939	-340
16	TESTI[2]	-10827	-340	49	VDDI	-8880	-340
17	ERR_OUT	-10768	-340	50	VDDI	-8821	-340
18	ERR_OUT	-10709	-340	51	VDDI	-8762	-340
19	TESTOUT[0]	-10650	-340	52	VDDI	-8703	-340
20	TESTOUT[1]	-10591	-340	53	VDDI	-8644	-340
21	TESTOUT[2]	-10532	-340	54	VDDI	-8585	-340
22	TESTOUT[3]	-10473	-340	55	VDDI	-8526	-340
23	TESTOUT[4]	-10414	-340	56	VDDI	-8467	-340
24	TESTOUT[5]	-10355	-340	57	SCL	-8408	-340
25	TESTOUT[6]	-10296	-340	58	SCL	-8349	-340
26	TESTOUT[7]	-10237	-340	59	SDA	-8290	-340
27	DGND	-10178	-340	60	SDA	-8231	-340
28	DGND	-10119	-340	61	SPI_I2C_SEL	-8172	-340
29	TESTI[3]	-10060	-340	62	SPI_I2C_SEL	-8113	-340
30	TESTI[4]	-10001	-340	63	CS	-8054	-340
31	TESTI[5]	-9942	-340	64	CS	-7995	-340
32	TESTI[6]	-9883	-340	65	GRB	-7936	-340
33	TESTI[7]	-9824	-340	66	GRB	-7877	-340

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
67	DGND	-7818	-340	100	HSYNC	-5871	-340
68	DGND	-7759	-340	101	VSYNC	-5812	-340
69	DB[0]	-7700	-340	102	VSYNC	-5753	-340
70	DB[0]	-7641	-340	103	DE	-5694	-340
71	DB[1]	-7582	-340	104	DE	-5635	-340
72	DB[1]	-7523	-340	105	DGND	-5576	-340
73	DGND	-7464	-340	106	DGND	-5517	-340
74	DGND	-7405	-340	107	DGND	-5458	-340
75	DB[2]	-7346	-340	108	DGND	-5399	-340
76	DB[2]	-7287	-340	109	DGND	-5340	-340
77	DB[3]	-7228	-340	110	DGND	-5281	-340
78	DB[3]	-7169	-340	111	DGND	-5222	-340
79	DGND	-7110	-340	112	DGND	-5163	-340
80	DGND	-7051	-340	113	VDDI	-5104	-340
81	DB[4]	-6992	-340	114	VDDI	-5045	-340
82	DB[4]	-6933	-340	115	VDDI	-4986	-340
83	DB[5]	-6874	-340	116	VDDI	-4927	-340
84	DB[5]	-6815	-340	117	VDDI	-4868	-340
85	DGND	-6756	-340	118	VDDI	-4809	-340
86	DGND	-6697	-340	119	VDDI	-4750	-340
87	DB[6]	-6638	-340	120	VDDI	-4691	-340
88	DB[6]	-6579	-340	121	DG[0]	-4632	-340
89	DB[7]	-6520	-340	122	DG[0]	-4573	-340
90	DB[7]	-6461	-340	123	DG[1]	-4514	-340
91	DGND	-6402	-340	124	DG[1]	-4455	-340
92	DGND	-6343	-340	125	DG[2]	-4396	-340
93	DCLKP	-6284	-340	126	DG[2]	-4337	-340
94	DCLKP	-6225	-340	127	DG[3]	-4278	-340
95	DCLKN	-6166	-340	128	DG[3]	-4219	-340
96	DCLKN	-6107	-340	129	DG[4]	-4160	-340
97	DGND	-6048	-340	130	DG[4]	-4101	-340
98	DGND	-5989	-340	131	DG[5]	-4042	-340
99	HSYNC	-5930	-340	132	DG[5]	-3983	-340

PAD No.	PIN Name	X	Y
133	DG[6]	-3924	-340
134	DG[6]	-3865	-340
135	DG[7]	-3806	-340
136	DG[7]	-3747	-340
137	DGND	-3688	-340
138	DGND	-3629	-340
139	DR[0]	-3570	-340
140	DR[0]	-3511	-340
141	DR[1]	-3452	-340
142	DR[1]	-3393	-340
143	DR[2]	-3334	-340
144	DR[2]	-3275	-340
145	DR[3]	-3216	-340
146	DR[3]	-3157	-340
147	DR[4]	-3098	-340
148	DR[4]	-3039	-340
149	DR[5]	-2980	-340
150	DR[5]	-2921	-340
151	DR[6]	-2862	-340
152	DR[6]	-2803	-340
153	DR[7]	-2744	-340
154	DR[7]	-2685	-340
155	DGND	-2626	-340
156	DGND	-2567	-340
157	VDIR	-2508	-340
158	VDIR	-2449	-340
159	HDIR	-2390	-340
160	HDIR	-2331	-340
161	SWAP	-2272	-340
162	SWAP	-2213	-340
163	DCLKPOL	-2154	-340
164	DCLKPOL	-2095	-340
165	HDPOL	-2036	-340

PAD No.	PIN Name	X	Y
166	HDPOL	-1977	-340
167	VDPOL	-1918	-340
168	VDPOL	-1859	-340
169	DGND	-1800	-340
170	DGND	-1741	-340
171	LVDS_FMT	-1682	-340
172	LVDS_FMT	-1623	-340
173	INTF	-1564	-340
174	INTF	-1505	-340
175	BIST_EN	-1446	-340
176	BIST_EN	-1387	-340
177	DUMMY	-1328	-340
178	DUMMY	-1269	-340
179	VCC	-1210	-340
180	VCC	-1151	-340
181	VCC	-1092	-340
182	VCC	-1033	-340
183	VDD	-974	-340
184	VDD	-915	-340
185	VDD	-856	-340
186	VDD	-797	-340
187	VDD	-738	-340
188	VDD	-679	-340
189	VDD	-620	-340
190	VDD	-561	-340
191	VDD	-502	-340
192	VDD	-443	-340
193	VDD	-384	-340
194	VDD	-325	-340
195	DUMMY	-266	-340
196	RGND	-207	-340
197	RGND	-148	-340
198	DUMMY	-89	-340

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
199	AGND	-30	-340	232	DUMMY	1918	-340
200	AGND	30	-340	233	VGSP	1977	-340
201	AGND	89	-340	234	VGSP	2036	-340
202	AGND	148	-340	235	DUMMY	2095	-340
203	AGND	207	-340	236	GVDD	2154	-340
204	AGND	266	-340	237	GVDD	2213	-340
205	AGND	325	-340	238	DUMMY	2272	-340
206	AGND	384	-340	239	TESTOUT[8]	2331	-340
207	AGND	443	-340	240	TESTOUT[8]	2390	-340
208	AGND	502	-340	241	TESTOUT[8]	2449	-340
209	AGND	561	-340	242	TESTOUT[8]	2508	-340
210	AGND	620	-340	243	TESTOUT[9]	2567	-340
211	DUMMY	679	-340	244	TESTOUT[9]	2626	-340
212	SGND	738	-340	245	TESTOUT[9]	2685	-340
213	SGND	797	-340	246	TESTOUT[9]	2744	-340
214	SGND	856	-340	247	DUMMY	2803	-340
215	SGND	915	-340	248	SGND	2862	-340
216	SGND	974	-340	249	SGND	2921	-340
217	SGND	1033	-340	250	SGND	2980	-340
218	SGND	1092	-340	251	SGND	3039	-340
219	SGND	1151	-340	252	SGND	3098	-340
220	SGND	1210	-340	253	SGND	3157	-340
221	SGND	1269	-340	254	SGND	3216	-340
222	SGND	1328	-340	255	SGND	3275	-340
223	SGND	1387	-340	256	SGND	3334	-340
224	SGND	1446	-340	257	SGND	3393	-340
225	SGND	1505	-340	258	SGND	3452	-340
226	DUMMY	1564	-340	259	SGND	3511	-340
227	V20	1623	-340	260	DUMMY	3570	-340
228	V20	1682	-340	261	SVCL	3629	-340
229	DUMMY	1741	-340	262	SVCL	3688	-340
230	GVCL	1800	-340	263	SVCL	3747	-340
231	GVCL	1859	-340	264	SVCL	3806	-340

PAD No.	PIN Name	X	Y
265	SVCL	3865	-340
266	SVCL	3924	-340
267	DUMMY	3983	-340
268	SVDD	4042	-340
269	SVDD	4101	-340
270	SVDD	4160	-340
271	SVDD	4219	-340
272	SVDD	4278	-340
273	SVDD	4337	-340
274	DUMMY	4396	-340
275	PGND	4455	-340
276	PGND	4514	-340
277	PGND	4573	-340
278	PGND	4632	-340
279	PGND	4691	-340
280	PGND	4750	-340
281	PGND	4809	-340
282	PGND	4868	-340
283	PGND	4927	-340
284	PGND	4986	-340
285	PGND	5045	-340
286	PGND	5104	-340
287	PGND	5163	-340
288	PGND	5222	-340
289	PGND	5281	-340
290	PGND	5340	-340
291	PGND	5399	-340
292	PGND	5458	-340
293	PGND	5517	-340
294	PGND	5576	-340
295	PGND	5635	-340
296	PGND	5694	-340
297	PGND	5753	-340
298	PGND	5812	-340
299	PGND	5871	-340
300	PGND	5930	-340
301	DUMMY	5989	-340
302	TESTOUT[10]	6048	-340
303	TESTOUT[10]	6107	-340
304	TESTOUT[10]	6166	-340
305	TESTOUT[10]	6225	-340
306	DUMMY	6284	-340
307	AVDD1	6343	-340
308	AVDD1	6402	-340
309	AVDD1	6461	-340
310	AVDD1	6520	-340
311	DUMMY	6579	-340
312	TESTOUT[11]	6638	-340
313	TESTOUT[11]	6697	-340
314	TESTOUT[11]	6756	-340
315	TESTOUT[11]	6815	-340
316	DUMMY	6874	-340
317	AVCL1	6933	-340
318	AVCL1	6992	-340
319	AVCL1	7051	-340
320	AVCL1	7110	-340
321	DUMMY	7169	-340
322	TESTOUT[12]	7228	-340
323	TESTOUT[12]	7287	-340
324	TESTOUT[12]	7346	-340
325	TESTOUT[12]	7405	-340
326	DUMMY	7464	-340
327	PVDD	7523	-340
328	PVDD	7582	-340
329	PVDD	7641	-340
330	PVDD	7700	-340

PAD No.	PIN Name	X	Y
331	PVDD	7759	-340
332	PVDD	7818	-340
333	PVDD	7877	-340
334	PVDD	7936	-340
335	PVDD	7995	-340
336	PVDD	8054	-340
337	PVDD	8113	-340
338	PVDD	8172	-340
339	PVDD	8231	-340
340	PVDD	8290	-340
341	PVDD	8349	-340
342	PVDD	8408	-340
343	PVDD	8467	-340
344	PVDD	8526	-340
345	PVDD	8585	-340
346	PVDD	8644	-340
347	PVDD	8703	-340
348	PVDD	8762	-340
349	PVDD	8821	-340
350	PVDD	8880	-340
351	PVDD	8939	-340
352	PVDD	8998	-340
353	DUMMY	9057	-340
354	TESTOUT[13]	9116	-340
355	TESTOUT[13]	9175	-340
356	TESTOUT[13]	9234	-340
357	TESTOUT[13]	9293	-340
358	TESTOUT[13]	9352	-340
359	TESTOUT[13]	9411	-340
360	DUMMY	9470	-340
361	VGHS	9529	-340
362	VGHS	9588	-340
363	VGHS	9647	-340

PAD No.	PIN Name	X	Y
364	VGHS	9706	-340
365	VGHS	9765	-340
366	VGHS	9824	-340
367	DUMMY	9883	-340
368	VGL	9942	-340
369	VGL	10001	-340
370	VGL	10060	-340
371	VGL	10119	-340
372	VGL	10178	-340
373	VGL	10237	-340
374	DUMMY	10296	-340
375	PGND	10355	-340
376	PGND	10414	-340
377	PGND	10473	-340
378	PGND	10532	-340
379	PGND	10591	-340
380	PGND	10650	-340
381	PGND	10709	-340
382	PGND	10768	-340
383	PGND	10827	-340
384	PGND	10886	-340
385	DUMMY (PVDD1)	10945	-340
386	DUMMY (PVDD1)	11004	-340
387	DUMMY (PVDD1)	11063	-340
388	DUMMY (PVDD1)	11122	-340
389	DUMMY (PVDD1)	11181	-340
390	DUMMY (PVDD1)	11240	-340
391	VCOM	11299	-340
392	VCOM	11358	-340
393	VCOM	11417	-340
394	VCOM	11476	-340
395	VCOM	11535	-340
396	VCOM	11594	-340

PAD No.	PIN Name	X	Y
397	VCOM	11653	-340
398	VCOM	11712	-340
399	VGHS	11606	330
400	VGHS	11592	215
401	VGHS	11578	330
402	VGHS	11564	215
403	VGHS	11550	330
404	VGHS	11536	215
405	VGL	11522	330
406	VGL	11508	215
407	VGL	11494	330
408	VGL	11480	215
409	VGL	11466	330
410	VGL	11452	215
411	GOR[1]	11382	330
412	GOR[1]	11368	215
413	GOR[1]	11354	330
414	GOR[2]	11340	215
415	GOR[2]	11326	330
416	GOR[2]	11312	215
417	GOR[3]	11298	330
418	GOR[3]	11284	215
419	GOR[3]	11270	330
420	GOR[4]	11256	215
421	GOR[4]	11242	330
422	GOR[4]	11228	215
423	GOR[5]	11214	330
424	GOR[5]	11200	215
425	GOR[5]	11186	330
426	GOR[6]	11172	215
427	GOR[6]	11158	330
428	GOR[6]	11144	215
429	GOR[7]	11130	330

PAD No.	PIN Name	X	Y
430	GOR[7]	11116	215
431	GOR[7]	11102	330
432	GOR[8]	11088	215
433	GOR[8]	11074	330
434	GOR[8]	11060	215
435	GOR[9]	11046	330
436	GOR[9]	11032	215
437	GOR[9]	11018	330
438	GOR[10]	11004	215
439	GOR[10]	10990	330
440	GOR[10]	10976	215
441	VGHS	10906	330
442	VGHS	10892	215
443	VGHS	10878	330
444	VGHS	10864	215
445	VGHS	10850	330
446	VGHS	10836	215
447	VGL	10822	330
448	VGL	10808	215
449	VGL	10794	330
450	VGL	10780	215
451	VGL	10766	330
452	VGL	10752	215
453	DUMMY	10682	330
454	DUMMY	10668	215
455	DUMMY	10654	330
456	DUMMY	10640	215
457	DUMMY	10626	330
458	DUMMY	10612	215
459	DUMMY	10598	330
460	DUMMY	10584	215
461	DUMMY	10570	330
462	DUMMY	10556	215

PAD No.	PIN Name	X	Y
463	DUMMY	10542	330
464	DUMMY	10528	215
465	DUMMY	10514	330
466	DUMMY	10500	215
467	DUMMY	10486	330
468	DUMMY	10472	215
469	DUMMY	10458	330
470	DUMMY	10444	215
471	DUMMY	10430	330
472	DUMMY	10416	215
473	DUMMY	10402	330
474	DUMMY	10388	215
475	DUMMY	10374	330
476	DUMMY	10360	215
477	DUMMY	10346	330
478	DUMMY	10332	215
479	DUMMY	10318	330
480	DUMMY	10304	215
481	DUMMY	10290	330
482	DUMMY	10276	215
483	DUMMY	10262	330
484	DUMMY	10248	215
485	DUMMY	10234	330
486	DUMMY	10220	215
487	DUMMY	10206	330
488	DUMMY	10192	215
489	DUMMY	10178	330
490	DUMMY	10164	215
491	DUMMY	10150	330
492	DUMMY	10136	215
493	DUMMY	10122	330
494	DUMMY	10108	215
495	DUMMY	10094	330

PAD No.	PIN Name	X	Y
496	DUMMY	10080	215
497	DUMMY	10066	330
498	DUMMY	10052	215
499	DUMMY	10038	330
500	DUMMY	10024	215
501	DUMMY	10010	330
502	DUMMY	9996	215
503	DUMMY	9982	330
504	DUMMY	9968	215
505	DUMMY	9954	330
506	DUMMY	9940	215
507	DUMMY	9926	330
508	DUMMY	9912	215
509	DUMMY	9898	330
510	DUMMY	9884	215
511	DUMMY	9870	330
512	DUMMY	9856	215
513	DUMMY	9842	330
514	DUMMY	9828	215
515	DUMMY	9814	330
516	DUMMY	9800	215
517	DUMMY	9786	330
518	DUMMY	9772	215
519	DUMMY	9758	330
520	DUMMY	9744	215
521	DUMMY	9730	330
522	DUMMY	9716	215
523	DUMMY	9702	330
524	DUMMY	9688	215
525	DUMMY	9674	330
526	DUMMY	9660	215
527	DUMMY	9646	330
528	DUMMY	9632	215

PAD No.	PIN Name	X	Y
529	DUMMY	9618	330
530	DUMMY	9604	215
531	DUMMY	9590	330
532	DUMMY	9576	215
533	DUMMY	9562	330
534	DUMMY	9548	215
535	DUMMY	9534	330
536	DUMMY	9520	215
537	DUMMY	9506	330
538	DUMMY	9492	215
539	DUMMY	9478	330
540	DUMMY	9464	215
541	DUMMY	9450	330
542	DUMMY	9436	215
543	DUMMY	9422	330
544	DUMMY	9408	215
545	DUMMY	9394	330
546	DUMMY	9380	215
547	DUMMY	9366	330
548	DUMMY	9352	215
549	DUMMY	9338	330
550	DUMMY	9324	215
551	SGND	9254	330
552	SGND	9240	215
553	SGND	9226	330
554	SGND	9212	215
555	SGND	9198	330
556	SGND	9184	215
557	SGND	9170	330
558	SGND	9156	215
559	SGND	9142	330
560	SGND	9128	215
561	SGND	9114	330

PAD No.	PIN Name	X	Y
562	SGND	9100	215
563	SGND	9086	330
564	SGND	9072	215
565	SGND	9058	330
566	SGND	9044	215
567	S1	8974	330
568	S2	8960	215
569	S3	8946	330
570	S4	8932	215
571	S5	8918	330
572	S6	8904	215
573	S7	8890	330
574	S8	8876	215
575	S9	8862	330
576	S10	8848	215
577	S11	8834	330
578	S12	8820	215
579	S13	8806	330
580	S14	8792	215
581	S15	8778	330
582	S16	8764	215
583	S17	8750	330
584	S18	8736	215
585	S19	8722	330
586	S20	8708	215
587	S21	8694	330
588	S22	8680	215
589	S23	8666	330
590	S24	8652	215
591	S25	8638	330
592	S26	8624	215
593	S27	8610	330
594	S28	8596	215

PAD No.	PIN Name	X	Y
595	S29	8582	330
596	S30	8568	215
597	S31	8554	330
598	S32	8540	215
599	S33	8526	330
600	S34	8512	215
601	S35	8498	330
602	S36	8484	215
603	S37	8470	330
604	S38	8456	215
605	S39	8442	330
606	S40	8428	215
607	S41	8414	330
608	S42	8400	215
609	S43	8386	330
610	S44	8372	215
611	S45	8358	330
612	S46	8344	215
613	S47	8330	330
614	S48	8316	215
615	S49	8302	330
616	S50	8288	215
617	S51	8274	330
618	S52	8260	215
619	S53	8246	330
620	S54	8232	215
621	S55	8218	330
622	S56	8204	215
623	S57	8190	330
624	S58	8176	215
625	S59	8162	330
626	S60	8148	215
627	S61	8134	330

PAD No.	PIN Name	X	Y
628	S62	8120	215
629	S63	8106	330
630	S64	8092	215
631	S65	8078	330
632	S66	8064	215
633	S67	8050	330
634	S68	8036	215
635	S69	8022	330
636	S70	8008	215
637	S71	7994	330
638	S72	7980	215
639	S73	7966	330
640	S74	7952	215
641	S75	7938	330
642	S76	7924	215
643	S77	7910	330
644	S78	7896	215
645	S79	7882	330
646	S80	7868	215
647	S81	7854	330
648	S82	7840	215
649	S83	7826	330
650	S84	7812	215
651	S85	7798	330
652	S86	7784	215
653	S87	7770	330
654	S88	7756	215
655	S89	7742	330
656	S90	7728	215
657	S91	7714	330
658	S92	7700	215
659	S93	7686	330
660	S94	7672	215

PAD No.	PIN Name	X	Y
661	S95	7658	330
662	S96	7644	215
663	S97	7630	330
664	S98	7616	215
665	S99	7602	330
666	S100	7588	215
667	S101	7574	330
668	S102	7560	215
669	S103	7546	330
670	S104	7532	215
671	S105	7518	330
672	S106	7504	215
673	S107	7490	330
674	S108	7476	215
675	S109	7462	330
676	S110	7448	215
677	S111	7434	330
678	S112	7420	215
679	S113	7406	330
680	S114	7392	215
681	S115	7378	330
682	S116	7364	215
683	S117	7350	330
684	S118	7336	215
685	S119	7322	330
686	S120	7308	215
687	S121	7294	330
688	S122	7280	215
689	S123	7266	330
690	S124	7252	215
691	S125	7238	330
692	S126	7224	215
693	S127	7210	330
694	S128	7196	215
695	S129	7182	330
696	S130	7168	215
697	S131	7154	330
698	S132	7140	215
699	S133	7126	330
700	S134	7112	215
701	S135	7098	330
702	S136	7084	215
703	S137	7070	330
704	S138	7056	215
705	S139	7042	330
706	S140	7028	215
707	S141	7014	330
708	S142	7000	215
709	S143	6986	330
710	S144	6972	215
711	S145	6958	330
712	S146	6944	215
713	S147	6930	330
714	S148	6916	215
715	S149	6902	330
716	S150	6888	215
717	S151	6874	330
718	S152	6860	215
719	S153	6846	330
720	S154	6832	215
721	S155	6818	330
722	S156	6804	215
723	S157	6790	330
724	S158	6776	215
725	S159	6762	330
726	S160	6748	215

PAD No.	PIN Name	X	Y
727	S161	6734	330
728	S162	6720	215
729	S163	6706	330
730	S164	6692	215
731	S165	6678	330
732	S166	6664	215
733	S167	6650	330
734	S168	6636	215
735	S169	6622	330
736	S170	6608	215
737	S171	6594	330
738	S172	6580	215
739	S173	6566	330
740	S174	6552	215
741	S175	6538	330
742	S176	6524	215
743	S177	6510	330
744	S178	6496	215
745	S179	6482	330
746	S180	6468	215
747	S181	6454	330
748	S182	6440	215
749	S183	6426	330
750	S184	6412	215
751	S185	6398	330
752	S186	6384	215
753	S187	6370	330
754	S188	6356	215
755	S189	6342	330
756	S190	6328	215
757	S191	6314	330
758	S192	6300	215
759	S193	6286	330

PAD No.	PIN Name	X	Y
760	S194	6272	215
761	S195	6258	330
762	S196	6244	215
763	S197	6230	330
764	S198	6216	215
765	S199	6202	330
766	S200	6188	215
767	S201	6174	330
768	S202	6160	215
769	S203	6146	330
770	S204	6132	215
771	S205	6118	330
772	S206	6104	215
773	S207	6090	330
774	S208	6076	215
775	S209	6062	330
776	S210	6048	215
777	S211	6034	330
778	S212	6020	215
779	S213	6006	330
780	S214	5992	215
781	S215	5978	330
782	S216	5964	215
783	S217	5950	330
784	S218	5936	215
785	S219	5922	330
786	S220	5908	215
787	S221	5894	330
788	S222	5880	215
789	S223	5866	330
790	S224	5852	215
791	S225	5838	330
792	S226	5824	215

PAD No.	PIN Name	X	Y
793	S227	5810	330
794	S228	5796	215
795	S229	5782	330
796	S230	5768	215
797	S231	5754	330
798	S232	5740	215
799	S233	5726	330
800	S234	5712	215
801	S235	5698	330
802	S236	5684	215
803	S237	5670	330
804	S238	5656	215
805	S239	5642	330
806	S240	5628	215
807	S241	5614	330
808	S242	5600	215
809	S243	5586	330
810	S244	5572	215
811	S245	5558	330
812	S246	5544	215
813	S247	5530	330
814	S248	5516	215
815	S249	5502	330
816	S250	5488	215
817	S251	5474	330
818	S252	5460	215
819	S253	5446	330
820	S254	5432	215
821	S255	5418	330
822	S256	5404	215
823	S257	5390	330
824	S258	5376	215
825	S259	5362	330

PAD No.	PIN Name	X	Y
826	S260	5348	215
827	S261	5334	330
828	S262	5320	215
829	S263	5306	330
830	S264	5292	215
831	S265	5278	330
832	S266	5264	215
833	S267	5250	330
834	S268	5236	215
835	S269	5222	330
836	S270	5208	215
837	S271	5194	330
838	S272	5180	215
839	S273	5166	330
840	S274	5152	215
841	S275	5138	330
842	S276	5124	215
843	S277	5110	330
844	S278	5096	215
845	S279	5082	330
846	S280	5068	215
847	S281	5054	330
848	S282	5040	215
849	S283	5026	330
850	S284	5012	215
851	S285	4998	330
852	S286	4984	215
853	S287	4970	330
854	S288	4956	215
855	S289	4942	330
856	S290	4928	215
857	S291	4914	330
858	S292	4900	215

PAD No.	PIN Name	X	Y
859	S293	4886	330
860	S294	4872	215
861	S295	4858	330
862	S296	4844	215
863	S297	4830	330
864	S298	4816	215
865	S299	4802	330
866	S300	4788	215
867	SGND	4718	330
868	SGND	4704	215
869	SGND	4690	330
870	SGND	4676	215
871	SGND	4662	330
872	SGND	4648	215
873	SGND	4634	330
874	SGND	4620	215
875	SGND	4606	330
876	SGND	4592	215
877	SGND	4578	330
878	SGND	4564	215
879	SGND	4550	330
880	SGND	4536	215
881	SGND	4522	330
882	SGND	4508	215
883	S301	4438	330
884	S302	4424	215
885	S303	4410	330
886	S304	4396	215
887	S305	4382	330
888	S306	4368	215
889	S307	4354	330
890	S308	4340	215
891	S309	4326	330

PAD No.	PIN Name	X	Y
892	S310	4312	215
893	S311	4298	330
894	S312	4284	215
895	S313	4270	330
896	S314	4256	215
897	S315	4242	330
898	S316	4228	215
899	S317	4214	330
900	S318	4200	215
901	S319	4186	330
902	S320	4172	215
903	S321	4158	330
904	S322	4144	215
905	S323	4130	330
906	S324	4116	215
907	S325	4102	330
908	S326	4088	215
909	S327	4074	330
910	S328	4060	215
911	S329	4046	330
912	S330	4032	215
913	S331	4018	330
914	S332	4004	215
915	S333	3990	330
916	S334	3976	215
917	S335	3962	330
918	S336	3948	215
919	S337	3934	330
920	S338	3920	215
921	S339	3906	330
922	S340	3892	215
923	S341	3878	330
924	S342	3864	215

PAD No.	PIN Name	X	Y
925	S343	3850	330
926	S344	3836	215
927	S345	3822	330
928	S346	3808	215
929	S347	3794	330
930	S348	3780	215
931	S349	3766	330
932	S350	3752	215
933	S351	3738	330
934	S352	3724	215
935	S353	3710	330
936	S354	3696	215
937	S355	3682	330
938	S356	3668	215
939	S357	3654	330
940	S358	3640	215
941	S359	3626	330
942	S360	3612	215
943	S361	3598	330
944	S362	3584	215
945	S363	3570	330
946	S364	3556	215
947	S365	3542	330
948	S366	3528	215
949	S367	3514	330
950	S368	3500	215
951	S369	3486	330
952	S370	3472	215
953	S371	3458	330
954	S372	3444	215
955	S373	3430	330
956	S374	3416	215
957	S375	3402	330

PAD No.	PIN Name	X	Y
958	S376	3388	215
959	S377	3374	330
960	S378	3360	215
961	S379	3346	330
962	S380	3332	215
963	S381	3318	330
964	S382	3304	215
965	S383	3290	330
966	S384	3276	215
967	S385	3262	330
968	S386	3248	215
969	S387	3234	330
970	S388	3220	215
971	S389	3206	330
972	S390	3192	215
973	S391	3178	330
974	S392	3164	215
975	S393	3150	330
976	S394	3136	215
977	S395	3122	330
978	S396	3108	215
979	S397	3094	330
980	S398	3080	215
981	S399	3066	330
982	S400	3052	215
983	S401	3038	330
984	S402	3024	215
985	S403	3010	330
986	S404	2996	215
987	S405	2982	330
988	S406	2968	215
989	S407	2954	330
990	S408	2940	215

PAD No.	PIN Name	X	Y
991	S409	2926	330
992	S410	2912	215
993	S411	2898	330
994	S412	2884	215
995	S413	2870	330
996	S414	2856	215
997	S415	2842	330
998	S416	2828	215
999	S417	2814	330
1000	S418	2800	215
1001	S419	2786	330
1002	S420	2772	215
1003	S421	2758	330
1004	S422	2744	215
1005	S423	2730	330
1006	S424	2716	215
1007	S425	2702	330
1008	S426	2688	215
1009	S427	2674	330
1010	S428	2660	215
1011	S429	2646	330
1012	S430	2632	215
1013	S431	2618	330
1014	S432	2604	215
1015	S433	2590	330
1016	S434	2576	215
1017	S435	2562	330
1018	S436	2548	215
1019	S437	2534	330
1020	S438	2520	215
1021	S439	2506	330
1022	S440	2492	215
1023	S441	2478	330

PAD No.	PIN Name	X	Y
1024	S442	2464	215
1025	S443	2450	330
1026	S444	2436	215
1027	S445	2422	330
1028	S446	2408	215
1029	S447	2394	330
1030	S448	2380	215
1031	S449	2366	330
1032	S450	2352	215
1033	S451	2338	330
1034	S452	2324	215
1035	S453	2310	330
1036	S454	2296	215
1037	S455	2282	330
1038	S456	2268	215
1039	S457	2254	330
1040	S458	2240	215
1041	S459	2226	330
1042	S460	2212	215
1043	S461	2198	330
1044	S462	2184	215
1045	S463	2170	330
1046	S464	2156	215
1047	S465	2142	330
1048	S466	2128	215
1049	S467	2114	330
1050	S468	2100	215
1051	S469	2086	330
1052	S470	2072	215
1053	S471	2058	330
1054	S472	2044	215
1055	S473	2030	330
1056	S474	2016	215

PAD No.	PIN Name	X	Y
1057	S475	2002	330
1058	S476	1988	215
1059	S477	1974	330
1060	S478	1960	215
1061	S479	1946	330
1062	S480	1932	215
1063	S481	1918	330
1064	S482	1904	215
1065	S483	1890	330
1066	S484	1876	215
1067	S485	1862	330
1068	S486	1848	215
1069	S487	1834	330
1070	S488	1820	215
1071	S489	1806	330
1072	S490	1792	215
1073	S491	1778	330
1074	S492	1764	215
1075	S493	1750	330
1076	S494	1736	215
1077	S495	1722	330
1078	S496	1708	215
1079	S497	1694	330
1080	S498	1680	215
1081	S499	1666	330
1082	S500	1652	215
1083	S501	1638	330
1084	S502	1624	215
1085	S503	1610	330
1086	S504	1596	215
1087	S505	1582	330
1088	S506	1568	215
1089	S507	1554	330

PAD No.	PIN Name	X	Y
1090	S508	1540	215
1091	S509	1526	330
1092	S510	1512	215
1093	S511	1498	330
1094	S512	1484	215
1095	S513	1470	330
1096	S514	1456	215
1097	S515	1442	330
1098	S516	1428	215
1099	S517	1414	330
1100	S518	1400	215
1101	S519	1386	330
1102	S520	1372	215
1103	S521	1358	330
1104	S522	1344	215
1105	S523	1330	330
1106	S524	1316	215
1107	S525	1302	330
1108	S526	1288	215
1109	S527	1274	330
1110	S528	1260	215
1111	S529	1246	330
1112	S530	1232	215
1113	S531	1218	330
1114	S532	1204	215
1115	S533	1190	330
1116	S534	1176	215
1117	S535	1162	330
1118	S536	1148	215
1119	S537	1134	330
1120	S538	1120	215
1121	S539	1106	330
1122	S540	1092	215

PAD No.	PIN Name	X	Y
1123	S541	1078	330
1124	S542	1064	215
1125	S543	1050	330
1126	S544	1036	215
1127	S545	1022	330
1128	S546	1008	215
1129	S547	994	330
1130	S548	980	215
1131	S549	966	330
1132	S550	952	215
1133	S551	938	330
1134	S552	924	215
1135	S553	910	330
1136	S554	896	215
1137	S555	882	330
1138	S556	868	215
1139	S557	854	330
1140	S558	840	215
1141	S559	826	330
1142	S560	812	215
1143	S561	798	330
1144	S562	784	215
1145	S563	770	330
1146	S564	756	215
1147	S565	742	330
1148	S566	728	215
1149	S567	714	330
1150	S568	700	215
1151	S569	686	330
1152	S570	672	215
1153	S571	658	330
1154	S572	644	215
1155	S573	630	330

PAD No.	PIN Name	X	Y
1156	S574	616	215
1157	S575	602	330
1158	S576	588	215
1159	S577	574	330
1160	S578	560	215
1161	S579	546	330
1162	S580	532	215
1163	S581	518	330
1164	S582	504	215
1165	S583	490	330
1166	S584	476	215
1167	S585	462	330
1168	S586	448	215
1169	S587	434	330
1170	S588	420	215
1171	S589	406	330
1172	S590	392	215
1173	S591	378	330
1174	S592	364	215
1175	S593	350	330
1176	S594	336	215
1177	S595	322	330
1178	S596	308	215
1179	S597	294	330
1180	S598	280	215
1181	S599	266	330
1182	S600	252	215
1183	SGND	182	330
1184	SGND	168	215
1185	SGND	154	330
1186	SGND	140	215
1187	SGND	126	330
1188	SGND	112	215

PAD No.	PIN Name	X	Y
1189	SGND	98	330
1190	SGND	84	215
1191	SGND	70	330
1192	SGND	56	215
1193	SGND	42	330
1194	SGND	28	215
1195	SGND	-28	215
1196	SGND	-42	330
1197	SGND	-56	215
1198	SGND	-70	330
1199	SGND	-84	215
1200	SGND	-98	330
1201	SGND	-112	215
1202	SGND	-126	330
1203	SGND	-140	215
1204	SGND	-154	330
1205	SGND	-168	215
1206	SGND	-182	330
1207	S601	-252	215
1208	S602	-266	330
1209	S603	-280	215
1210	S604	-294	330
1211	S605	-308	215
1212	S606	-322	330
1213	S607	-336	215
1214	S608	-350	330
1215	S609	-364	215
1216	S610	-378	330
1217	S611	-392	215
1218	S612	-406	330
1219	S613	-420	215
1220	S614	-434	330
1221	S615	-448	215

PAD No.	PIN Name	X	Y
1222	S616	-462	330
1223	S617	-476	215
1224	S618	-490	330
1225	S619	-504	215
1226	S620	-518	330
1227	S621	-532	215
1228	S622	-546	330
1229	S623	-560	215
1230	S624	-574	330
1231	S625	-588	215
1232	S626	-602	330
1233	S627	-616	215
1234	S628	-630	330
1235	S629	-644	215
1236	S630	-658	330
1237	S631	-672	215
1238	S632	-686	330
1239	S633	-700	215
1240	S634	-714	330
1241	S635	-728	215
1242	S636	-742	330
1243	S637	-756	215
1244	S638	-770	330
1245	S639	-784	215
1246	S640	-798	330
1247	S641	-812	215
1248	S642	-826	330
1249	S643	-840	215
1250	S644	-854	330
1251	S645	-868	215
1252	S646	-882	330
1253	S647	-896	215
1254	S648	-910	330

PAD No.	PIN Name	X	Y
1255	S649	-924	215
1256	S650	-938	330
1257	S651	-952	215
1258	S652	-966	330
1259	S653	-980	215
1260	S654	-994	330
1261	S655	-1008	215
1262	S656	-1022	330
1263	S657	-1036	215
1264	S658	-1050	330
1265	S659	-1064	215
1266	S660	-1078	330
1267	S661	-1092	215
1268	S662	-1106	330
1269	S663	-1120	215
1270	S664	-1134	330
1271	S665	-1148	215
1272	S666	-1162	330
1273	S667	-1176	215
1274	S668	-1190	330
1275	S669	-1204	215
1276	S670	-1218	330
1277	S671	-1232	215
1278	S672	-1246	330
1279	S673	-1260	215
1280	S674	-1274	330
1281	S675	-1288	215
1282	S676	-1302	330
1283	S677	-1316	215
1284	S678	-1330	330
1285	S679	-1344	215
1286	S680	-1358	330
1287	S681	-1372	215

PAD No.	PIN Name	X	Y
1288	S682	-1386	330
1289	S683	-1400	215
1290	S684	-1414	330
1291	S685	-1428	215
1292	S686	-1442	330
1293	S687	-1456	215
1294	S688	-1470	330
1295	S689	-1484	215
1296	S690	-1498	330
1297	S691	-1512	215
1298	S692	-1526	330
1299	S693	-1540	215
1300	S694	-1554	330
1301	S695	-1568	215
1302	S696	-1582	330
1303	S697	-1596	215
1304	S698	-1610	330
1305	S699	-1624	215
1306	S700	-1638	330
1307	S701	-1652	215
1308	S702	-1666	330
1309	S703	-1680	215
1310	S704	-1694	330
1311	S705	-1708	215
1312	S706	-1722	330
1313	S707	-1736	215
1314	S708	-1750	330
1315	S709	-1764	215
1316	S710	-1778	330
1317	S711	-1792	215
1318	S712	-1806	330
1319	S713	-1820	215
1320	S714	-1834	330

PAD No.	PIN Name	X	Y
1321	S715	-1848	215
1322	S716	-1862	330
1323	S717	-1876	215
1324	S718	-1890	330
1325	S719	-1904	215
1326	S720	-1918	330
1327	S721	-1932	215
1328	S722	-1946	330
1329	S723	-1960	215
1330	S724	-1974	330
1331	S725	-1988	215
1332	S726	-2002	330
1333	S727	-2016	215
1334	S728	-2030	330
1335	S729	-2044	215
1336	S730	-2058	330
1337	S731	-2072	215
1338	S732	-2086	330
1339	S733	-2100	215
1340	S734	-2114	330
1341	S735	-2128	215
1342	S736	-2142	330
1343	S737	-2156	215
1344	S738	-2170	330
1345	S739	-2184	215
1346	S740	-2198	330
1347	S741	-2212	215
1348	S742	-2226	330
1349	S743	-2240	215
1350	S744	-2254	330
1351	S745	-2268	215
1352	S746	-2282	330
1353	S747	-2296	215

PAD No.	PIN Name	X	Y
1354	S748	-2310	330
1355	S749	-2324	215
1356	S750	-2338	330
1357	S751	-2352	215
1358	S752	-2366	330
1359	S753	-2380	215
1360	S754	-2394	330
1361	S755	-2408	215
1362	S756	-2422	330
1363	S757	-2436	215
1364	S758	-2450	330
1365	S759	-2464	215
1366	S760	-2478	330
1367	S761	-2492	215
1368	S762	-2506	330
1369	S763	-2520	215
1370	S764	-2534	330
1371	S765	-2548	215
1372	S766	-2562	330
1373	S767	-2576	215
1374	S768	-2590	330
1375	S769	-2604	215
1376	S770	-2618	330
1377	S771	-2632	215
1378	S772	-2646	330
1379	S773	-2660	215
1380	S774	-2674	330
1381	S775	-2688	215
1382	S776	-2702	330
1383	S777	-2716	215
1384	S778	-2730	330
1385	S779	-2744	215
1386	S780	-2758	330

PAD No.	PIN Name	X	Y
1387	S781	-2772	215
1388	S782	-2786	330
1389	S783	-2800	215
1390	S784	-2814	330
1391	S785	-2828	215
1392	S786	-2842	330
1393	S787	-2856	215
1394	S788	-2870	330
1395	S789	-2884	215
1396	S790	-2898	330
1397	S791	-2912	215
1398	S792	-2926	330
1399	S793	-2940	215
1400	S794	-2954	330
1401	S795	-2968	215
1402	S796	-2982	330
1403	S797	-2996	215
1404	S798	-3010	330
1405	S799	-3024	215
1406	S800	-3038	330
1407	S801	-3052	215
1408	S802	-3066	330
1409	S803	-3080	215
1410	S804	-3094	330
1411	S805	-3108	215
1412	S806	-3122	330
1413	S807	-3136	215
1414	S808	-3150	330
1415	S809	-3164	215
1416	S810	-3178	330
1417	S811	-3192	215
1418	S812	-3206	330
1419	S813	-3220	215

PAD No.	PIN Name	X	Y
1420	S814	-3234	330
1421	S815	-3248	215
1422	S816	-3262	330
1423	S817	-3276	215
1424	S818	-3290	330
1425	S819	-3304	215
1426	S820	-3318	330
1427	S821	-3332	215
1428	S822	-3346	330
1429	S823	-3360	215
1430	S824	-3374	330
1431	S825	-3388	215
1432	S826	-3402	330
1433	S827	-3416	215
1434	S828	-3430	330
1435	S829	-3444	215
1436	S830	-3458	330
1437	S831	-3472	215
1438	S832	-3486	330
1439	S833	-3500	215
1440	S834	-3514	330
1441	S835	-3528	215
1442	S836	-3542	330
1443	S837	-3556	215
1444	S838	-3570	330
1445	S839	-3584	215
1446	S840	-3598	330
1447	S841	-3612	215
1448	S842	-3626	330
1449	S843	-3640	215
1450	S844	-3654	330
1451	S845	-3668	215
1452	S846	-3682	330

PAD No.	PIN Name	X	Y
1453	S847	-3696	215
1454	S848	-3710	330
1455	S849	-3724	215
1456	S850	-3738	330
1457	S851	-3752	215
1458	S852	-3766	330
1459	S853	-3780	215
1460	S854	-3794	330
1461	S855	-3808	215
1462	S856	-3822	330
1463	S857	-3836	215
1464	S858	-3850	330
1465	S859	-3864	215
1466	S860	-3878	330
1467	S861	-3892	215
1468	S862	-3906	330
1469	S863	-3920	215
1470	S864	-3934	330
1471	S865	-3948	215
1472	S866	-3962	330
1473	S867	-3976	215
1474	S868	-3990	330
1475	S869	-4004	215
1476	S870	-4018	330
1477	S871	-4032	215
1478	S872	-4046	330
1479	S873	-4060	215
1480	S874	-4074	330
1481	S875	-4088	215
1482	S876	-4102	330
1483	S877	-4116	215
1484	S878	-4130	330
1485	S879	-4144	215

PAD No.	PIN Name	X	Y
1486	S880	-4158	330
1487	S881	-4172	215
1488	S882	-4186	330
1489	S883	-4200	215
1490	S884	-4214	330
1491	S885	-4228	215
1492	S886	-4242	330
1493	S887	-4256	215
1494	S888	-4270	330
1495	S889	-4284	215
1496	S890	-4298	330
1497	S891	-4312	215
1498	S892	-4326	330
1499	S893	-4340	215
1500	S894	-4354	330
1501	S895	-4368	215
1502	S896	-4382	330
1503	S897	-4396	215
1504	S898	-4410	330
1505	S899	-4424	215
1506	S900	-4438	330
1507	SGND	-4508	215
1508	SGND	-4522	330
1509	SGND	-4536	215
1510	SGND	-4550	330
1511	SGND	-4564	215
1512	SGND	-4578	330
1513	SGND	-4592	215
1514	SGND	-4606	330
1515	SGND	-4620	215
1516	SGND	-4634	330
1517	SGND	-4648	215
1518	SGND	-4662	330

PAD No.	PIN Name	X	Y
1519	SGND	-4676	215
1520	SGND	-4690	330
1521	SGND	-4704	215
1522	SGND	-4718	330
1523	S901	-4788	215
1524	S902	-4802	330
1525	S903	-4816	215
1526	S904	-4830	330
1527	S905	-4844	215
1528	S906	-4858	330
1529	S907	-4872	215
1530	S908	-4886	330
1531	S909	-4900	215
1532	S910	-4914	330
1533	S911	-4928	215
1534	S912	-4942	330
1535	S913	-4956	215
1536	S914	-4970	330
1537	S915	-4984	215
1538	S916	-4998	330
1539	S917	-5012	215
1540	S918	-5026	330
1541	S919	-5040	215
1542	S920	-5054	330
1543	S921	-5068	215
1544	S922	-5082	330
1545	S923	-5096	215
1546	S924	-5110	330
1547	S925	-5124	215
1548	S926	-5138	330
1549	S927	-5152	215
1550	S928	-5166	330
1551	S929	-5180	215

PAD No.	PIN Name	X	Y
1552	S930	-5194	330
1553	S931	-5208	215
1554	S932	-5222	330
1555	S933	-5236	215
1556	S934	-5250	330
1557	S935	-5264	215
1558	S936	-5278	330
1559	S937	-5292	215
1560	S938	-5306	330
1561	S939	-5320	215
1562	S940	-5334	330
1563	S941	-5348	215
1564	S942	-5362	330
1565	S943	-5376	215
1566	S944	-5390	330
1567	S945	-5404	215
1568	S946	-5418	330
1569	S947	-5432	215
1570	S948	-5446	330
1571	S949	-5460	215
1572	S950	-5474	330
1573	S951	-5488	215
1574	S952	-5502	330
1575	S953	-5516	215
1576	S954	-5530	330
1577	S955	-5544	215
1578	S956	-5558	330
1579	S957	-5572	215
1580	S958	-5586	330
1581	S959	-5600	215
1582	S960	-5614	330
1583	S961	-5628	215
1584	S962	-5642	330

PAD No.	PIN Name	X	Y
1585	S963	-5656	215
1586	S964	-5670	330
1587	S965	-5684	215
1588	S966	-5698	330
1589	S967	-5712	215
1590	S968	-5726	330
1591	S969	-5740	215
1592	S970	-5754	330
1593	S971	-5768	215
1594	S972	-5782	330
1595	S973	-5796	215
1596	S974	-5810	330
1597	S975	-5824	215
1598	S976	-5838	330
1599	S977	-5852	215
1600	S978	-5866	330
1601	S979	-5880	215
1602	S980	-5894	330
1603	S981	-5908	215
1604	S982	-5922	330
1605	S983	-5936	215
1606	S984	-5950	330
1607	S985	-5964	215
1608	S986	-5978	330
1609	S987	-5992	215
1610	S988	-6006	330
1611	S989	-6020	215
1612	S990	-6034	330
1613	S991	-6048	215
1614	S992	-6062	330
1615	S993	-6076	215
1616	S994	-6090	330
1617	S995	-6104	215
1618	S996	-6118	330
1619	S997	-6132	215
1620	S998	-6146	330
1621	S999	-6160	215
1622	S1000	-6174	330
1623	S1001	-6188	215
1624	S1002	-6202	330
1625	S1003	-6216	215
1626	S1004	-6230	330
1627	S1005	-6244	215
1628	S1006	-6258	330
1629	S1007	-6272	215
1630	S1008	-6286	330
1631	S1009	-6300	215
1632	S1010	-6314	330
1633	S1011	-6328	215
1634	S1012	-6342	330
1635	S1013	-6356	215
1636	S1014	-6370	330
1637	S1015	-6384	215
1638	S1016	-6398	330
1639	S1017	-6412	215
1640	S1018	-6426	330
1641	S1019	-6440	215
1642	S1020	-6454	330
1643	S1021	-6468	215
1644	S1022	-6482	330
1645	S1023	-6496	215
1646	S1024	-6510	330
1647	S1025	-6524	215
1648	S1026	-6538	330
1649	S1027	-6552	215
1650	S1028	-6566	330

PAD No.	PIN Name	X	Y
1651	S1029	-6580	215
1652	S1030	-6594	330
1653	S1031	-6608	215
1654	S1032	-6622	330
1655	S1033	-6636	215
1656	S1034	-6650	330
1657	S1035	-6664	215
1658	S1036	-6678	330
1659	S1037	-6692	215
1660	S1038	-6706	330
1661	S1039	-6720	215
1662	S1040	-6734	330
1663	S1041	-6748	215
1664	S1042	-6762	330
1665	S1043	-6776	215
1666	S1044	-6790	330
1667	S1045	-6804	215
1668	S1046	-6818	330
1669	S1047	-6832	215
1670	S1048	-6846	330
1671	S1049	-6860	215
1672	S1050	-6874	330
1673	S1051	-6888	215
1674	S1052	-6902	330
1675	S1053	-6916	215
1676	S1054	-6930	330
1677	S1055	-6944	215
1678	S1056	-6958	330
1679	S1057	-6972	215
1680	S1058	-6986	330
1681	S1059	-7000	215
1682	S1060	-7014	330
1683	S1061	-7028	215

PAD No.	PIN Name	X	Y
1684	S1062	-7042	330
1685	S1063	-7056	215
1686	S1064	-7070	330
1687	S1065	-7084	215
1688	S1066	-7098	330
1689	S1067	-7112	215
1690	S1068	-7126	330
1691	S1069	-7140	215
1692	S1070	-7154	330
1693	S1071	-7168	215
1694	S1072	-7182	330
1695	S1073	-7196	215
1696	S1074	-7210	330
1697	S1075	-7224	215
1698	S1076	-7238	330
1699	S1077	-7252	215
1700	S1078	-7266	330
1701	S1079	-7280	215
1702	S1080	-7294	330
1703	S1081	-7308	215
1704	S1082	-7322	330
1705	S1083	-7336	215
1706	S1084	-7350	330
1707	S1085	-7364	215
1708	S1086	-7378	330
1709	S1087	-7392	215
1710	S1088	-7406	330
1711	S1089	-7420	215
1712	S1090	-7434	330
1713	S1091	-7448	215
1714	S1092	-7462	330
1715	S1093	-7476	215
1716	S1094	-7490	330

PAD No.	PIN Name	X	Y
1717	S1095	-7504	215
1718	S1096	-7518	330
1719	S1097	-7532	215
1720	S1098	-7546	330
1721	S1099	-7560	215
1722	S1100	-7574	330
1723	S1101	-7588	215
1724	S1102	-7602	330
1725	S1103	-7616	215
1726	S1104	-7630	330
1727	S1105	-7644	215
1728	S1106	-7658	330
1729	S1107	-7672	215
1730	S1108	-7686	330
1731	S1109	-7700	215
1732	S1110	-7714	330
1733	S1111	-7728	215
1734	S1112	-7742	330
1735	S1113	-7756	215
1736	S1114	-7770	330
1737	S1115	-7784	215
1738	S1116	-7798	330
1739	S1117	-7812	215
1740	S1118	-7826	330
1741	S1119	-7840	215
1742	S1120	-7854	330
1743	S1121	-7868	215
1744	S1122	-7882	330
1745	S1123	-7896	215
1746	S1124	-7910	330
1747	S1125	-7924	215
1748	S1126	-7938	330
1749	S1127	-7952	215

PAD No.	PIN Name	X	Y
1750	S1128	-7966	330
1751	S1129	-7980	215
1752	S1130	-7994	330
1753	S1131	-8008	215
1754	S1132	-8022	330
1755	S1133	-8036	215
1756	S1134	-8050	330
1757	S1135	-8064	215
1758	S1136	-8078	330
1759	S1137	-8092	215
1760	S1138	-8106	330
1761	S1139	-8120	215
1762	S1140	-8134	330
1763	S1141	-8148	215
1764	S1142	-8162	330
1765	S1143	-8176	215
1766	S1144	-8190	330
1767	S1145	-8204	215
1768	S1146	-8218	330
1769	S1147	-8232	215
1770	S1148	-8246	330
1771	S1149	-8260	215
1772	S1150	-8274	330
1773	S1151	-8288	215
1774	S1152	-8302	330
1775	S1153	-8316	215
1776	S1154	-8330	330
1777	S1155	-8344	215
1778	S1156	-8358	330
1779	S1157	-8372	215
1780	S1158	-8386	330
1781	S1159	-8400	215
1782	S1160	-8414	330

PAD No.	PIN Name	X	Y
1783	S1161	-8428	215
1784	S1162	-8442	330
1785	S1163	-8456	215
1786	S1164	-8470	330
1787	S1165	-8484	215
1788	S1166	-8498	330
1789	S1167	-8512	215
1790	S1168	-8526	330
1791	S1169	-8540	215
1792	S1170	-8554	330
1793	S1171	-8568	215
1794	S1172	-8582	330
1795	S1173	-8596	215
1796	S1174	-8610	330
1797	S1175	-8624	215
1798	S1176	-8638	330
1799	S1177	-8652	215
1800	S1178	-8666	330
1801	S1179	-8680	215
1802	S1180	-8694	330
1803	S1181	-8708	215
1804	S1182	-8722	330
1805	S1183	-8736	215
1806	S1184	-8750	330
1807	S1185	-8764	215
1808	S1186	-8778	330
1809	S1187	-8792	215
1810	S1188	-8806	330
1811	S1189	-8820	215
1812	S1190	-8834	330
1813	S1191	-8848	215
1814	S1192	-8862	330
1815	S1193	-8876	215

PAD No.	PIN Name	X	Y
1816	S1194	-8890	330
1817	S1195	-8904	215
1818	S1196	-8918	330
1819	S1197	-8932	215
1820	S1198	-8946	330
1821	S1199	-8960	215
1822	S1200	-8974	330
1823	SGND	-9044	215
1824	SGND	-9058	330
1825	SGND	-9072	215
1826	SGND	-9086	330
1827	SGND	-9100	215
1828	SGND	-9114	330
1829	SGND	-9128	215
1830	SGND	-9142	330
1831	SGND	-9156	215
1832	SGND	-9170	330
1833	SGND	-9184	215
1834	SGND	-9198	330
1835	SGND	-9212	215
1836	SGND	-9226	330
1837	SGND	-9240	215
1838	SGND	-9254	330
1839	DUMMY	-9324	215
1840	DUMMY	-9338	330
1841	DUMMY	-9352	215
1842	DUMMY	-9366	330
1843	DUMMY	-9380	215
1844	DUMMY	-9394	330
1845	DUMMY	-9408	215
1846	DUMMY	-9422	330
1847	DUMMY	-9436	215
1848	DUMMY	-9450	330

PAD No.	PIN Name	X	Y
1849	DUMMY	-9464	215
1850	DUMMY	-9478	330
1851	DUMMY	-9492	215
1852	DUMMY	-9506	330
1853	DUMMY	-9520	215
1854	DUMMY	-9534	330
1855	DUMMY	-9548	215
1856	DUMMY	-9562	330
1857	DUMMY	-9576	215
1858	DUMMY	-9590	330
1859	DUMMY	-9604	215
1860	DUMMY	-9618	330
1861	DUMMY	-9632	215
1862	DUMMY	-9646	330
1863	DUMMY	-9660	215
1864	DUMMY	-9674	330
1865	DUMMY	-9688	215
1866	DUMMY	-9702	330
1867	DUMMY	-9716	215
1868	DUMMY	-9730	330
1869	DUMMY	-9744	215
1870	DUMMY	-9758	330
1871	DUMMY	-9772	215
1872	DUMMY	-9786	330
1873	DUMMY	-9800	215
1874	DUMMY	-9814	330
1875	DUMMY	-9828	215
1876	DUMMY	-9842	330
1877	DUMMY	-9856	215
1878	DUMMY	-9870	330
1879	DUMMY	-9884	215
1880	DUMMY	-9898	330
1881	DUMMY	-9912	215

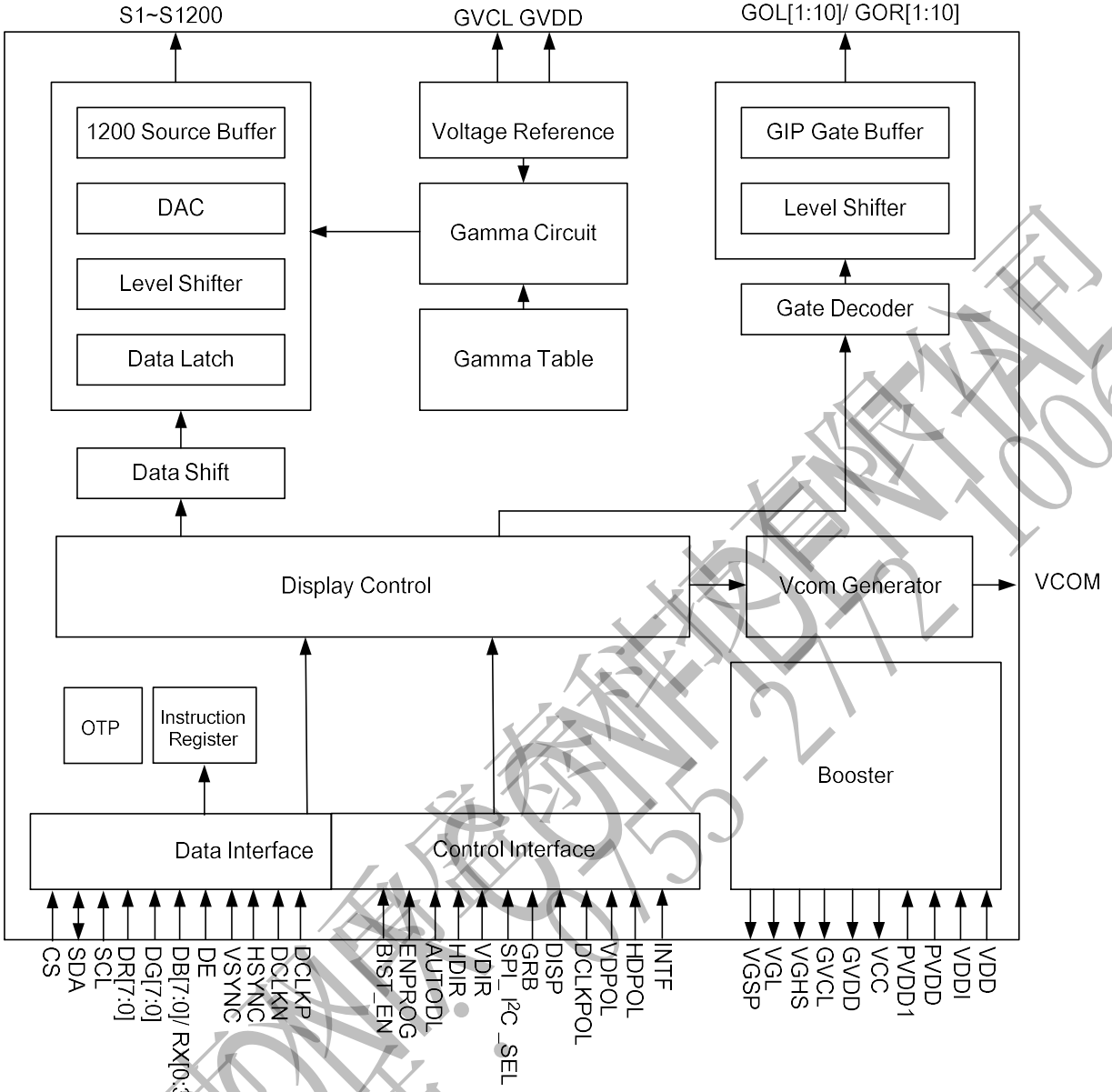
PAD No.	PIN Name	X	Y
1882	DUMMY	-9926	330
1883	DUMMY	-9940	215
1884	DUMMY	-9954	330
1885	DUMMY	-9968	215
1886	DUMMY	-9982	330
1887	DUMMY	-9996	215
1888	DUMMY	-10010	330
1889	DUMMY	-10024	215
1890	DUMMY	-10038	330
1891	DUMMY	-10052	215
1892	DUMMY	-10066	330
1893	DUMMY	-10080	215
1894	DUMMY	-10094	330
1895	DUMMY	-10108	215
1896	DUMMY	-10122	330
1897	DUMMY	-10136	215
1898	DUMMY	-10150	330
1899	DUMMY	-10164	215
1900	DUMMY	-10178	330
1901	DUMMY	-10192	215
1902	DUMMY	-10206	330
1903	DUMMY	-10220	215
1904	DUMMY	-10234	330
1905	DUMMY	-10248	215
1906	DUMMY	-10262	330
1907	DUMMY	-10276	215
1908	DUMMY	-10290	330
1909	DUMMY	-10304	215
1910	DUMMY	-10318	330
1911	DUMMY	-10332	215
1912	DUMMY	-10346	330
1913	DUMMY	-10360	215
1914	DUMMY	-10374	330

PAD No.	PIN Name	X	Y
1915	DUMMY	-10388	215
1916	DUMMY	-10402	330
1917	DUMMY	-10416	215
1918	DUMMY	-10430	330
1919	DUMMY	-10444	215
1920	DUMMY	-10458	330
1921	DUMMY	-10472	215
1922	DUMMY	-10486	330
1923	DUMMY	-10500	215
1924	DUMMY	-10514	330
1925	DUMMY	-10528	215
1926	DUMMY	-10542	330
1927	DUMMY	-10556	215
1928	DUMMY	-10570	330
1929	DUMMY	-10584	215
1930	DUMMY	-10598	330
1931	DUMMY	-10612	215
1932	DUMMY	-10626	330
1933	DUMMY	-10640	215
1934	DUMMY	-10654	330
1935	DUMMY	-10668	215
1936	DUMMY	-10682	330
1937	VGL	-10752	215
1938	VGL	-10766	330
1939	VGL	-10780	215
1940	VGL	-10794	330
1941	VGL	-10808	215
1942	VGL	-10822	330
1943	VGHS	-10836	215
1944	VGHS	-10850	330
1945	VGHS	-10864	215
1946	VGHS	-10878	330
1947	VGHS	-10892	215

PAD No.	PIN Name	X	Y
1948	VGHS	-10906	330
1949	GOL[10]	-10976	215
1950	GOL[10]	-10990	330
1951	GOL[10]	-11004	215
1952	GOL[9]	-11018	330
1953	GOL[9]	-11032	215
1954	GOL[9]	-11046	330
1955	GOL[8]	-11060	215
1956	GOL[8]	-11074	330
1957	GOL[8]	-11088	215
1958	GOL[7]	-11102	330
1959	GOL[7]	-11116	215
1960	GOL[7]	-11130	330
1961	GOL[6]	-11144	215
1962	GOL[6]	-11158	330
1963	GOL[6]	-11172	215
1964	GOL[5]	-11186	330
1965	GOL[5]	-11200	215
1966	GOL[5]	-11214	330
1967	GOL[4]	-11228	215
1968	GOL[4]	-11242	330
1969	GOL[4]	-11256	215
1970	GOL[3]	-11270	330
1971	GOL[3]	-11284	215
1972	GOL[3]	-11298	330
1973	GOL[2]	-11312	215
1974	GOL[2]	-11326	330
1975	GOL[2]	-11340	215
1976	GOL[1]	-11354	330
1977	GOL[1]	-11368	215
1978	GOL[1]	-11382	330
1979	VGL	-11452	215
1980	VGL	-11466	330

PAD No.	PIN Name	X	Y
1981	VGL	-11480	215
1982	VGL	-11494	330
1983	VGL	-11508	215
1984	VGL	-11522	330
1985	VGHS	-11536	215
1986	VGHS	-11550	330
1987	VGHS	-11564	215
1988	VGHS	-11578	330
1989	VGHS	-11592	215
1990	VGHS	-11606	330
1991	L_MARK	-11812	-337
1992	R_MARK	11812	-337

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 Pin Function

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="3">3-Wire SPI / I^{2}C Interface Pins</td></tr>
<tr><td>SPI_ I^{2}C _SEL</td><td>I</td><td>3-wire SPI and I^{2}C interface control.
<table>
<tr><th>SPI_ I^{2}C _SEL</th><th>Function Description</th></tr>
<tr><td>L</td><td>I^{2}C interface</td></tr>
<tr><td>H</td><td>3-wire SPI interface (Default)</td></tr>
</table></td></tr>
<tr><td>CS</td><td>I</td><td>Serial communication chip selection.
CS is not used in I^{2}C interface and should be connected to “H”.</td></tr>
<tr><td>SDA</td><td>I/O</td><td>Serial communication data input and output.</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial communication clock input.</td></tr>
<tr><td colspan="3">Control Pins</td></tr>
<tr><td>GRB</td><td>I</td><td>Global reset pin. When GRB is “L”, internal initialization procedure is executed.</td></tr>
<tr><td>DISP</td><td>I</td><td>DISP sets the display mode.
<table>
<tr><th>DISP</th><th>Function Description</th></tr>
<tr><td>L</td><td>Standby mode (Default)</td></tr>
<tr><td>H</td><td>Normal display mode</td></tr>
</table></td></tr>
<tr><td>HDIR</td><td>I</td><td>Horizontal scan direction control pin. This pin must be connected to “H” or “L” according to system application.
<table>
<tr><th>HDIR</th><th>Function Description</th></tr>
<tr><td>L</td><td>From right to left</td></tr>
<tr><td>H</td><td>From left to right(Default)</td></tr>
</table></td></tr>
<tr><td>VDIR</td><td>I</td><td>Vertical scan direction control pin. This pin must be connected to “H” or “L” according to system application.
<table>
<tr><th>VDIR</th><th>Function Description</th></tr>
<tr><td>L</td><td>From down to up.</td></tr>
<tr><td>H</td><td>From up to down. (Default)</td></tr>
</table></td></tr>
<tr><td>AUTODL</td><td>I</td><td>OTP trim function control pin. When normal display, AUTODL should be set to “H” and the value in the OTP will be downloaded automatically.
<table>
<tr><th>AUTODL</th><th>Function Description</th></tr>
<tr><td>L</td><td>Disable auto-refresh function</td></tr>
<tr><td>H</td><td>Enable auto-refresh function(Default)</td></tr>
</table></td></tr>
<tr><td>ENPROG</td><td>I</td><td>OTP program control pin. Please keep it in “L” when OTP is not programming.
<table>
<tr><th>ENPROG</th><th>Function Description</th></tr>
<tr><td>L</td><td>Disable OTP program function(Default)</td></tr>
<tr><td>H</td><td>Enable OTP program function</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BIST_EN</td><td>I</td><td>BIST function control pin.
<table>
<tr><th>BIST_EN</th><th>Function Description</th></tr>
<tr><td>L</td><td>Disable BIST function(Default)</td></tr>
<tr><td>H</td><td>Enable BIST function</td></tr>
</table></td></tr>
<tr><td>INTF</td><td>I</td><td>Set RGB interface or LVDS interface.
<table>
<tr><th>INTF</th><th>Function Description</th></tr>
<tr><td>L</td><td>RGB interface mode(Default)</td></tr>
<tr><td>H</td><td>LVDS interface mode</td></tr>
</table></td></tr>
<tr><td colspan="3">Interface Control Pins</td></tr>
<tr><td>VDPOL</td><td>I</td><td>VDPOL sets VSYNC polarity in RGB interface and sets LVDS 3- / 4- lane in LVDS interface.
<table>
<tr><th>MCU Type</th><th>VDPOL</th><th>Function Description</th></tr>
<tr><td rowspan="2">RGB interface</td><td>L</td><td>VSYNC polarity: positive</td></tr>
<tr><td>H</td><td>VSYNC polarity: negative(Default)</td></tr>
<tr><td rowspan="2">LVDS interface</td><td>L</td><td>LVDS 3 lane</td></tr>
<tr><td>H</td><td>LVDS 4 lane(Default)</td></tr>
</table></td></tr>
<tr><td>HDPOL</td><td>I</td><td>HDPOL sets HSYNC polarity in RGB interface.
<table>
<tr><th>HDPOL</th><th>Function Description</th></tr>
<tr><td>L</td><td>HSYNC polarity: positive</td></tr>
<tr><td>H</td><td>HSYNC polarity: negative(Default)</td></tr>
</table>
HDPOL is not used in LVDS interface and should be connected to “H”.</td></tr>
<tr><td>DCLKPOL</td><td>I</td><td>DCLKPOL sets DCLK polarity in RGB interface.
<table>
<tr><th>DCLKPOL</th><th>Function Description</th></tr>
<tr><td>L</td><td>DCLK polarity: positive</td></tr>
<tr><td>H</td><td>DCLK polarity: negative(Default)</td></tr>
</table>
DCLKPOL is not used in LVDS interface and should be connected to “H”.</td></tr>
<tr><td>LVDS_FMT</td><td>I</td><td>LVDS_FMT sets LVDS data format.
<table>
<tr><th>LVDS_FMT</th><th>Function Description</th></tr>
<tr><td>L</td><td>VESA Mode</td></tr>
<tr><td>H</td><td>JEIDA Mode(Default)</td></tr>
</table>
LVDS_FMT is not used in RGB interface and should be connected to “L”.</td></tr>
<tr><td>SWAP</td><td>I</td><td>SWAP is a reserved test pin. Please set it according to the following table.
<table>
<tr><th>MCU Type</th><th>Function Description</th></tr>
<tr><td>RGB interface</td><td>SWAP pin must be connected to “L”.</td></tr>
<tr><td>LVDS interface</td><td>SWAP pin must be connected to “H”</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="3">Input Interface Pins</td></tr>
<tr><td>DR[7:0]
DG[7:0]
DB[7:0]</td><td>I</td><td>RGB interface and LVDS interface data input pins.
LVDS pin define please refer to section 7.4.1 LVDS Input Pin Mapping Table.
<table>
<tr><th>MCU Type</th><th colspan="2">Function Description</th></tr>
<tr><td rowspan="3">RGB interface</td><td>DR[7:0]</td><td>8 bit data bus display for red data.</td></tr>
<tr><td>DG[7:0]</td><td>8 bit data bus display for green data.</td></tr>
<tr><td>DB[7:0]</td><td>8 bit data bus display for blue data.</td></tr>
<tr><td rowspan="6">LVDS interface</td><td>DR[7:0]</td><td>DR[7:0] are not used in LVDS mode and should be connected to “L”.</td></tr>
<tr><td>DG[7:0]</td><td>DG[7:0] are not used in LVDS mode and should be connected to “L”.</td></tr>
<tr><td>DB[1:0]</td><td>LVDS input lane: RX0N/ RX0P</td></tr>
<tr><td>DB[3:2]</td><td>LVDS input lane: RX1N/ RX1P</td></tr>
<tr><td>DB[5:4]</td><td>LVDS input lane: RX2N/ RX2P</td></tr>
<tr><td>DB[7:6]</td><td>LVDS input lane: RX3N/ RX3P</td></tr>
</table></td></tr>
<tr><td>DCLKP</td><td>I</td><td>Pixel clock/ LVDS DCLKP control pin, this pin function is selected by INTF.
<table>
<tr><th>MCU Type</th><th>Function Description</th></tr>
<tr><td>RGB interface</td><td>RGB interface: pixel clock input pin</td></tr>
<tr><td>LVDS interface</td><td>LVDS interface: DCLKP, detail pin define please refer to section 7.4.1LVDS Input Pin Mapping Table.</td></tr>
</table></td></tr>
<tr><td>DCLKN</td><td>I</td><td>LVDS DCLKN control pin, this pin function is selected by INTF.
<table>
<tr><th>MCU Type</th><th>Function Description</th></tr>
<tr><td>RGB interface</td><td>RGB interface: DCLKN is not used in RGB interface and should be connected to “L”.</td></tr>
<tr><td>LVDS interface</td><td>LVDS interface: DCLKN, detail pin define please refer to section 7.4.1LVDS Input Pin Mapping Table.</td></tr>
</table></td></tr>
<tr><td>HSYNC</td><td>I</td><td>Horizontal sync signal applied to the RGB interface.
HSYNC is not used in LVDS interface and should be connected to “L”.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>Vertical sync signal applied to the RGB interface.
VSYNC is not used in LVDS interface and should be connected to “L”.</td></tr>
<tr><td>DE</td><td>I</td><td>Data input enable applied to the RGB interface.
DE is not used in LVDS interface and should be connected to “L”.</td></tr>
<tr><td colspan="3">Source / Gate Driver Pins</td></tr>
<tr><td>S[1200:1]</td><td>O</td><td>Source driver output signals.</td></tr>
<tr><td>GOR[10:1]
GOL[10:1]</td><td>O</td><td>GIP control signals</td></tr>
</table>

Name	Type	Description
VCOM Generator Pin		
VCOM	O	Power supply for the TFT-LCD common electrode.
Power Supply Pins		
VDDI	P	Power supply for digital I/O pins.
VDD	P	Power supply for analog circuit.
PVDD	P	Power supply for charge pump circuit.
DUMMY (PVDD1)	P	Power supply for charge pump circuit (enhance). The power supply is determined by system power, panel loading and display quality.
DGND	P	Ground pin for digital circuit.
AGND	P	Ground pin for analog circuit.
PGND	P	Ground pin for charge pump circuit.
SGND	P	Ground pin for source circuit.
RGND	P	Ground pin for reference circuit.
Power Circuit Pins		
VGHS	C	Positive power supply for gate driver.
VGL	C	Negative power supply for gate driver.
SVDD	C	DC/DC converter for positive source OP-AMP driver.
SVCL	C	DC/DC converter for negative source OP-AMP driver.
GVDD	PO	Positive voltage output of grayscale power.
GVCL	PO	Negative voltage output of grayscale power.
AVDD1	C	DC/DC converter for positive gamma and GVDD reference voltage.
AVCL1	C	DC/DC converter for negative gamma and GVCL reference voltage.
VCC	PO	Monitor pin of internal digital power.
Test Pins		
VGSP	T	Monitor pin for VCOM".
VPP	T	Reserved for OTP test only, please leave it open.
V20	T	Reserved for testing only, please leave it open.
ERR_OUT	T	Reserved for testing only, please leave it open.
TEST_I[14:0]	T	Reserved for testing only, please leave these pins open.
TESTOUT[13:0]	T	Reserved for testing only, please leave these pins open.
DUMMY	D	Dummy pin, please leave these pins open.

Note: 1. I: input, O: output, I/O: input/output, P: power input, PO: power out, D: dummy, T: test pin, C: capacitor pin

2. If hardware pin is not used, please fix to "H" by VDDI or "L" by DGND

6.2 Hardware Pin Configuration Pin Mapping Software Register Setting

The following settings can be selected by hardware pins and software registers.

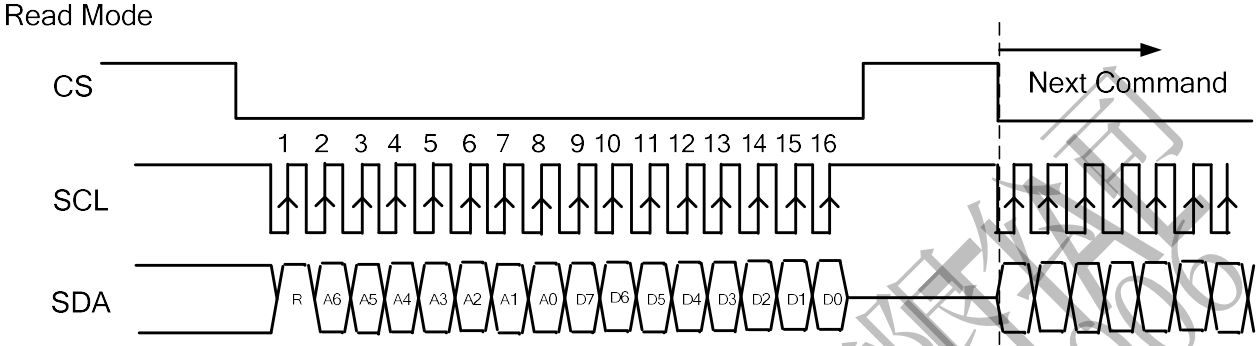
Hardware Setting (use in power on/off sequence)	Software Setting (use in normal operation mode)
GRB	10h[3]
DISP	10h[0]
VDIR	19h[6]
HDIR	19h[5]
AUTODL	1Ch[2]
VDPOL	1Bh[7]
HDPOL	1Bh[6]
DCLKPOL	1Bh[4]

7. COMMUNICATION INTERFACE

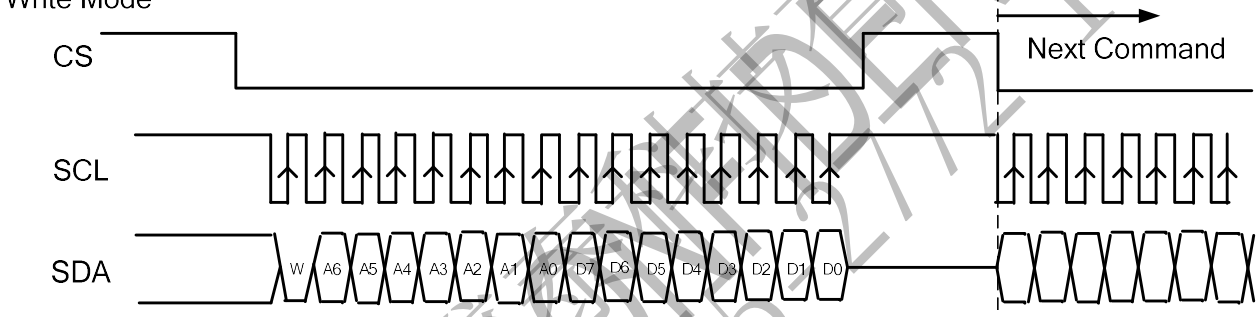
7.1 3-wire Serial Interface

R/W: Read/Write mode control bit.
R/W=1: Read mode
R/W=0: Write mode

Read Mode



Write Mode



a. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.

b. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.

c. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.

d. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.

e. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data before then rising edge of CS pulse are valid data.

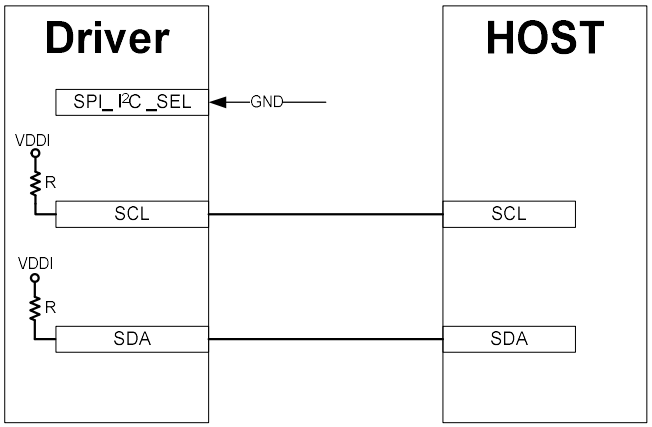
f. Serial block operates with the SCL clock

g. Serial data can be accepted in the power save mode.

h. After power on reset or GRB reset, it is required 100ms delay to begin SPI communication.

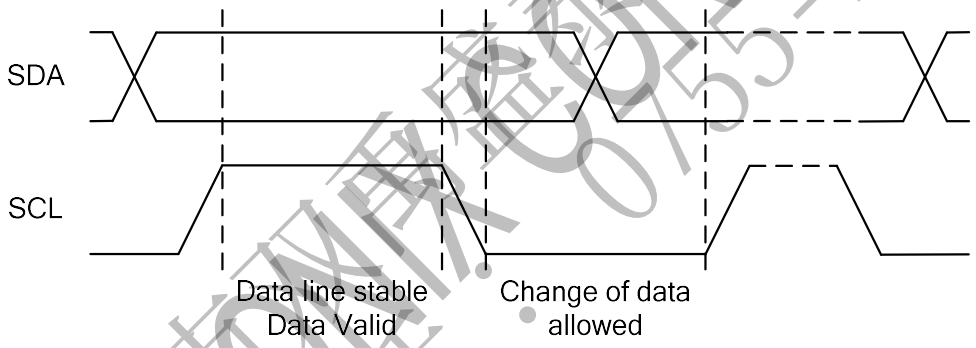
7.2 I²C Interface

The I²C Interface is bi-directional two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines have built-in pull up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.



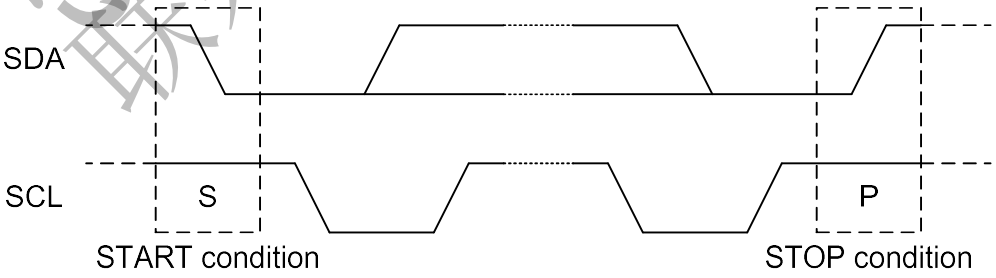
7.2.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated as follows.

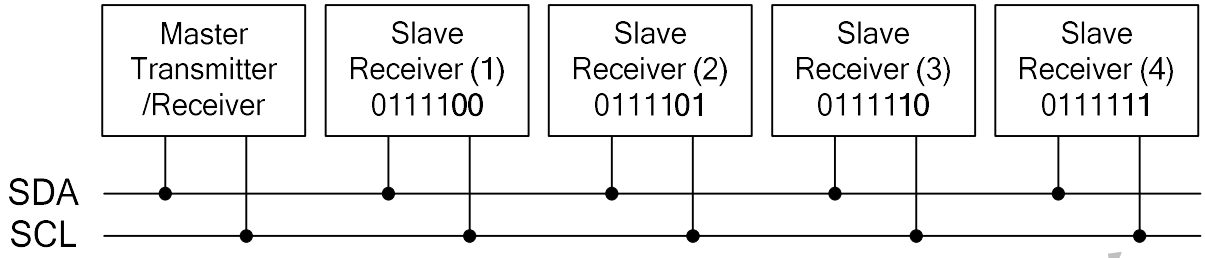


7.2.2 START and STOP Conditions

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated as follows.



7.2.3 System Configuration



The system configuration is illustrated above and some word-definitions are explained below:

a. Transmitter: the device which sends the data to the bus.

b. Receiver: the device which receives the data from the bus.

c. Master: the device which initiates a transfer generates clock signals and terminates a transfer.

d. Slave: the device which is addressed by a master.

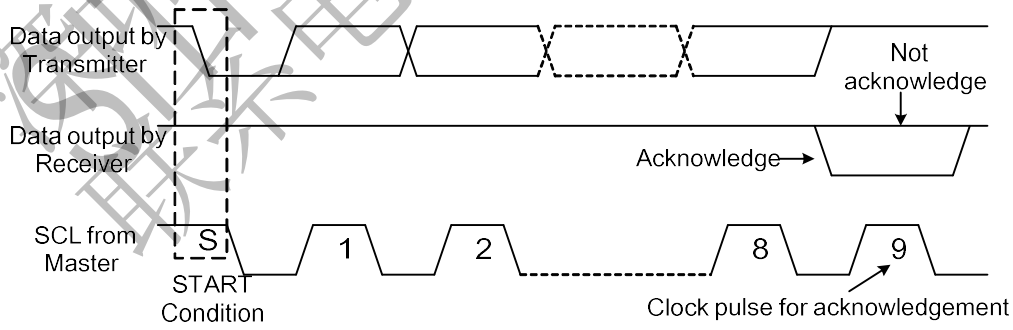
e. Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.

f. Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.

g. Synchronization: procedure to synchronize the clock signals of two or more devices.

7.2.4 Acknowledgment

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C Interface is illustrated as follows.



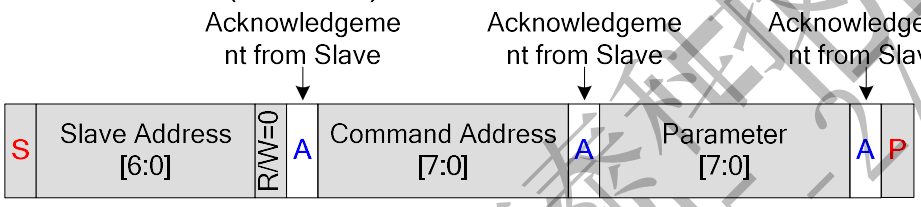
7.2.5 I²C Interface Protocol

The driver supports command/data write to addressed slaves on the bus. Before any data is transmitted on the I²C Interface, the device which should respond is addressed first. The default slave address is 0111100b and the three times I²C address could be OTP programing.

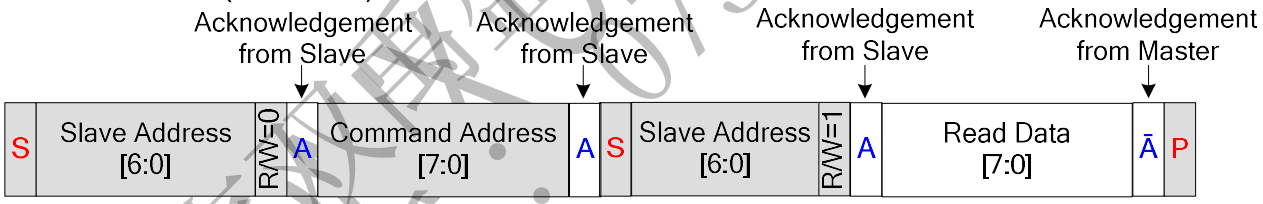
The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master. The register write/ read transference sequence are described as follows.

Write Mode (R/W="0")



Read Mode (R/W="1")



S: start condition
P: stop condition
A: acknowledge
Ā: no-acknowledge

master to slave

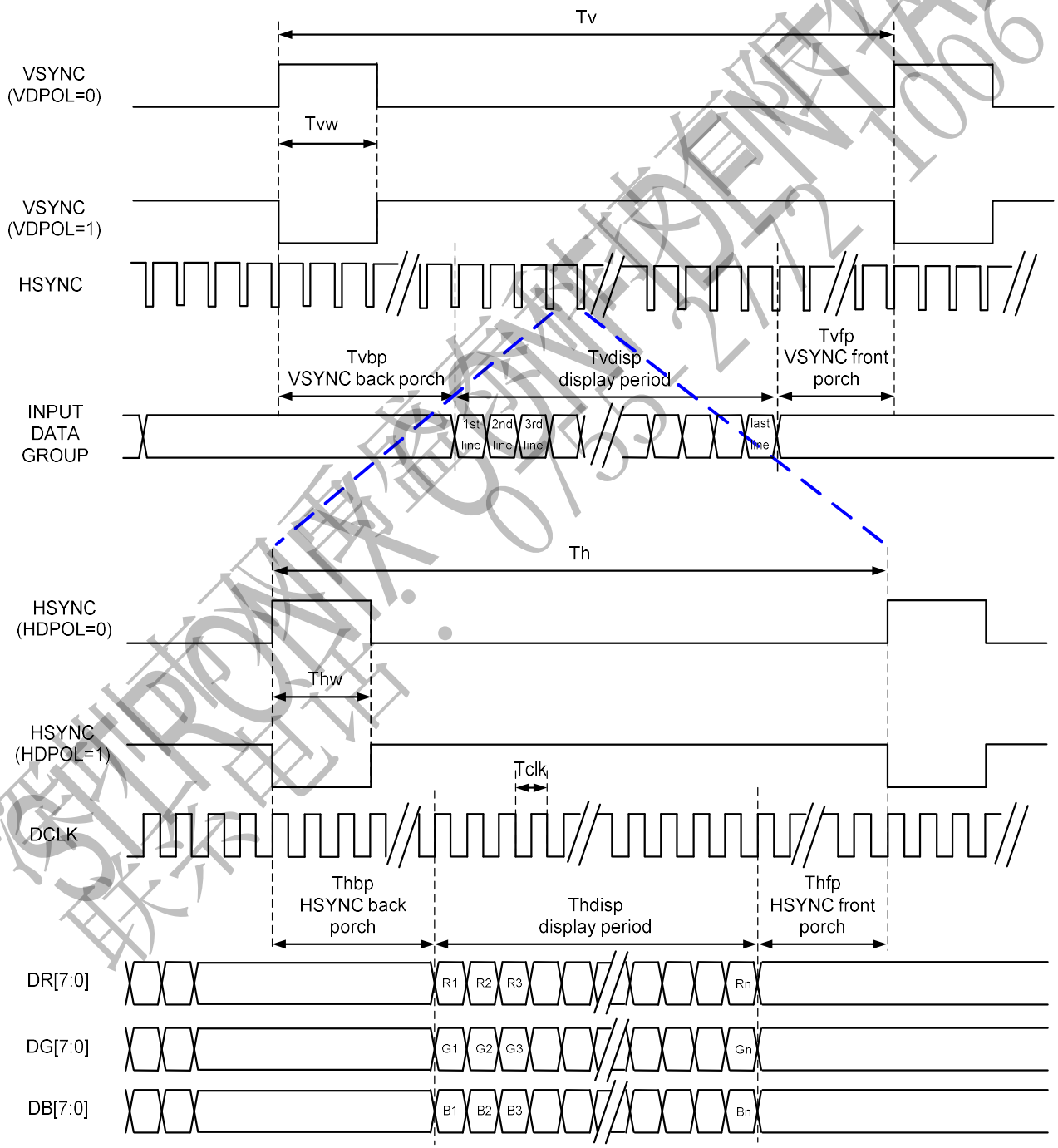
slave to master

7.3 RGB Interface

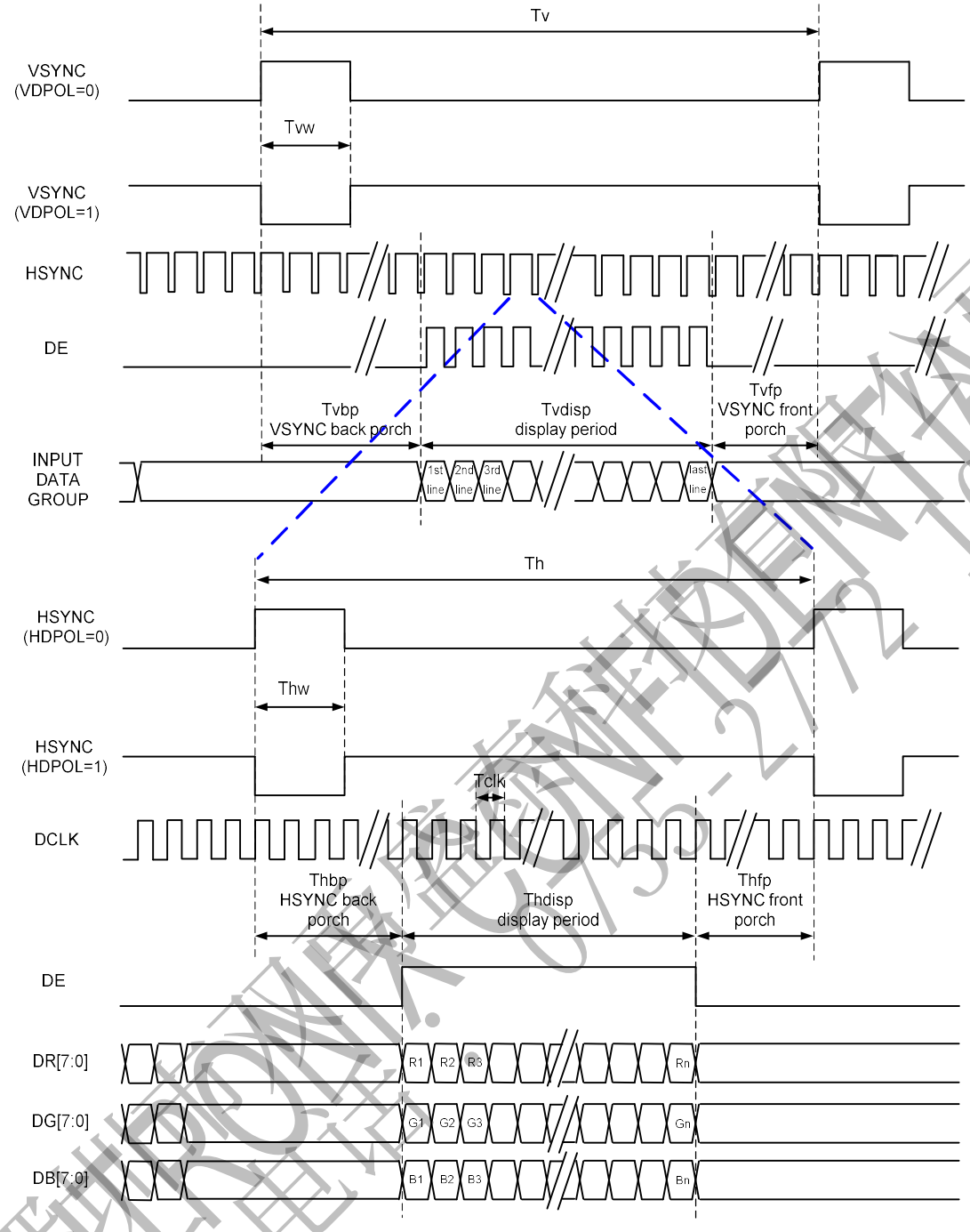
RGB Mode Selection Table	DCLK	HSYNC	VSYNC	DE
SYNC - DE Mode	Input	Input	Input	Input
SYNC Mode	Input	Input	Input	GND
DE Mode	Input	GND	GND	Input

Note: “Input” means these signals are driven by host side

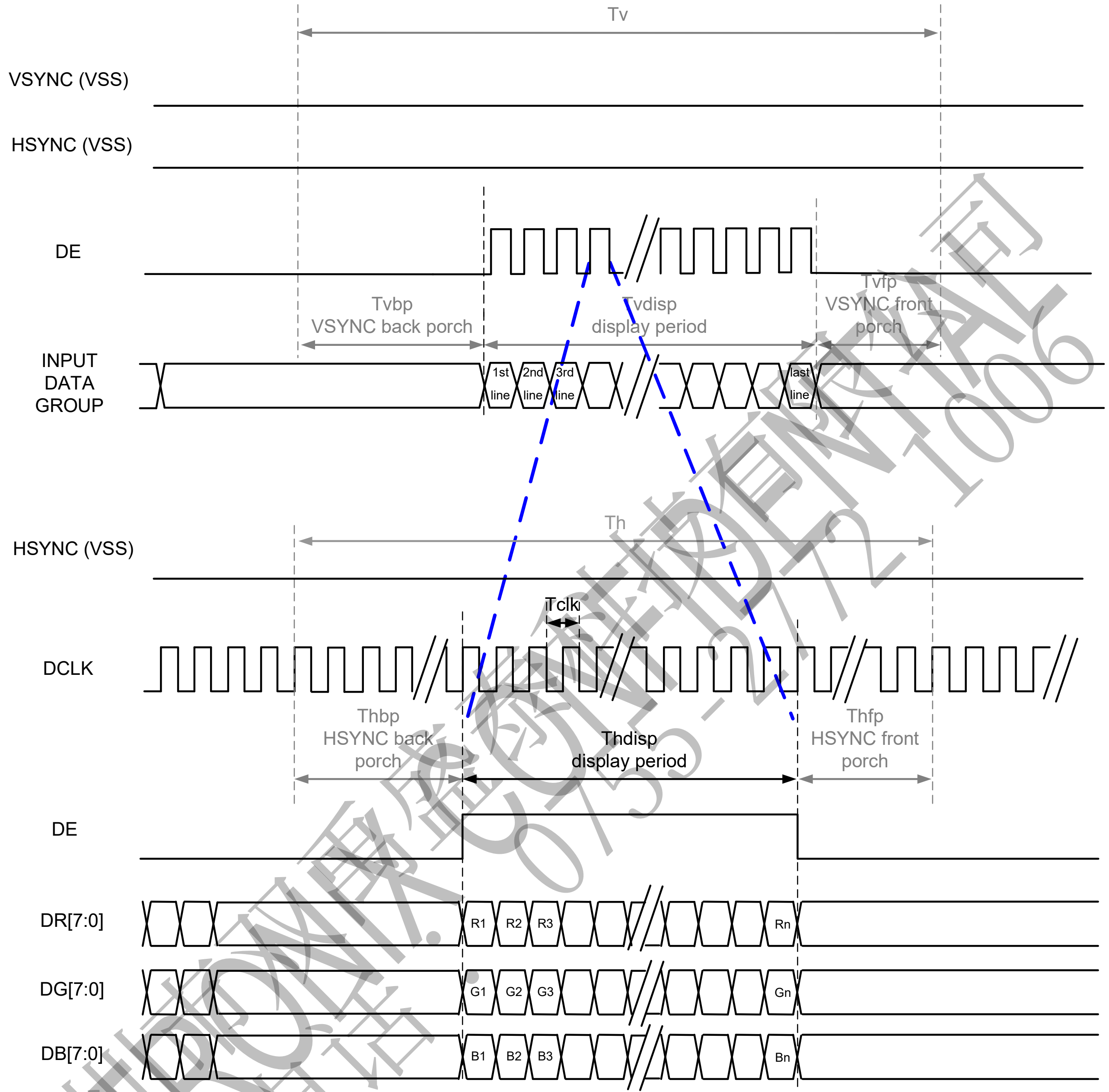
7.3.1 SYNC Mode



7.3.2 SYNC-DE Mode



7.3.3 DE Mode


Tv
VSYNC (VSS)
HSYNC (VSS)
DE
Tvbp
VSYNC back porch
Tvdisp
display period
Tvfp
VSYNC front porch
INPUT DATA GROUP
1st line
2nd line
3rd line
last line
Th
HSYNC (VSS)
Tclk
DCLK
Thbp
HSYNC back porch
Thdisp
display period
Thfp
HSYNC front porch
DE
DR[7:0]
R1
R2
R3
Rn
DG[7:0]
G1
G2
G3
Gn
DB[7:0]
B1
B2
B3
Bn

7.3.4 Parallel 24-bit RGB Input Timing Table

Parallel 24-bit RGB Input Timing (PVDD=PVDD1=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

Parallel 24-bit RGB Interface Timing Table							
Item		**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
DCLK Frequency		Fclk	23	25	27	MHz	
HSYNC	Period Time	Th	808	816	896	DCLK	
	Display Period	Thdisp		800		DCLK	
	Back Porch	Thbp	4	8	48	DCLK	
	Front Porch	Thfp	4	8	48	DCLK	
	Pulse Width	Thw	2	4	8	DCLK	
VSYNC	Period Time	Tv	492	496	504	HSYNC	
	Display Period	Tvdisp		480		HSYNC	
	Back Porch	Tvbp	6	8	12	HSYNC	
	Front Porch	Tvfp	6	8	12	HSYNC	
	Pulse Width	Tvw	2	4	8	HSYNC	

Note: 1. The minimum blanking time depends on the GIP timing of the panel specification

2. To ensure the compatibility of different panels, it is recommended to use the typical setting.

3. It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

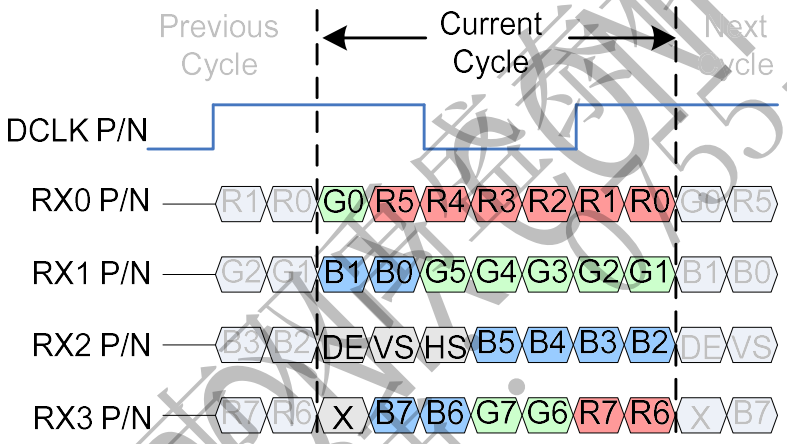
7.4 LVDS Interface

7.4.1 LVDS Input Pin Mapping Table

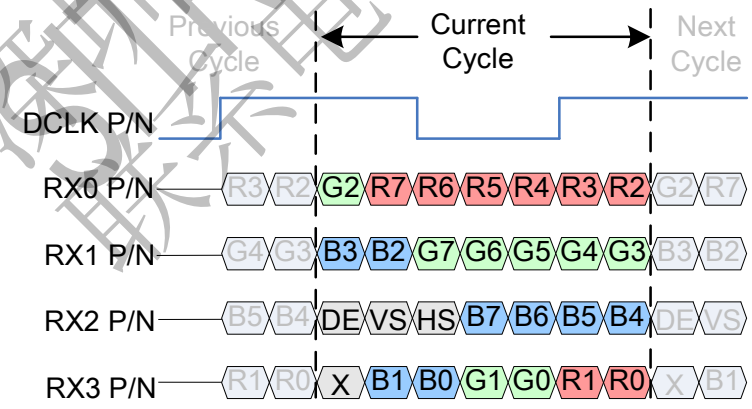
Pin Name RGB (LVDS)	LVDS 3 lane	LVDS 4 Lane
DCLKN	DCLKN	DCLKN
DCLKP	DCLKP	DCLKP
DB0	RX0P	RX0P
DB1	RX0N	RX0N
DB2	RX1P	RX1P
DB3	RX1N	RX1N
DB4	RX2P	RX2P
DB5	RX2N	RX2N
DB6	-	RX3P
DB7	-	RX3N

Note: Symbol "-" means reserve pin and should fix to "L" by DGND.

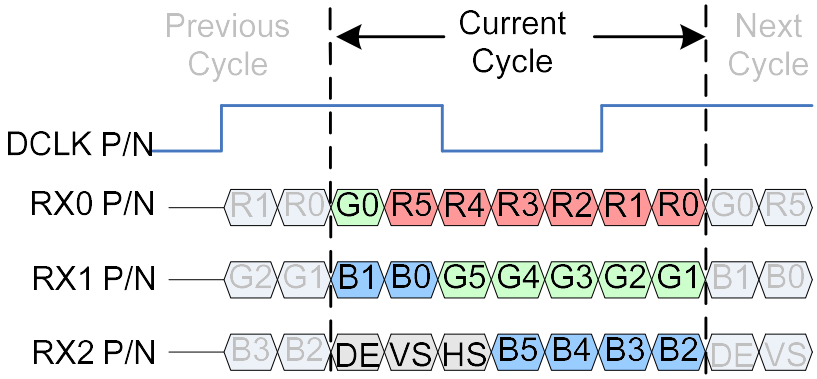
7.4.2 4 Lane VESA Data Format Color Bit Map



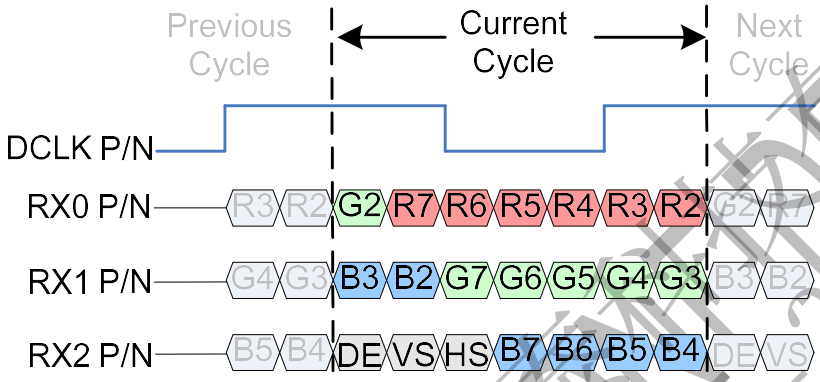
7.4.3 4 Lane JEIDA Data Format Color Bit Map



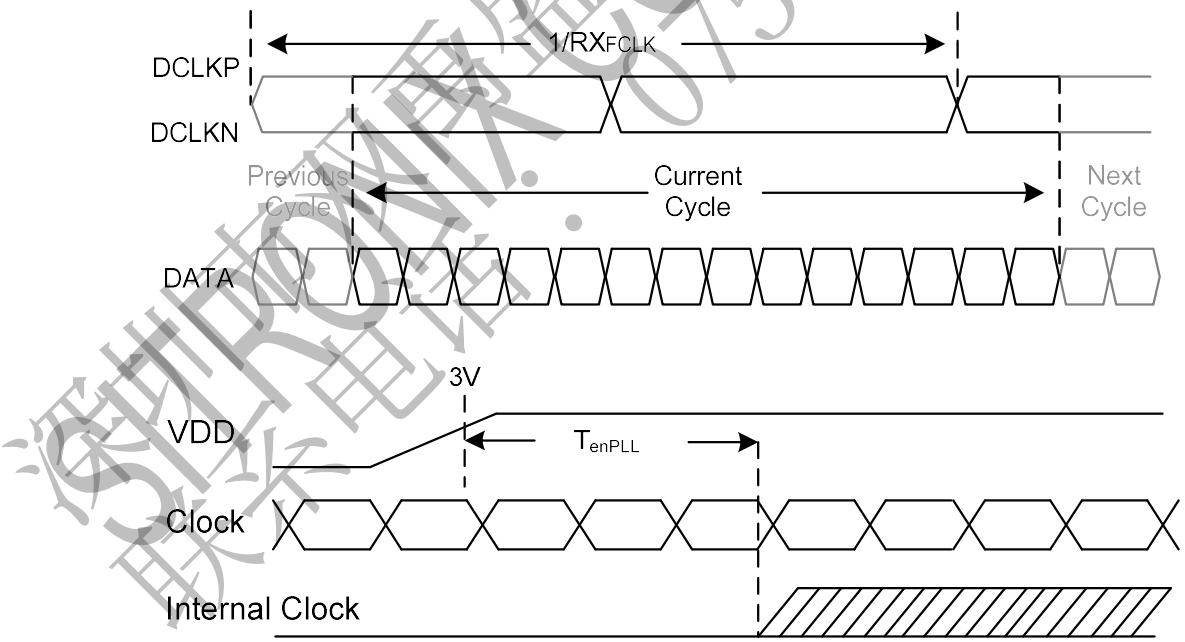
7.4.4 3 Lane VESA Mode Color Bit Map

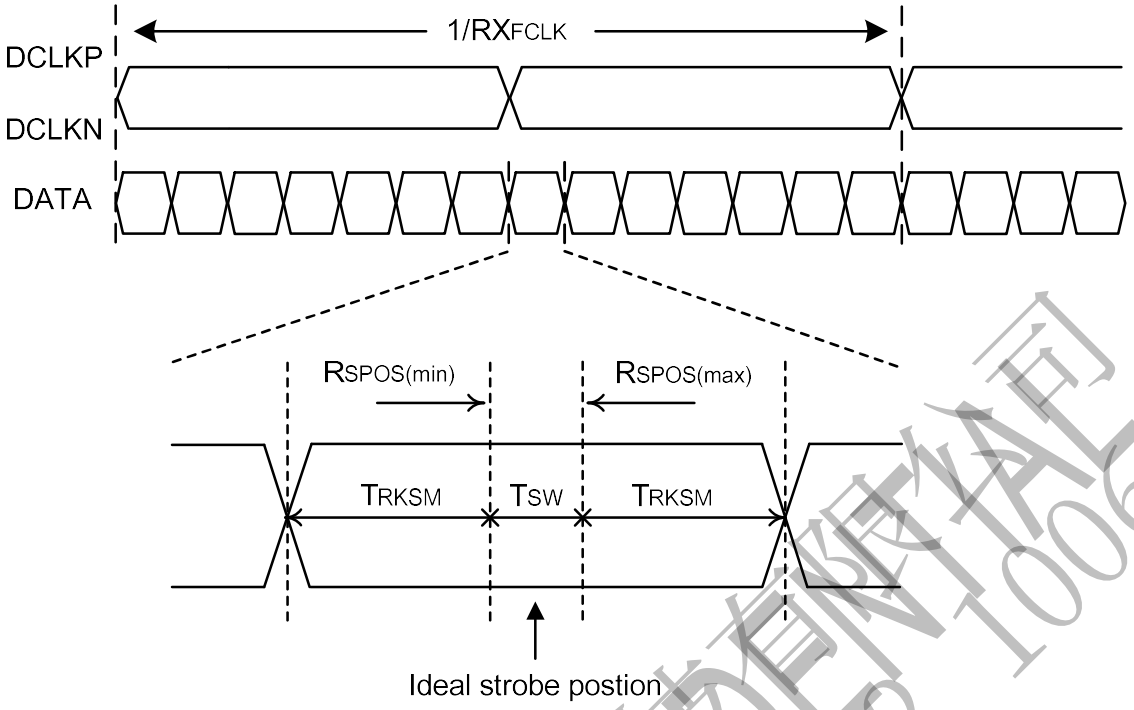


7.4.5 3 Lane JEIDA Mode Color Bit Map



7.4.6 LVDS Input Timing Table





RRKSM : Receiver strobe margin
RSPOS : Receiver strobe position
TSW : Strobe width (internal DATA sampling window)

LVDS Input Timing (PVDD=PVDD1=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	RX_{FCLK}	23	25	27	MHz	
Input Data Skew Margin	T_{RSKM}	400			ps	
Clock High Time	T_{LVCH}	4/(7 x RX_{FCLK})			ns	
Clock Low Time	T_{LVCL}	3/(7 x RX_{FCLK})			ns	
PLL Wake-up Time	T_{enPLL}			150	us	
LVDS Spread Spectrum Clocking (SSC) Tolerance of LVDS Receiver						
Modulation Frequency	SSC_{MF}			100	KHz	
Modulation Rate	SSC_{MR}			+/-3	%	

8. REGISTER LIST

8.1 Register Summary

COMMAND TABLE1										
Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	W	0	0	0	0	GRB	0	0	DISP	08h
11h	W	CONTRAST[7:0]								40h
12h	W	0	SUB_CONTRAST_R[6:0]							40h
13h	W	0	SUB_CONTRAST_B[6:0]							40h
14h	W	BRIGHTNESS[7:0]								40h
15h	W	0	SUB_BRIGHTNESS_R[6:0]							40h
16h	W	0	SUB_BRIGHTNESS_B[6:0]							40h
17h	W	H_BLANKING[7:0]								08h
18h	W	V_BLANKING[7:0]								08h
19h	W	MVA_TN	VDIR	HDIR	SBGR	0	0	0	0	-
1Ah	W	LVDS_FMT	1	0	LANE_SEL	0	0	0	0	-
1Bh	W	VDPOL	HDPOL	DEPOL	DCLKPOL	0	1	1	1	-
1Ch	W	0	0	0	0	0	AUTODL	0	0	-
COMMAND TABLE2										
Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	R/W	0	1	VRHP[5:0]						--
41h	R/W	0	VRHN[6:0]							--
45h	R/W	VGL[2:0]			1	VGHS[2:0]			1	--
46h	R/W	T4T[1:0]		T3T[1:0]		T2T[1:0]		T1T[1:0]		--
47h	R/W	0	0	0	0	0	SOURCE_AP[2:0]			--

Note: 1. When GRB is “Low”, all registers reset to default values.

2. Symbol “-” means this value is set by the customer.

3. Symbol “--” means this value is OTP setting according to system application, panel loading and display quality.

4. Do not use instructions not listed in these tables.

GAMMA COMMAND TABLE										
Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	R/W	0	RATIO1[1:0]		VRF0P[4:0]					--
21h	R/W	0	PFP6[3]	PFP0[3]	VOS0P[4:0]					--
22h	R/W	PFP0[2:0]			PKP0[4:0]					--
23h	R/W	PFP1[2:0]			PKP1[4:0]					--
24h	R/W	PFP2[2:0]			PKP2[4:0]					--
25h	R/W	PFP3[2:0]			PKP3[4:0]					--
26h	R/W	PFP4[2:0]			PKP4[4:0]					--
27h	R/W	PFP5[2:0]			PKP5[4:0]					--
28h	R/W	PFP6[2:0]			PKP6[4:0]					--
29h	R/W	0	0	0	PKP7[4:0]					--
30h	R/W	0	RATIO2[1:0]		VRF0N[4:0]					--
31h	R/W	0	PFN6[3]	PFN0[3]	VOS0N[4:0]					--
32h	R/W	PFN0[2:0]			PKN0[4:0]					--
33h	R/W	PFN1[2:0]			PKN1[4:0]					--
34h	R/W	PFN2[2:0]			PKN2[4:0]					--
35h	R/W	PFN3[2:0]			PKN3[4:0]					--
36h	R/W	PFN4[2:0]			PKN4[4:0]					--
37h	R/W	PFN5[2:0]			PKN5[4:0]					--
38h	R/W	PFN6[2:0]			PKN6[4:0]					--
39h	R/W	0	0	0	PKN7[4:0]					--

Note: 1. When GRB is “Low”, all registers reset to default values.

2. Symbol “--” means this value is OTP setting according to system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

OTP COMMAND TABLE											
Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
01h	R/W	0	ID1[6:0]							--
02h	R/W	0	ID2[6:0]							--
03h	R/W	0	ID3[6:0]							--
04h	R/W	0	I^2CID[6:0]							78h
05h	R/W	0	VMF[6:0]							40h
60h	W	0	1	0	0	0	1	OTPEN	0	44h
65h	W	OTPACK[7:0]								00h
66h	R	0	0	0	0	0	CMD2 OTP TIME[2:0]			-
67h	R	0	0	0	0	0	GAMMA OTP TIME[2:0]			-
68h	R	0	0	0	0	0	ID1 OTP TIME[2:0]			-
69h	R	0	0	0	0	0	ID2 OTP TIME[2:0]			-
6Ah	R	0	0	0	0	0	ID3 OTP TIME[2:0]			-
6Bh	R	0	0	0	0	0	I^2CID OTP TIME[2:0]			-
6Ch	R	0	0	0	0	0	VMF OTP TIME[2:0]			-

Note: 1. When GRB is "Low", all registers reset to default values.

2. Symbol "-" means this value is OTP read value.

3. Symbol "--" means this value is OTP setting according to parameters of system application, panel loading and display quality.

4. Do not use instructions not listed in these tables.

8.2 Command Table1 Register Description

8.2.1 GRB、DISP CONTROL (10h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	W	0	0	0	0	GRB	0	0	DISP	08h

Designation	Description
GRB	Reset register setting GRB=0: reset all registers to default value GRB=1: normal operation
DISP	Display on/off control DISP=0: standby mode DISP=1: normal mode

8.2.2 CONTRAST (11h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
11h	W	CONTRAST[7:0]								40h

Designation	Description
CONTRAST[7:0]	Set RGB contrast level, the range of gain is 0~3.984 CONTRAST=00h: contrast gain=0 CONTRAST=40h: contrast gain=1 CONTRAST=FFh: contrast gain=3.984

8.2.3 SUB_CONTRAST_R (12h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	W	0	SUB_CONTRAST_R[6:0]							40h

Designation	Description
SUB_CONTRAST_R[6:0]	Set red color sub-contrast level, the range of gain is 0.75~1.246 SUB_CONTRAST_R=00h: contrast gain=0.75 SUB_CONTRAST_R=40h: contrast gain=1 SUB_CONTRAST_R=7Fh: contrast gain=1.246

8.2.4 SUB_CONTRAST_B (13h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
13h	W	0	SUB_CONTRAST_B[6:0]							40h

Designation	Description
SUB_CONTRAST_B[6:0]	Set blue color sub-contrast level, the range of gain is 0.75~1.246 SUB_CONTRAST_B=00h: contrast gain=0.75 SUB_CONTRAST_B=40h: contrast gain=1 SUB_CONTRAST_B=7Fh: contrast gain=1.246

8.2.5 BRIGHTNESS (14h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
14h	W	BRIGHTNESS[7:0]								40h

Designation	Description
BRIGHTNESS[7:0]	Set RGB brightness level, the range of brightness is -64~+191 BRIGHTNESS=00h: -64 BRIGHTNESS=40h: 0 BRIGHTNESS=FFh: +191

8.2.6 SUB-BRIGHTNESS_R (15h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
15h	W	0	SUB_BRIGHTNESS_R[6:0]							40h

Designation	Description
SUB_BRIGHTNESS_R [6:0]	Set red color sub-brightness level, the range of brightness is -64~+63 SUB_BRIGHTNESS_R=00h: -64 SUB_BRIGHTNESS_R=40h: 0 SUB_BRIGHTNESS_R=7Fh: +63

8.2.7 SUB-BRIGHTNESS_B (16h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
16h	W	0	SUB_BRIGHTNESS_B[6:0]							40h

Designation	Description
SUB_BRIGHTNESS_B [6:0]	Set blue color sub-brightness level, the range of brightness is -64~+63 SUB_BRIGHTNESS_B=00h: -64 SUB_BRIGHTNESS_B=40h: 0 SUB_BRIGHTNESS_B=7Fh: +63

8.2.8 H_BLANKING (17h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
17h	W	H_BLANKING[7:0]								08h

Designation	Description
H_BLANKING[7:0]	The HSYNC back porch setting of RGB interface

8.2.9 V_BLANKING (18h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	R/W	V_BLANKING[7:0]								08h

Designation	Description
V_BLANKING[7:0]	The VSYNC back porch setting of RGB interface

8.2.10 DISPLAY MODE SETTING (19h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
19h	W	MVA_TN	VDIR	HDIR	SBGR	0	0	0	0	-

Designation	Description
MVA_TN	MVA_TN=0: TN mode for panel display. MVA_TN=1: VA mode for panel display.
VDIR	Vertical scan direction setting VDIR= 0: from bottom to top, L(n)(first line) → L(n-1) →…→ L2 → L1(last line) VDIR= 1: from top to bottom, L1(first line) → L2 →…→ L(n-1) → L(n)(last line)
HDIR	Horizontal scan direction setting HDIR= 0: from right to left, Y(n)(first data) → Y(n-1) →…→ Y2 → Y1(last data) HDIR= 1: from left to right, Y1(first data) → Y2 →…→ Y(n-1) → Y(n)(last data)
SBGR	Data of red and blue exchange SBGR= 0: normal, DR[7:0]→DR[7:0] and DB[7:0]→DB[7:0] SBGR= 1: exchange, DR[7:0]→DB[7:0] and DB[7:0]→DR[7:0]

8.2.11 LVDS MODE SETTING (1Ah)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	W	LVDS_FMT	1	0	LANE_SEL	0	0	0	0	-

Designation	Description
LVDS_FMT	Set data format of LVDS interface LVDS_FMT: 0 = VESA; 1 = JEIDA
LANE_SEL	Set data lane of LVDS interface LANE_SEL: 0 = 3 lane; 1 = 4 lane

8.2.12 RGB INTERFACE POLARITY SETTING (1Bh)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Bh	W	VDPOL	HDPOL	DEPOL	DCLKPOL	0	1	1	1	-

Designation	Description
VDPOL	VSYNC polarity setting VDPOL= 0: positive polarity VDPOL= 1: negative polarity
HDPOL	HSYNC polarity setting HDPOL= 0: positive polarity HDPOL= 1: negative polarity
DEPOL	DE polarity setting DEPOL= 0: positive polarity DEPOL= 1: negative polarity
DCLKPOL	DCLK polarity setting DCLKPOL= 0: positive polarity DCLKPOL= 1: negative polarity

8.2.13 OTP AUTO DOWNLOAD CONTROL (1Ch)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	W	0	0	0	0	0	AUTODL	0	0	-

Designation	Description
AUTODL	OTP auto-refresh function control AUTODL= 0: disable auto-refresh function AUTODL= 1: enable auto-refresh function

8.3 Command Table2 Register Description

8.3.1 GVDD SETTING (40h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	R/W	0	1	VRHP[5:0]						--

Designation	Description
VRHP[5:0]	GVDD level setting

VRHP[5:0]	GVDD	VRHP[5:0]	GVDD	VRHP[5:0]	GVDD	VRHP[5:0]	GVDD
000000	5.9680	010000	5.7120	100000	5.4560	110000	5.2000
000001	5.9520	010001	5.6960	100001	5.4400	110001	5.1840
000010	5.9360	010010	5.6800	100010	5.4240	110010	5.1680
000011	5.9200	010011	5.6640	100011	5.4080	110011	5.1520
000100	5.9040	010100	5.6480	100100	5.3920	110100	5.1360
000101	5.8880	010101	5.6320	100101	5.3760	110101	5.1200
000110	5.8720	010110	5.6160	100110	5.3600	110110	5.1040
000111	5.8560	010111	5.6000	100111	5.3440	110111	5.0880
001000	5.8400	011000	5.5840	101000	5.3280	111000	5.0720
001001	5.8240	011001	5.5680	101001	5.3120	111001	5.0560
001010	5.8080	011010	5.5520	101010	5.2960	111010	5.0400
001011	5.7920	011011	5.5360	101011	5.2800	111011	5.0240
001100	5.7760	011100	5.5200	101100	5.2640	111100	5.0080
001101	5.7600	011101	5.5040	101101	5.2480	111101	4.9920
001110	5.7440	011110	5.4880	101110	5.2320	111110	4.9760
001111	5.7280	011111	5.4720	101111	5.2160	111111	4.9600

8.3.2 GVCL SETTING (41h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
41h	R/W	0	VRHN[6:0]							--

Designation	Description
VRHN[6:0]	GVCL level setting

VRHN[6:0]	GVCL	VRHN[6:0]	GVCL	VRHN[6:0]	GVCL	VRHN[6:0]	GVCL
0100000	-4.4800	0111000	-4.0960	1010000	-3.7120	1101000	-3.3280
0100001	-4.4640	0111001	-4.0800	1010001	-3.6960	1101001	-3.3120
0100010	-4.4480	0111010	-4.0640	1010010	-3.6800	1101010	-3.2960
0100011	-4.4320	0111011	-4.0480	1010011	-3.6640	1101011	-3.2800
0100100	-4.4160	0111100	-4.0320	1010100	-3.6480	1101100	-3.2640
0100101	-4.4000	0111101	-4.0160	1010101	-3.6320	1101101	-3.2480
0100110	-4.3840	0111110	-4.0000	1010110	-3.6160	1101110	-3.2320
0100111	-4.3680	0111111	-3.9840	1010111	-3.6000	1101111	-3.2160
0101000	-4.3520	1000000	-3.9680	1011000	-3.5840	1110000	-3.2000
0101001	-4.3360	1000001	-3.9520	1011001	-3.5680	1110001	-3.1840
0101010	-4.3200	1000010	-3.9360	1011010	-3.5520	1110010	-3.1680
0101011	-4.3040	1000011	-3.9200	1011011	-3.5360	1110011	-3.1520
0101100	-4.2880	1000100	-3.9040	1011100	-3.5200	1110100	-3.1360
0101101	-4.2720	1000101	-3.8880	1011101	-3.5040	1110101	-3.1200
0101110	-4.2560	1000110	-3.8720	1011110	-3.4880	1110110	-3.1040
0101111	-4.2400	1000111	-3.8560	1011111	-3.4720	1110111	-3.0880
0110000	-4.2240	1001000	-3.8400	1100000	-3.4560	1111000	-3.0720
0110001	-4.2080	1001001	-3.8240	1100001	-3.4400	1111001	-3.0560
0110010	-4.1920	1001010	-3.8080	1100010	-3.4240	1111010	-3.0400
0110011	-4.1760	1001011	-3.7920	1100011	-3.4080	1111011	-3.0240
0110100	-4.1600	1001100	-3.7760	1100100	-3.3920	1111100	-3.0080
0110101	-4.1440	1001101	-3.7600	1100101	-3.3760	1111101	-2.9920
0110110	-4.1280	1001110	-3.7440	1100110	-3.3600	1111110	-2.9760
0110111	-4.1120	1001111	-3.7280	1100111	-3.3440	1111111	-2.9600

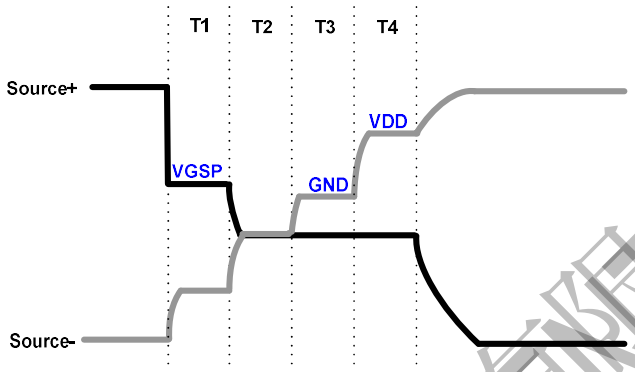
8.3.3 VGHS, VGL SETTING (45h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
45h	R/W	VGL[2:0]			1	VGHS[2:0]			1	--

Designation	Description
VGL[2:0]	VGL level setting VGL[2:0] / VGL (V) 000 / -7 001 / -8 010 / -8.5 011 / -9.5 100 / -10.5 101 / -11.5
VGHS[2:0]	VGHS level setting VGHS[2:0] / VGHS (V) 000 / 12 001 / 13 010 / 14 011 / 15 100 / 15.5

8.3.4 SOURCE EQUALIZE TIME SETTING (46h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
46h	R/W	T4T[1:0]		T3T[1:0]		T2T[1:0]		T1T[1:0]		--

Designation	Description
T4T[1:0] T3T[1:0] T2T[1:0] T1T[1:0]	

Source equalizing T4 timing setting

T4T[1:0]	T4 (DCLK)
00	6
01	12
10	24
11	48

Source equalizing T3 timing setting

T3T[1:0]	T3 (DCLK)
00	1
01	12
10	24
11	48

Source equalizing T2 timing setting

T2T[1:0]	T2 (DCLK)
00	1
01	12
10	24
11	48

Source equalizing T1 timing setting

T1T[1:0]	T1 (DCLK)
00	OFF
01	1
10	6
11	12

8.3.5 SOURCE OP-AMP POWER SETTING (47h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
47h	R/W	0	0	0	0	0	SOURCE_AP[2:0]			--

Designation	Description
SOURCE_AP[2:0]	Source driving ability setting. When value is higher, the source output current will increase.

SOURCE_AP[2:0]	Source Power
000	Level 1 (lowest)
001	Level 2 (minimal)
010	Level 3 (minimal to medium)
011	Level 4 (medium)
100	Level 5 (medium to large)
101	Level 6 (large)
110	Level 7 (large to highest)
111	Level 8 (highest)

Note: The setting value needs to be adjusted according to the display performance.

8.4 Gamma Table Register Description

8.4.1 GAMMA SETTING (20h~29h, 30h~39h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	R/W	0	RATIO1[1:0]		VRFP0P[4:0]					--
21h	R/W	0	PFP6[3]	PFP0[3]	VOS0P[4:0]					--
22h	R/W	PFP0[2:0]			PKP0[4:0]					--
23h	R/W	PFP1[2:0]			PKP1[4:0]					--
24h	R/W	PFP2[2:0]			PKP2[4:0]					--
25h	R/W	PFP3[2:0]			PKP3[4:0]					--
26h	R/W	PFP4[2:0]			PKP4[4:0]					--
27h	R/W	PFP5[2:0]			PKP5[4:0]					--
28h	R/W	PFP6[2:0]			PKP6[4:0]					--
29h	R/W	0	0	0	PKP7[4:0]					--
30h	R/W	0	RATIO2[1:0]		VRFP0N[4:0]					--
31h	R/W	0	PFN6[3]	PFN0[3]	VOS0N[4:0]					--
32h	R/W	PFN0[2:0]			PKN0[4:0]					--
33h	R/W	PFN1[2:0]			PKN1[4:0]					--
34h	R/W	PFN2[2:0]			PKN2[4:0]					--
35h	R/W	PFN3[2:0]			PKN3[4:0]					--
36h	R/W	PFN4[2:0]			PKN4[4:0]					--
37h	R/W	PFN5[2:0]			PKN5[4:0]					--
38h	R/W	PFN6[2:0]			PKN6[4:0]					--
39h	R/W	0	0	0	PKN7[4:0]					--

Designation	Description
PKP0[4:0]	V16 gamma selection
PKN0[4:0]	
PKP1[4:0]	V32 gamma selection
PKN1[4:0]	
PKP2[4:0]	V48 gamma selection
PKN2[4:0]	
PKP3[4:0]	V80 gamma selection
PKN3[4:0]	
PKP4[4:0]	V176 gamma selection
PKN4[4:0]	
PKP5[4:0]	V208 gamma selection
PKN5[4:0]	
PKP6[4:0]	V224 gamma selection
PKN6[4:0]	

PKP7[4:0]	V240 gamma selection
PKN7[4:0]	
VRF0P[4:0]	V8 gamma selection
VRF0N[4:0]	
VOS0P[4:0]	V248 gamma selection
VOS0N[4:0]	
PFP0[3:0]	V12 gamma selection
PFN0[3:0]	
PFP1[2:0]	V64 gamma selection
PFN1[2:0]	
PFP2[2:0]	V104 gamma selection
PFN2[2:0]	
PFP3[2:0]	V128 gamma selection
PFN3[2:0]	
PFP4[2:0]	V152 gamma selection
PFN4[2:0]	
PFP5[2:0]	V192 gamma selection
PFN5[2:0]	
PFP6[3:0]	V244 gamma selection
PFN6[3:0]	
RATIO1[1:0]	V248-V255 gamma ratio selection
RATIO2[1:0]	V0-V8 gamma ratio selection

8.5 OTP Table Register Description

8.5.1 ID1 SETTING (01h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
01h	R/W	0	ID1[6:0]							--

Designation	Description
ID1[6:0]	Built-in OTP for ID1 setting.

8.5.2 ID2 SETTING (02h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	R/W	0	ID2[6:0]							--

Designation	Description
ID2[6:0]	Built-in OTP for ID2 setting.

8.5.3 ID3 SETTING (03h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
03h	R/W	0	ID3[6:0]							--

Designation	Description
ID3[6:0]	Built-in OTP for ID3 setting.

8.5.4 I2C ID SETTING (04h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
04h	R/W	0	I^2CID[6:0]							78h

Designation	Description
I^2CID[6:0]	Built-in OTP for I^2C slave address setting.

8.5.5 VCOM OFFSET SETTING (05h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
05h	R/W	0	VMF[6:0]							40h

Designation	Description
VMF[6:0]	VCOM offset setting

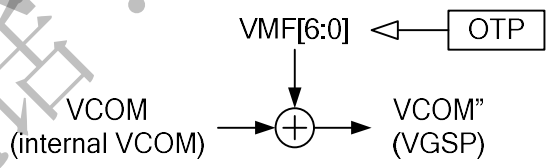
VMF[6]	VMF[5:0]	VCOM”	GVDD	GVCL
0	000000	VCOM+64d	VRHP[6:0]+64d	VRHN[6:0]+64d
0	000001	VCOM+63d	VRHP[6:0]+63d	VRHN[6:0]+63d
0	000010	VCOM+62d	VRHP[6:0]+62d	VRHN[6:0]+62d
0	|	|	|	|
0	111110	VCOM+2d	VRHP[6:0]+2d	VRHN[6:0]+2d
0	111111	VCOM+1d	VRHP[6:0]+1d	VRHN[6:0]+1d
1	000000	VCOM+0d	VRHP[6:0]	VRHN[6:0]
1	000001	VCOM-1d	VRHP[6:0]-1d	VRHN[6:0]-1d
1	000010	VCOM-2d	VRHP[6:0]-2d	VRHN[6:0]-2d
1	|	|	|	|
1	111110	VCOM-62d	VRHP[6:0]-62d	VRHN[6:0]-62d
1	111111	VCOM-63d	VRHP[6:0]-63d	VRHN[6:0]-63d

Note: 1. d=16mV

2. Adjustable VCOM offset (OTP) can be used to compensate feedthrough tolerance and its limitation couldn’t exceed the maximum voltage range of GVDD and GVCL.

3. VCOM” ≤ GVDD-Vop = GVCL+Vop

Vop is the operation voltage of liquid crystal.



8.5.6 OTP FUNCTION CONTROL (60h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
60h	W	0	1	0	0	0	1	OTPEN	0	44h

Designation	Description
OTPEN	OTP programming function control OTPEN = 0: disable OTP programming function OTPEN = 1: enable OTP programming function

8.5.7 OTP ACKNOWLEDGEMENT CONTROL (65h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
65h	W	OTPACK[7:0]								00h

Designation	Description
OTPACK[7:0]	OTP active selection item. OTPACK[7:0] / Description 31h / ID1 program 32h / ID2 program 33h / ID3 program 34h / I²C I/F ID program 3Ah / VCOM offset program 4Bh / Command 2 program 5Ch / Gamma program

8.5.8 COMMAND 2 PROGRAM TIMES (66h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
66h	R	0	0	0	0	0	CMD2 OTP TIME[2:0]			--

Designation	Description
CMD2 OTP TIME[2:0]	Read COMMAND 2 remaining programmable times.

8.5.9 GAMMA PROGRAM TIMES (67h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
67h	R	0	0	0	0	0	GAMMA OTP TIME[2:0]			--

Designation	Description
GAMMA OTP TIME[2:0]	Read GAMMA remaining programmable times.

8.5.10 ID1 PROGRAM TIMES (68h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
68h	R	0	0	0	0	0	ID1 OTP TIME[2:0]			--

Designation	Description
ID1 OTP TIME[2:0]	Read ID1 remaining programmable times.

8.5.11 ID2 PROGRAM TIMES (69h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
69h	R	0	0	0	0	0	ID2 OTP TIME[2:0]			--

Designation	Description
ID2 OTP TIME[2:0]	Read ID2 remaining programmable times.

8.5.12 ID3 PROGRAM TIMES (6Ah)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ah	R	0	0	0	0	0	ID3 OTP TIME[2:0]			--

Designation	Description
ID3 OTP TIME[2:0]	Read ID3 remaining programmable times.

8.5.13 I²C ID PROGRAM TIMES (6Bh)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Bh	R	0	0	0	0	0	I²CID OTP TIME[2:0]			--

Designation	Description
I²CID OTP TIME[2:0]	Read I²CID remaining programmable times.

8.5.14 VCOM OFFEST PROGRAM TIMES (6Ch)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ch	R	0	0	0	0	0	VMF OTP TIME[2:0]			--

Designation	Description
VMF OTP TIME[2:0]	Read VCOM offset remaining programmable times.

9. ELECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	VDD	- 0.3 ~ +4.0	V
IO Supply Voltage	VDDI	- 0.3 ~ +4.0	V
Charge Pump Supply Voltage	PVDD	- 0.3 ~ +4.0	V
Enhance Charge Pump Supply Voltage	PVDD1	- 0.3 ~ +4.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Output Voltage Range	VOUT	-0.3 ~ VDDI + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Note:

1. *That the stress exceeds the Limiting Value listed above it may cause the driver IC permanent damage. These values are for stress only. IC should be operated under the DC/AC Characteristic conditions for normal operation. If these conditions are not met, IC operation may be error and the reliability may be deteriorated.*
2. *Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.*
3. *Insure the voltage levels of VDDI, VDD, PVDD, PVDD1 always matches the correct relation:*
   3.1V ≦ VDDI ≦ VDD = PVDD=PVDD1 ≦ 3.6V
4. *VIN should be less than or equal to 3.6V. (VIN ≤ 3.6V)*
5. *Panel display quality depends on panel loading, and it may have the different performance at low/high temperature.*
6. *To avoid IC being affected by backlight temperature, it is recommended that the backlight led position shouldn't be near the periphery of IC.*
7. *IC can be operated normally at -30~85 degrees, but display quality at high/low temperatures may have different effect according to different panel characteristics.*

9.2 DC Characteristics

DC Electrical Characteristics (PVDD=PVDD1=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

9.2.1 Recommended Operating Range

DC Electrical Characteristics (PVDD=PVDD1=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VDD	3.1	3.3	3.6	V	
IO Supply Voltage	VDDI	3.1	3.3	3.6	V	
Charge Pump Supply Voltage	PVDD	3.1	3.3	3.6	V	
Enhance Charge Pump Supply Voltage	PVDD1	3.1	3.3	3.6	V	

9.2.2 DC Characteristics for Digital Circuit

DC Electrical Characteristics (PVDD=PVDD1=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic-High Input Voltage	Vih	0.7VDDI	-	VDDI	V	
Logic-Low Input Voltage	Vil	DGND	-	0.3VDDI	V	
Logic-High Output Voltage	Voh	VDDI-0.4	-	VDDI	V	
Logic-Low Output Voltage	Vol	DGND	-	DGND+0.4	V	

9.2.3 DC Characteristics for Analog Circuit

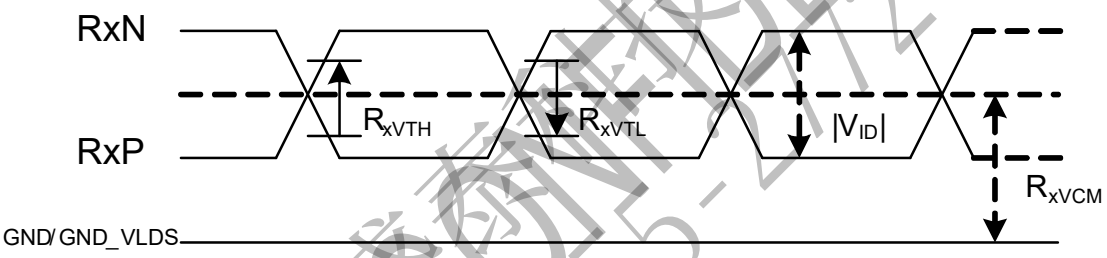
DC Electrical Characteristics (PVDD=PVDD1=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Positive High-Voltage Power	VGHS	12	15	15.5	V	No Load@ FR=60Hz
Negative High-Voltage Power	VGL	-11.5	-10	-7	V	
Output Voltage Deviation	Vod	-	±40	±50	mV	
Standby Current	Isc	-	-	50	uA	
Operation Current	Ioc	-	50	-	mA	

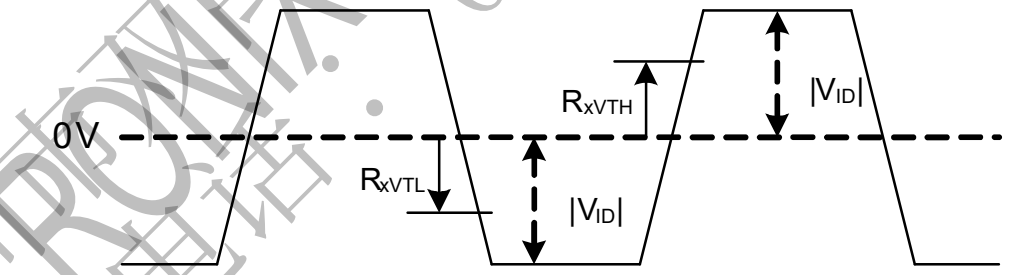
9.2.4 DC Characteristics for LVDS Receiver Circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential Input High Threshold Voltage	R_{xVTH}	-	-	0.1	V	R_{xVCM} = 1.2V
Differential Input Low Threshold Voltage	R_{xVTL}	-0.1	-	-	V	
Input Voltage Range (Singled-End)	R_{xVIN}	0	-	VDD-1.0	V	
Differential Input Common Mode Voltage	R_{xVCM}	$\lvert V_{ID} \rvert$ /2	-	2.4-$\lvert V_{ID} \rvert$/2	V	
Differential Input Voltage	$\lvert V_{ID} \rvert$	0.2	-	0.6	V	
Differential Input Leakage Current	RV_{xliz}	-10	-	10	uA	
LVDS Digital Operating Current	I_{VDD_LVDS}	-	10	15	mA	
LVDS Digital Stand-by Current	I_{STBD_LVDS}	-	10	50	uA	
Differential Input Termination Resistance	R_{ID}	90	100	110	Ω	

Single End Signals



Differential Signals



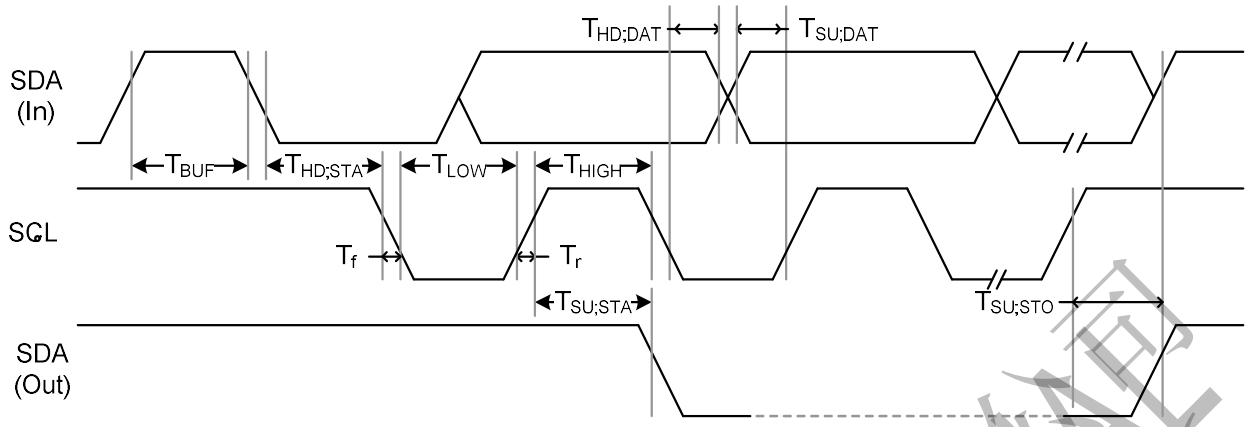
9.3 AC Characteristics

AC Electrical Characteristics (PVDD=PVDD1=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

9.3.1 System Operation AC Characteristics

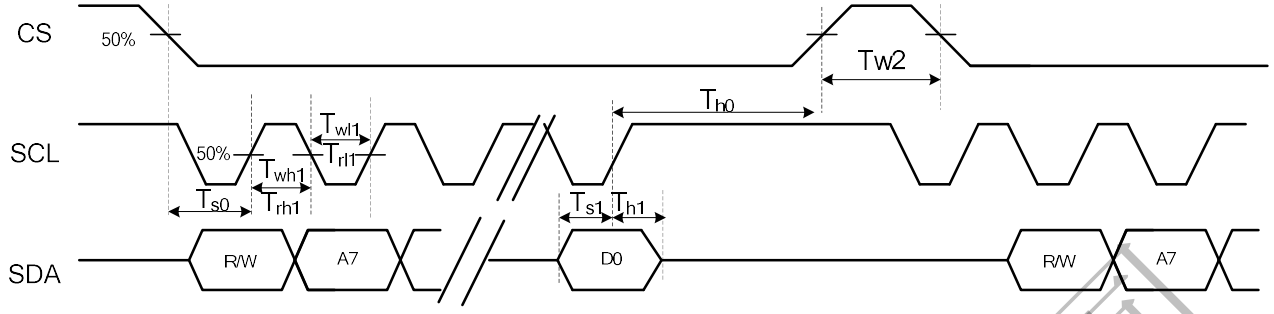
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD Power Source Slew Time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB Pulse Width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
SD Output Stable Time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD Output Rise and Fall Time	Tgst	-	-	6	us	Output settled (5%~95%), Loading = 4.7k+29.8pF

9.3.2 System Bus Timing for I²C Interface



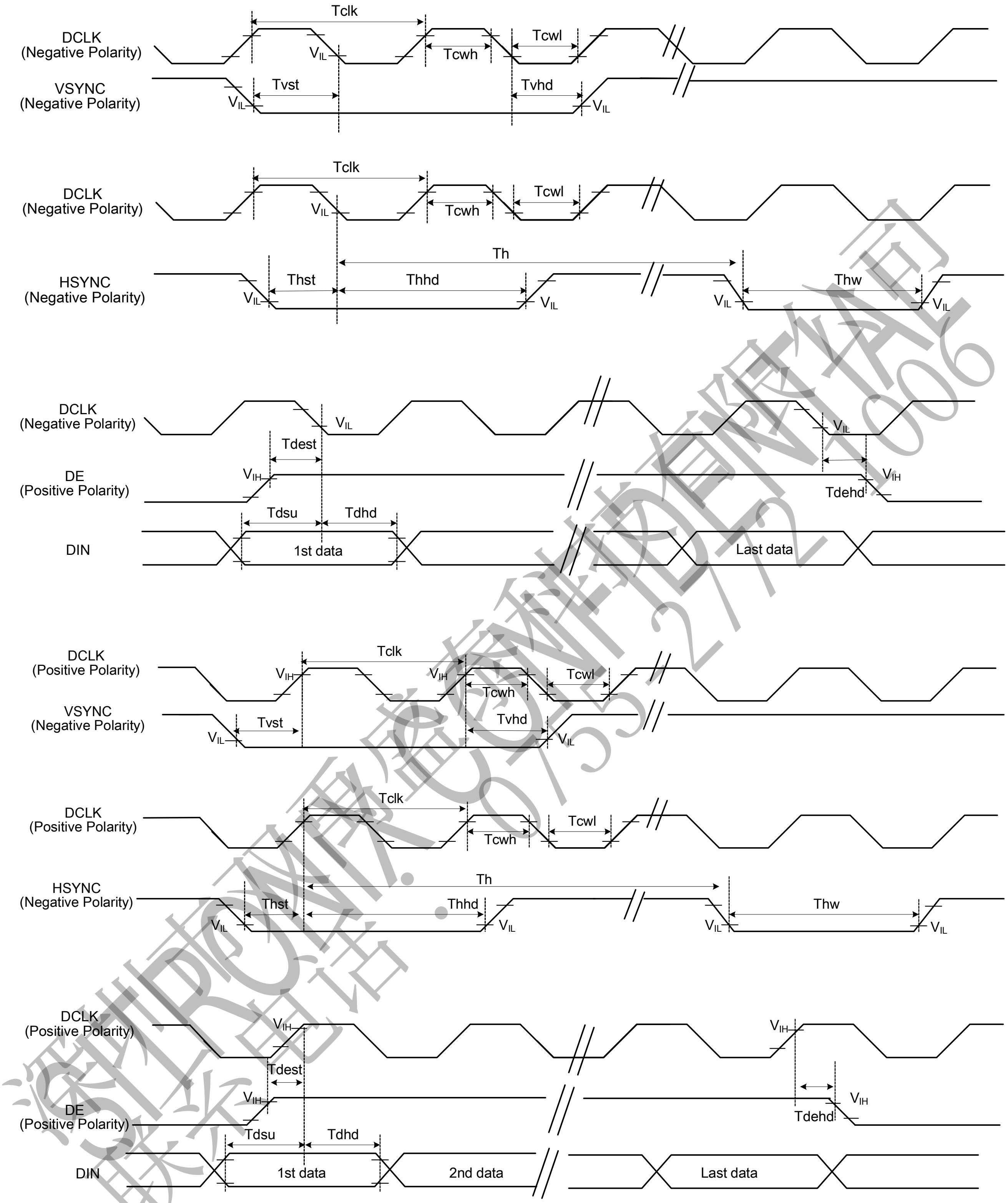
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCL Clock Frequency	F_{SCL}	-	-	400	KHz	
SCL Clock Low Period	T_{LOW}	1300	-	-	ns	
SCL Clock High Period	T_{HIGH}	600	-	-	ns	
Signal Rise Time	T_r	20+0.1Cb	-	300	ns	
Signal Fall Time	T_f	20+0.1Cb	-	300	ns	
Start Condition Setup Time	$T_{SU;STA}$	600	-	-	ns	
Start Condition Hold Time	$T_{HD;STA}$	600	-	-	ns	
Data Setup Time	$T_{SU;DAT}$	100	-	-	ns	
Data Hold Time	$T_{HD;DAT}$	0	-	900	ns	
Setup Time for STOP Condition	$T_{SU;STO}$	600	-	-	ns	
Bus Free Time Between a STOP and START	T_{BUF}	100	-	-	ns	
Capacitive load represented by each bus line	Cb	-	-	400	pF	
Tolerable Spike Width on Bus	T_{SW}	-	-	50	ns	

9.3.3 System Bus Timing for 3-Wire SPI Interface



Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CS Input Setup Time	T_{s0}	50	-	-	ns	
Serial Data Input Setup Time	T_{s1}	50	-	-	ns	
CS Input Hold Time	T_{h0}	50	-	-	ns	
Serial Data Input Hold Time	T_{h1}	50	-	-	ns	
SCL Write Pulse High Width	T_{wh1}	50	-	2000	ns	
SCL Write Pulse Low Width	T_{wl1}	50	-	2000	ns	
SCL Read Pulse High Width	T_{rh1}	300	-	2000	ns	
SCL Read Pulse Low Width	T_{rl1}	300	-	2000	ns	
CS Pulse High Width	T_{w2}	400	-	-	ns	

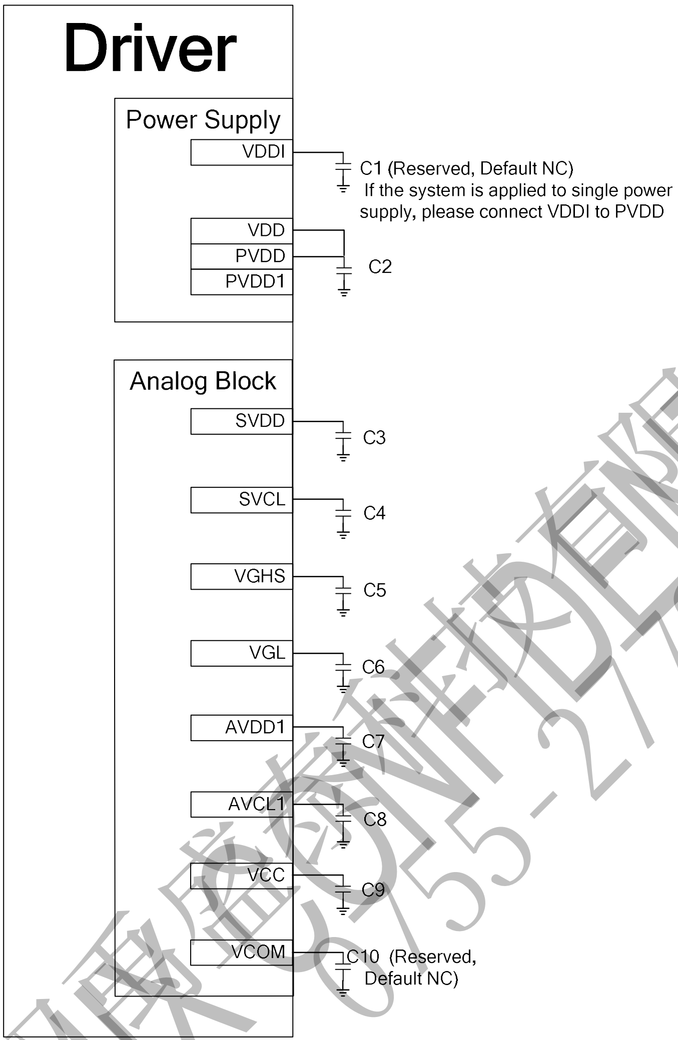
9.3.4 System Bus Timing for RGB Interface



Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK Pulse Duty	Tclk	40	50	60	%	
VSYNC Setup Time	Tvst	10	-	-	ns	
VSYNC Hold Time	Tvhd	10	-	-	ns	
HSYNC Setup Time	Thst	10	-	-	ns	
HSYNC Hold Time	Thhd	10	-	-	ns	
Data Setup Time	Tdsu	10	-	-	ns	
Data Hold Time	Tdhd	10	-	-	ns	
DE Setup Time	Tdest	10	-	-	ns	
DE Hold Time	Tdehd	10	-	-	ns	

10. APPLICATION CIRCUIT

10.1 External Component of Power Circuit



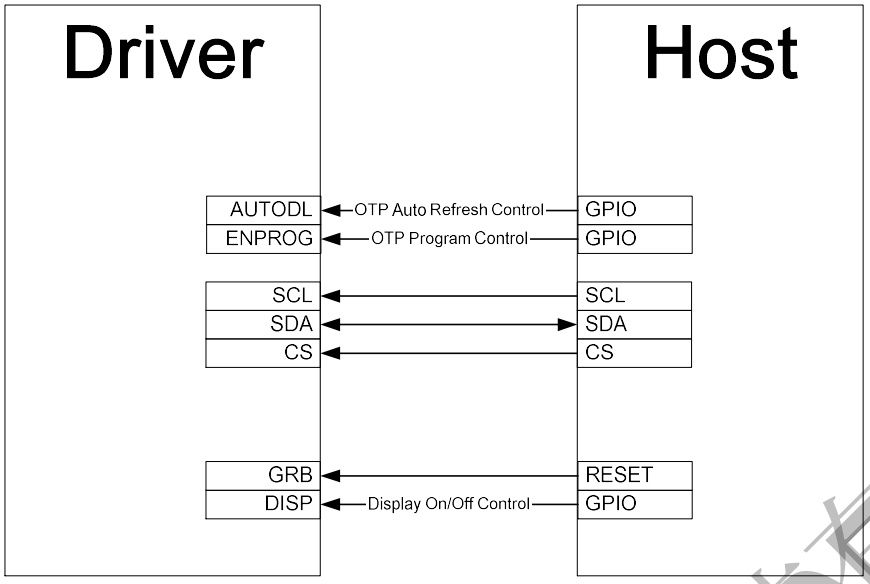
Symbol	Capacitance (uF)	Voltage Proof (V)	Note
C1	2.2	6	Default NC
C2	2.2	6	
C3	2.2	10	
C4	2.2	10	
C5	2.2	25	
C6	2.2	25	
C7	2.2	10	
C8	2.2	10	
C9	2.2	6	
C10	2.2	6	Default NC

Note: 1. Industrial products must add capacitors C2~C9, consumer products must add capacitors C2~C7 and capacitors C8~C9 can be determined by the panel loading, display quality and system power.

2. Capacitor C1 must be added to VDDI when using LVDS interface.

3. Capacitor C10 is required for special case.

10.1.1 OTP Application Circuit



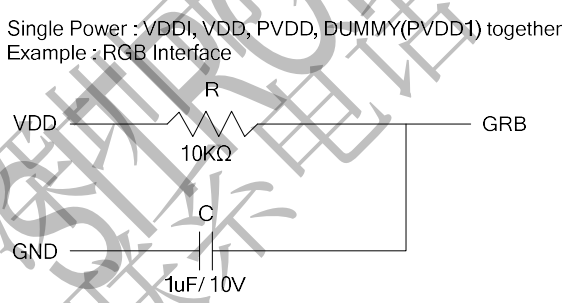
Pin Connection	Description
AUTODL	OTP auto-refresh function control
ENPROG	OTP program function control

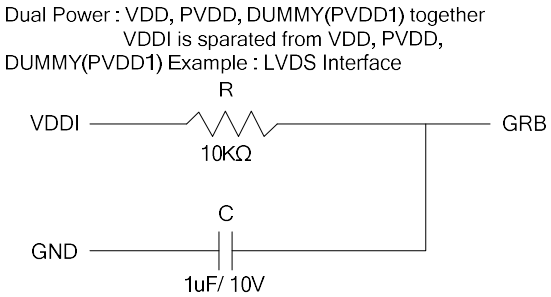
Note: 1. For detailed pin description please refer to section 6.1 PIN DESCRIPTION.

2. AUTODL, ENPROG, SCL, SDA, CS, GRB, DISP are the pins for OTP burning, please wire out to connector or keep reserved testing points.

10.1.2 Reset Application Circuit

The input level of GRB pin can enable/disable power on reset function, please wire out to connector or use the following circuit to reset.





10.2 Input Color Format Application Circuit

10.2.1 Pin Assignment for RGB Interface

Pin		Parallel RGB		
		888	666	565
VSYNC	SYNC Mode	VSYNC	VSYNC	VSYNC
	DE Mode	x	x	x
HSYNC	SYNC Mode	HSYNC	HSYNC	HSYNC
	DE Mode	x	x	x
DE	SYNC Mode	x	x	x
	DE Mode	DE	DE	DE
DCLK		DCLK	DCLK	DCLK
DR0		R0	x	x
DR1		R1	x	x
DR2		R2	R2	x
DR3		R3	R3	R3
DR4		R4	R4	R4
DR5		R5	R5	R5
DR6		R6	R6	R6
DR7		R7	R7	R7
DG0		G0	x	x
DG1		G1	x	x
DG2		G2	G2	G2
DG3		G3	G3	G3
DG4		G4	G4	G4
DG5		G5	G5	G5
DG6		G6	G6	G6
DG7		G7	G7	G7
DB0		B0	x	x
DB1		B1	x	x
DB2		B2	B2	x
DB3		B3	B3	B3
DB4		B4	B4	B4
DB5		B5	B5	B5
DB6		B6	B6	B6
DB7		B7	B7	B7

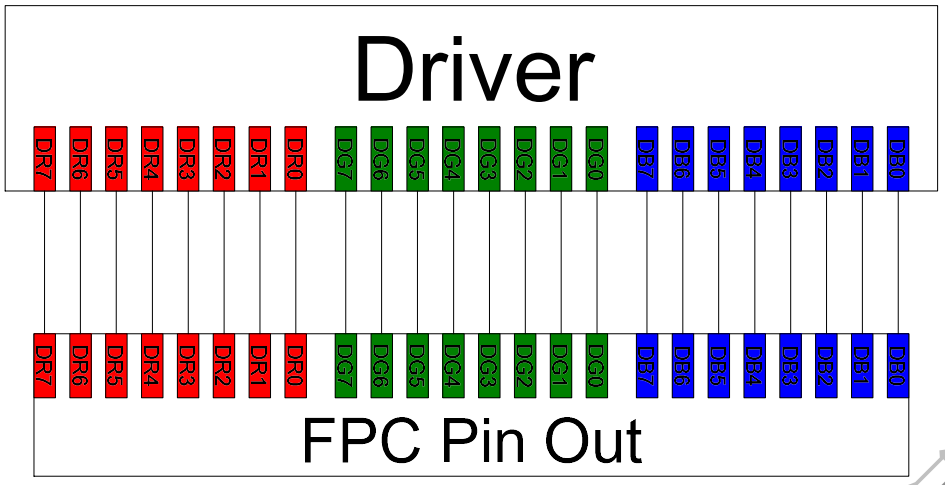
10.2.2 Data Format

Parallel RGB888					
Pin	1st Data	2nd Data	3rd Data	…	Nth Data
DR0	1'R0	2'R0	3'R0	…	N'R0
DR1	1'R1	2'R1	3'R1	…	N'R1
DR2	1'R2	2'R2	3'R2	…	N'R2
DR3	1'R3	2'R3	3'R3	…	N'R3
DR4	1'R4	2'R4	3'R4	…	N'R4
DR5	1'R5	2'R5	3'R5	…	N'R5
DR6	1'R6	2'R6	3'R6	…	N'R6
DR7	1'R7	2'R7	3'R7	…	N'R7
DG0	1'G0	2'G0	3'G0	…	N'G0
DG1	1'G1	2'G1	3'G1	…	N'G1
DG2	1'G2	2'G2	3'G2	…	N'G2
DG3	1'G3	2'G3	3'G3	…	N'G3
DG4	1'G4	2'G4	3'G4	…	N'G4
DG5	1'G5	2'G5	3'G5	…	N'G5
DG6	1'G6	2'G6	3'G6	…	N'G6
DG7	1'G7	2'G7	3'G7	…	N'G7
DB0	1'B0	2'B0	3'B0	…	N'B0
DB1	1'B1	2'B1	3'B1	…	N'B1
DB2	1'B2	2'B2	3'B2	…	N'B2
DB3	1'B3	2'B3	3'B3	…	N'B3
DB4	1'B4	2'B4	3'B4	…	N'B4
DB5	1'B5	2'B5	3'B5	…	N'B5
DB6	1'B6	2'B6	3'B6	…	N'B6
DB7	1'B7	2'B7	3'B7	…	N'B7

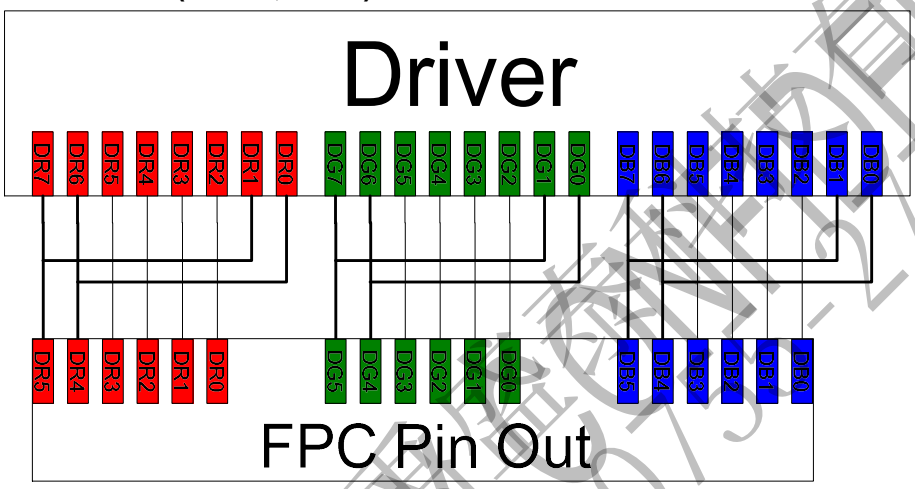
Parallel RGB666					
Pin	1st Data	2nd Data	3rd Data	…	Nth Data
DR0	x	x	x	…	x
DR1	x	x	x	…	x
DR2	1'R0	2'R0	3'R0	…	N'R0
DR3	1'R1	2'R1	3'R1	…	N'R1
DR4	1'R2	2'R2	3'R2	…	N'R2
DR5	1'R3	2'R3	3'R3	…	N'R3
DR6	1'R4	2'R4	3'R4	…	N'R4
DR7	1'R5	2'R5	3'R5	…	N'R5
DG0	x	x	x	…	x
DG1	x	x	x	…	x
DG2	1'G0	2'G0	3'G0	…	N'G0
DG3	1'G1	2'G1	3'G1	…	N'G1
DG4	1'G2	2'G2	3'G2	…	N'G2
DG5	1'G3	2'G3	3'G3	…	N'G3
DG6	1'G4	2'G4	3'G4	…	N'G4
DG7	1'G5	2'G5	3'G5	…	N'G5
DB0	x	x	x	…	x
DB1	x	x	x	…	x
DB2	1'B0	2'B0	3'B0	…	N'B0
DB3	1'B1	2'B1	3'B1	…	N'B1
DB4	1'B2	2'B2	3'B2	…	N'B2
DB5	1'B3	2'B3	3'B3	…	N'B3
DB6	1'B4	2'B4	3'B4	…	N'B4
DB7	1'B5	2'B5	3'B5	…	N'B5

Parallel RGB565					
Pin	1st Data	2nd Data	3rd Data	…	Nth Data
DR0	x	x	x	…	x
DR1	x	x	x	…	x
DR2	x	x	x	…	x
DR3	1'R0	2'R0	3'R0	…	N'R0
DR4	1'R1	2'R1	3'R1	…	N'R1
DR5	1'R2	2'R2	3'R2	…	N'R2
DR6	1'R3	2'R3	3'R3	…	N'R3
DR7	1'R4	2'R4	3'R4	…	N'R4
DG0	x	x	x	…	x
DG1	x	x	x	…	x
DG2	1'G0	2'G0	3'G0	…	N'G0
DG3	1'G1	2'G1	3'G1	…	N'G1
DG4	1'G2	2'G2	3'G2	…	N'G2
DG5	1'G3	2'G3	3'G3	…	N'G3
DG6	1'G4	2'G4	3'G4	…	N'G4
DG7	1'G5	2'G5	3'G5	…	N'G5
DB0	x	x	x	…	x
DB1	x	x	x	…	x
DB2	x	x	x	…	x
DB3	1'B0	2'B0	3'B0	…	N'B0
DB4	1'B1	2'B1	3'B1	…	N'B1
DB5	1'B2	2'B2	3'B2	…	N'B2
DB6	1'B3	2'B3	3'B3	…	N'B3
DB7	1'B4	2'B4	3'B4	…	N'B4

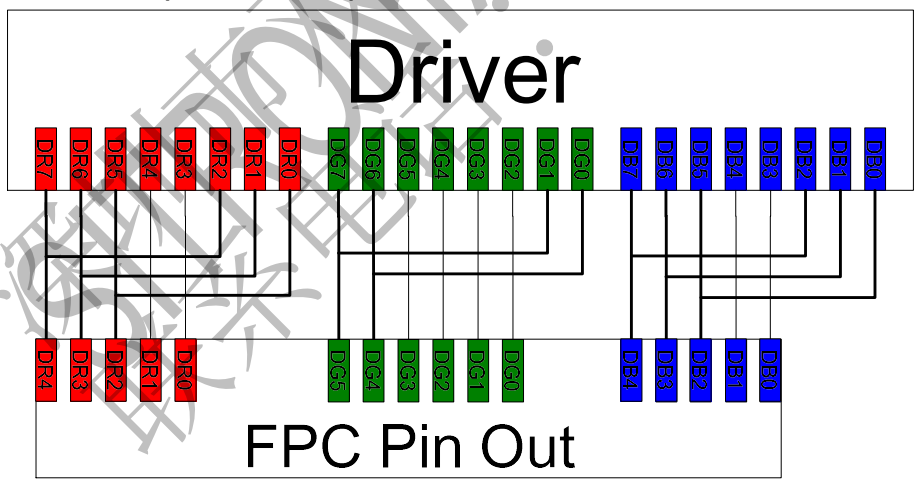
10.2.3 16.7M (R G B, 8 8 8) INPUT COLOR FORMAT



10.2.4 262K (R G B, 6 6 6) INPUT COLOR FORMAT

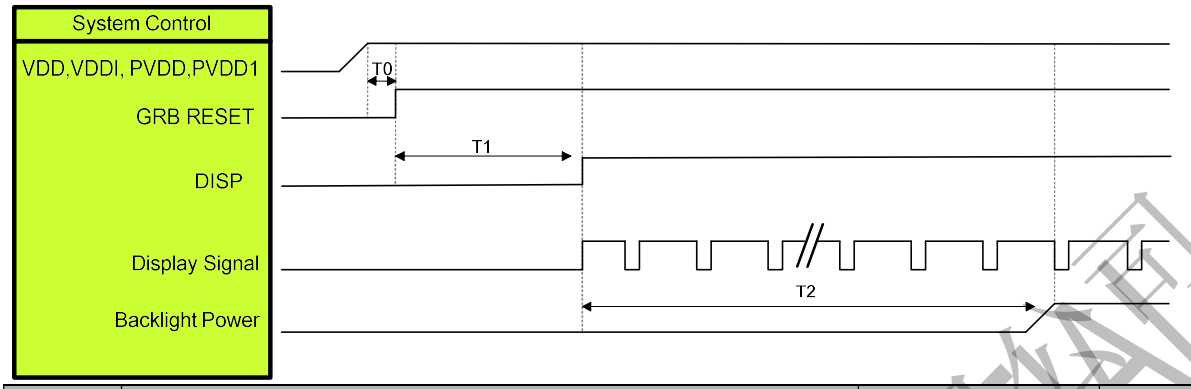


10.2.5 65K (R G B, 5 6 5) INPUT COLOR FORMAT



11. POWER ON/OFF SEQUENCE

11.1 Power On Sequence



Symbol	Description	Min. Time	Unit
T0	System power stability to GRB RESET signal	0	ms
T1	GRB RESET= “High” to DISP=”High”	10	ms
T2	Display Signal output to Backlight Power on	250	ms

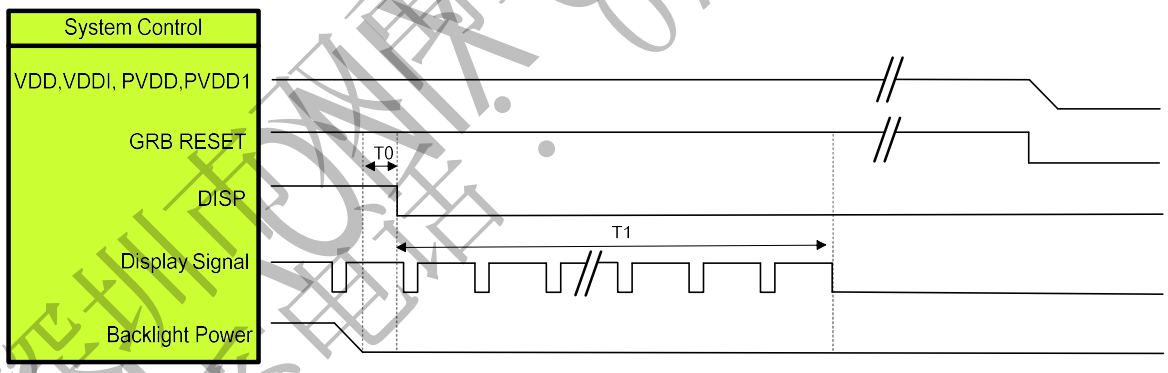
Note :

1. When DISP pull “H” or “L”, IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0]

3: LVDS interface Display signal: DCLK P/N; RX[3:0] P/N

11.2 Power Off Sequence



Symbol	Description	Min. Time	Unit
T0	Backlight Power off to DISP=”Low”	5	ms
T1	DISP=”Low” to IC internal voltage discharge complete	100	ms

Note :

1. When DISP pull “H” or “L”, IC will execute the internal power on or power off procedures. Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.
2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0]
3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N

12. RECOMMENDED PANEL ROUTING RESISTANCE

The recommended wiring resistance values are given below. Resistance values will restrict the maximum current capability of the power supply system and thus must be designed within the recommended range.

Pin Number	Pin Name	Unit: ohm
1	VDDI	<1
2	VDD	<1
3	PVDD	<1
4	PVDD1	<1
5	DGND	<1
6	AGND	<1
7	SGND	<1
8	PGND	<1
9	SVCL	<3
10	SVDD	<3
11	VCOM	<3
12	RGND	<50
13	AVCL1	<50
14	AVDD1	<50
15	GVDD	<50
16	GVCL	<50
17	VGSP	<50
18	VCC	<50
19	VGHS	<50
20	VGL	<50
21	SPI_I2C_SEL	<50
22	CS	<50
23	SDA	<50
24	SCL	<50
25	DISP	<50
26	GRB	<50
27	DCLKN	<50
28	DCLKP	<50
29	DR[7:0]	<50
30	DG[7:0]	<50

Pin Number	Pin Name	Unit: ohm
31	DB[7:0]	<50
32	DE	<50
33	VSYNC	<50
34	HSYNC	<50
35	AUTODL	<50
36	HDIR	<50
37	VDIR	<50
38	INTF	<50
39	SWAP	<50
40	VDPOL	<50
41	HDPOL	<50
42	DCLKPOL	<50
43	ENPROG	<50
44	VPP	<50
45	BIST_EN	<50
46	LVDS_FMT	<50
47	V20	<50
48	ERR_OUT	<50
49	TESTI[14:0]	<50
50	TESTOUT[13:0]	<50
51	DUMMY	<50

13. COLOR FILTER ARRANGEMENT

This IC supports the stripe color filter of dual-gate application. The arrangement of color filter on panel is shown as below.

14. REVISION HISTORY

Revision	Description	Date
V0.1	1st edition	2018/05
V0.2	2nd edition	2018/07
V0.3	3rd edition	2018/12
V0.4	Modify Pad CENTER COORDINATES (P9)	2018/12
V0.4a	Remove LVDS Function	2019/04
V0.4b	Modify features description (P6) Modify command description 19h/ 1Bh/1Ch (P58, P59)	2019/05
V0.4c	Modify note description (P71)	2019/06
V0.4d	Modify application circuit (P78)	2019/06
V0.4e	Modify Application Range of Power Supply Modify Bump Dimension Modify Typing Error	2019/08
0.6a	Add LVDS Function Add Input Color Format Application Circuit	2020/03
0.6b	Modify the Diagram of SYNC-DE Mode (P51) Modify the Timing of RGB Interface (P83) Modify External Component of Power Circuit (P84)	2020/04
0.7	Modify VCOM and OTP Description (P6) Add GRB Pin and Modify Table Format (P45) Modify the Timing Table of RGB Interface (P53) Modify VCOM Offset (05h) Description (P73) Modify Command Description 66h/ 67h/ 68h/ 68h/ 69h/ 6Ah/ 6Bh/ 6Ch (P74,P75) Add Backlight Description (P76) Add IC Temperature and Display Effect Description (P76) Modify DC Characteristics and Operation Current(P77) Add OTP Application Circuit (P85) Add Reset Application Circuit (P85) Add DISP Description of Power on/off Sequence (P91)	2020/06
1.0	Modify Application Product Description (P6) Modify the SYNC Mode, SYNC-DE Mode, DE Mode Diagrams (P50~P52) Modify System Bus Timing for 3-Wire SPI Interface (P81) Modify External Component of Power Circuit (P84)	2020/10