ST7315

128 x 64 Dot Matrix OLED/PLED

Segment/Common Driver with Controller

Datasheet

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Sitronix Technology Corporation

LIST OF CONTENT

1. GENERAL DESCRIPTION

ST7315 is a single-chip dot matrix OLED/PLED driver which incorporates controller and common/segment drivers. It contains 128-segment and 64-common driver circuit. This chip can be connected directly to a microprocessor with 8-bit parallel interface, 4-line serial interface (SPI-4), 3-line serial interface (SPI-3) and I2C serial interface. Display data sent from MPU is stored in the internal Display Data RAM (DDRAM) of 128x64 bits. It performs the display data read/write operation without external operating clock, and the power consumption can be minimized. In addition, since all necessary oscillation circuit and low power consumption circuit for OLED/PLED system are built-in, ST7315 constructs an OLED/PLED display system with the fewest components.

2. FEATURES

- Display Maximum Resolution:
- - Capacity: 128-segment * 64-common
- Microprocessor Interface
  - 8-bit 8080 and 6800 interface support
  - 3-wire SPI and 4-wire SPI serial interface
  - I^2C interface
- On-Chip Power System
  - VDD: 2.7V ~ 3.3V (TYP)
  - VBAT: 2.7V ~ 4.2V (TYP)
- Wide Supply Voltage Range
  - VOLED (Internal Power): 6.0V (VBAT=2.7V~4.2V)
  - VOLED (Internal Power): 7.5V~ 9.0V (VBAT=2.7V~4.2V)
  - VOLED (External Power): 6.0V~16.5V (VBAT=Floating)
  - VCOMH: 0.65*VOLED ~ 0.83*VOLED
  - Segment maximum source current: 240uA
  - Common maximum sink current: 30mA
- On Chip Build-In Circuits
  - Charge pump power circuit
  - Timing controller
  - Internal OSC
  - Power on reset (POR)
- Internal or external I_{REF} selection
- Crosstalk compensation
- Built-in Multi-OTP Programming Circuit
  - Internal VPP power supply
  -Contrast Adjustment
  -2bit ID program
- Temperature Range: -40℃ to 85℃
- Package: COG
- Part Number: ST7315-G5
- **Design for consumer applications; this product is not designed for use in cars, motorcycles, marine equipment, aircraft equipment, military equipment and other applications in extreme environment.**

3. COMMUNICATION INTERFACE

3.1 Microprocessor Interface

3.1.1 CSB Select Input

CSB pin is s used for chip selection. ST7315 can interface with an MPU when CSB is "L". If CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In serial interface (3-Line, 4-Line SPI and I^2C), the internal shift register and serial counter are reset when CSB is “H”.

3.1.2 Parallel / Serial Interface

ST7315 has five types of interface for kinds of MPU. The MPU interface is selected by IF[2:0] pins as shown in Table1.

Table 1 Parallel/Serial Interface Mode

Type	IF2	IF1	IF0	Interface mode
Serial	L	L	L	4-line serial interface
	L	L	H	3-line serial interface
	L	H	L	I^2C serial interface
Parallel	H	H	L	8bit 8080-series MPU mode
	H	L	L	8bit 6800-series MPU mode

3.1.3 Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by IF[2:0] as shown in Table 2. The data transfer type is determined by signals of A0, ERD and RWR as shown in Table 3.

Table 2 Microprocessor Selection for Parallel Interface

IF1	IF0	CSB	A0	ERD	RWR	D[7:0]	MPU Interface
H	L	CSB	A0	E	R/W	D[7:0]	6800-series
H	H			/RD	/WR		8080-series

Table 3 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Internal status read
L	H	L	H	L	Writes to internal register (instruction)

3.1.4 Serial Interface

Interface	CSB	A0	ERD	RWR	D[7:0]
3-Line SPI	CSB	--	--	--	D[0]= SCL, D[1:2]=SDA, D[3:7]= GND
4-Line SPI	CSB	A0	--	--	D[0]= SCL, D[1:2]=SDA, D[3:7]= GND
I^2C interface	L	H/ L	--	--	D[0]=SCL, D1=SDA_IN, D[2]=SDA_OUT, D[7:3]=GND, A0=SA[0]. Refer to I^2C interface.

Note:

1. The un-used pins are marked as "--" and should be fixed to "H" by VDD.
2. The option setting to be "H" should connect to VDD.
3. The option setting to be "L" should connect to DGND.

3.1.5 3-Line Serial Interface

The 3-Line SPI (9-bit) uses 3 pins (CSB, SDA & SCL) to communicate with MPU. When CSB is "L", IC is active and the SDA and SCL pins are enabled. Serial data is latched at the rising edge of serial clock. The internal shift register collects serial bits and reformat them into 8-bit data after the last (9^{th}) clock. After CSB returns to "H", IC is inactive and the internal shift register and counter are reset. The parameter/command indicator is the "A0" bit at the 1^{st} bit of each 9-bit serial data.

In 3-Line interface, A0 pin is not available. The 1^{st} output bit defines command byte or parameter byte.

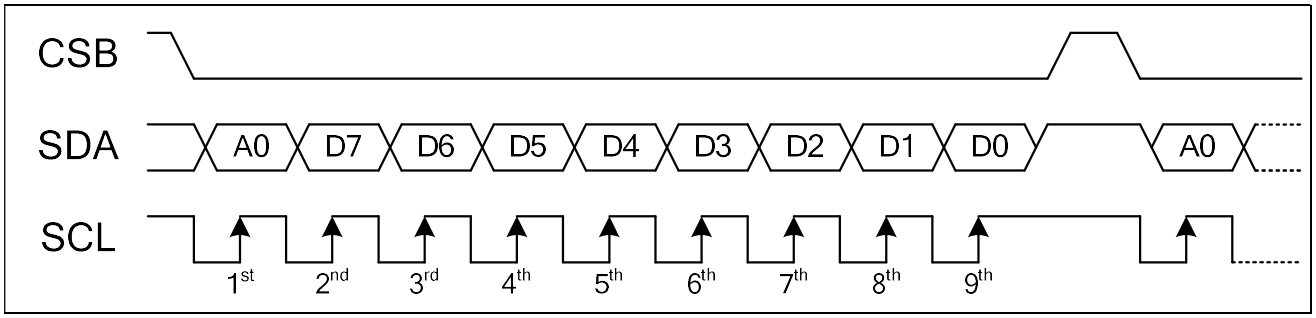


Figure 1 Write Operation of 3-Line SPI

After entering the “Read Status” instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.

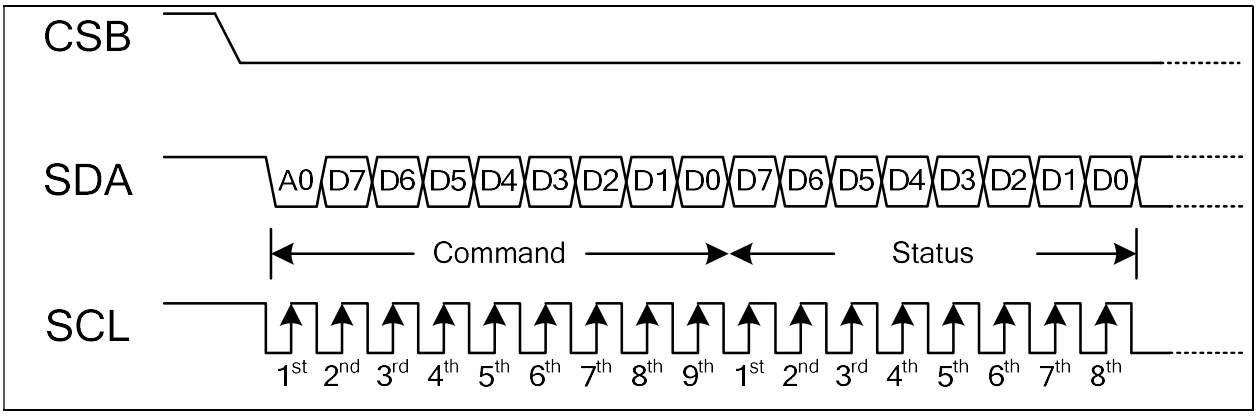


Figure 2 Read Operation of 3-Line SPI

3.1.6 4-Line Serial Interface

ST7315 is active when CSB is “L”, and serial data (SDA) and serial clock (SCL) inputs are enabled. When CSB is “H”, ST7315 is not active, and the internal 8-bit shift register and 3-bit counter are reset. The DDRAM column address pointer will be increased by one automatically after writing each byte of DDRAM.

The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. Serial data (SDA) is latched at the rising edge of serial clock (SCL). After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

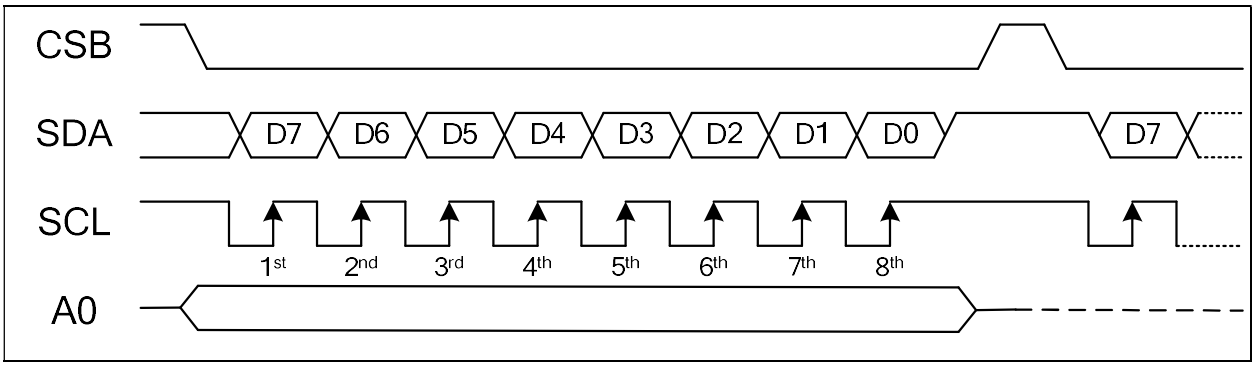


Figure 3 Write Operation of 4-Line SPI

After entering the “Read Mode” to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.

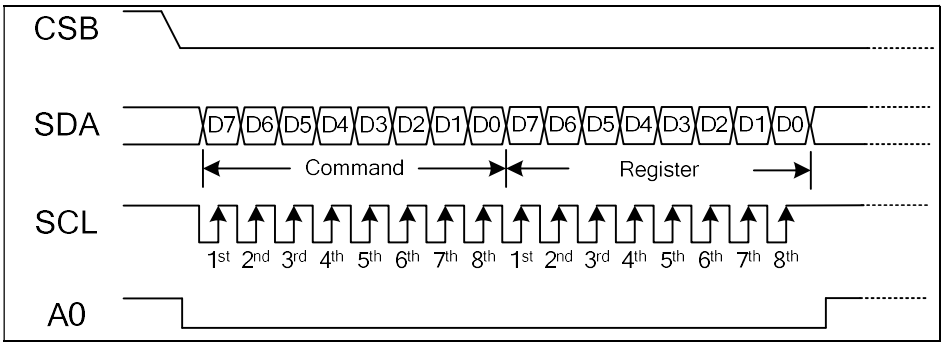


Figure 4 Read Operation of 4-Line SPI

3.1.7 I²C Serial Interface

The I²C Interface is bi-directional two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines have built-in pull up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated as follows.

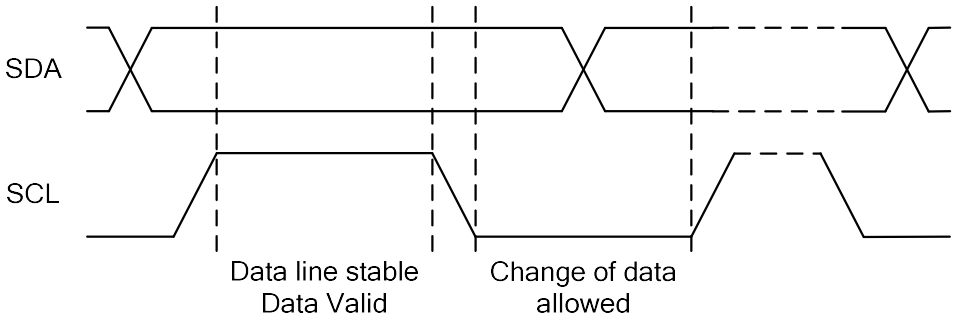


Figure 5 Bit Transfer

START and STOP Conditions

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated as follows.

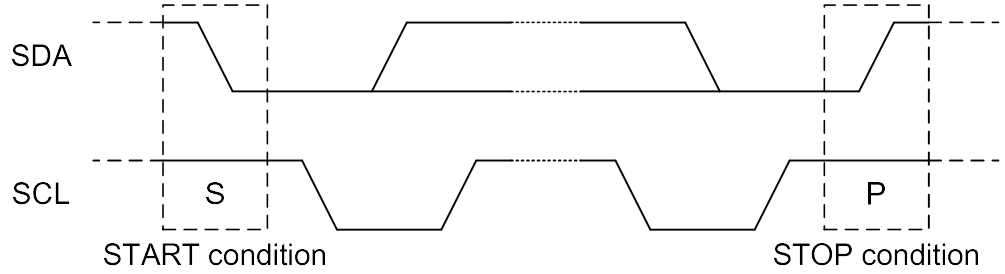


Figure 6 Definitions of START and STOP Condition

System Configuration

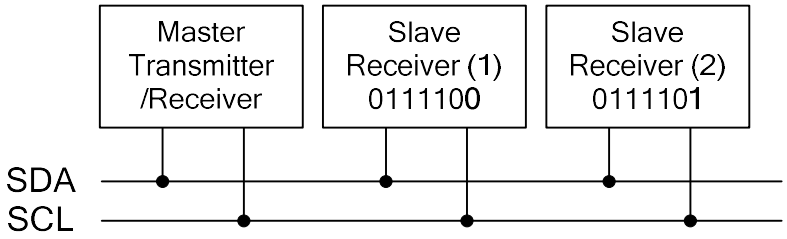


Figure 7 System Configuration

The system configuration is illustrated above and some word-definitions are explained below:

a. Transmitter: the device which sends the data to the bus.

b. Receiver: the device which receives the data from the bus.

c. Master: the device which initiates a transfer generates clock signals and terminates a transfer.

d. Slave: the device which is addressed by a master.

e. Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.

f. Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.

g. Synchronization: procedure to synchronize the clock signals of two or more devices.

Acknowledgment

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I²C Interface is illustrated as follows.

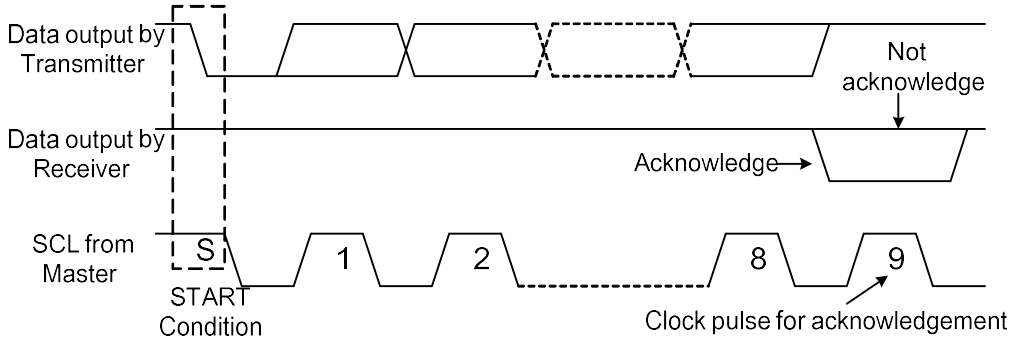
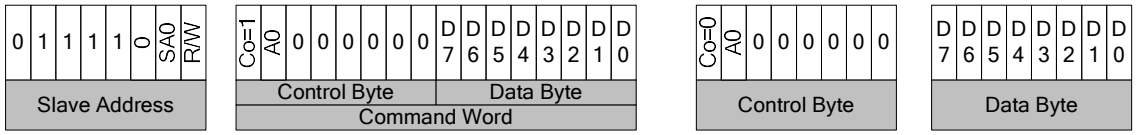


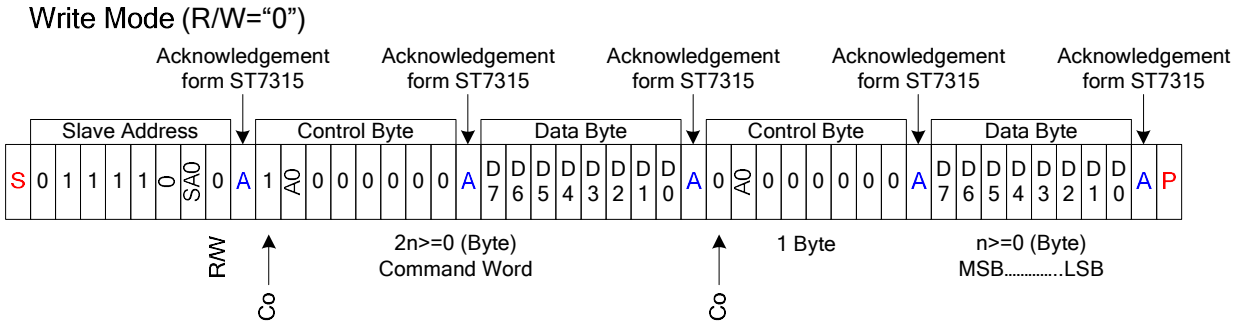
Figure 8 Acknowledgement of I²C Interface

I2C Interface Protocol

The driver supports command/data write to addressed slaves on the bus. Before any data is transmitted on the I²C Interface, the device which should respond is addressed first. The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master. The register write/ read transference sequence are described as follows.





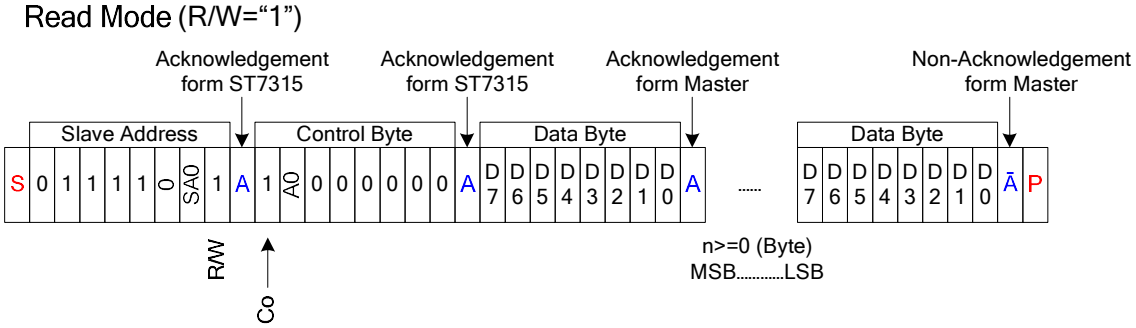


Figure 9 I²C Interface Protocol

3.2 Data Transfer

ST7315 uses bus holder and internal data bus for data transfer with MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in **Figure 10** And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in **Figure 11**. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

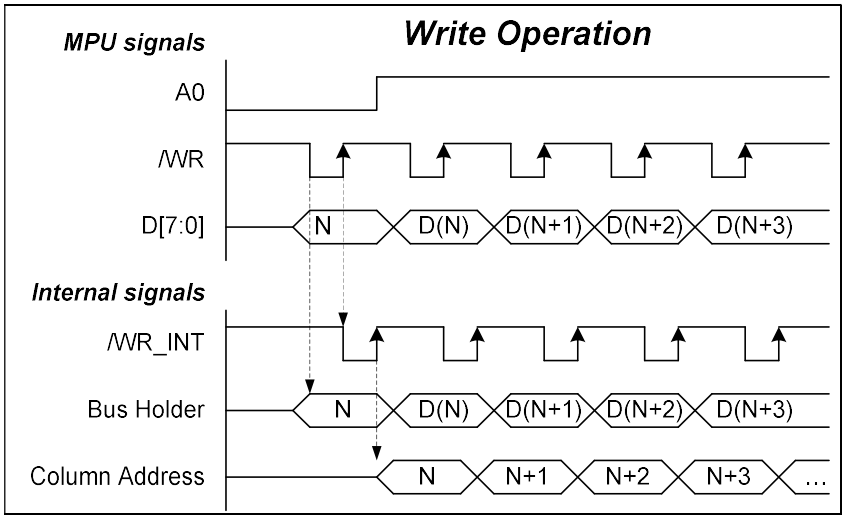


Figure 10 Data Transfer: Write

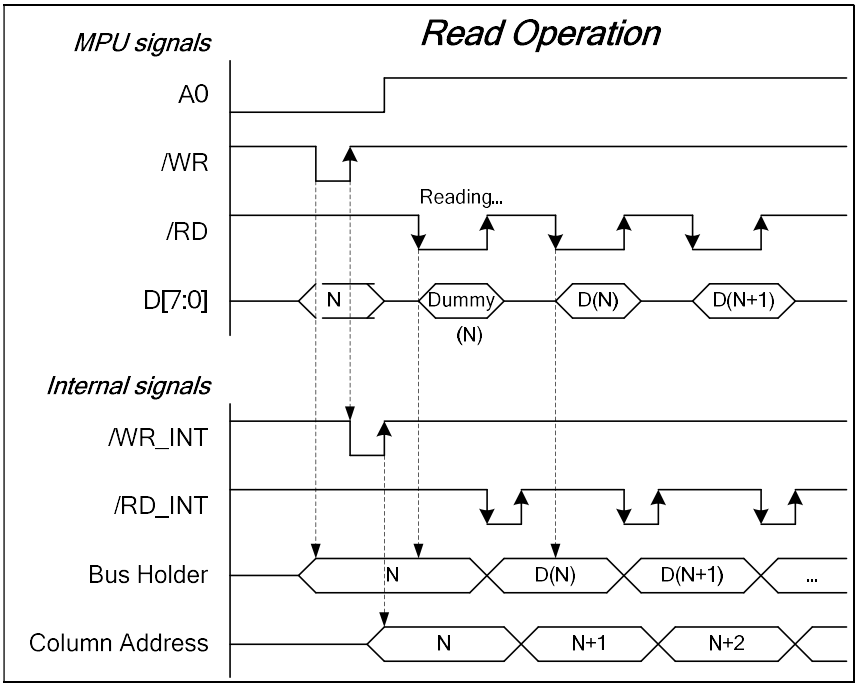


Figure 11 Data Transfer: Read

3.3 Display Data RAM (DDRAM)

ST75315 is built-in a RAM with 128X64 bit capacity which stores the display data. The display data RAM (DDRAM) store the dot data of the panel. It is an addressable array with 128 columns by 64 rows (8-page). The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified (please refer to Figure 12 for detailed illustration). The rows are divided into: 8 pages (Page-0 ~ Page-7) each with 8 lines (for COM0~63). The display data (D7~D0) corresponds to the panel common-line direction and D0 is on top. All pages can be accessed through D[7:0] directly. Refer to Figure 13 for detailed illustration. The microprocessor can write to and read from DDRAM by the I/O buffer. Since the OLED controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the screen flicker or data-conflict.

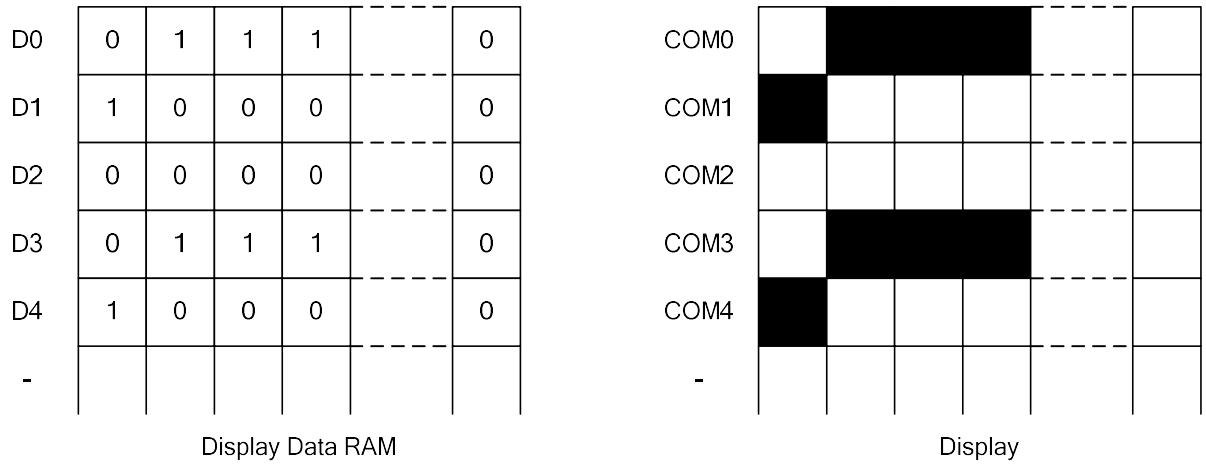


Figure 12 DDRAM Mapping Modes

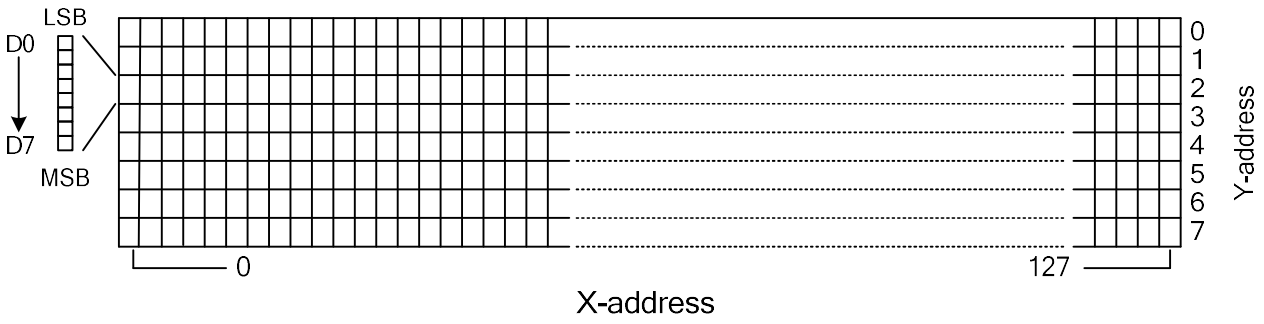


Figure 13 DDRAM Format

3.3.1 Addressing

Data is downloaded into the Display Data RAM matrix in ST7315 as byte-format. The Display Data RAM has a matrix of 128 by 64 bits. The address ranges are: X=0~127 (column address), Y=0~7 (page address). Addresses outside these ranges are not allowed.

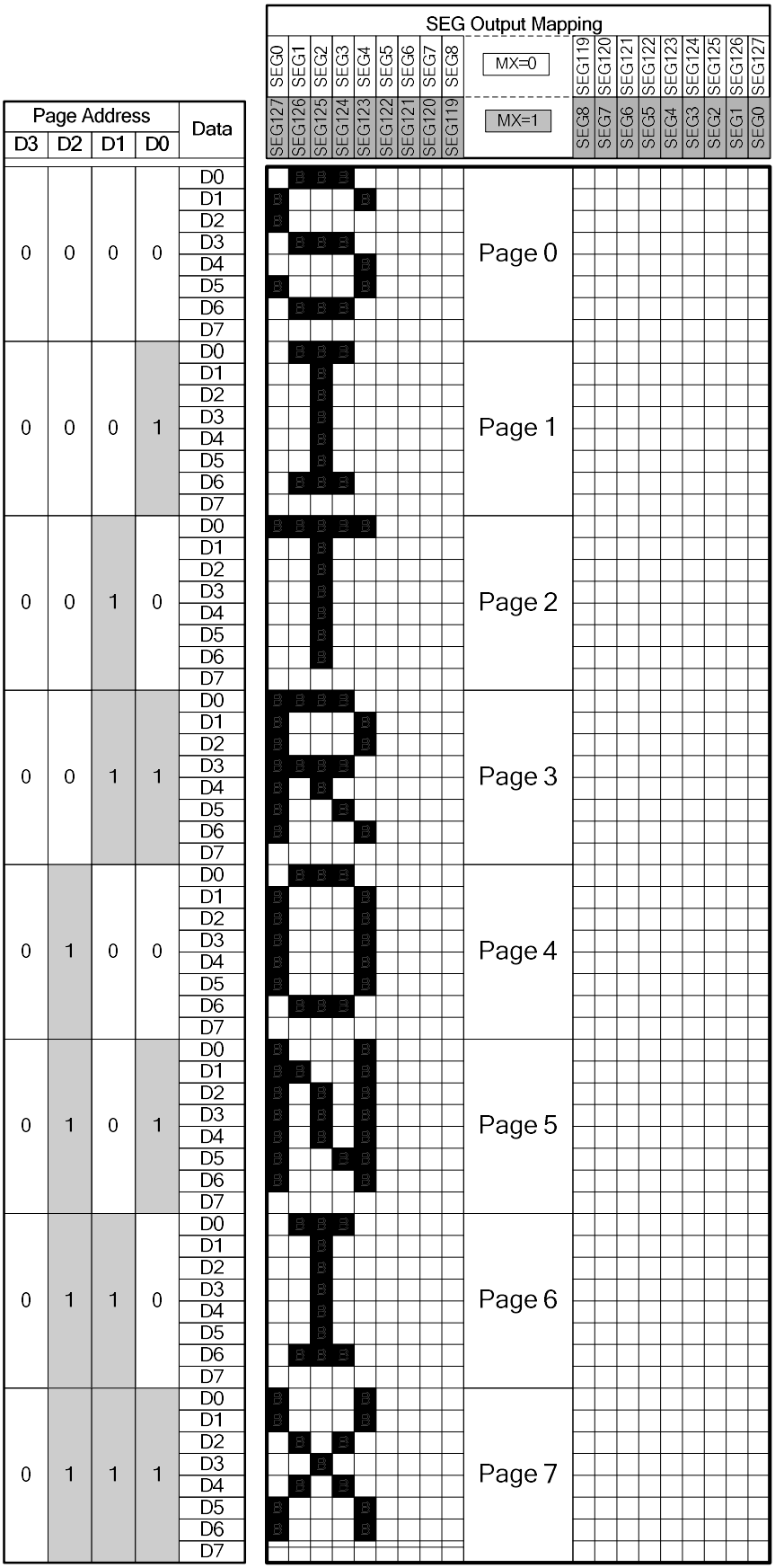
3.3.2 Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates 3-bit Page Address Register which can be modified by the “Page Address Set” instruction only. The Page Address must be set before accessing DDRAM content.

3.3.3 Column Address Circuit

The column address of DDRAM is specified by the Column Address Set command. Column Address Circuit has 8-bit preset counter that provides Column Address to the Display Data RAM (DDRAM). This allows MPU accessing DDRAM content continuously. The column address is automatically incremented from the start up to the end column. During auto-increment, the column address returns to the column start address as the end column is reached.
Furthermore, Register MX and MY makes it possible to invert the relationship between the DDRAM and the outputs (COM/SEG).

3.4 DDRAM SEG Output Mapping



3.5 Partial Display

ST7315 realizes the Partial Display function with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on panel, driving duty is programmable via the instruction. Moreover, built-in power supply circuits are controlled by the instruction for adjusting the driving voltages.

3.6 Power System

The built-in power circuits generate the voltage and current which are necessary to drive the OLED. It consumes low power with the fewest external component.

I_{SEG} Driving Current

This is used to derive the incoming power sources into the different levels of internal use voltage and current.

1. VOLED is the most positive voltage supply.
2. VCOMH is the common deselected level. It is internally regulated.
3. PGND is the ground path of the analog and panel current.
4. IREF is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current is:

I_{SEG} = Contrast / 256 x IREF x scale factor in which the contrast (0~255) is set by Set Contrast command 81h; and the scale factor is 8 by default.

When external IREF is used, the magnitude of IREF is controlled by the value of resistor, which is connected between IREF pin and VSS. It is recommended to set IREF to 30±2uA so as to achieve I_{SEG} = 240uA at maximum contrast 255

4. RESET CIRCUIT

Setting RSTB pin to “L” can initialize internal function. While RSTB is “L”, no instruction can be accepted. RSTB pin must connect to the reset pin of MPU and initialization by RSTB pin is essential before operating. After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write a display pattern) before turning the Display ON.

The default values of registers are listed below:

Procedure	Hardware Reset
DDRAM Content	No Change
Data Address Mode	DA[1:0]=[1, 0]
Page Address 1	Y[2:0]=7h
Set Page Address 2	PS[2:0]=0h, PE[2:0]=7h
Set Column Address 1	X[6:0] = 0h
Set Column Address 2	CS[6:0]=00h, CE[6:0]=7Fh
Start Line	SL[5:0]=00h
Set Contrast	EV[7:0]=7Fh
SEG Direction	MX=0h
All Pixel On	AP=0h
Inverse Display	INV=0h
Set Duty	DT=3Fh
Internal Iref	EXT=0h; IREF=0h
Display ON/OFF	DSP=0
COM Direction	MY=0h
Set COM0	C[5:0]=0h
Frequency Rate	FR[3:0]=8h, DK[3:0]=0h
Pre-Charge Period	P1[3:0]=2h, P2[3:0]=2h
COM Pin Configuration	ALT=1h; VDIR=0h
Set V_{COMH}	VC[1:0]=2h
Power Control	VB=0h, CP[1:0]=0h
Horizontal Scroll Setting	HS=0h; SPS[2:0]=0h; ST[2:0]=0h; SPE[2:0]=0h; SCS[6:0]=0h; SCE[6:0]=7Fh
Vertical and Horizontal Scroll Setting	VHS[1:0]=0h; SPS[2:0]=0h; ST[2:0]=0h; SPE[2:0]=0h; SVO[5:0]=0h; SCS[6:0]=0h; SCE[6:0]=7Fh, SHC=0
Vertical Scroll Area	SVF[5:0]=0h; SVN[6:0]=3Fh
Content Scroll Setup	HS=0h; SPS[2:0]=0h; SPE[2:0]=0h; SCS[6:0=0h; SCE[6:0]=7Fh
Set Fade Out and Blinking	FO[3:0]=0h; FB[1:0]=0h

Procedure	Hardware Reset
Zoom In	ZI=0h
Set Contrast Offset	Sign=0h; OF[5:0]=0h

5. REGISTER LIST

5.1 Instruction Table

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Set Data Address Mode	0	0	0	0	1	0	0	0	0	0	Set the data filling method
	0	0	0	0	0	0	0	0	DA1	DA0	
Set Page Address 1	0	0	1	0	1	1	0	Y2	Y1	Y0	Set page address : 0h≦Y≦7h This command is only for page address mode
Set Page Address 2	0	0	0	0	1	0	0	0	1	0	Set page address : Starting page address : 0h≦PS≦7h Ending page address : 0h≦PE≦7h
	0	0	0	0	0	0	0	PS2	PS1	PS0	
	0	0	0	0	0	0	0	PE2	PE1	PE0	
Set Column Address 1	0	0	0	0	0	0	X3	X2	X1	X0	Set column address : 00h≦X≦7Fh
	0	0	0	0	0	1	0	X6	X5	X4	
Set Column Address 2	0	0	0	0	1	0	0	0	0	1	Set column address : Starting column address : 00h≦CS≦7Fh Ending column address : 00h≦CE≦7Fh
	0	0	0	CS6	CS5	CS4	CS3	CS2	CS1	CS0	
	0	0	0	CE6	CE5	CE4	CE3	CE2	CE1	CE0	
Set Start Line	0	0	0	1	SL5	SL4	SL3	SL2	SL1	SL0	Specify line address for the 1st display line of RAM 00h≦SL≦3Fh
Set Contrast	0	0	1	0	0	0	0	0	0	1	Set contrast level
	0	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=0: SEG0 to SEG127 MX=1: SEG127 to SEG0
All Pixel On	0	0	1	0	1	0	0	1	0	AP	AP=0: Normal display AP=1: Set all pixel on

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Inverse Display	0	0	1	0	1	0	0	1	1	INV	Set inverse display INV=0: Normal display INV=1: Inverse display
Set Duty	0	0	1	0	1	0	1	0	0	0	Set display duty 00h≦DT≦3Fh
	0	0	0	0	DT5	DT4	DT3	DT2	DT1	DT0	
Set Internal IREF	0	0	1	0	1	0	1	1	0	1	Iref: Set Iref value EXT: external Iref on/off
	0	0	0	0	Iref	EXT	0	0	0	0	
Display ON/OFF	0	0	1	0	1	0	1	1	1	DSP	Set LCD Display DSP=0: Display off DSP=1: Display on
COM Direction	0	0	1	1	0	0	MY	0	0	0	Set output direction of COM MY=0: COM0 to COM[N-1] MY=1: COM[N-1] to COM0 Where N is the Multiplex ratio
Set COM0	0	0	1	1	0	1	0	0	1	1	Specify a COM pin to be COM0
	0	0	-	-	C5	C4	C3	C2	C1	C0	
Set Frame Rate	0	0	1	1	0	1	0	1	0	1	DK[3:0]: DCLK dividing ratio FR[3:0]: Frame rate setting
	0	0	FR3	FR2	FR1	FR0	DK3	DK2	DK1	DK0	
Pre-Charge Period	0	0	1	1	0	1	1	0	0	1	P1[3:0]: Set DCLK in the phase 1 period P2[3:0]: Set DCLK in the phase 2 period
	0	0	P23	P22	P21	P20	P13	P12	P11	P10	
COM Pin Configuration	0	0	1	1	0	1	1	0	1	0	ALT: Alternative COM pins configuration VDIR: COM left and right swap
	0	0	0	0	VDIR	ALT	0	0	1	0	
Set V_{COMH}	0	0	1	1	0	1	1	0	1	1	Set V_{COMH} voltage
	0	0	0	0	VC1	VC0	0	0	0	0	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Power Control	0	0	1	0	0	0	1	1	0	1	CP[1:0]: Set LCD driving voltage VB: Control built-in power charge pump voltage
	0	0	CP1	0	0	1	0	VB	0	CP0	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Horizontal Scroll Setting	0	0	0	0	1	0	0	1	1	HS	HS: Horizontal scroll direction SPS[2:0]: Set start page address ST[2:0]: Set time interval between each scroll step SPE[2:0]: Set end page address SCS[6:0]: Set column start address SCE[6:0]: Set column end address
	0	0	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	SPS2	SPS1	SPS0	
	0	0	0	0	0	0	0	ST2	ST1	ST0	
	0	0	0	0	0	0	0	SPE2	SPE1	SPE0	
	0	0	0	SCS6	SCS5	SCS4	SCS3	SCS2	SCS1	SCS0	
	0	0	0	SCE6	SCE5	SCE4	SCE3	SCE2	SCE1	SCE0	
Vertical and Horizontal Scroll Setting	0	0	0	0	1	0	1	0	VHS1	VHS0	VHS[1:0]: Scroll direction SHC: Horizontal scroll on/off SPS[2:0]: Set start page address ST[2:0]: Set time interval between each scroll step SPE[2:0]: Set end page address SVO[5:0]: Vertical scroll offset SCS[6:0]: Set column start address SCE[6:0]: Set column end address
	0	0	0	0	0	0	0	0	0	SHC	
	0	0	0	0	0	0	0	SPS2	SPS1	SPS0	
	0	0	0	0	0	0	0	ST2	ST1	ST0	
	0	0	0	0	0	0	0	SPE2	SPE1	SPE0	
	0	0	0	0	SVO5	SVO4	SVO3	SVO2	SVO1	SVO0	
	0	0	0	SCS6	SCS5	SCS4	SCS3	SCS2	SCS1	SCS0	
	0	0	0	SCE6	SCE5	SCE4	SCE3	SCE2	SCE1	SCE0	
Stop Scroll	0	0	0	0	1	0	1	1	1	0	Set scroll stop
Start Scroll	0	0	0	0	1	0	1	1	1	1	Set scroll start

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Vertical Scroll Area	0	0	1	0	1	0	0	0	1	1	SVF[5:0]: Set number of rows in top fixed area SVN[6:0]: Set number of rows in scroll area
	0	0	0	0	SVF5	SVF4	SVF3	SVF2	SVF1	SVF0	
	0	0	0	SVN6	SVN5	SVN4	SVN3	SVN2	SVN1	SVN0	
Content Scroll Setup	0	0	0	0	1	0	1	1	0	HS	HS: Scroll horizontal direction SPS[2:0]: Set start page address SPS[2:0]: Set start page address SPE[2:0]: Set end page address SCS[6:0]: Set column start address SCE[6:0]: Set column end address
	0	0	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	SPS2	SPS1	SPS0	
	0	0	0	0	0	0	0	0	0	1	
	0	0	0	0	0	0	0	SPE2	SPE1	SPE0	
	0	0	0	SCS6	SCS5	SCS4	SCS3	SCS2	SCS1	SCS0	
	0	0	0	SCE6	SCE5	SCE4	SCE3	SCE2	SCE1	SCE0	
Set Fade Out and Blinking	0	0	0	0	1	0	0	0	1	1	FO[3:0]: Set time interval between each fade step FB[1:0]: Enable fade out or blinking mode
	0	0	0	0	FB1	FB0	FO3	FO2	FO1	FO0	
Zoom In	0	0	1	1	0	1	0	1	1	0	IN=0: Zoom in disable IN=1: Zoom in enable
	0	0	0	0	0	0	0	0	0	ZI	
Clean DDRAM	0	0	1	0	0	1	0	1	0	0	Clear Ram to all 0
	0	0	0	1	0	1	1	0	1	0	
	0	0	1	0	0	0	0	0	0	0	
	0	0	1	0	0	1	0	1	0	0	
	0	0	1	0	1	0	0	1	0	1	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Crosstalk Compensation	0	0	1	0	0	1	0	1	0	0	Crosstalk Compensation ON
	0	0	0	1	0	1	1	0	1	0	
	0	0	0	0	0	0	0	0	0	0	
	0	0	0	0	1	1	0	0	0	0	
	0	0	0	0	0	0	0	1	0	0	
	0	0	1	1	0	0	0	0	0	0	
	0	0	1	0	0	0	0	0	0	0	
	0	0	1	0	0	1	0	1	0	0	
	0	0	1	0	1	0	0	1	0	1	
Deep Sleep IN	0	0	1	0	0	1	0	1	0	0	Deep Sleep IN
	0	0	0	1	0	1	1	0	1	0	
	0	0	1	0	0	0	0	0	1	0	
	0	0	0	1	0	1	0	1	0	1	
	0	0	0	1	0	1	0	1	0	1	
	0	0	1	0	1	0	1	0	1	0	
	0	0	1	0	1	0	1	0	1	0	
Set Contrast Offset	0	0	1	0	0	1	0	1	0	0	Set Contrast Offset for OTP Program value
	0	0	0	1	0	1	1	0	1	0	
	0	0	1	1	1	0	1	0	0	1	
	0	0	0	Sign	OF5	OF4	OF3	OF2	OF1	OF0	
	0	0	1	0	0	1	0	1	0	0	
	0	0	1	0	1	0	0	1	0	1	

Command 2 (Read Register Table)											
INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Read Program Times	0	0	1	0	0	1	0	1	0	0	Remain Program times Register (Read Only)
	0	0	0	1	0	1	1	0	1	0	
	0	0	0	0	0	0	0	1	1	1	
	0	1	0	0	IDtr2	IDtr1	IDtr0	EVtr2	EVtr1	EVtr0	
	0	0	1	0	0	1	0	1	0	0	
	0	0	1	0	1	0	0	1	0	1	
Read ID	0	0	1	0	0	1	0	1	0	0	ID Register (Read Only)
	0	0	0	1	0	1	1	0	1	0	
	0	0	0	0	0	0	1	1	1	1	
	0	1	ID1	D0	0	0	0	0	0	0	
	0	0	1	0	0	1	0	1	0	0	
	0	0	1	0	1	0	0	1	0	1	

OTP Register List											
INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
ID and Contrast Program times	0	0	0	0	0	0	0	0	0	0	Only for OTP Programing
	0	0	0	0	IDtw2	IDtw1	IDtw0	EVtw2	EVtw1	EVtw0	
OTP ID Program	0	0	0	0	0	0	0	1	1	1	Program ID
	0	0	0	0	ID2[1:0]		ID1[1:0]		ID0[1:0]		
Contrast Offset	0	0	0	0	0	0	0	1	0	0	Contrast Offset0
	0	0	0	Sign	OF5	OF4	OF3	OF2	OF1	OF0	

Note : 1. Symbol “-” means this bit can be H“ or “L”

2. Do not use instructions not listed in the table.

5.2 Instruction Table

5.2.1 Set Data Address Mode

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0	0	0
0	0	0	0	0	0	0	0	DA1	DA0

DA1	DA0	Description
0	0	Horizontal Address Mode
0	1	Vertical Address Mode
1	0	Page Address Mode
1	1	Reserve

5.2.2 Set Page Address 1

This instruction is used to define the Y address of the display RAM. This command is only for page address mode.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	0	Y2	Y1	Y0

Y2	Y1	Y0	Description
0	0	0	Page0
0	0	1	Page1
:	:	:	:
1	1	0	Page6
1	1	1	Page7

5.2.3 Set Page Address 2

This instruction is used to define area of DDRAM where MCU can access. The page address is automatically increased by one(+1) after column address counter is over CE[6:0]. The page address will return to starting page address PS[2:0] immediately when page address increases one over the ending page address PE[2:0]. The PS[2:0] setting must be equal to or less than PE[2:0]. When PS[2:0] or PE[2:0] is larger than 7h,out of DDRAM range will be ignored. This command is only for horizontal or vertical addressing mode.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0	1	0
0	0	0	0	0	0	0	PS2	PS1	PS0
0	0	0	0	0	0	0	PE2	PE1	PE0

PS2	PS1	PS0	Description
0	0	0	Page0
0	0	1	Page1
:	:	:	:
1	1	0	Page6
1	1	1	Page7

PE2	PE1	PE0	Description
0	0	0	Page0
0	0	1	Page1
:	:	:	:
1	1	0	Page6
1	1	1	Page7

5.2.4 Set Column Address 1

This instruction is used to define the X address of the display RAM. The column address is automatically increased by one after each byte of display data access. The X[6:0] setting must be less than or equal to 7Fh. If X[6:0] setting is larger than 7Fh, out of DDRAM range will be ignored. This command is only for page address mode.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	X3	X2	X1	X0
0	0	0	0	0	1	0	X6	X5	X4

X6	X5	X4	X3	X2	X1	X0	Description
0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	1	Column 1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	Column 126
1	1	1	1	1	1	1	Column 127

5.2.5 Set Column Address 2

This instruction is used to define area of DDRAM where MCU can access. The column address is automatically increased by one(+1) after each DDRAM access. After the ending column address CE[6:0], column address returns to starting column address CS[6:0] The CS[6:0] setting must be equal to or less than CE[6:0]. When CS[6:0] or CE[6:0] is larger than 7Fh, out of DDRAM range will be ignored. This command is only for horizontal or vertical addressing mode.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0	0	1
0	0	0	CS6	CS5	CS4	CS3	CS2	CS1	CS0
0	0	0	CE6	CE5	CE4	CE3	CE2	CE1	CE0

CS6	CS5	CS4	CS3	CS2	CS1	CS0	Description
0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	1	Column 1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	Column 126
1	1	1	1	1	1	1	Column 127

CE6	CE5	CE4	CE3	CE2	CE1	CE0	Description
0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	1	Column 1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	Column 126
1	1	1	1	1	1	1	Column 127

5.2.6 Set Start Line

This instruction sets the line address of the Display Data RAM to determine the initial display line. The display data of the specified line address is displayed at the top row (COM0) of the LCD panel.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	SL5	SL4	SL3	SL2	SL1	SL0

5.2.7 Set Contrast

This is double byte instruction. The first byte set contrast adjust mode and the following instruction will change the EV setting. That means these 2 bytes must be used together.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0	0	1
0	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0

Note: The range of EV[7:0] is 00h~FFh.

5.2.8 Segment Direction

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	MX

Flag	Description
MX	MX=0: SEG0->SEG127 MX=1: SEG127 -> SEG0

5.2.9 All Pixel On

This instruction will let all segments output the selected voltage and make all pixels turned ON.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	0	AP

Flag	Description
AP	AP=0: Normal display AP=1: All pixel on

5.2.10 Inverse Display

This instruction changes the selected and non-selected voltage of SEG. The display will be inversed (White -> Black, Black -> White) while the display data in the DDRAM is never changed.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	1	INV

Flag	Description
INV	INV=0: Normal display INV=1: Inverse display

5.2.11 Set Duty

This instruction is used to set duty of the module.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	0	0	0
0	0	0	0	DT5	DT4	DT3	DT2	DT1	DT0

DT5	DT4	DT3	DT2	DT1	DT0	Duty
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Note: The range of DT[5:0] is 00h~3Fh.

5.2.12 Set Internal IREF

This instruction is used to set Iref settings.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	0	1
0	0	0	0	Iref	EXT	0	0	0	0

Flag	Description
Iref	This setting is only for internal Iref use Iref = 19uA : output max. I_{SEG} = 150uA Iref = 30uA : output max. I_{SEG} = 240uA
EXT	EXT=0: External Iref enable EXT=1: External Iref disable

5.2.13 Display ON/OFF

The instruction turns the display ON or OFF.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	1	DSP

Flag	Description
DSP	DSP=0: Display off mode DSP=1: Display on mode

5.2.14 COM Direction

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	MY	0	0	0

Flag	Description
MY	MY=0: COM0->COM63 MY=1: COM63 -> COM0

5.2.15 Set COM0

This instruction sets the initial row (COM) of the panel. By using this instruction, it is possible to realize the window moving without the change of display data.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	0	0	1	1
0	0	0	0	C5	C4	C3	C2	C1	C0

5.2.16 Set Frame Rate

DK[3:0]: Define the divide ratio of the display clocks

FR[3:0]: Set the Oscillator Frequency.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	0	1	0	1
0	0	FR3	FR2	FR1	FR0	DK3	DK2	DK1	DK0

DK3	DK2	DK1	DK0	Level
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

FR3	FR2	FR1	FR0	Level
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

5.2.17 Pre-charge Period

This instruction sets the number of DCLK in the period.

P2[3:0]: Set Segment discharge period. D[7:4] (P2x)=0h is invalid entry.

P1[3:0]: Set Segment pre-charge period. D[3:0] (P1x)=0h is invalid entry.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	1	0	0	1
0	0	P23	P22	P21	P20	P13	P12	P11	P10

P13	P12	P11	P10	DCLK
0	0	0	1	2
0	0	0	1	4
:	:	:	:	:
1	1	1	0	28
1	1	1	1	30

P23	P22	P21	P20	DCLK
0	0	0	1	2
0	0	0	1	4
:	:	:	:	:
1	1	1	0	28
1	1	1	1	30

5.2.18 COM Pin Configuration

This instruction sets the hardware pins configuration.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	1	0	1	0
0	0	0	0	VDIR	ALT	0	0	1	0

Flag	Description
ALT	ALT=0: Normal Mode ALT=1: Interlace Mode
VDIR	VDIR=0: Normal Mode (COM0->COM63) VDIR=1: Reverse Mode (COM63 -> COM0)

5.2.19 Set V_{COMH}

This Instruction sets V_{COMH} voltage level.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	1	0	1	1
0	0	0	0	VC1	VC0	0	0	0	0

VC1	VC0	Description
0	0	~0.65 x VOLED
0	1	~0.71 x VOLED
1	0	~0.77 x VOLED
1	1	~0.83 x VOLED

5.2.20 NOP

This instruction will do nothing when receiving this command.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	1

5.2.21 Power Control

This instruction controls the power voltage of the built-in booster.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	1	1	0	1
0	0	CP1	0	0	1	0	VB	0	CP0

Flag	Description
VB	VB=0: Built-in booster off for external VOLED VB=1: Built-in booster on for internal VOLED

CP1	CP0	LCD Voltage
0	0	7.5V
0	1	6.0V
1	0	8.5V
1	1	9.0V

5.2.22 Horizontal Scroll Setting

This instruction sets the horizontal scrolling of the display. It can realize horizontal dynamic scrolling.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	1	1	HS
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	SPS2	SPS1	SPS0
0	0	0	0	0	0	0	ST2	ST1	ST0
0	0	0	0	0	0	0	SPE2	SPE1	SPE0
0	0	0	SCS6	SCS5	SCS4	SCS3	SCS2	SCS1	SCS0
0	0	0	SCE6	SCE5	SCE4	SCE3	SCE2	SCE1	SCE0

Horizontal scroll direction (scroll by 1 column)

Flag	Description
HS	HS=0: Scroll horizontally from left to right HS=1: Scroll horizontally from right to left

Set page start address

SPS2	SPS1	SPS0	Description
0	0	0	Page 0
0	0	1	Page 1
:	:	:	:
1	1	0	Page 6
1	1	1	Page 7

Set time interval between each scroll step

ST2	ST1	ST0	Frame
0	0	0	6
0	0	1	32
0	1	0	64
0	1	1	128
1	0	0	3
1	0	1	4
1	1	0	5
1	1	1	2

Set page end address. The SPE[2:0] setting must be equal to or larger than SPS[2:0].

SPE2	SPE1	SPE0	Description
0	0	0	Page 0
0	0	1	Page 1
:	:	:	
1	1	0	Page 6
1	1	1	Page 7

Set column start address

SCS6	SCS5	SCS4	SCS3	SCS2	SCS1	SCS0	Description
0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	1	Column 1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	Column 126
1	1	1	1	1	1	1	Column 127

Set column end address. The SCE[6:0] setting must be equal to or larger than SCS[2:0].

SCE6	SCE5	SCE4	SCE3	SCE2	SCE1	SCE0	Description
0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	1	Column 1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	Column 126
1	1	1	1	1	1	1	Column 127

5.2.23 Vertical and Horizontal Scroll Setting

This instruction sets the vertical scrolling of the display. It can realize vertical dynamic scrolling.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	0	VHS1	VHS0
0	0	0	0	0	0	0	0	0	SHC
0	0	0	0	0	0	0	SPS2	SPS1	SPS0
0	0	0	0	0	0	0	ST2	ST1	ST0
0	0	0	0	0	0	0	SPE2	SPE1	SPE0
0	0	0	0	SVO5	SVO4	SVO3	SVO2	SVO1	SVO0
0	0	0	SCS6	SCS5	SCS4	SCS3	SCS2	SCS1	SCS0
0	0	0	SCE6	SCE5	SCE4	SCE3	SCE2	SCE1	SCE0

Set scroll direction

VHS2	VHS1	Description
0	0	Reserve
0	1	Scroll vertically from left to right
1	0	Scroll vertically from right to left
1	1	Reserve

Set number of column scroll offset

Flag	Description
SHC	SHC=0: No horizontal scroll SHC=1: Horizontal scroll by 1 column

Set page start address

SPS2	SPS1	SPS0	Description
0	0	0	Page 0
0	0	1	Page 1
:	:	:	:
1	1	0	Page 6
1	1	1	Page 7

Set time interval between each scroll step

ST2	ST1	ST0	Frame
0	0	0	6
0	0	1	32
0	1	0	64
0	1	1	128
1	0	0	3
1	0	1	4
1	1	0	5
1	1	1	2

Set page end address. The SPE[2:0] setting must be equal to or larger than SPS[2:0].

SPE2	SPE1	SPE0	Description
0	0	0	Page 0
0	0	1	Page 1
:	:	:	:
1	1	0	Page 6
1	1	1	Page 7

Set number of vertical scroll offset. The SVO[5:0] must be less than SVN[6:0] in A3h.

SVO5	SVO4	SVO3	SVO2	SVO1	SVO0	Description
0	0	0	0	0	0	0 row
0	0	0	0	0	1	1 row
:	:	:	:	:	:	:
1	1	1	1	1	0	62 rows
1	1	1	1	1	1	63 rows

Set column start address

SCS6	SCS5	SCS4	SCS3	SCS2	SCS1	SCS0	Description
0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	1	Column 1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	Column 126
1	1	1	1	1	1	1	Column 127

Set column end address. The SCE[6:0] setting must be equal to or larger than SCS[6:0].

SCE6	SCE5	SCE4	SCE3	SCE2	SCE1	SCE0	Description
0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	1	Column 1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	Column 126
1	1	1	1	1	1	1	Column 127

5.2.24 Stop Scroll

Stop display scrolling.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	1	1	0

Note: After sending 2Eh command to stop the scrolling action, the ram data needs to be rewritten.

5.2.25 Start Scroll

Start display scrolling.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	1	1	1

5.2.26 Vertical Scroll Area

This instruction sets vertical scroll area of the display.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	1	1
0	0	0	0	SVF5	SVF4	SVF3	SVF2	SVF1	SVF0
0	0	0	SVN6	SVN5	SVN4	SVN3	SVN2	SVN1	SVN0

Set the number of rows scrolled in the fixed area at the top. The top display fixed area is the top content of the DDRAM.

SVF5	SVF4	SVF3	SVF2	SVF1	SVF0	Description
0	0	0	0	0	0	Row 0
0	0	0	0	0	1	Row 1
:	:	:	:	:	:	:
1	1	1	1	1	0	Row 62
1	1	1	1	1	1	Row 63

Set the number of rows in the scrolling area. This is the number of rows used for vertical scrolling. The scrolling area starts from the first row below the top fixed area.

SVN6	SVN5	SVN4	SVN3	SVN2	SVN1	SVN0	Description
0	0	0	0	0	0	0	Row 0
0	0	0	0	0	0	1	Row 1
:	:	:	:	:	:	:	:
0	1	1	1	1	1	0	Row 62
0	1	1	1	1	1	1	Row 63

1. SVF[5:0]+SVN[6:0]<=DT[6:0]

2. SVN[6:0]<=DT[6:0]

3. SVO[5:0]<=DT[6:0]

4. SL[5:0] <=DT[6:0]

5. The last row of the scroll area shifts to the first row of the scroll area

6. For 64 Duty display:

   SVF[5:0]=0, SVN[6:0]=64: whole area scrolls

   SVF[5:0]=0, SVN[6:0]<64: top area scrolls

SVF[5:0] + SVN[6:0] < 64: central area scrolls

SVF[5:0] + SVN[6:0]=64: bottom area scrolls

5.2.27 Content Scroll Setup

This instruction sets the horizontal scrolling of the display.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	1	0	HS
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	SPS2	SPS1	SPS0
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	SPE2	SPE1	SPE0
0	0	0	SCS6	SCS5	SCS4	SCS3	SCS2	SCS1	SCS0
0	0	0	SCE6	SCE5	SCE4	SCE3	SCE2	SCE1	SCE0

Horizontal scroll direction

Flag	Description
HS	HS=0: Scroll horizontally by one column from left to right HS=1: Scroll horizontally by one column from right to left

Set page start address

SPS2	SPS1	SPS0	Description
0	0	0	Page 0
0	0	1	Page 1
:	:	:	:
1	1	0	Page 6
1	1	1	Page 7

Set page end address. The SPE[2:0] setting must be equal to or larger than SPS[2:0].

SPE2	SPE1	SPE0	Description
0	0	0	Page 0
0	0	1	Page 1
:	:	:	:
1	1	0	Page 6
1	1	1	Page 7

Set column start address

SCS6	SCS5	SCS4	SCS3	SCS2	SCS1	SCS0	Description
0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	1	Column 1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	Column 126
1	1	1	1	1	1	1	Column 127

Set column end address. The SCE[6:0] setting must be equal to or larger than SCS[2:0].

SCE6	SCE5	SCE4	SCE3	SCE2	SCE1	SCE0	Description
0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	1	Column 1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	Column 126
1	1	1	1	1	1	1	Column 127

5.2.28 Set Fade Out and Blinking

When fad out mode is enabled, the contrast gradually decreases until all pixels are turned off. When fad out mode is disabled, the output follows the DDRAM content. When blink mode is enabled, the contrast will gradually decrease until all pixels off, and then contrast will gradually increase to restore normal display. The process loops continuously until the blinking mode is disabled.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0	1	1
0	0	0	0	FB1	FB0	FO3	FO2	FO1	FO0

Set time interval between each fade step

FO3	FO2	FO1	FO0	Description
0		0	0	8 frames
0		0	1	16 frames
:		:	:	:
1		1	0	120 frames
1		1	1	128 frames

Set fade out and blinking mode

FB1	FB0	Description
0	0	fade out: OFF; blinking: OFF
0	1	Reserve
1	0	fade out: ON
1	1	blinking: ON

5.2.29 Zoom In

This instruction sets display zoom in mode.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	1	0	1	1	0
0	0	0	0	0	0	0	0	0	ZI

Flag	Description
ZI	ZI=0: Disable ZI=1: Enable

5.2.30 Clean DDRAM

This instruction can be used to clear the DDRAM data to 0.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	1	0	0
0	0	0	1	0	1	1	0	1	0
0	0	1	0	0	0	0	0	0	0
0	0	1	0	0	1	0	1	0	0
0	0	1	0	1	0	0	1	0	1

5.2.31 Crosstalk Compensation

This instruction can be used to compensate for the crosstalk of the display.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	1	0	0
0	0	0	1	0	1	1	0	1	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0	0	0
0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0
0	0	1	0	0	1	0	1	0	0
0	0	1	0	1	0	0	1	0	1

5.2.32 Deep Sleep IN

This instruction is used to enter Deep Sleep IN mode. Exit this mode need by hardware reset.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	1	0	0
0	0	0	1	0	1	1	0	1	0
0	0	1	0	0	0	0	0	1	0
0	0	0	1	0	1	0	1	0	1
0	0	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1	0
0	0	1	0	1	0	1	0	1	0

5.2.33 Set Contrast Offset

Contrast Offset is used to fine tune contrast for different panel. It can be programmed by OTP.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	1	0	0
0	0	0	1	0	1	1	0	1	0
0	0	1	1	1	0	1	0	0	1
0	0	0	Sign	OF5	OF4	OF3	OF2	OF1	OF0
0	0	1	0	0	1	0	1	0	0
0	0	1	0	1	0	0	1	0	1

Flag	Description
Sign	Sign=1: Minus Offset value Sign=0: Plus Offset value
OF[5:0]	Contrast Offset value

5.2.34 Read Program Times

IDtr[2:0] can be read for program times and please refer to Read Register Flow.

EVtr[2:0] can be read for program times and please refer to Read Register Flow.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	1	0	0
0	0	0	1	0	1	1	0	1	0
0	0	0	0	0	0	0	1	1	1
0	1	0	0	IDtr2	IDtr1	IDtRr0	EVtr2	EVtr1	EVtr0
0	0	1	0	0	1	0	1	0	0
0	0	1	0	1	0	0	1	0	1

5.2.35 Read ID

ID[1:0] can be read for ID code and please refer to Read Register Flow

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	0	1	0	0
0	0	0	1	0	1	1	0	1	0
0	0	0	0	0	0	1	1	1	1
0	1	ID1	ID0	0	0	0	0	0	0
0	0	1	0	0	1	0	1	0	0
0	0	1	0	1	0	0	1	0	1

5.2.36 ID and Contrast Program times

IDtw[2:0] is ID code of program times and it can be programmed by OTP Program Flow.

EVtw[2:0] is contrast offset of program times and it can be programmed by OTP Program Flow.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	IDtw2	IDtw1	IDtw0	EVtw2	EVtw1	EVtw0

IDtw[2:0]	Select ID
111	No Program ID
110	ID0[1:0]
100	ID1[1:0]
000	ID2[1:0]
Other	Unavailable

EVtw[2:0]	Select Contrast Offset
111	No Contrast Offset
110	Contrast Offset0
100	Contrast Offset1
000	Contrast Offset2
Other	Unavailable

5.2.37 OTP ID Program

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	1
0	0	0	0	ID[5:0]					

ID can be program by OTP program flow.

ID[5:0]	Description
ID	ID range is 0~3

5.2.38 Contrast Offset

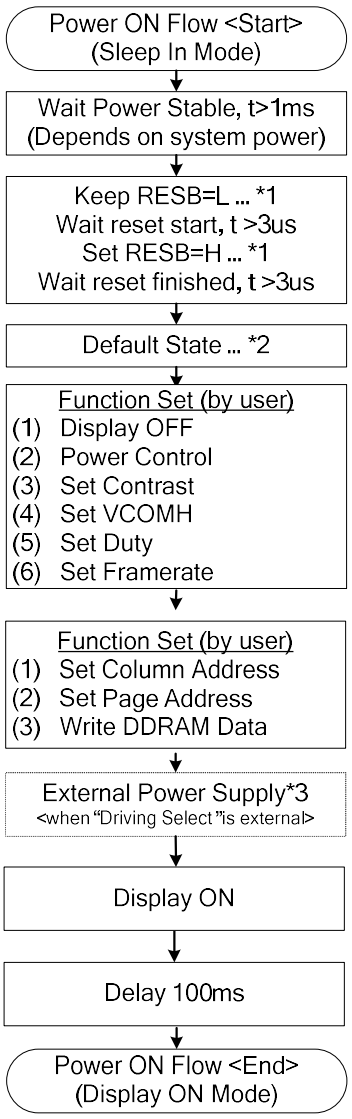
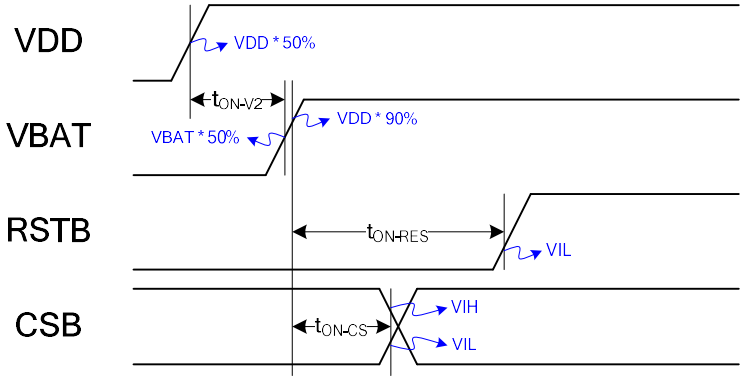
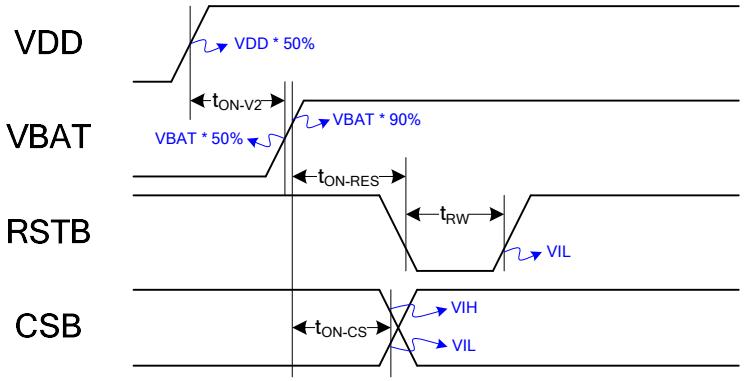
Contrast Offset is used to write contrast level into OTP.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	0
0	0	0	Sign	OF5	OF4	OF3	OF2	OF1	OF0

Flag	Description
Sign	Sign=1: Minus Offset value Sign=0: Plus Offset value
OF[5:0]	Contrast Offset value

6. OPERATION FLOW

6.1 Power ON

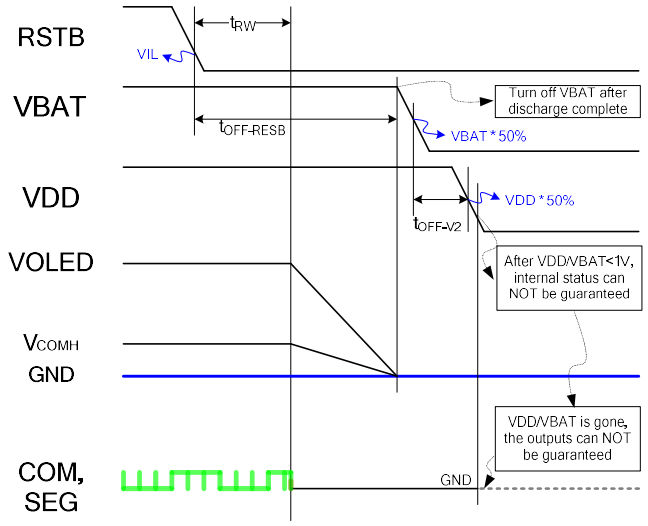
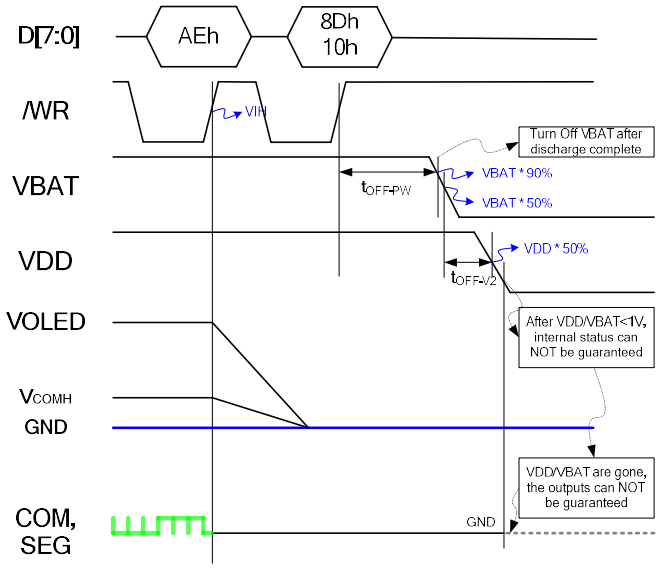
Referential Operation Flow	Operation Sequence
	Case-1: RSTB=L while Power ON  Case-2: RSTB=H while Power ON 

Note

1. Please refer to the specification of tRW and tR.
2. Refer to the section of RESET CIRCUIT
3. The detail instruction functionality is described in Power Control instruction.
4. The power stable is defined as the time that the later power (VDD or VBAT) reaches 90% of its rated voltage.

Item	Symbol	Requirement	Description
VBAT power ON delay	t_{ON-V2}	No Limitation	VDD and VBAT can be applied in any order. IC will NOT be damaged when one of VDD and VBAT is ON but another is OFF. Power stable is defined as the time that the later power (VDD or VBAT) reaches 90% of its rated voltage. Recommend Setting: -50ms ≤ t_{ON-V2} ≤ No Limitation.
RSTB input time	t_{ON-RES}	Case-1 t_{RW} ≤ t_{ON-RES} Case-2 No Limitation	RSTB=L can be input at any time after power is stable. t_{RW} & t_R should match the timing specification of RSTB. RSTB has priority over CSB. Recommend Setting: 0 ≤ t_{ON-RES} ≤ 50 ms.
CSB input time	t_{ON-CS}	No Limitation	CSB can be input at any time after power is stable.

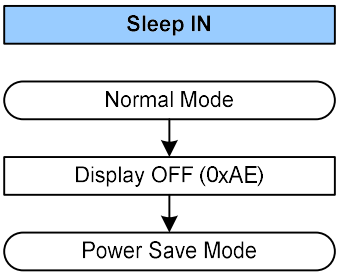
6.2 Power OFF

Referential Operation Flow	Operation Sequence
Case-2 Power OFF Flow <Start> ↓ Display OFF ↓ Internal Power Stop <Power Control OFF> or External Power Stop <When Power Supply is external > ↓ Wait 100ms ↓ VDD, VBAT Power OFF ↓ Power OFF Flow <End>	Case-1: Use RSTB  Case-2: Power OFF at Sleep State 

Item		Symbol	Requirement	Description
Power OFF Time	Case-1	$t_{OFF-RESB}$	200ms ≤$t_{OFF-RESB}$	Power can be turned OFF after built-in power becomes GND.
	Case-2	t_{OFF-PW}	100ms ≤ t_{OFF-PW}	
VBAT power ON delay		t_{OFF-V2}	No Limitation	VDD and VBAT can be powered down in any order. IC will NOT be damaged when one of VDD and VBAT is ON but another is OFF. Recommend Setting: 0 ≤ t_{OFF-V2} ≤ 5ms

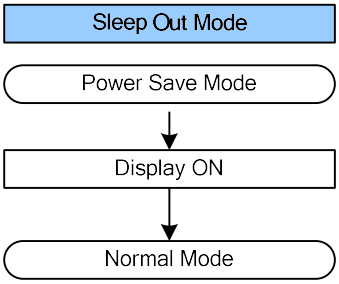
Note: In Case-2, RSTB can fall to GND at the same time as VDD.

6.3 Sleep In



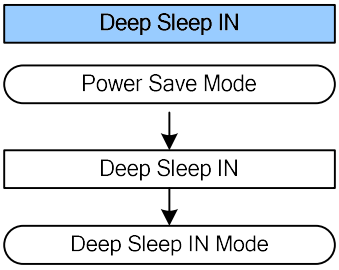
Reference C Code	
WriteCommand (0xAE);	//Display OFF

6.4 Sleep Out



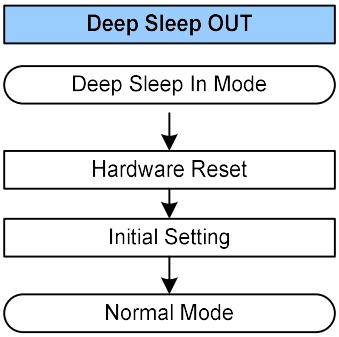
Reference C Code	
WriteCommand(0xAF);	//Display ON

6.5 Deep Sleep In

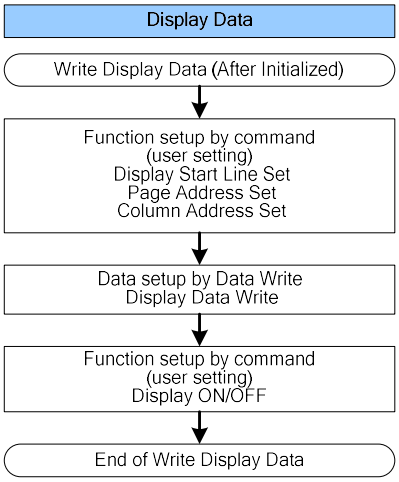


Reference C Code	
WriteCommand(0xAE); WriteCommand(0x94); WriteCommand(0x5A); WriteCommand(0x82); WriteCommand(0x55); WriteCommand(0x55); WriteCommand(0xAA); WriteCommand(0xAA);	//Enter Deep Sleep In Mode

6.6 Deep Sleep Out



6.7 Display Data



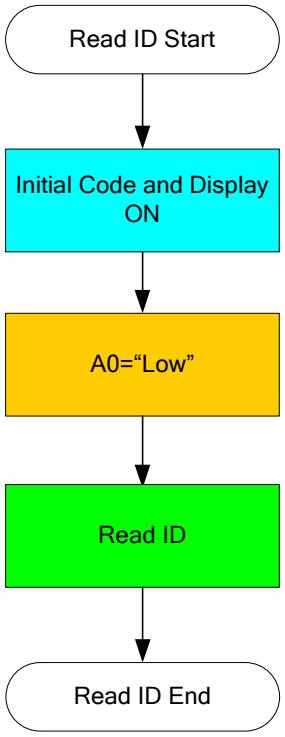
Reference C Code

```
Extern unsigned char picture[8][128];                    //Picture must be set
Void WriteDisplayData(void)
{
    int page=0, column=0;                                //Picture data
    int pageAddr=0xB0;                                   //Set page=page0

    WriteCommand(0x40);                                  //Set start line address=0x00

    for( page=0; page<8; page++)                         //Send picture data
    {                                                   //From page 0 to page 8
        WriteCommand(pageAddr);                          //Set Page
        WriteCommand(0x10);                              //Set MSB Column address
        WriteCommand(0x00);                              //Set LSB Column address
        for( column=0; column<128; column++)              //Send picture data
        {                                               //From column 0 to column 128
            WriteData(picture[page][column]);            //Write picture data
        }
        pageAddr++;                                      //Set page= next page
    }
}
    WriteCommand(0xAF);                                  //Display ON(0xAF)
```

6.8 OTP Operation

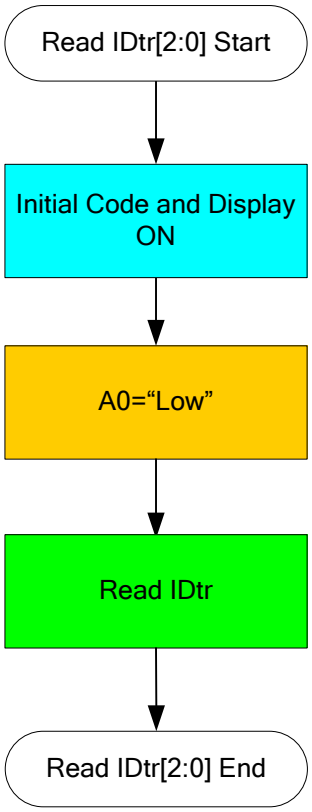
When OTP programming process starts, the VBAT voltage must be ≧ 3.0V.

6.8.1 Read ID Register Flow



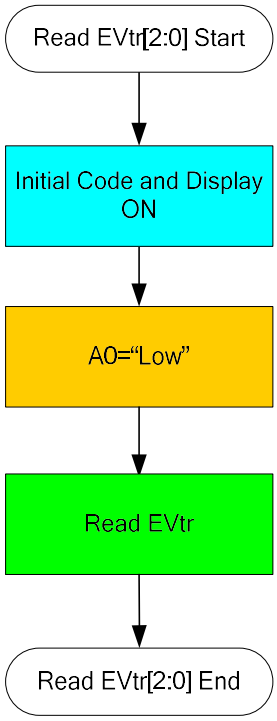

```
Unsigned char Read_ID()
{
    unsigned char ID;
    Writecommand(0x94);
    Writecommand(0x5A);
    Writecommand(0x60);
    Writecommand(0x0F);
    Writecommand(0x61);
    ID=(Read_1Byte() &0xC0)>>6;
    Writecommand(0x94);
    Writecommand(0xA5);
    Return ID;
}
```

6.8.2 Read ID Program Times Register Flow



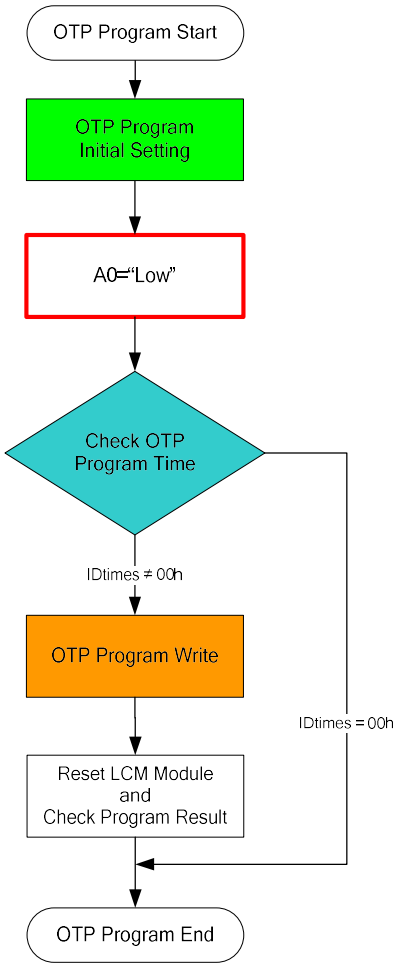

```
unsigned char Read_IDtr()
{
    unsigned char IDtr;
    Writecommand(0x94);
    Writecommand(0x5A);
    Writecommand(0x60);
    Writecommand(0x07);
    Writecommand(0x61);
    IDtr=(Read_1Byte()&0x38)>>3;
    Writecommand(0x94);
    Writecommand(0xA5);
    Return IDtr;
}
```

6.8.3 Read Contrast Offset Program Times Register Flow




```
Unsigned char Read_EVtr()
{
    unsigned char EVtr;
    Writecommand(0x94);
    Writecommand(0x5A);
    Writecommand(0x60);
    Writecommand(0x07);
    Writecommand(0x61);
    EVtr=(Read_1Byte()&0x07);
    Writecommand(0x94);
    Writecommand(0xA5);
    Return EVtr;
}
```

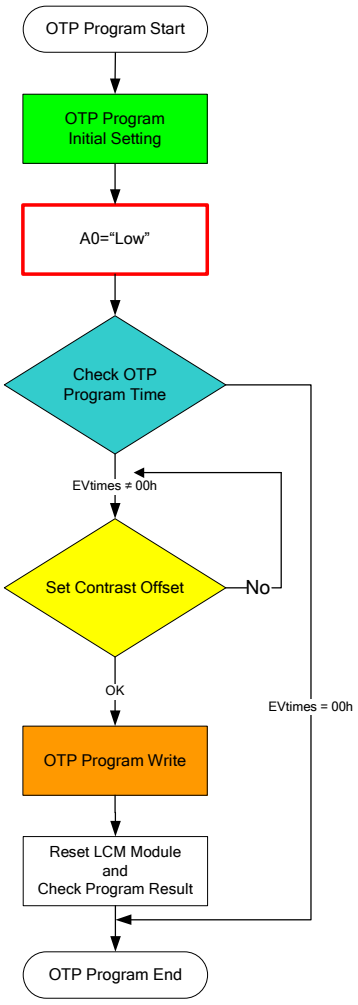
6.8.4 OTP ID Program Flow




```
unsigned char IDtimes, EVtimes;
ST7315_OTP_Program_Initial_Setting()
{
    Writecommand(0xAD);
    Writecommand (0x10);
    Writecommand (0x8D);
    Writecommand (0x95);
    Writecommand (0xDB);
    Writecommand (0x30);
    Writecommand (0x81);
    Writecommand (0x00);
    Writecommand (0xAF);
}
```

```
void Check_OTP_Program_Time()
{
    IDtimes= ReadIDtr();
    EVtimes= ReadEVtr();
    If(IDtimes !=0x00)
    OTP_Program_Write_ID(ID);
}


void OTP_Program_Write_ID(unsigned char id)
{
    Writecommand (0x94);
    Writecommand (0x5A);
    Writecommand (0xE2);
    Writecommand (0x5A);
    Writecommand (0x69);
    Writecommand (0xEE);
    Writecommand (0x04);
    Writecommand (0x2C);
    Writecommand (0xD4);
    Writecommand (0x10);
    Delay_ms(150);
    Writecommand (0xE4);
    Writecommand (0x00);
    Writecommand ((0xF8 <<(4-IDtimes)) | EVtimes);
    Writecommand (0xE1);
    Writecommand (0x29);
    Writecommand (0xA5);
    Delay_ms(100);
    Writecommand (0xE4);
    Writecommand (0x07);
    Writecommand (((0xFC | id)<<(3- IDtimes)*2));
    Writecommand (0xE1);
    Writecommand (0x29);
    Writecommand (0xA5);
    Delay_ms(100);
    Writecommand (0x94);
    Writecommand (0xA5);
}
```

6.8.5 OTP Contrast Offset Program Flow




```
unsigned char IDtimes, EVtimes;
ST7315_OTP_Program_Initial_Setting()
{
    Writecommand(0xAD);
    Writecommand (0x10);
    Writecommand (0x8D);
    Writecommand (0x95);
    Writecommand (0xDB);
    Writecommand (0x30);
    Writecommand (0x81);
     Writecommand (0x00);
    Writecommand (0xAF);
}
```

```
void set_ContrastOffset(unsigned char offset)
{
    WriteCMD(0x94);
    WriteCMD(0x5a);
    WriteCMD(0xE9);
    WriteCMD(offset);
    WriteCMD(0x94);
    WriteCMD(0xA5);
}

void OTP_Program_Write_ContrastOffset(unsigned char offset)
{
    Writecommand (0x94);
    Writecommand (0x5A);
    Writecommand (0xE2);
    Writecommand (0x5A);
    Writecommand (0x69);
    Writecommand (0xEE);
    Writecommand (0x04);
    Writecommand (0x2C);
    Writecommand (0xD4);
    Writecommand (0x10);
    Delay_ms(150);
    Writecommand (0xE4);
    Writecommand (0x00);
    Writecommand ( 0xC0 | (IDtimes<<3) | (0x07 << (4-EVtimes))&0x07);
    Writecommand (0xE1);
    Writecommand (0x29);
    Writecommand (0xA5);
    Delay_ms(100);
    Writecommand (0xE4);
    Writecommand (0x04+(3-Evtimes));
    Writecommand (offset);
    Writecommand (0xE1);
    Writecommand (0x29);
    Writecommand (0xA5);
    Delay_ms(100);
    Writecommand (0x94);
```

```
    Writecommand (0xA5);
}

void Check_OTP_Program_Time()
{
    IDtimes= ReadIDtr();
    EVtimes= ReadEVtr();
    If(EVtimes != 0x00)
      OTP_Program_Write_ContrastOffset(ContrastOffset);
}
```

7. HANDING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

8. ELECTRICAL SPECIFICATIONS

8.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
IO Supply Voltage	VDD	-0.3 to +5.5	V
Power Supply Voltage	VBAT	-0.3 to +5.5	V
VOLED Supply Voltage	VOLED	0 to 18	V
SEG output Voltage	VSEG	0 to VOLED	V
COM output Voltage	VCOM	0 to 0.9*VOLED	V
Input Voltage	Vin	GND-0.5 to VDD+0.5	V
Operating Temperature Range	TA	-40 to +85	℃
Storage Temperature Range	TSTG	-65 to +150	℃

Notes

1. *Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.*
2. *That the stress exceeds the Limiting Value listed above it may cause the driver IC permanent damage. These values are for stress only. IC should be operated under the DC/Timing Characteristic conditions for normal operation. If these conditions are not met, IC operation may be error and the reliability may be deteriorated.*
3. *Insure the voltage levels of VBAT, VOLED and VCOMH always match the correct relation: VOLED > VCOMH > VBAT > VSS*
4. *VIN should be less than or equal to 5.5V. (VIN ≤ 5.5V)*

8.2 DC Characteristics

DC Electrical Characteristics (VDD= 3.3V, GND= 0V, TA=25°C, Bare Chip)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Digital Power Supply	VDD	2.4	-	3.6	V	
Analog Power Supply	VBAT	2.4	-	4.5	V	
Charge Pump Regulator Supply (Charge Pump Output Voltage ITO resistance < 3Ω for charge pump related pins)	VOLED 6V Mode	5.5	6	-	V	VBAT = 2.4V~4.5V, Maximum output loading = 4mA
	VOLED 7.5V Mode	7	7.5	-	V	VBAT = 3.0V~4.5V, Maximum output loading = 8mA
	VOLED 8.5V Mode	8	8.5	-	V	VBAT = 3.6V~4.5V, Maximum output loading = 12mA
	VOLED 9V Mode	8.5	9	-	V	VBAT = 3.8V~4.5V, Maximum output loading = 12mA
Sleep Mode Current	I_{DD}	-	-	10	uA	VDD = 2.4V~3.6V VOLED = 6.0V~16.5V Display OFF
	I_{BAT}	-	-	10	uA	VDD = 2.4V~3.6V VBAT = 2.4V~4.5V Display OFF
	I_{OLED}	-	-	10	uA	VDD = 2.4V~3.6V VOLED = 6.0V~16.5V Display OFF
Display ON Current (Pattern: All ON)	I_{OLED}	-	625	1000	uA	VDD = 2.8V VOLED = 12V IREF = 30uA Contrast=FFh
	I_{DD}	-	240	330	uA	VDD = 2.8V VOLED = 12V IREF = 30uA Contrast=FFh

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Segment Output Current (Display ON)	I_{SEG}	-	240	-	uA	VDD=2.8V, VOLED=12V, IREF=30uA Contrast=FFh
		-	165	-	uA	VDD=2.8V, VOLED=12V, IREF=30uA Contrast=AFh
		-	60	-	uA	VDD=2.8V, VOLED=12V, IREF=30uA Contrast=3Fh
	I_{SEG}	-	150	-	uA	VDD=2.8V, VOLED=7.5V, IREF=19uA Contrast=FFh
		-	104	-	uA	VDD=2.8V, VOLED=7.5V, IREF=19uA Contrast=AFh
		-	38	-	uA	VDD=2.8V, VOLED=7.5V, IREF=19uA Contrast=3Fh
Segment Output Current Uniformity	Dev	-3	-	+3	%	Dev = (I_{SEG} – IMID)/IMID IMID = (IMAX + IMIN)/2 I_{SEG} [0:127] = Segment current at contrast=FFh
Adjacent Pin Output Current Uniformity (Contrast = FF)	Adj. Dev	-2	-	+2	%	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])
Logic-High Input Voltage	V_{IH}	0.8 x VDD	-	-	V	
Logic-Low Input Voltage	V_{IL}	-	-	0.2 x VDD	V	
Logic-High Output Voltage	V_{OH}	0.9 x VDD	-	-	V	
Logic-Low Output Voltage	V_{OL}	-	-	0.1 x VDD	V	

8.3 AC Characteristics

AC Electrical Characteristics (VDD= 2.8V, GND= 0V, TA=25°C, Bare Chip)

8.3.1 System Operation AC Characteristics

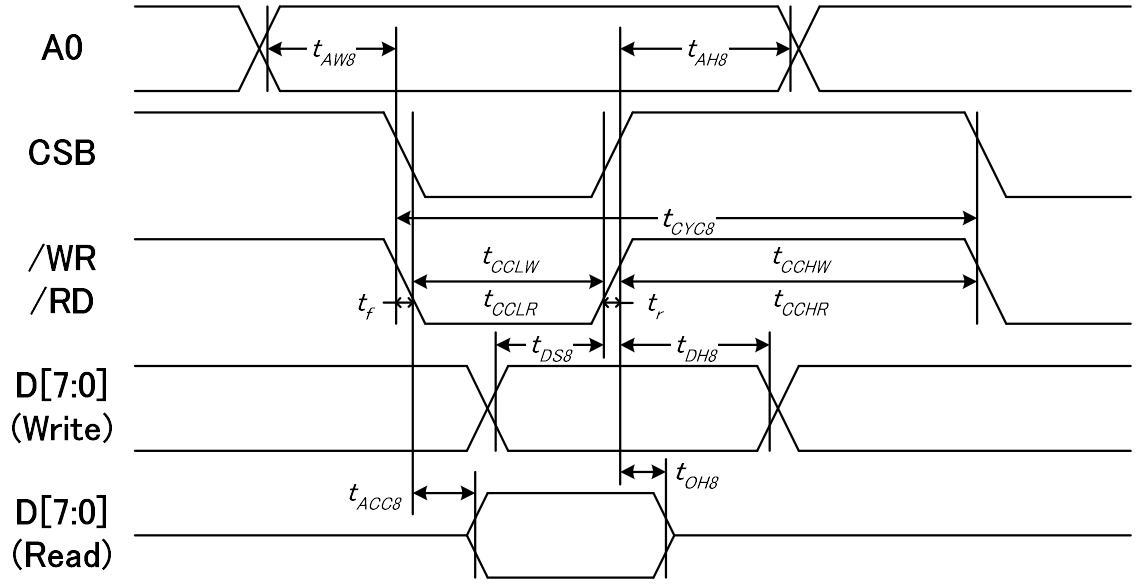
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Frequency of Display Timing Generator	FOSC(1)	620	688	756	KHz	VDD=2.8V
Frame Frequency	FRM	-	Foscx1 / (DxKx64)(2)	-	Hz	128x64 Normal Mode, Display ON, Internal Oscillator Enabled

Note : 1. FOSC stands for the frequency value of the internal oscillator and the value is measured when command D5h is in default value.

2. D: divide ratio (default value = 1)

K: number of display clocks per row period (default value = 103)

8.3.2 8080 Interface



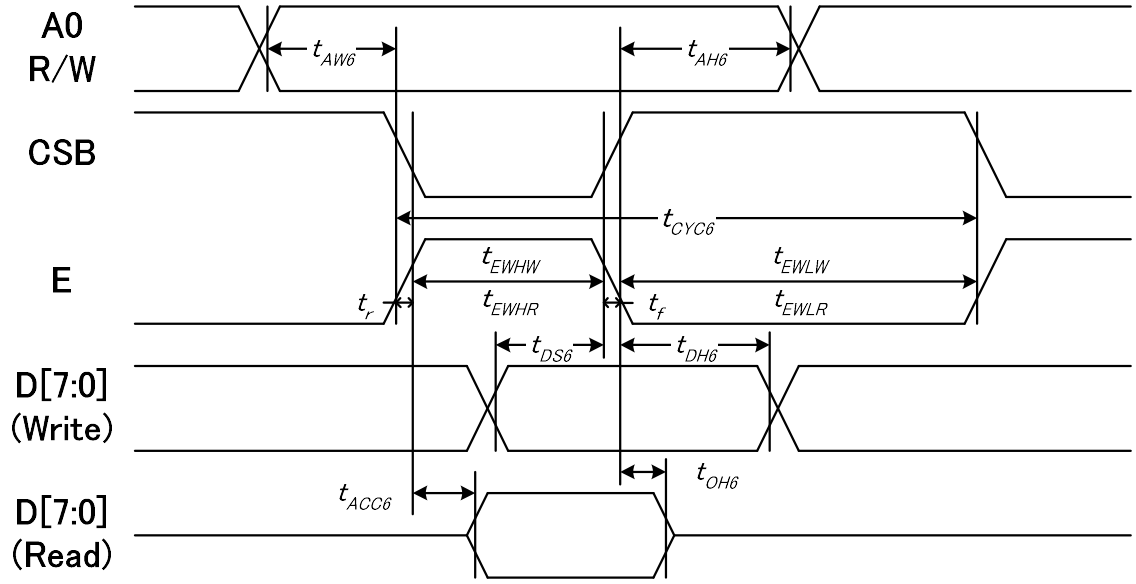
(VDD= 2.4V~3.3V, GND= 0V, TA=25°C, Bare Chip)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8	-	10	-	ns
Address hold time		tAH8	-	0	-	
System cycle time	/WR	tCYC8	-	300	-	
/WR L pulse width (WRITE)		tCCLW	-	60	-	
/WR H pulse width (WRITE)		tCCHW	-	60	-	
/RD L pulse width (READ)	RD	tCCLR	-	120	-	
/RD H pulse width (READ)		tCCHR	-	60	-	
WRITE Data setup time	D[7:0]	tDS8	-	40	-	
WRITE Data hold time		tDH8	-	20	-	
READ access time		tACC8	-	-	140	
READ Output disable time		tOH8	-	-	70	

1 The input signal rise time and fall time (tr, tf) is specified at 40 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

2 All timing is specified using 20% and 80% of VDD as the reference.

8.3.3 6800 Interface



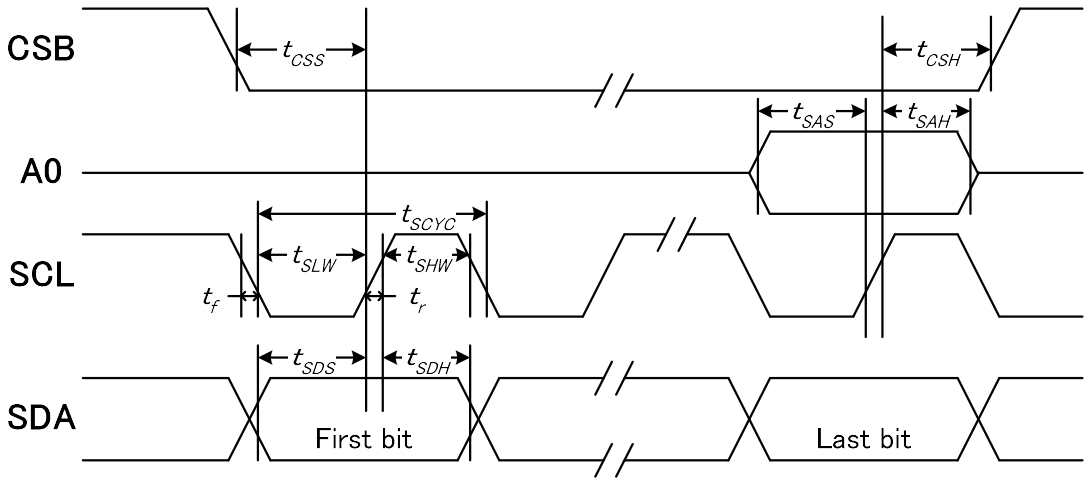
(VDD= 2.4V~3.3V, GND= 0V, TA=25°C, Bare Chip)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6	-	5	-	ns
Address hold time		tAH6	-	0	-	
System cycle time	E	tCYC6	-	300	-	
Enable L pulse width (WRITE)		tEWLW	-	60	-	
Enable H pulse width (WRITE)		tEWHW	-	60	-	
Enable L pulse width (READ)		tEWLR	-	120	-	
Enable H pulse width (READ)		tEWHR	-	60	-	
Write data setup time	D[7:0]	tDS6	-	40	-	
Write data hold time		tDH6	-	7	-	
Read data access time		tACC6	-	-	140	
Read data output disable time		tOH6	-	-	70	

1 The input signal rise time and fall time (tr, tf) is specified at 40 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

2 All timing is specified using 20% and 80% of VDD as the reference.

8.3.4 4SPI Interface



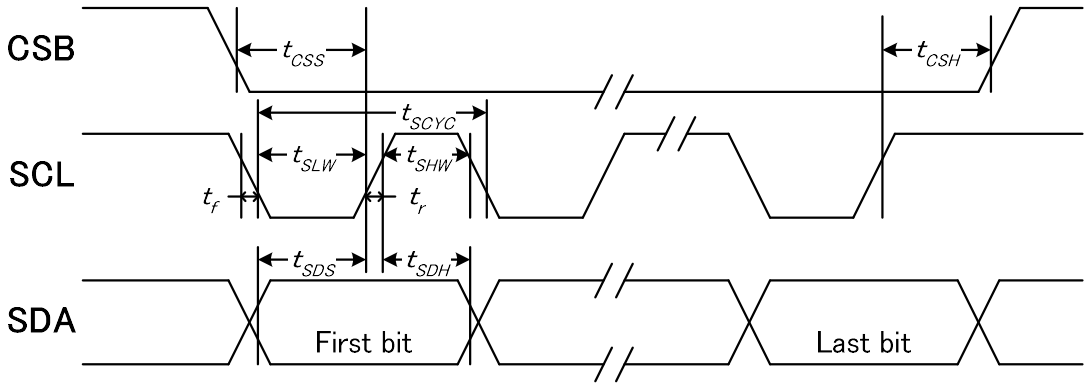
(VDD= 2.4V~3.3V, GND= 0V, TA=25°C, Bare Chip)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		100	-	ns
SCL “H” pulse width		tSHW		20	-	
SCL “L” pulse width		tSLW		20	-	
Address setup time	A0	tSAS		15	-	
Address hold time		tSAH		15	-	
Data setup time	SDA	tSDS		15	-	
Data hold time		tSDH		15	-	
CSB-SCL time	CSB	tCSS		20	-	
CSB-SCL time		tCSH		10	-	

1 The input signal rise time and fall time (tr, tf) is specified at 40 ns or less.

2 All timing is specified using 20% and 80% of VDD as the reference.

8.3.5 3SPI Interface



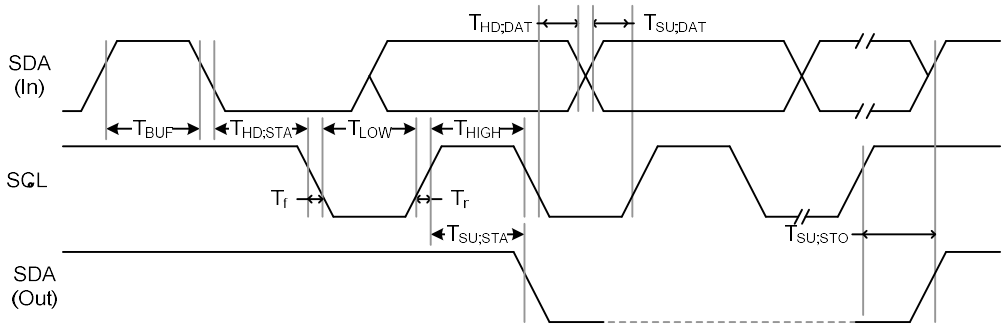
(VDD= 2.4V~3.3V, GND= 0V, TA=25°C, Bare Chip)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		100	-	ns
SCL “H” pulse width		tSHW		20	-	
SCL “L” pulse width		tSLW		20	-	
Data setup time	SDA	tSDS		15	-	
Data hold time		tSDH		15	-	
Chip select setup time	CSB	tCSS		20	-	
Chip select hold time		tCSH		10	-	

1 The input signal rise time and fall time (tr, tf) is specified at 40 ns or less.

2 All timing is specified using 20% and 80% of VDD as the reference.

8.3.6 I²C Interface



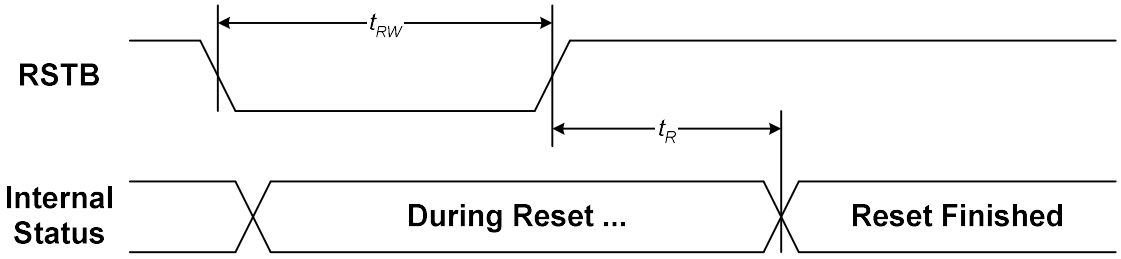
(VDD= 2.4V~3.3V, GND= 0V, TA=25°C, Bare Chip)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCL Clock Frequency	FSCL	-	-	400	KHz	
Signal Rise Time	Tr	-	-	300	ns	
Signal Fall Time	Tf	-	-	300	ns	
Start Condition Setup Time	TSU;STA	600	-	-	ns	
Start Condition Hold Time	THD;STA	600	-	-	ns	
Data Setup Time	TSU;DAT	100	-	-	ns	
Data Hold Time	THD;DAT	300	-	-	ns	
Setup Time for STOP Condition	TSU;STO	600	-	-	ns	
Bus Free Time Between a STOP and START	TBUF	1300	-	-	ns	

1 The input signal rise time and fall time (tr, tf) is specified at 40 ns or less.

2 All timing is specified using 20% and 80% of VDD as the reference.

8.3.7 Reset Timing



(VDD= 2.4V~3.3V, GND= 0V, TA=25°C, Bare Chip)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		-	3	us
Reset “L” pulse width	tRW		3	-	us

9. REVISION HISTORY

Version	Date	Description
V0.6s	2021/2/3	6th Edition