ST7785M

240RGB x 320 dot 262K Color with Frame Memory Single-Chip TFT Controller/Driver

Datasheet

Version 0.0

2020/01

Sitronix Technology Corporation

LIST OF CONTENT

1 GENERAL DESCRIPTION

The ST7785M is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 720 source line and 320 gate line driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts 8-bits/9-bits parallel, SPI, RGB 6bits and MIPI interface. Display data can be stored in the on-chip display data RAM of 240x320x18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuit necessary to drive liquid crystal; it is possible to make a display system with the fewest components.

2 FEATURES

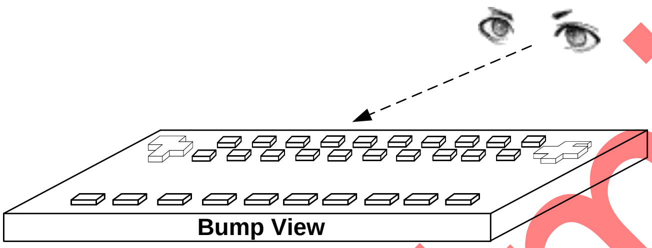
- Single chip TFT-LCD Controller/Driver with On-chip Frame Memory (FM)
- Display Resolution: 240*RGB (H) *320(V)
- Frame Memory Size: 240 x 320 x 18-bit = 1,382,400 bits
- LCD Driver Output Circuits
  - Source Outputs: 240 RGB Channels
  - Gate Outputs: 320 Channels
  - Common Electrode Output
- Display Colors (Color Mode)
  - Full Color: 262K, RGB=(666) max., Idle Mode Off
  - Color Reduce: 8-color, RGB=(111), Idle Mode On
- Programmable Pixel Color Format (Color Depth) for Various Display Data input Format
  - 12-bit/pixel: RGB=(444)
  - 16-bit/pixel: RGB=(565)
  - 18-bit/pixel: RGB=(666)
- Display Interface
  - Parallel 8080-series MCU Interface (8-bit, 9-bit)
  - 6-bit RGB Interface(VSYNC, HSYNC, DOTCLK, ENABLE, DB[5:0])
  - Serial Peripheral Interface(SPI Interface)
  - VSYNC Interface
  - MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 data lane pairs)
- Display Features
  - Programmable Partial Display Duty
  - CABC for saving current consumption
  - Color enhancement
- On Chip Build-In Circuits
  - DC/DC Converter
  - Adjustable VCOM Generation
  - Non-Volatile (NV) Memory to Store Initial Register Setting and Factory Default Value (Module ID, Module Version, etc)
  - Timing Controller
  - 4 preset Gamma curve with separated RGB Gamma setting
  - Internal VPP for NV Memory
- Build-In NV Memory for LCD Initial Register Setting
  - 8-bits for ID1 setting
  - 8-bits for ID2 setting
  - 8-bits for ID3 setting

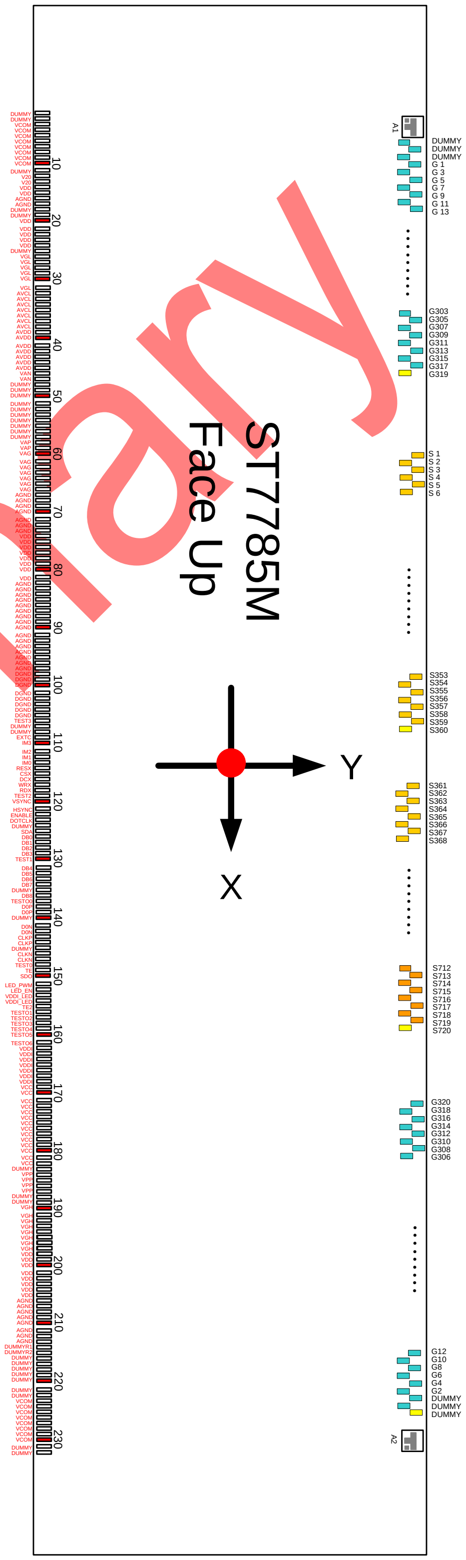
- 6-bits for VCOM Offset adjustment
- Driving Algorithm
  - Dot Inversion
  - Column Inversion
- Wide Supply Voltage Range
  - I/O Voltage (VDDI to DGND): 1.65V ~ 3.3V (VDDI≦ VDD)
  - Analog Voltage (VDD to AGND): 2.4V ~ 3.3V
- On-Chip Power System
  - Source Voltage (VAP (GVDD) to VAN (GVCL)): +6.4~-4.6V
  - VCOM level: GND
  - Gate driver HIGH level (VGH to AGND): +12.2V ~ +14.97V
  - Gate driver LOW level (VGL to AGND): -12.5V ~ -7.16V
  - Adjustable voltage range for feed through compensation: 0.1V~1.675V
- Optimized layout for COG Assembly
- Operate temperature range: −30℃ to +85℃
- Lower Power Consumption

3 PAD ARRANGEMENT

3.1 Output Bump Dimension

Au bump height	9µm
Au bump size	Gate : 13.5µm x 60µm (G1~G320)
	Source : 13.5µm x 71µm (S1~S720)
	40µm x 31.8µm
	Input Pads : Pad 12 to Pad 239



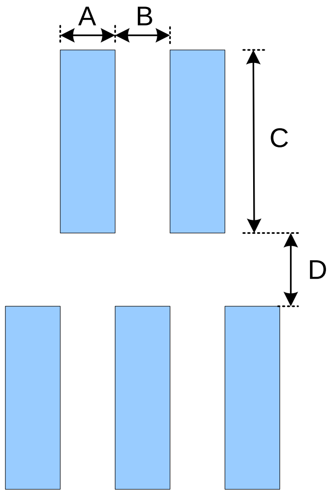


3.2 Input Bump Dimension

- **Output Pads**

S1~S720、G1~G320、DUMMY

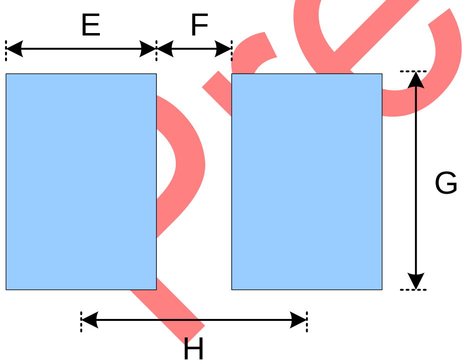
(No.233~1278)



Symbol	Item	Size
A	Bump Width	13.5 um
B	Bump Gap 1 (Horizontal)	14.5 um
C	Bump Height (S1~S720)	71 um
	Bump Height (G1~G320)	60 um
D	Bump Gap 2 (Vertical)	31 um

- **Input Pads**

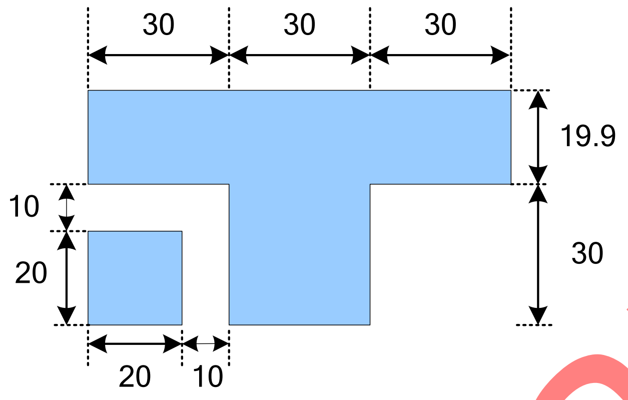
No.1~232



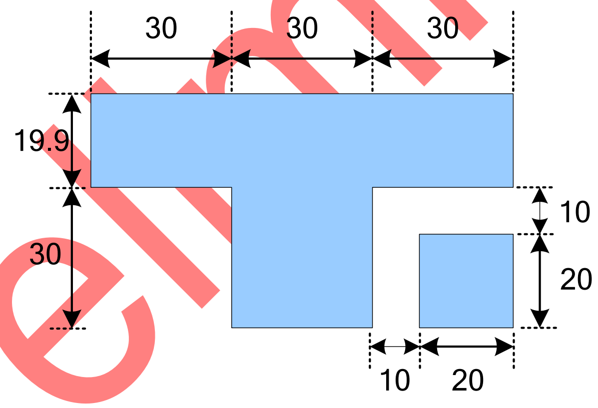
Symbol	Item	Size
E	Bump Width	40 um
F	Bump Gap	20 um
G	Bump Height	31.8 um
H	Bump Pitch	60 um

3.3 Alignment Mark Dimension

- **Alignment Mark : A1(X,Y)=(-7480,226.5)**



- **Alignment Mark : A2(X,Y)=(+7480,226.5)**



3.4 Chip Information

Chip size	15385µm x 533µm (Tolerance ± 40µm)
Chip thickness	200µm
Pad Location	Pad center
Coordinate Origin	Chip center

4 PAD CENTER COORDINATES

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	DUMMY	-7292.5	-234.6	33	AVCL	-5372.5	-234.6	65	VAG	-3452.5	-234.6
2	DUMMY	-7232.5	-234.6	34	AVCL	-5312.5	-234.6	66	VAG	-3392.5	-234.6
3	VCOM	-7172.5	-234.6	35	AVCL	-5252.5	-234.6	67	AGND	-3332.5	-234.6
4	VCOM	-7112.5	-234.6	36	AVCL	-5192.5	-234.6	68	AGND	-3272.5	-234.6
5	VCOM	-7052.5	-234.6	37	AVCL	-5132.5	-234.6	69	AGND	-3212.5	-234.6
6	VCOM	-6992.5	-234.6	38	AVCL	-5072.5	-234.6	70	AGND	-3152.5	-234.6
7	VCOM	-6932.5	-234.6	39	AVDD	-5012.5	-234.6	71	AGND	-3092.5	-234.6
8	VCOM	-6872.5	-234.6	40	AVDD	-4952.5	-234.6	72	AGND	-3032.5	-234.6
9	VCOM	-6812.5	-234.6	41	AVDD	-4892.5	-234.6	73	AGND	-2972.5	-234.6
10	VCOM	-6752.5	-234.6	42	AVDD	-4832.5	-234.6	74	VDD	-2912.5	-234.6
11	DUMMY	-6692.5	-234.6	43	AVDD	-4772.5	-234.6	75	VDD	-2852.5	-234.6
12	V20	-6632.5	-234.6	44	AVDD	-4712.5	-234.6	76	VDD	-2792.5	-234.6
13	V20	-6572.5	-234.6	45	AVDD	-4652.5	-234.6	77	VDD	-2732.5	-234.6
14	VDD	-6512.5	-234.6	46	VAN	-4592.5	-234.6	78	VDD	-2672.5	-234.6
15	VDD	-6452.5	-234.6	47	VAN	-4532.5	-234.6	79	VDD	-2612.5	-234.6
16	AGND	-6392.5	-234.6	48	DUMMY	-4472.5	-234.6	80	VDD	-2552.5	-234.6
17	AGND	-6332.5	-234.6	49	DUMMY	-4412.5	-234.6	81	VDD	-2492.5	-234.6
18	DUMMY	-6272.5	-234.6	50	DUMMY	-4352.5	-234.6	82	AGND	-2432.5	-234.6
19	DUMMY	-6212.5	-234.6	51	DUMMY	-4292.5	-234.6	83	AGND	-2372.5	-234.6
20	VDD	-6152.5	-234.6	52	DUMMY	-4232.5	-234.6	84	AGND	-2312.5	-234.6
21	VDD	-6092.5	-234.6	53	DUMMY	-4172.5	-234.6	85	AGND	-2252.5	-234.6
22	VDD	-6032.5	-234.6	54	DUMMY	-4112.5	-234.6	86	AGND	-2192.5	-234.6
23	VDD	-5972.5	-234.6	55	DUMMY	-4052.5	-234.6	87	AGND	-2132.5	-234.6
24	VDD	-5912.5	-234.6	56	DUMMY	-3992.5	-234.6	88	AGND	-2072.5	-234.6
25	DUMMY	-5852.5	-234.6	57	DUMMY	-3932.5	-234.6	89	AGND	-2012.5	-234.6
26	VGL	-5792.5	-234.6	58	VAP	-3872.5	-234.6	90	AGND	-1952.5	-234.6
27	VGL	-5732.5	-234.6	59	VAP	-3812.5	-234.6	91	AGND	-1892.5	-234.6
28	VGL	-5672.5	-234.6	60	VAG	-3752.5	-234.6	92	AGND	-1832.5	-234.6
29	VGL	-5612.5	-234.6	61	VAG	-3692.5	-234.6	93	AGND	-1772.5	-234.6
30	VGL	-5552.5	-234.6	62	VAG	-3632.5	-234.6	94	AGND	-1712.5	-234.6
31	VGL	-5492.5	-234.6	63	VAG	-3572.5	-234.6	95	AGND	-1652.5	-234.6
32	AVCL	-5432.5	-234.6	64	VAG	-3512.5	-234.6	96	AGND	-1592.5	-234.6

PAD No.	PIN Name	X	Y
97	AGND	-1532.5	-234.6
98	DGND	-1472.5	-234.6
99	DGND	-1412.5	-234.6
100	DGND	-1352.5	-234.6
101	DGND	-1292.5	-234.6
102	DGND	-1232.5	-234.6
103	DGND	-1172.5	-234.6
104	DGND	-1112.5	-234.6
105	DGND	-1052.5	-234.6
106	TEST3	-992.5	-234.6
107	DUMMY	-932.5	-234.6
108	DUMMY	-872.5	-234.6
109	EXTC	-812.5	-234.6
110	IM3	-752.5	-234.6
111	IM2	-692.5	-234.6
112	IM1	-632.5	-234.6
113	IM0	-572.5	-234.6
114	RESX	-512.5	-234.6
115	CSX	-452.5	-234.6
116	DCX	-392.5	-234.6
117	WRX	-332.5	-234.6
118	RDX	-272.5	-234.6
119	TEST2	-212.5	-234.6
120	VSYNC	-152.5	-234.6
121	HSYNC	-92.5	-234.6
122	ENABLE	-32.5	-234.6
123	DOTCLK	27.5	-234.6
124	DUMMY	87.5	-234.6
125	SDA	160	-234.6
126	DB0	245	-234.6
127	DB1	330	-234.6
128	DB2	415	-234.6
129	DB3	500	-234.6
130	TEST1	572.5	-234.6

PAD No.	PIN Name	X	Y
131	DB4	645	-234.6
132	DB5	730	-234.6
133	DB6	815	-234.6
134	DB7	900	-234.6
135	DUMMY	972.5	-234.6
136	DB8	1045	-234.6
137	TESTO0	1130	-234.6
138	D0P	1215	-234.6
139	D0P	1300	-234.6
140	DUMMY	1372.5	-234.6
141	D0N	1445	-234.6
142	D0N	1530	-234.6
143	CLKP	1615	-234.6
144	CLKP	1700	-234.6
145	DUMMY	1772.5	-234.6
146	CLKN	1845	-234.6
147	CLKN	1930	-234.6
148	TEST0	2002.5	-234.6
149	TE	2075	-234.6
150	SDO	2160	-234.6
151	LED_PWM	2245	-234.6
152	LED_EN	2330	-234.6
153	VDDI_LED	2402.5	-234.6
154	VDDI_LED	2462.5	-234.6
155	TE2	2535	-234.6
156	TESTO1	2620	-234.6
157	TESTO2	2705	-234.6
158	TESTO3	2790	-234.6
159	TESTO4	2875	-234.6
160	TESTO5	2960	-234.6
161	TESTO6	3032.5	-234.6
162	VDDI	3092.5	-234.6
163	VDDI	3152.5	-234.6
164	VDDI	3212.5	-234.6

PAD No.	PIN Name	X	Y
165	VDDI	3272.5	-234.6
166	VDDI	3332.5	-234.6
167	VDDI	3392.5	-234.6
168	VDDI	3452.5	-234.6
169	VCC	3512.5	-234.6
170	VCC	3572.5	-234.6
171	VCC	3632.5	-234.6
172	VCC	3692.5	-234.6
173	VCC	3752.5	-234.6
174	VCC	3812.5	-234.6
175	VCC	3872.5	-234.6
176	VCC	3932.5	-234.6
177	VCC	3992.5	-234.6
178	VCC	4052.5	-234.6
179	VCC	4112.5	-234.6
180	VCC	4172.5	-234.6
181	VCC	4232.5	-234.6
182	VCC	4292.5	-234.6
183	DUMMY	4352.5	-234.6
184	VPP	4412.5	-234.6
185	VPP	4472.5	-234.6
186	VPP	4532.5	-234.6
187	VPP	4592.5	-234.6
188	DUMMY	4652.5	-234.6
189	DUMMY	4712.5	-234.6
190	VGH	4772.5	-234.6
191	VGH	4832.5	-234.6
192	VGH	4892.5	-234.6
193	VGH	4952.5	-234.6
194	VGH	5012.5	-234.6
195	VGH	5072.5	-234.6
196	VGH	5132.5	-234.6
197	VGH	5192.5	-234.6
198	VDD	5252.5	-234.6

PAD No.	PIN Name	X	Y
199	VDD	5312.5	-234.6
200	VDD	5372.5	-234.6
201	VDD	5432.5	-234.6
202	VDD	5492.5	-234.6
203	VDD	5552.5	-234.6
204	VDD	5612.5	-234.6
205	VDD	5672.5	-234.6
206	AGND	5732.5	-234.6
207	AGND	5792.5	-234.6
208	AGND	5852.5	-234.6
209	AGND	5912.5	-234.6
210	AGND	5972.5	-234.6
211	AGND	6032.5	-234.6
212	AGND	6092.5	-234.6
213	AGND	6152.5	-234.6
214	DUMMYR1	6212.5	-234.6
215	DUMMYR2	6272.5	-234.6
216	DUMMY	6332.5	-234.6
217	DUMMY	6392.5	-234.6
218	DUMMY	6452.5	-234.6
219	DUMMY	6512.5	-234.6
220	DUMMY	6572.5	-234.6
221	DUMMY	6632.5	-234.6
222	DUMMY	6692.5	-234.6
223	VCOM	6752.5	-234.6
224	VCOM	6812.5	-234.6
225	VCOM	6872.5	-234.6
226	VCOM	6932.5	-234.6
227	VCOM	6992.5	-234.6
228	VCOM	7052.5	-234.6
229	VCOM	7112.5	-234.6
230	VCOM	7172.5	-234.6
231	DUMMY	7232.5	-234.6
232	DUMMY	7292.5	-234.6

PAD No.	PIN Name	X	Y
233	DUMMY	7399	220.5
234	DUMMY	7385	129.5
235	DUMMY	7371	220.5
236	G2	7357	129.5
237	G4	7343	220.5
238	G6	7329	129.5
239	G8	7315	220.5
240	G10	7301	129.5
241	G12	7287	220.5
242	G14	7273	129.5
243	G16	7259	220.5
244	G18	7245	129.5
245	G20	7231	220.5
246	G22	7217	129.5
247	G24	7203	220.5
248	G26	7189	129.5
249	G28	7175	220.5
250	G30	7161	129.5
251	G32	7147	220.5
252	G34	7133	129.5
253	G36	7119	220.5
254	G38	7105	129.5
255	G40	7091	220.5
256	G42	7077	129.5
257	G44	7063	220.5
258	G46	7049	129.5
259	G48	7035	220.5
260	G50	7021	129.5
261	G52	7007	220.5
262	G54	6993	129.5
263	G56	6979	220.5
264	G58	6965	129.5
265	G60	6951	220.5
266	G62	6937	129.5

PAD No.	PIN Name	X	Y
267	G64	6923	220.5
268	G66	6909	129.5
269	G68	6895	220.5
270	G70	6881	129.5
271	G72	6867	220.5
272	G74	6853	129.5
273	G76	6839	220.5
274	G78	6825	129.5
275	G80	6811	220.5
276	G82	6797	129.5
277	G84	6783	220.5
278	G86	6769	129.5
279	G88	6755	220.5
280	G90	6741	129.5
281	G92	6727	220.5
282	G94	6713	129.5
283	G96	6699	220.5
284	G98	6685	129.5
285	G100	6671	220.5
286	G102	6657	129.5
287	G104	6643	220.5
288	G106	6629	129.5
289	G108	6615	220.5
290	G110	6601	129.5
291	G112	6587	220.5
292	G114	6573	129.5
293	G116	6559	220.5
294	G118	6545	129.5
295	G120	6531	220.5
296	G122	6517	129.5
297	G124	6503	220.5
298	G126	6489	129.5
299	G128	6475	220.5
300	G130	6461	129.5

PAD No.	PIN Name	X	Y
301	G132	6447	220.5
302	G134	6433	129.5
303	G136	6419	220.5
304	G138	6405	129.5
305	G140	6391	220.5
306	G142	6377	129.5
307	G144	6363	220.5
308	G146	6349	129.5
309	G148	6335	220.5
310	G150	6321	129.5
311	G152	6307	220.5
312	G154	6293	129.5
313	G156	6279	220.5
314	G158	6265	129.5
315	G160	6251	220.5
316	G162	6237	129.5
317	G164	6223	220.5
318	G166	6209	129.5
319	G168	6195	220.5
320	G170	6181	129.5
321	G172	6167	220.5
322	G174	6153	129.5
323	G176	6139	220.5
324	G178	6125	129.5
325	G180	6111	220.5
326	G182	6097	129.5
327	G184	6083	220.5
328	G186	6069	129.5
329	G188	6055	220.5
330	G190	6041	129.5
331	G192	6027	220.5
332	G194	6013	129.5
333	G196	5999	220.5
334	G198	5985	129.5
335	G200	5971	220.5
336	G202	5957	129.5
337	G204	5943	220.5
338	G206	5929	129.5
339	G208	5915	220.5
340	G210	5901	129.5
341	G212	5887	220.5
342	G214	5873	129.5
343	G216	5859	220.5
344	G218	5845	129.5
345	G220	5831	220.5
346	G222	5817	129.5
347	G224	5803	220.5
348	G226	5789	129.5
349	G228	5775	220.5
350	G230	5761	129.5
351	G232	5747	220.5
352	G234	5733	129.5
353	G236	5719	220.5
354	G238	5705	129.5
355	G240	5691	220.5
356	G242	5677	129.5
357	G244	5663	220.5
358	G246	5649	129.5
359	G248	5635	220.5
360	G250	5621	129.5
361	G252	5607	220.5
362	G254	5593	129.5
363	G256	5579	220.5
364	G258	5565	129.5
365	G260	5551	220.5
366	G262	5537	129.5
367	G264	5523	220.5
368	G266	5509	129.5
369	G268	5495	220.5
370	G270	5481	129.5
371	G272	5467	220.5
372	G274	5453	129.5
373	G276	5439	220.5
374	G278	5425	129.5
375	G280	5411	220.5
376	G282	5397	129.5
377	G284	5383	220.5
378	G286	5369	129.5
379	G288	5355	220.5
380	G290	5341	129.5
381	G292	5327	220.5
382	G294	5313	129.5
383	G296	5299	220.5
384	G298	5285	129.5
385	G300	5271	220.5
386	G302	5257	129.5
387	G304	5243	220.5
388	G306	5229	129.5
389	G308	5215	220.5
390	G310	5201	129.5
391	G312	5187	220.5
392	G314	5173	129.5
393	G316	5159	220.5
394	G318	5145	129.5
395	G320	5131	220.5
396	S720	5075	124
397	S719	5061	215
398	S718	5047	124
399	S717	5033	215
400	S716	5019	124
401	S715	5005	215
402	S714	4991	124

PAD No.	PIN Name	X	Y
403	S713	4977	215
404	S712	4963	124
405	S711	4949	215
406	S710	4935	124
407	S709	4921	215
408	S708	4907	124
409	S707	4893	215
410	S706	4879	124
411	S705	4865	215
412	S704	4851	124
413	S703	4837	215
414	S702	4823	124
415	S701	4809	215
416	S700	4795	124
417	S699	4781	215
418	S698	4767	124
419	S697	4753	215
420	S696	4739	124
421	S695	4725	215
422	S694	4711	124
423	S693	4697	215
424	S692	4683	124
425	S691	4669	215
426	S690	4655	124
427	S689	4641	215
428	S688	4627	124
429	S687	4613	215
430	S686	4599	124
431	S685	4585	215
432	S684	4571	124
433	S683	4557	215
434	S682	4543	124
435	S681	4529	215
436	S680	4515	124

PAD No.	PIN Name	X	Y
437	S679	4501	215
438	S678	4487	124
439	S677	4473	215
440	S676	4459	124
441	S675	4445	215
442	S674	4431	124
443	S673	4417	215
444	S672	4403	124
445	S671	4389	215
446	S670	4375	124
447	S669	4361	215
448	S668	4347	124
449	S667	4333	215
450	S666	4319	124
451	S665	4305	215
452	S664	4291	124
453	S663	4277	215
454	S662	4263	124
455	S661	4249	215
456	S660	4235	124
457	S659	4221	215
458	S658	4207	124
459	S657	4193	215
460	S656	4179	124
461	S655	4165	215
462	S654	4151	124
463	S653	4137	215
464	S652	4123	124
465	S651	4109	215
466	S650	4095	124
467	S649	4081	215
468	S648	4067	124
469	S647	4053	215
470	S646	4039	124

PAD No.	PIN Name	X	Y
471	S645	4025	215
472	S644	4011	124
473	S643	3997	215
474	S642	3983	124
475	S641	3969	215
476	S640	3955	124
477	S639	3941	215
478	S638	3927	124
479	S637	3913	215
480	S636	3899	124
481	S635	3885	215
482	S634	3871	124
483	S633	3857	215
484	S632	3843	124
485	S631	3829	215
486	S630	3815	124
487	S629	3801	215
488	S628	3787	124
489	S627	3773	215
490	S626	3759	124
491	S625	3745	215
492	S624	3731	124
493	S623	3717	215
494	S622	3703	124
495	S621	3689	215
496	S620	3675	124
497	S619	3661	215
498	S618	3647	124
499	S617	3633	215
500	S616	3619	124
501	S615	3605	215
502	S614	3591	124
503	S613	3577	215
504	S612	3563	124

PAD No.	PIN Name	X	Y
505	S611	3549	215
506	S610	3535	124
507	S609	3521	215
508	S608	3507	124
509	S607	3493	215
510	S606	3479	124
511	S605	3465	215
512	S604	3451	124
513	S603	3437	215
514	S602	3423	124
515	S601	3409	215
516	S600	3395	124
517	S599	3381	215
518	S598	3367	124
519	S597	3353	215
520	S596	3339	124
521	S595	3325	215
522	S594	3311	124
523	S593	3297	215
524	S592	3283	124
525	S591	3269	215
526	S590	3255	124
527	S589	3241	215
528	S588	3227	124
529	S587	3213	215
530	S586	3199	124
531	S585	3185	215
532	S584	3171	124
533	S583	3157	215
534	S582	3143	124
535	S581	3129	215
536	S580	3115	124
537	S579	3101	215
538	S578	3087	124
539	S577	3073	215
540	S576	3059	124
541	S575	3045	215
542	S574	3031	124
543	S573	3017	215
544	S572	3003	124
545	S571	2989	215
546	S570	2975	124
547	S569	2961	215
548	S568	2947	124
549	S567	2933	215
550	S566	2919	124
551	S565	2905	215
552	S564	2891	124
553	S563	2877	215
554	S562	2863	124
555	S561	2849	215
556	S560	2835	124
557	S559	2821	215
558	S558	2807	124
559	S557	2793	215
560	S556	2779	124
561	S555	2765	215
562	S554	2751	124
563	S553	2737	215
564	S552	2723	124
565	S551	2709	215
566	S550	2695	124
567	S549	2681	215
568	S548	2667	124
569	S547	2653	215
570	S546	2639	124
571	S545	2625	215
572	S544	2611	124
573	S543	2597	215
574	S542	2583	124
575	S541	2569	215
576	S540	2555	124
577	S539	2541	215
578	S538	2527	124
579	S537	2513	215
580	S536	2499	124
581	S535	2485	215
582	S534	2471	124
583	S533	2457	215
584	S532	2443	124
585	S531	2429	215
586	S530	2415	124
587	S529	2401	215
588	S528	2387	124
589	S527	2373	215
590	S526	2359	124
591	S525	2345	215
592	S524	2331	124
593	S523	2317	215
594	S522	2303	124
595	S521	2289	215
596	S520	2275	124
597	S519	2261	215
598	S518	2247	124
599	S517	2233	215
600	S516	2219	124
601	S515	2205	215
602	S514	2191	124
603	S513	2177	215
604	S512	2163	124
605	S511	2149	215
606	S510	2135	124

PAD No.	PIN Name	X	Y
607	S509	2121	215
608	S508	2107	124
609	S507	2093	215
610	S506	2079	124
611	S505	2065	215
612	S504	2051	124
613	S503	2037	215
614	S502	2023	124
615	S501	2009	215
616	S500	1995	124
617	S499	1981	215
618	S498	1967	124
619	S497	1953	215
620	S496	1939	124
621	S495	1925	215
622	S494	1911	124
623	S493	1897	215
624	S492	1883	124
625	S491	1869	215
626	S490	1855	124
627	S489	1841	215
628	S488	1827	124
629	S487	1813	215
630	S486	1799	124
631	S485	1785	215
632	S484	1771	124
633	S483	1757	215
634	S482	1743	124
635	S481	1729	215
636	S480	1715	124
637	S479	1701	215
638	S478	1687	124
639	S477	1673	215
640	S476	1659	124

PAD No.	PIN Name	X	Y
641	S475	1645	215
642	S474	1631	124
643	S473	1617	215
644	S472	1603	124
645	S471	1589	215
646	S470	1575	124
647	S469	1561	215
648	S468	1547	124
649	S467	1533	215
650	S466	1519	124
651	S465	1505	215
652	S464	1491	124
653	S463	1477	215
654	S462	1463	124
655	S461	1449	215
656	S460	1435	124
657	S459	1421	215
658	S458	1407	124
659	S457	1393	215
660	S456	1379	124
661	S455	1365	215
662	S454	1351	124
663	S453	1337	215
664	S452	1323	124
665	S451	1309	215
666	S450	1295	124
667	S449	1281	215
668	S448	1267	124
669	S447	1253	215
670	S446	1239	124
671	S445	1225	215
672	S444	1211	124
673	S443	1197	215
674	S442	1183	124

PAD No.	PIN Name	X	Y
675	S441	1169	215
676	S440	1155	124
677	S439	1141	215
678	S438	1127	124
679	S437	1113	215
680	S436	1099	124
681	S435	1085	215
682	S434	1071	124
683	S433	1057	215
684	S432	1043	124
685	S431	1029	215
686	S430	1015	124
687	S429	1001	215
688	S428	987	124
689	S427	973	215
690	S426	959	124
691	S425	945	215
692	S424	931	124
693	S423	917	215
694	S422	903	124
695	S421	889	215
696	S420	875	124
697	S419	861	215
698	S418	847	124
699	S417	833	215
700	S416	819	124
701	S415	805	215
702	S414	791	124
703	S413	777	215
704	S412	763	124
705	S411	749	215
706	S410	735	124
707	S409	721	215
708	S408	707	124

PAD No.	PIN Name	X	Y
709	S407	693	215
710	S406	679	124
711	S405	665	215
712	S404	651	124
713	S403	637	215
714	S402	623	124
715	S401	609	215
716	S400	595	124
717	S399	581	215
718	S398	567	124
719	S397	553	215
720	S396	539	124
721	S395	525	215
722	S394	511	124
723	S393	497	215
724	S392	483	124
725	S391	469	215
726	S390	455	124
727	S389	441	215
728	S388	427	124
729	S387	413	215
730	S386	399	124
731	S385	385	215
732	S384	371	124
733	S383	357	215
734	S382	343	124
735	S381	329	215
736	S380	315	124
737	S379	301	215
738	S378	287	124
739	S377	273	215
740	S376	259	124
741	S375	245	215
742	S374	231	124
743	S373	217	215
744	S372	203	124
745	S371	189	215
746	S370	175	124
747	S369	161	215
748	S368	147	124
749	S367	133	215
750	S366	119	124
751	S365	105	215
752	S364	91	124
753	S363	77	215
754	S362	63	124
755	S361	49	215
756	S360	-49	124
757	S359	-63	215
758	S358	-77	124
759	S357	-91	215
760	S356	-105	124
761	S355	-119	215
762	S354	-133	124
763	S353	-147	215
764	S352	-161	124
765	S351	-175	215
766	S350	-189	124
767	S349	-203	215
768	S348	-217	124
769	S347	-231	215
770	S346	-245	124
771	S345	-259	215
772	S344	-273	124
773	S343	-287	215
774	S342	-301	124
775	S341	-315	215
776	S340	-329	124
777	S339	-343	215
778	S338	-357	124
779	S337	-371	215
780	S336	-385	124
781	S335	-399	215
782	S334	-413	124
783	S333	-427	215
784	S332	-441	124
785	S331	-455	215
786	S330	-469	124
787	S329	-483	215
788	S328	-497	124
789	S327	-511	215
790	S326	-525	124
791	S325	-539	215
792	S324	-553	124
793	S323	-567	215
794	S322	-581	124
795	S321	-595	215
796	S320	-609	124
797	S319	-623	215
798	S318	-637	124
799	S317	-651	215
800	S316	-665	124
801	S315	-679	215
802	S314	-693	124
803	S313	-707	215
804	S312	-721	124
805	S311	-735	215
806	S310	-749	124
807	S309	-763	215
808	S308	-777	124
809	S307	-791	215
810	S306	-805	124

PAD No.	PIN Name	X	Y
811	S305	-819	215
812	S304	-833	124
813	S303	-847	215
814	S302	-861	124
815	S301	-875	215
816	S300	-889	124
817	S299	-903	215
818	S298	-917	124
819	S297	-931	215
820	S296	-945	124
821	S295	-959	215
822	S294	-973	124
823	S293	-987	215
824	S292	-1001	124
825	S291	-1015	215
826	S290	-1029	124
827	S289	-1043	215
828	S288	-1057	124
829	S287	-1071	215
830	S286	-1085	124
831	S285	-1099	215
832	S284	-1113	124
833	S283	-1127	215
834	S282	-1141	124
835	S281	-1155	215
836	S280	-1169	124
837	S279	-1183	215
838	S278	-1197	124
839	S277	-1211	215
840	S276	-1225	124
841	S275	-1239	215
842	S274	-1253	124
843	S273	-1267	215
844	S272	-1281	124

PAD No.	PIN Name	X	Y
845	S271	-1295	215
846	S270	-1309	124
847	S269	-1323	215
848	S268	-1337	124
849	S267	-1351	215
850	S266	-1365	124
851	S265	-1379	215
852	S264	-1393	124
853	S263	-1407	215
854	S262	-1421	124
855	S261	-1435	215
856	S260	-1449	124
857	S259	-1463	215
858	S258	-1477	124
859	S257	-1491	215
860	S256	-1505	124
861	S255	-1519	215
862	S254	-1533	124
863	S253	-1547	215
864	S252	-1561	124
865	S251	-1575	215
866	S250	-1589	124
867	S249	-1603	215
868	S248	-1617	124
869	S247	-1631	215
870	S246	-1645	124
871	S245	-1659	215
872	S244	-1673	124
873	S243	-1687	215
874	S242	-1701	124
875	S241	-1715	215
876	S240	-1729	124
877	S239	-1743	215
878	S238	-1757	124

PAD No.	PIN Name	X	Y
879	S237	-1771	215
880	S236	-1785	124
881	S235	-1799	215
882	S234	-1813	124
883	S233	-1827	215
884	S232	-1841	124
885	S231	-1855	215
886	S230	-1869	124
887	S229	-1883	215
888	S228	-1897	124
889	S227	-1911	215
890	S226	-1925	124
891	S225	-1939	215
892	S224	-1953	124
893	S223	-1967	215
894	S222	-1981	124
895	S221	-1995	215
896	S220	-2009	124
897	S219	-2023	215
898	S218	-2037	124
899	S217	-2051	215
900	S216	-2065	124
901	S215	-2079	215
902	S214	-2093	124
903	S213	-2107	215
904	S212	-2121	124
905	S211	-2135	215
906	S210	-2149	124
907	S209	-2163	215
908	S208	-2177	124
909	S207	-2191	215
910	S206	-2205	124
911	S205	-2219	215
912	S204	-2233	124

PAD No.	PIN Name	X	Y
913	S203	-2247	215
914	S202	-2261	124
915	S201	-2275	215
916	S200	-2289	124
917	S199	-2303	215
918	S198	-2317	124
919	S197	-2331	215
920	S196	-2345	124
921	S195	-2359	215
922	S194	-2373	124
923	S193	-2387	215
924	S192	-2401	124
925	S191	-2415	215
926	S190	-2429	124
927	S189	-2443	215
928	S188	-2457	124
929	S187	-2471	215
930	S186	-2485	124
931	S185	-2499	215
932	S184	-2513	124
933	S183	-2527	215
934	S182	-2541	124
935	S181	-2555	215
936	S180	-2569	124
937	S179	-2583	215
938	S178	-2597	124
939	S177	-2611	215
940	S176	-2625	124
941	S175	-2639	215
942	S174	-2653	124
943	S173	-2667	215
944	S172	-2681	124
945	S171	-2695	215
946	S170	-2709	124

PAD No.	PIN Name	X	Y
947	S169	-2723	215
948	S168	-2737	124
949	S167	-2751	215
950	S166	-2765	124
951	S165	-2779	215
952	S164	-2793	124
953	S163	-2807	215
954	S162	-2821	124
955	S161	-2835	215
956	S160	-2849	124
957	S159	-2863	215
958	S158	-2877	124
959	S157	-2891	215
960	S156	-2905	124
961	S155	-2919	215
962	S154	-2933	124
963	S153	-2947	215
964	S152	-2961	124
965	S151	-2975	215
966	S150	-2989	124
967	S149	-3003	215
968	S148	-3017	124
969	S147	-3031	215
970	S146	-3045	124
971	S145	-3059	215
972	S144	-3073	124
973	S143	-3087	215
974	S142	-3101	124
975	S141	-3115	215
976	S140	-3129	124
977	S139	-3143	215
978	S138	-3157	124
979	S137	-3171	215
980	S136	-3185	124

PAD No.	PIN Name	X	Y
981	S135	-3199	215
982	S134	-3213	124
983	S133	-3227	215
984	S132	-3241	124
985	S131	-3255	215
986	S130	-3269	124
987	S129	-3283	215
988	S128	-3297	124
989	S127	-3311	215
990	S126	-3325	124
991	S125	-3339	215
992	S124	-3353	124
993	S123	-3367	215
994	S122	-3381	124
995	S121	-3395	215
996	S120	-3409	124
997	S119	-3423	215
998	S118	-3437	124
999	S117	-3451	215
1000	S116	-3465	124
1001	S115	-3479	215
1002	S114	-3493	124
1003	S113	-3507	215
1004	S112	-3521	124
1005	S111	-3535	215
1006	S110	-3549	124
1007	S109	-3563	215
1008	S108	-3577	124
1009	S107	-3591	215
1010	S106	-3605	124
1011	S105	-3619	215
1012	S104	-3633	124
1013	S103	-3647	215
1014	S102	-3661	124

PAD No.	PIN Name	X	Y
1015	S101	-3675	215
1016	S100	-3689	124
1017	S99	-3703	215
1018	S98	-3717	124
1019	S97	-3731	215
1020	S96	-3745	124
1021	S95	-3759	215
1022	S94	-3773	124
1023	S93	-3787	215
1024	S92	-3801	124
1025	S91	-3815	215
1026	S90	-3829	124
1027	S89	-3843	215
1028	S88	-3857	124
1029	S87	-3871	215
1030	S86	-3885	124
1031	S85	-3899	215
1032	S84	-3913	124
1033	S83	-3927	215
1034	S82	-3941	124
1035	S81	-3955	215
1036	S80	-3969	124
1037	S79	-3983	215
1038	S78	-3997	124
1039	S77	-4011	215
1040	S76	-4025	124
1041	S75	-4039	215
1042	S74	-4053	124
1043	S73	-4067	215
1044	S72	-4081	124
1045	S71	-4095	215
1046	S70	-4109	124
1047	S69	-4123	215
1048	S68	-4137	124

PAD No.	PIN Name	X	Y
1049	S67	-4151	215
1050	S66	-4165	124
1051	S65	-4179	215
1052	S64	-4193	124
1053	S63	-4207	215
1054	S62	-4221	124
1055	S61	-4235	215
1056	S60	-4249	124
1057	S59	-4263	215
1058	S58	-4277	124
1059	S57	-4291	215
1060	S56	-4305	124
1061	S55	-4319	215
1062	S54	-4333	124
1063	S53	-4347	215
1064	S52	-4361	124
1065	S51	-4375	215
1066	S50	-4389	124
1067	S49	-4403	215
1068	S48	-4417	124
1069	S47	-4431	215
1070	S46	-4445	124
1071	S45	-4459	215
1072	S44	-4473	124
1073	S43	-4487	215
1074	S42	-4501	124
1075	S41	-4515	215
1076	S40	-4529	124
1077	S39	-4543	215
1078	S38	-4557	124
1079	S37	-4571	215
1080	S36	-4585	124
1081	S35	-4599	215
1082	S34	-4613	124

PAD No.	PIN Name	X	Y
1083	S33	-4627	215
1084	S32	-4641	124
1085	S31	-4655	215
1086	S30	-4669	124
1087	S29	-4683	215
1088	S28	-4697	124
1089	S27	-4711	215
1090	S26	-4725	124
1091	S25	-4739	215
1092	S24	-4753	124
1093	S23	-4767	215
1094	S22	-4781	124
1095	S21	-4795	215
1096	S20	-4809	124
1097	S19	-4823	215
1098	S18	-4837	124
1099	S17	-4851	215
1100	S16	-4865	124
1101	S15	-4879	215
1102	S14	-4893	124
1103	S13	-4907	215
1104	S12	-4921	124
1105	S11	-4935	215
1106	S10	-4949	124
1107	S9	-4963	215
1108	S8	-4977	124
1109	S7	-4991	215
1110	S6	-5005	124
1111	S5	-5019	215
1112	S4	-5033	124
1113	S3	-5047	215
1114	S2	-5061	124
1115	S1	-5075	215
1116	G319	-5131	129.5

PAD No.	PIN Name	X	Y
1117	G317	-5145	220.5
1118	G315	-5159	129.5
1119	G313	-5173	220.5
1120	G311	-5187	129.5
1121	G309	-5201	220.5
1122	G307	-5215	129.5
1123	G305	-5229	220.5
1124	G303	-5243	129.5
1125	G301	-5257	220.5
1126	G299	-5271	129.5
1127	G297	-5285	220.5
1128	G295	-5299	129.5
1129	G293	-5313	220.5
1130	G291	-5327	129.5
1131	G289	-5341	220.5
1132	G287	-5355	129.5
1133	G285	-5369	220.5
1134	G283	-5383	129.5
1135	G281	-5397	220.5
1136	G279	-5411	129.5
1137	G277	-5425	220.5
1138	G275	-5439	129.5
1139	G273	-5453	220.5
1140	G271	-5467	129.5
1141	G269	-5481	220.5
1142	G267	-5495	129.5
1143	G265	-5509	220.5
1144	G263	-5523	129.5
1145	G261	-5537	220.5
1146	G259	-5551	129.5
1147	G257	-5565	220.5
1148	G255	-5579	129.5
1149	G253	-5593	220.5
1150	G251	-5607	129.5

PAD No.	PIN Name	X	Y
1151	G249	-5621	220.5
1152	G247	-5635	129.5
1153	G245	-5649	220.5
1154	G243	-5663	129.5
1155	G241	-5677	220.5
1156	G239	-5691	129.5
1157	G237	-5705	220.5
1158	G235	-5719	129.5
1159	G233	-5733	220.5
1160	G231	-5747	129.5
1161	G229	-5761	220.5
1162	G227	-5775	129.5
1163	G225	-5789	220.5
1164	G223	-5803	129.5
1165	G221	-5817	220.5
1166	G219	-5831	129.5
1167	G217	-5845	220.5
1168	G215	-5859	129.5
1169	G213	-5873	220.5
1170	G211	-5887	129.5
1171	G209	-5901	220.5
1172	G207	-5915	129.5
1173	G205	-5929	220.5
1174	G203	-5943	129.5
1175	G201	-5957	220.5
1176	G199	-5971	129.5
1177	G197	-5985	220.5
1178	G195	-5999	129.5
1179	G193	-6013	220.5
1180	G191	-6027	129.5
1181	G189	-6041	220.5
1182	G187	-6055	129.5
1183	G185	-6069	220.5
1184	G183	-6083	129.5

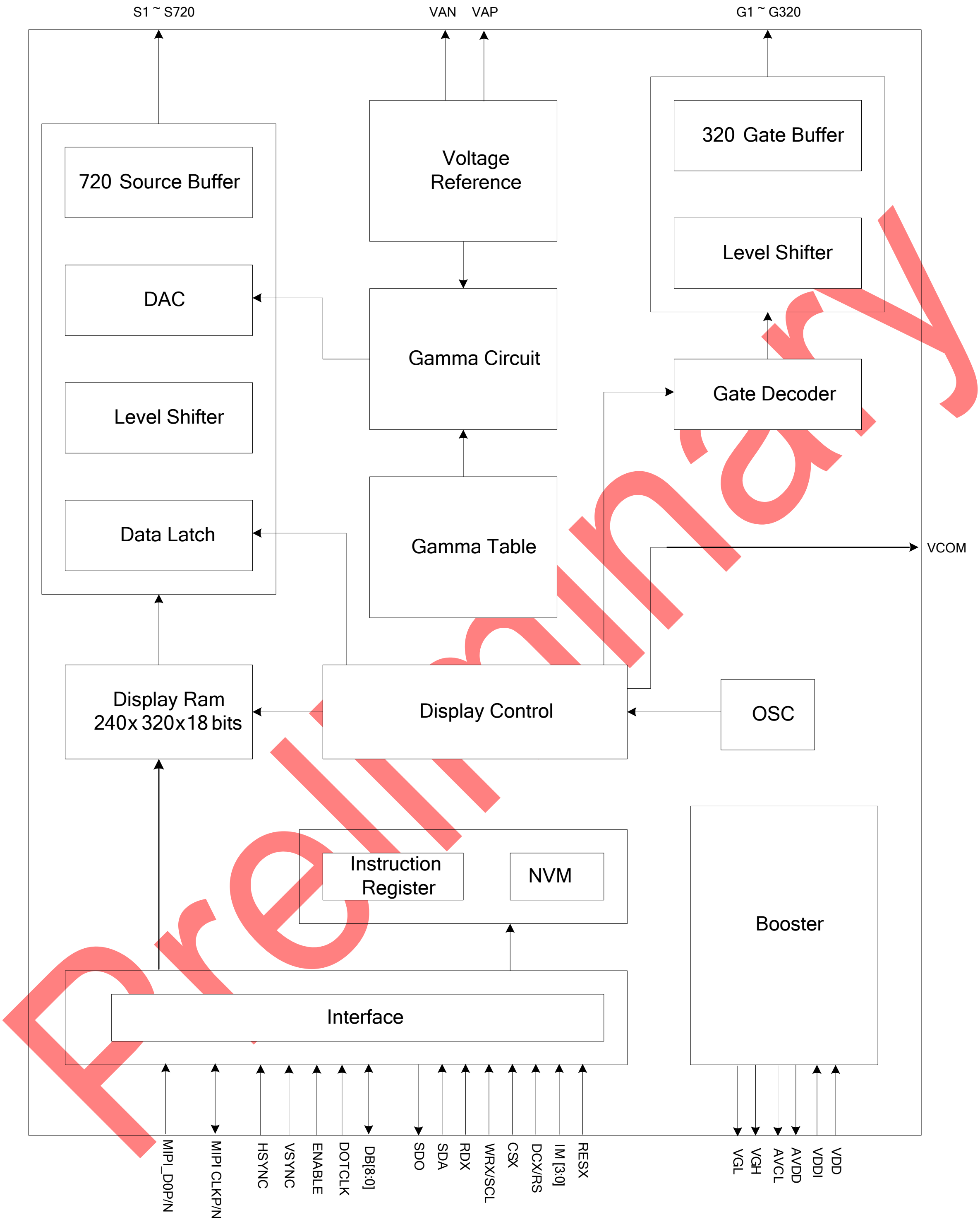
PAD No.	PIN Name	X	Y
1185	G181	-6097	220.5
1186	G179	-6111	129.5
1187	G177	-6125	220.5
1188	G175	-6139	129.5
1189	G173	-6153	220.5
1190	G171	-6167	129.5
1191	G169	-6181	220.5
1192	G167	-6195	129.5
1193	G165	-6209	220.5
1194	G163	-6223	129.5
1195	G161	-6237	220.5
1196	G159	-6251	129.5
1197	G157	-6265	220.5
1198	G155	-6279	129.5
1199	G153	-6293	220.5
1200	G151	-6307	129.5
1201	G149	-6321	220.5
1202	G147	-6335	129.5
1203	G145	-6349	220.5
1204	G143	-6363	129.5
1205	G141	-6377	220.5
1206	G139	-6391	129.5
1207	G137	-6405	220.5
1208	G135	-6419	129.5
1209	G133	-6433	220.5
1210	G131	-6447	129.5
1211	G129	-6461	220.5
1212	G127	-6475	129.5
1213	G125	-6489	220.5
1214	G123	-6503	129.5
1215	G121	-6517	220.5
1216	G119	-6531	129.5
1217	G117	-6545	220.5
1218	G115	-6559	129.5

PAD No.	PIN Name	X	Y
1219	G113	-6573	220.5
1220	G111	-6587	129.5
1221	G109	-6601	220.5
1222	G107	-6615	129.5
1223	G105	-6629	220.5
1224	G103	-6643	129.5
1225	G101	-6657	220.5
1226	G99	-6671	129.5
1227	G97	-6685	220.5
1228	G95	-6699	129.5
1229	G93	-6713	220.5
1230	G91	-6727	129.5
1231	G89	-6741	220.5
1232	G87	-6755	129.5
1233	G85	-6769	220.5
1234	G83	-6783	129.5
1235	G81	-6797	220.5
1236	G79	-6811	129.5
1237	G77	-6825	220.5
1238	G75	-6839	129.5
1239	G73	-6853	220.5

PAD No.	PIN Name	X	Y
1240	G71	-6867	129.5
1241	G69	-6881	220.5
1242	G67	-6895	129.5
1243	G65	-6909	220.5
1244	G63	-6923	129.5
1245	G61	-6937	220.5
1246	G59	-6951	129.5
1247	G57	-6965	220.5
1248	G55	-6979	129.5
1249	G53	-6993	220.5
1250	G51	-7007	129.5
1251	G49	-7021	220.5
1252	G47	-7035	129.5
1253	G45	-7049	220.5
1254	G43	-7063	129.5
1255	G41	-7077	220.5
1256	G39	-7091	129.5
1257	G37	-7105	220.5
1258	G35	-7119	129.5
1259	G33	-7133	220.5
1260	G31	-7147	129.5

PAD No.	PIN Name	X	Y
1261	G29	-7161	220.5
1262	G27	-7175	129.5
1263	G25	-7189	220.5
1264	G23	-7203	129.5
1265	G21	-7217	220.5
1266	G19	-7231	129.5
1267	G17	-7245	220.5
1268	G15	-7259	129.5
1269	G13	-7273	220.5
1270	G11	-7287	129.5
1271	G9	-7301	220.5
1272	G7	-7315	129.5
1273	G5	-7329	220.5
1274	G3	-7343	129.5
1275	G1	-7357	220.5
1276	DUMMY	-7371	129.5
1277	DUMMY	-7385	220.5
1278	DUMMY	-7399	129.5
	ALIGN_L	-7480	226.5
	ALIGN_R	7480	226.5

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1 Power Supply Pins

Name	I/O	Description	Connect Pin
VDD	I	Power Supply for Analog, Digital System and Booster Circuit.	VDD
VDDI	I	Power Supply for I/O System.	VDDI
VDDI_LED	I	Power Supply for LED driver. Please fix this pad to VDDI level.	VDDI
AGND	I	System Ground for Analog System and Booster Circuit.	GND
DGND	I	System Ground for I/O System and Digital System.	GND

6.2 Interface Logic Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect Pin</th></tr>
<tr><td>IM3, IM2,
IM1, IM0</td><td>I</td><td>-The MCU / MIPI interface mode select.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80-8bit parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-9bit parallel I/F</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>MIPI I/F</td><td>D0P/N,
CLKP/N</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-line 9bit serial I/F</td><td>SDA: in/out</td></tr>
<tr><td>2 data lane serial I/F</td><td>SDA: in/out
WRX: in</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F</td><td>SDA: in/out</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>MIPI I/F</td><td>D0N/P
CLKN/P</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-line 9bit serial I/F Ⅱ</td><td>SDA: in
SDO: out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F Ⅱ</td><td>SDA: in
SDO: out</td></tr>
</table>
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>CLKP</th><th>CLKN</th><th>D0P</th><th>D0N</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>CLKP</td><td>CLKN</td><td>D0P</td><td>D0N</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>CLKN</td><td>CLKP</td><td>D0N</td><td>D0P</td></tr>
</table>
</td><td>DGND/VDDI</td></tr>
<tr><td>EXTC</td><td>I</td><td>-Select to access extension command (“Low”: system command 1, “High”: system command 1 and 2).
-When programming NVM, this pin should connect to high level.</td><td>DGND/VDDI</td></tr>
<tr><td>VPP</td><td>I</td><td>-When programming NVM, it needs external power supply voltage (7.5V); the current of Ivpp must be more than 10mA.
-If not used, let this pin open.</td><td>-</td></tr>
<tr><td>RESX</td><td>I</td><td>-This signal will reset the device and it must be applied to properly initialize the chip.
-Signal is active low.</td><td>MCU</td></tr>
<tr><td>CSX</td><td>I</td><td>-Chip selection pin
Low enable.
High disable.</td><td>MCU</td></tr>
<tr><td>DCX</td><td>I</td><td>-Display data/command selection pin in parallel interface.
-This pin is used to be serial interface clock.(SCL)</td><td>MCU</td></tr>
</table>

Name	I/O	Description	Connect Pin
		DCX='1': display data or parameter. DCX='0': command data. -If not used, please fix this pin at VDDI or DGND.	
RDX	I	-Read enable in 8080 MCU parallel interface. -If not used, please fix this pin at VDDI or DGND.	MCU
WRX	I	-Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. -If not used, please fix this pin at VDDI or DGND.	MCU
VSYNC	I	-Vertical (Frame) synchronizing input signal for RGB interface operation. -If not used, please fix to the VDDI or DGND.	MCU
HSYNC	I	-Horizontal (Line) synchronizing input signal for RGB interface operation. - If not used, please fix to VDDI or DGND.	MCU
ENABLE	I	-Data enable signal for RGB interface operation. -If not used, please fix this pin at VDDI or DGND.	MCU
DOTCLK	I	-Dot clock signal for RGB interface operation. -If not used, please fix this pin at VDDI or DGND.	MCU
SDA	I/O	-When IM3: Low, SPI interface input/output pin. -When IM3: High, SPI interface input pin. -The data is latched on the rising edge of the SCL signal. -If not used, please fix this pin at VDDI or DGND level.	MCU
SDO	O	-SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.	MCU
DB[8:0]	I/O	-DB [8:0] are used as MCU parallel interface data bus. 8-bit I/F: when IM3:0, DB [7:0] are used. 9-bit I/F: when IM3:0, DB [8:0] are used. -DB [5:0] are used as RGB interface data bus. 6-bit RGB I/F: DB[5:0] are used. -If not used, please fix this pin at VDDI or DGND.	MCU
TE	O	-Tearing effect signal is used to synchronize MCU to frame memory writing. -If not used, please let this pin open	MCU

Note1. "1" = VDDI level, "0" = DGND level.

Note2. When in parallel mode, unused data pins must be connected to "1" or "0".

Note3. When CSX="1", there is no influence to the parallel and serial interface.

6.3 MIPI Interface Pins

Name	I/O	Description	Connect pin
CLKP	I	MIPI-DSI clock lane positive-end input pin. -If not used, please fix this pin at DGND.	MCU
CLKN	I	MIPI-DSI clock lane negative-end input pin. -If not used, please fix this pin at DGND.	MCU
D0P	I/O	MIPI-DSI data lane positive-end input pin. -If not used, please fix this pin at DGND.	MCU
D0N	I/O	MIPI-DSI data lane negative-end input pin. -If not used, please fix this pin at DGND.	MCU

6.4 Driver Output Pins

Name	I/O	Description	Connect pin
S1 to S720	O	-Source driver output pad.	LCD
G1 to G320	O	-Gate driver output pad. VGH: Selecting Gate Lines Level. VGL: Non-selecting Gate Lines Level.	LCD
AVDD	O	-Power pad for analog circuit.	OPEN
VAP(GVDD)	O	- A power output of grayscale voltage generator.	OPEN
AVCL	O	- A power supply pin for generating VAN.	OPEN
VAN(GVCL)	O	- A power output (Negative) of grayscale voltage generator.	OPEN
VGH	O	- Power output pin for gate driver	OPEN
VGL	O	- Power output (Negative) pin for gate driver	OPEN
VCC	O	- Monitoring pin of internal digital reference voltage.	OPEN
VCOM	O	- A power supply for the TFT-LCD common electrode.	GND
LED_PWM	O	-Output pad for PWM output signal to driving LED. -If not used, keep it open.	-
LED_EN	O	-Output pad for enabling LED. -If not used, keep it open.	-

6.5 Test and other pins

TEST3~TEST0	I	Input pins for testing. Please open these pins.	OPEN
TE2	O	Output pin for testing. Please keep this pin floating.	OPEN
TESTO6~TESTO0	O	Output pins for testing. Please keep these pins floating.	OPEN

DUMMY	-	These pins are dummy (no electrical characteristic) Can pass signal through these pads on TFT panel. Please open these pins.	OPEN
DUMMYR1 DUMMYR2	-	These pins are dummy (no electrical characteristic). DUMMYR1 and DUMMYR2 are connected each other internally.	OPEN
VAG V20	O	Used for monitoring Please keep these pins floating.	OPEN

7 DRIVER ELECTRICAL CHARACTERISTICS

7.1 Absolute Operation Range

Item	Symbol	Rating	Unit
Supply Voltage	VDD	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VDDI	- 0.3 ~ +4.6	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.5	V
Logic Output Voltage Range	VO	-0.3 ~ VDDI + 0.5	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Table 1 Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 DC Characteristics

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD	Operating voltage	2.4	2.75	3.3	V	
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	
Gate Driver High Voltage	VGH		12.2		14.97	V	Note 4
Gate Driver Low Voltage	VGL		-12.5		-7.16	V	
Gate Driver Supply Voltage		| VGH-VGL |	19.36		27.47	V	Note 5
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI			1	uA	Note 1
Logic-Low Input Current	IIL	VIN = VSS	-1			uA	Note 1
Input Leakage Current	IIL	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM Voltage							
VCOM amplitude	VCOM			VSS		V	
Source Driver							
Source Output Range	Vsout		VAN		VAP	V	
Gamma Reference Voltage(Positive)	VAP		4.45		6.4	V	Note 6
Gamma Reference Voltage(Negative)	VAN		-4.6		-2.65	V	
Source Output Settling Time	Tr	Below with 99% precision			20	us	Note 2
Output Offset Voltage	VOFFSET				35	mV	Note 3

Table 2 Basic DC Characteristics

Notes:

1. TA= -30 to 70℃ (to +85℃ no damage).

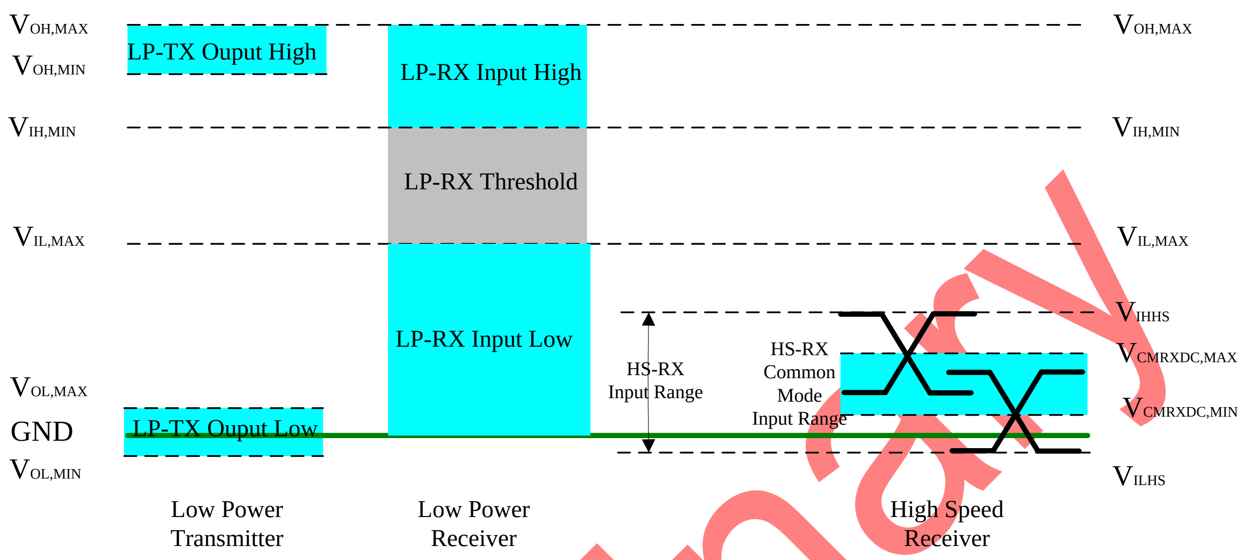
2. Source channel loading= 2KΩ+12pF/channel, Gate channel loading=5KΩ+40pF/channel.

3. The Max. value is between measured point of source output and gamma setting value.

4. When evaluating the maximum and minimum of VGH, VDD=2.8V.

5. The maximum value of |VGH-VGL| cannot over 30V.

6. Default register setting of Vcom and Vcomoffset is 20h



VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	V_{LPH}	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Logic 0 input threshold	V_{IL}	0-	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	1350	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V

7.3 Power Consumption

Ta=25℃, Frame rate = 60Hz, Registers setting are IC default setting.

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
Normal Mode	Black	TBD	TBD	TBD	TBD
Partial + Idle Mode (48 lines)	Black	TBD	TBD	TBD	TBD
Sleep-in Mode	N/A	TBD	TBD	TBD	TBD

Table 3 Power Consumption

Notes:

1. The Current Consumption is DC characteristics of ST7785M.

2. Typical: VDDI=1.8V, VDD=2.75V; Maximum: VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V

7.4 AC Characteristics

7.4.1 8080 Series MCU Parallel Interface Characteristics: 9/8-bit Bus

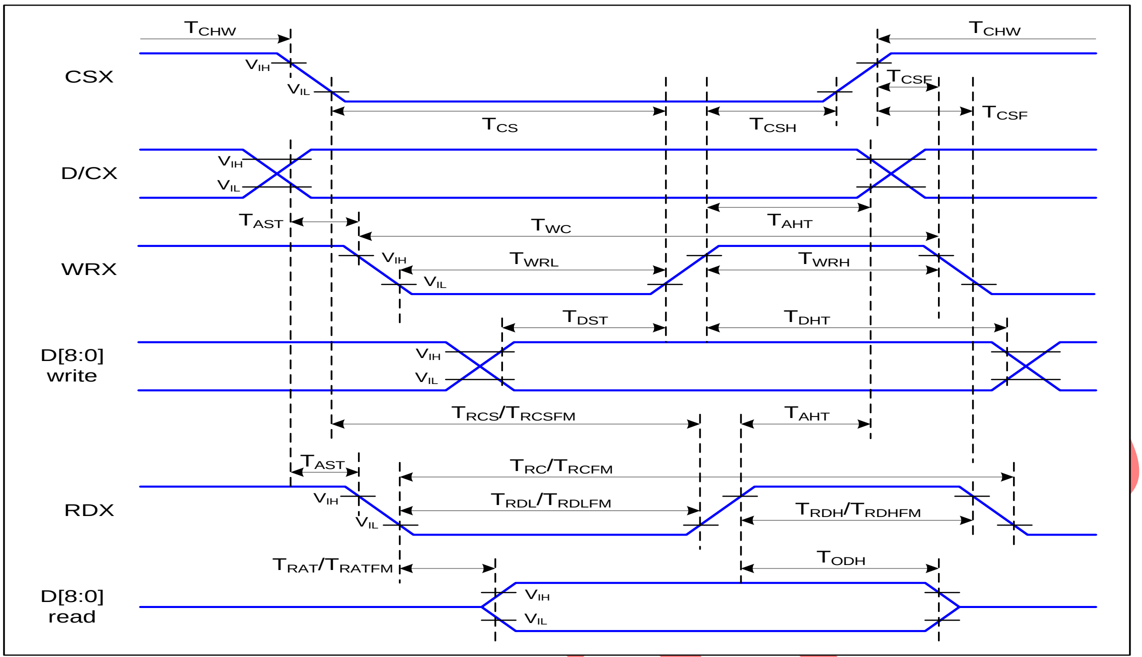


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	TBD		ns	-
	T_{AHT}	Address hold time (Write/Read)	TBD		ns	
CSX	T_{CHW}	Chip select "H" pulse width	TBD		ns	-
	T_{CS}	Chip select setup time (Write)	TBD		ns	
	T_{RCS}	Chip select setup time (Read ID)	TBD		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	TBD		ns	
	T_{CSF}	Chip select wait time (Write/Read)	TBD		ns	
	T_{CSH}	Chip select hold time	TBD		ns	
WRX	T_{WC}	Write cycle	TBD		ns	
	T_{WRH}	Control pulse "H" duration	TBD		ns	
	T_{WRL}	Control pulse "L" duration	TBD		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	TBD		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	TBD		ns	
	T_{RDL}	Control pulse "L" duration (ID)	TBD		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	TBD		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	TBD		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	TBD		ns	
D[8:0]	T_{DST}	Data setup time	TBD		ns	For CL=30pF

	T_{DHT}	Data hold time	TBD		ns	
	T_{RAT}	Read access time (ID)		TBD	ns	
	T_{RATFM}	Read access time (FM)		TBD	ns	
	T_{ODH}	Output disable time	TBD	TBD	ns	

Table 4 8080 Parallel Interface Characteristics

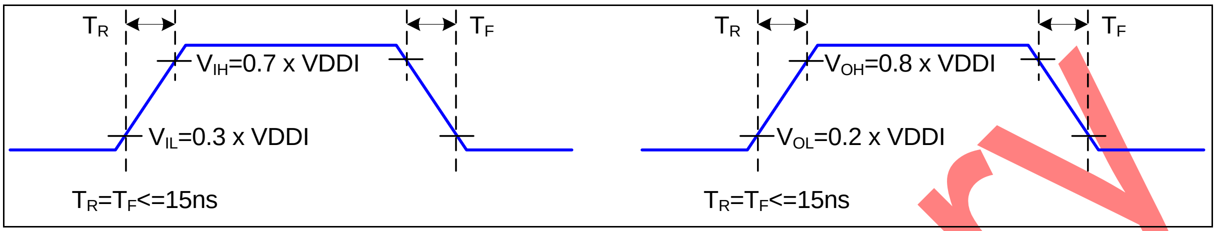


Figure 2 Rising and Falling Timing for I/O Signal

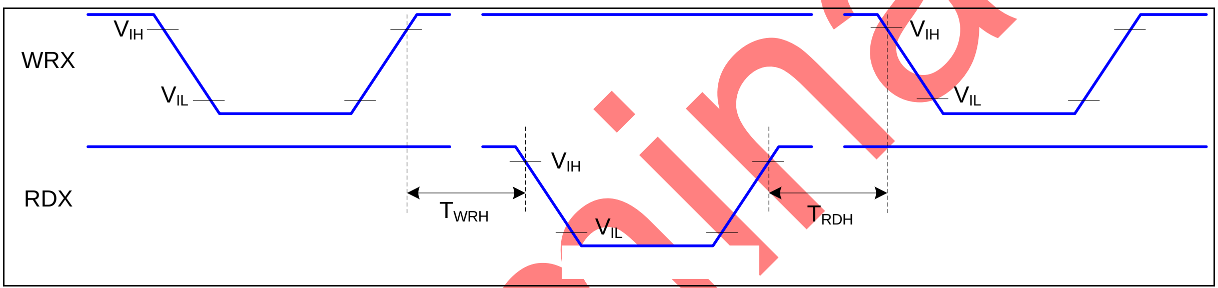


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.2 Serial Interface Characteristics (3-line serial):

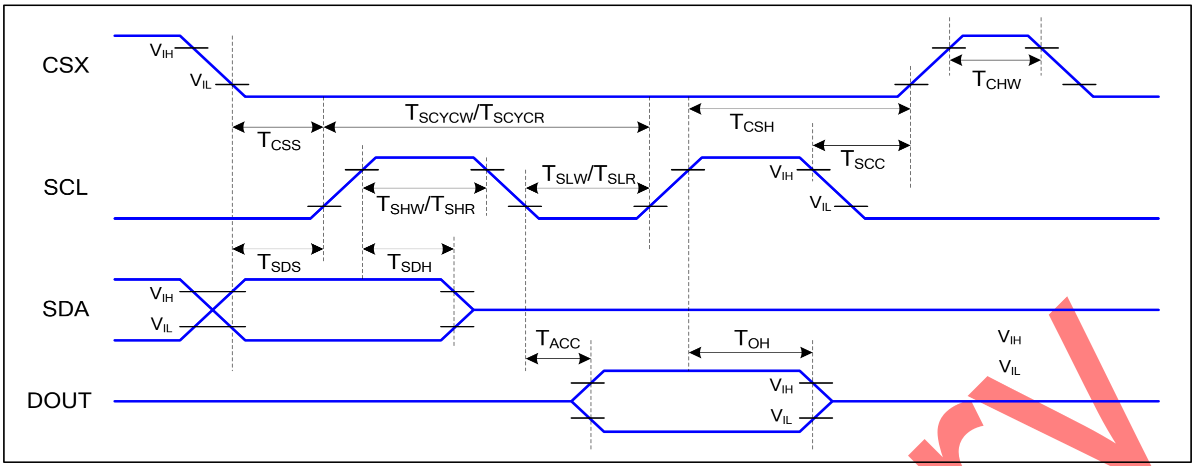


Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD		ns	
	T_{CSH}	Chip select hold time (write)	TBD		ns	
	T_{CSS}	Chip select setup time (read)	TBD		ns	
	T_{SCC}	Chip select hold time (read)	TBD		ns	
	T_{CHW}	Chip select "H" pulse width	TBD		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD		ns	
	T_{SHW}	SCL "H" pulse width (Write)	TBD		ns	
	T_{SLW}	SCL "L" pulse width (Write)	TBD		ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD		ns	
	T_{SHR}	SCL "H" pulse width (Read)	TBD		ns	
	T_{SLR}	SCL "L" pulse width (Read)	TBD		ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD		ns	
	T_{SDH}	Data hold time	TBD		ns	
DOUT	T_{ACC}	Access time	TBD	TBD	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.3 Serial Interface Characteristics (4-line serial):

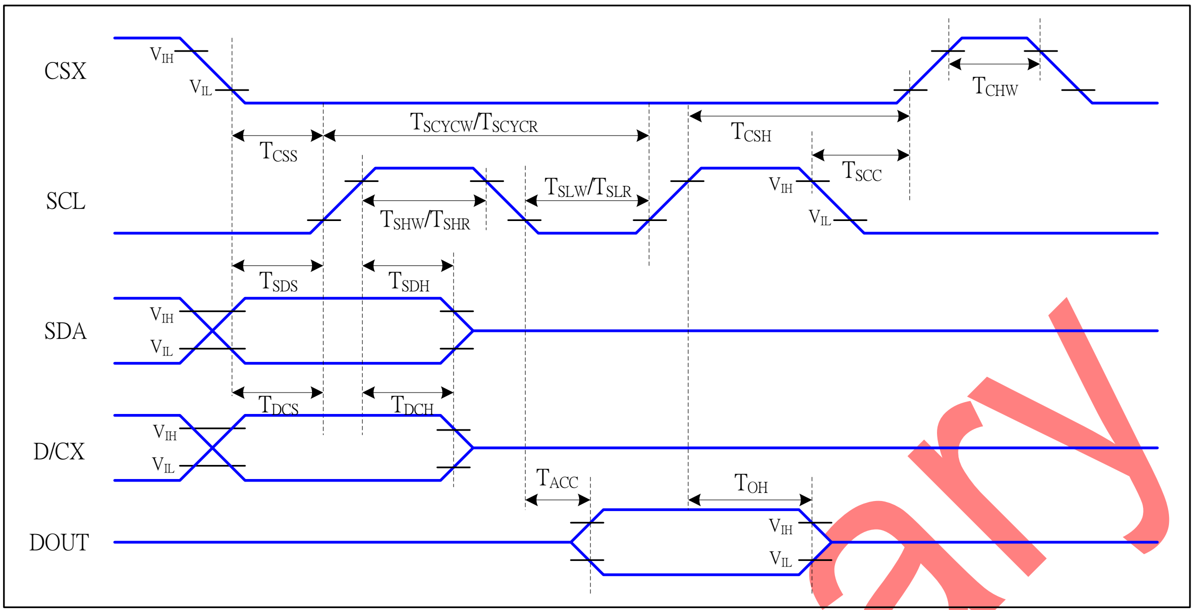


Figure 5 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	TBD		ns	
	T_{CSH}	Chip select hold time (write)	TBD		ns	
	T_{CSS}	Chip select setup time (read)	TBD		ns	
	T_{SCC}	Chip select hold time (read)	TBD		ns	
	T_{CHW}	Chip select "H" pulse width	TBD		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	TBD		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	TBD		ns	
	T_{SLW}	SCL "L" pulse width (Write)	TBD		ns	
	T_{SCYCR}	Serial clock cycle (Read)	TBD		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	TBD		ns	
	T_{SLR}	SCL "L" pulse width (Read)	TBD		ns	
D/CX	T_{DCS}	D/CX setup time	TBD		ns	
	T_{DCH}	D/CX hold time	TBD		ns	
SDA (DIN)	T_{SDS}	Data setup time	TBD		ns	
	T_{SDH}	Data hold time	TBD		ns	
DOUT	T_{ACC}	Access time	TBD	TBD	ns	For maximum CL=30pF
	T_{OH}	Output disable time	TBD	TBD	ns	For minimum CL=8pF

Table 6 4-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.4 RGB Interface Characteristics:

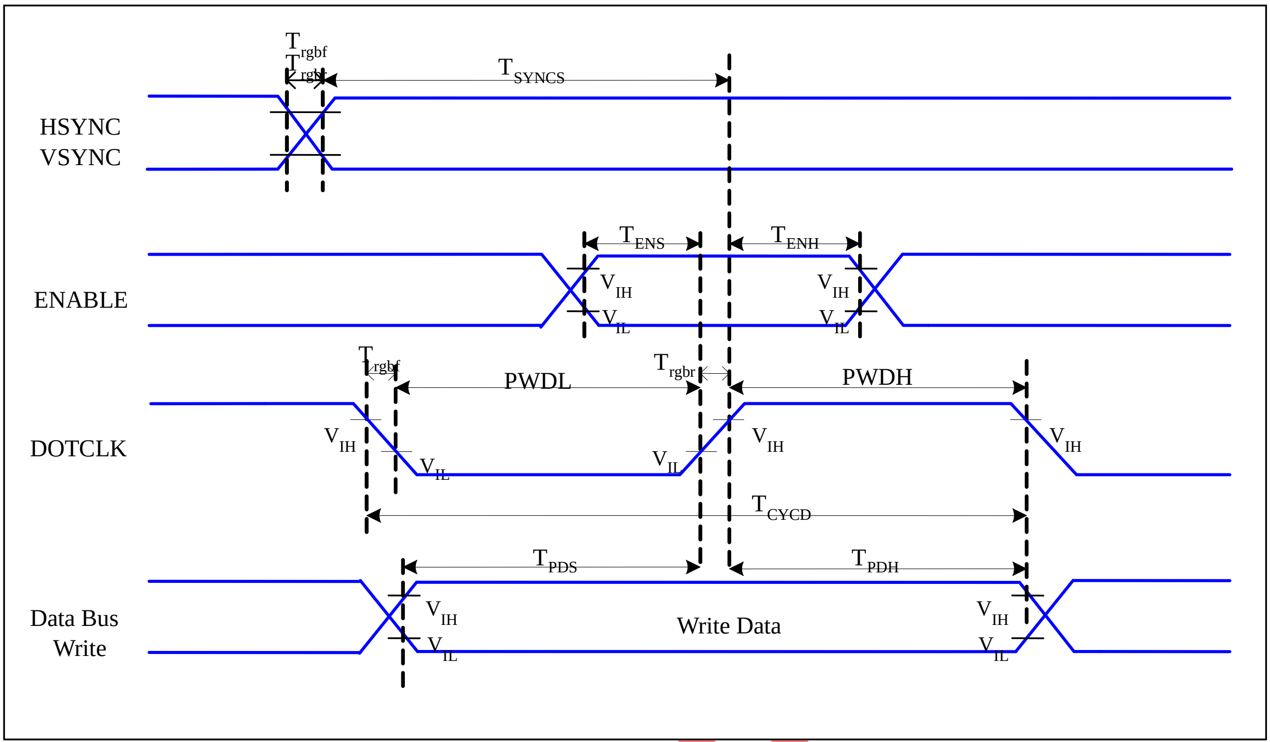


Figure 6 RGB Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	TBD	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	TBD	-	ns	
	T_{ENH}	Enable Hold Time	TBD	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	TBD	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	TBD	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	TBD	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	TBD	ns	
DB	T_{PDS}	PD Data Setup Time	TBD	-	ns	
	T_{PDH}	PD Data Hold Time	TBD	-	ns	

Table 7 18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	TBD	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	TBD	-	ns	
	T_{ENH}	Enable Hold Time	TBD	-	ns	

DOTCLK	PWDH	DOTCLK High-level Pulse Width	TBD	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	TBD	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	TBD	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	TBD	ns	
DB	T_{PDS}	PD Data Setup Time	TBD	-	ns	
	T_{PDH}	PD Data Hold Time	TBD	-	ns	

Table 8 6 Bits RGB Interface Timing Characteristics

7.4.5 MIPI Interface Characteristics

7.4.5.1 High Speed Mode

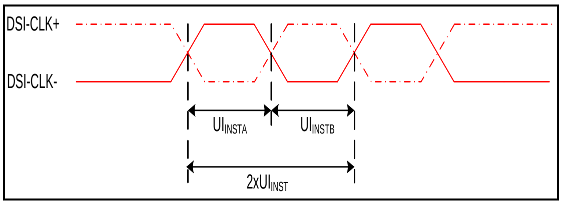


Figure 7 DSI clock channel timing

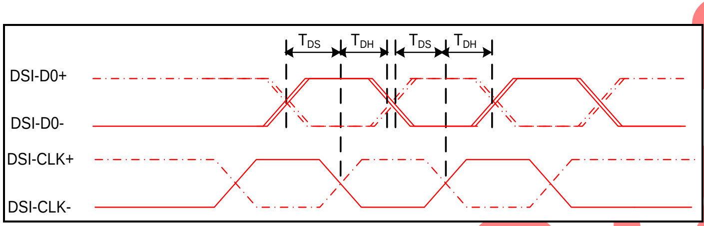


Figure 8 Rising and falling time on clock and data channel

VDDI=1.8, VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	TBD	TBD	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	TBD	TBD	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	TBD	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	TBD	-	UI	

Table 9 MIPI Interface- High Speed Mode Timing Characteristics

7.4.5.2 Lowe Power Mode

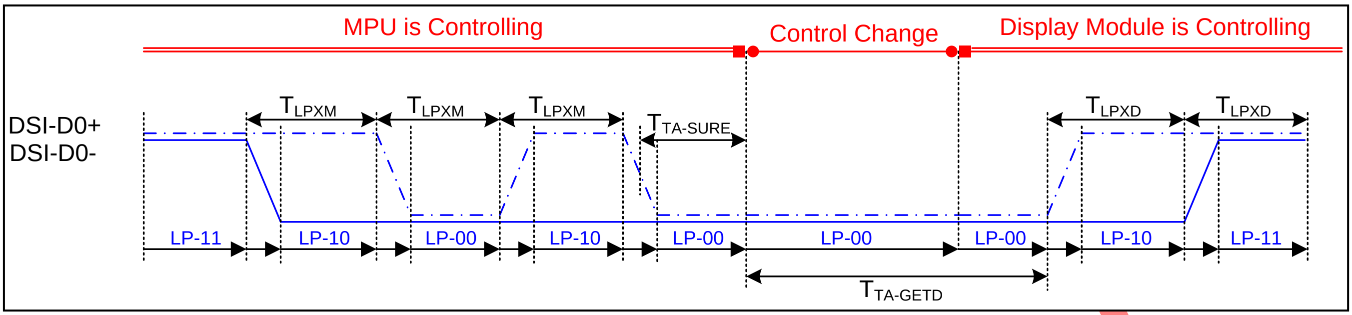


Figure 9 Bus Turnaround (BTA) from display module to MPU Timing

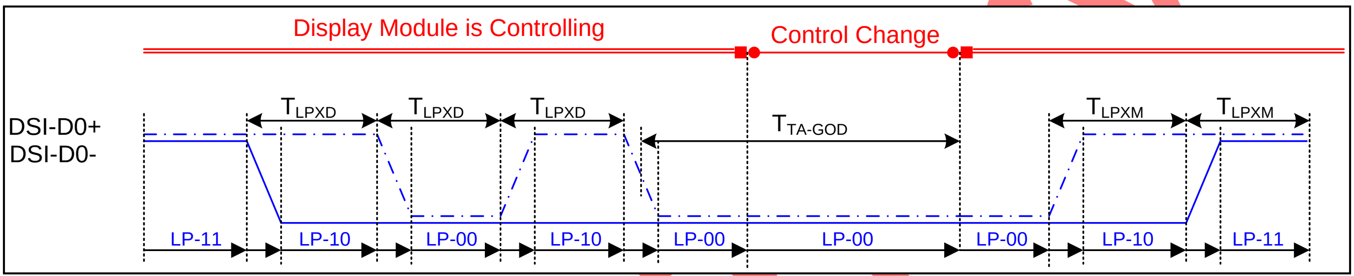


Figure 10 Bus Turnaround (BTA) from MPU to display module Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

Table 10 MIPI Interface Low Power Mode Timing Characteristics

7.4.5.3 DSI Bursts Mode

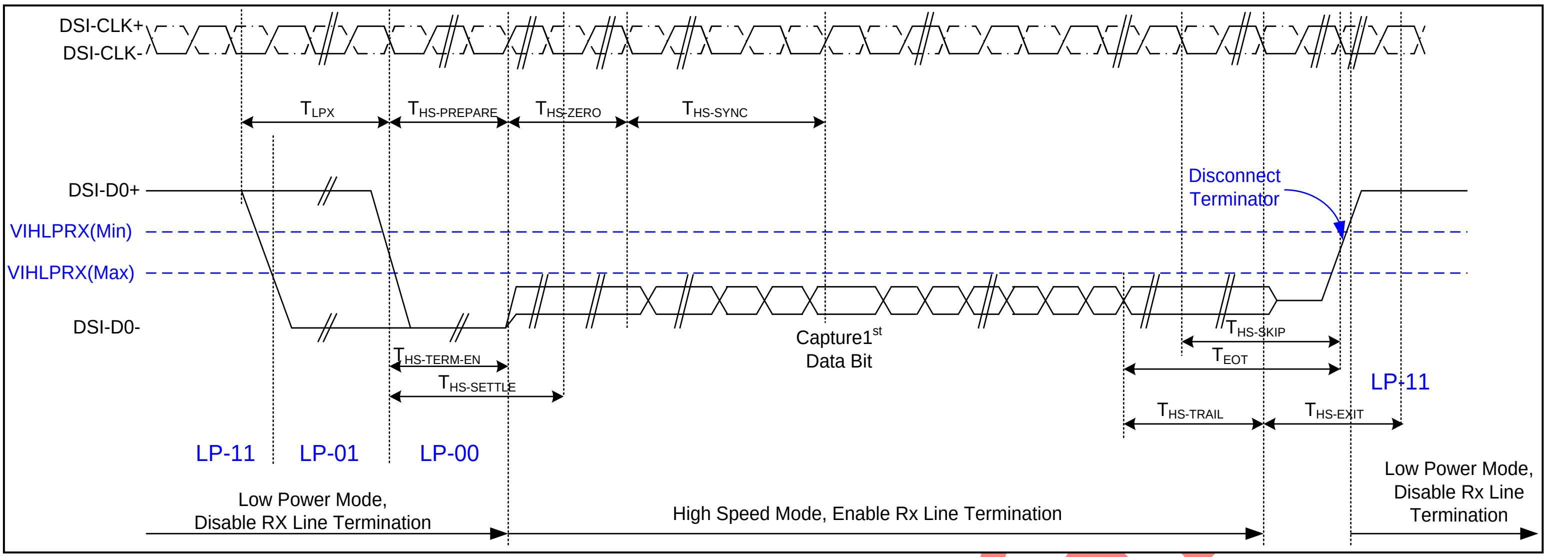


Figure 11 **Data lanes-Low Power Mode to/from High Speed Mode Timing**

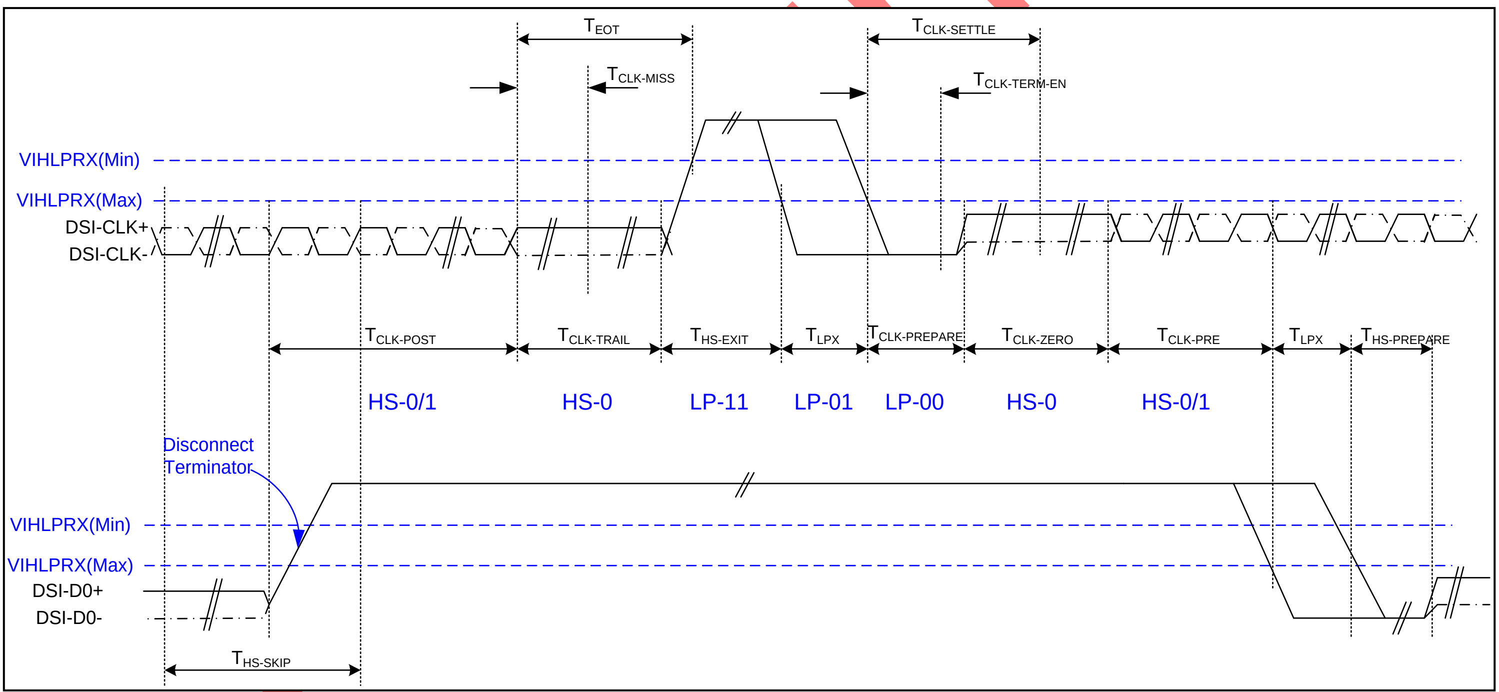


Figure 12 **Clock lanes- High Speed Mode to/from Low Power Mode Timing**

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

7.4.6 Reset Timing:

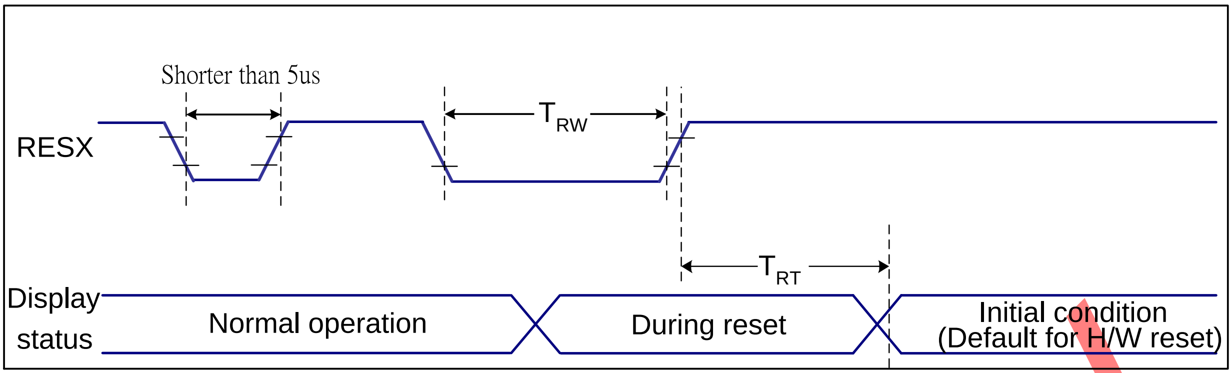


Figure 13 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	TBD	-	us
	TRT	Reset cancel	-	TBD (Note 1, 5)	ms
				TBD (Note 1, 6, 7)	ms

Table 11 Reset Timing

Notes:

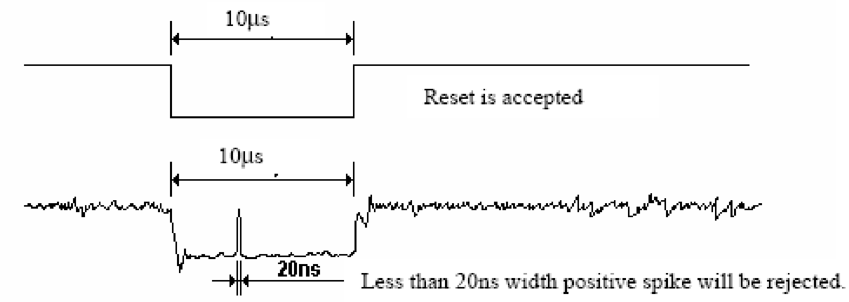
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8 FUNCTION DESCRIPTION

8.1 MPU Interface Type Selection

ST7785M supports 8/9 bit parallel data bus for 8080 series CPU, RGB serial interfaces. Selection of these interfaces are set by IM [3:0] pins as shown below.

IM3	IM2	IM1	IM0	Interface	Read Back Data Bus Selection
0	0	0	0	80-8bit parallel I/F	DB[7:0]
0	0	0	1	Reserved	-
0	0	1	0	80-9bit parallel I/F	DB[8:0]
0	0	1	1	Reserved	-,
0	1	0	0	MIPI I/F	CLKP/N , D0P/N
0	1	0	1	3-line 9bit serial I/F	SDA: in/out
				2 data lane serial I/F	SDA: in/out, WRX: in
0	1	1	0	4-line 8bit serial I/F	SDA: in/out
0	1	1	1	Reserved	-,
1	0	0	0	Reserved	-,
1	0	0	1	Reserved	-,
1	0	1	0	Reserved	-,
1	0	1	1	Reserved	-,
1	1	0	0	MIPI I/F	CLKN/P , D0N/P
1	1	0	1	3-line 9bit serial I/F Ⅱ	SDA: in/ SDO: out
1	1	1	0	4-line 8bit serial I/F Ⅱ	SDA: in/ SDO: out

Table 12 Interface Type Selection

8.2 8080 Series MCU Parallel Interface

The MCU can use one of following interfaces: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write enable, RDX is the parallel data read enable and D[8:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[8:0] bits is either display data or command parameter. When D/C='0', D[8:0] bits is command. The interface functions of 8080-series parallel interface are given in following table.

IM3	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Read back selection
0	0	0	0	8-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
					1	↑	1	Read 8-bit display data (D7 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)
0	0	1	0	9-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
					1	1	↑	Write 9-bit display data or 8-bit parameter (D8 to D0)
					1	↑	1	Read 9-bit display data (D8 to D0)
					1	↑	1	Read 8-bit parameter or status (D7 to D0)

Table 13 the function of 8080-series parallel interface

8.2.1 Write cycle sequence

The write cycle means that the host writes information (command / data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (DCX, RDX, WRX) and data signals (DB[8:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

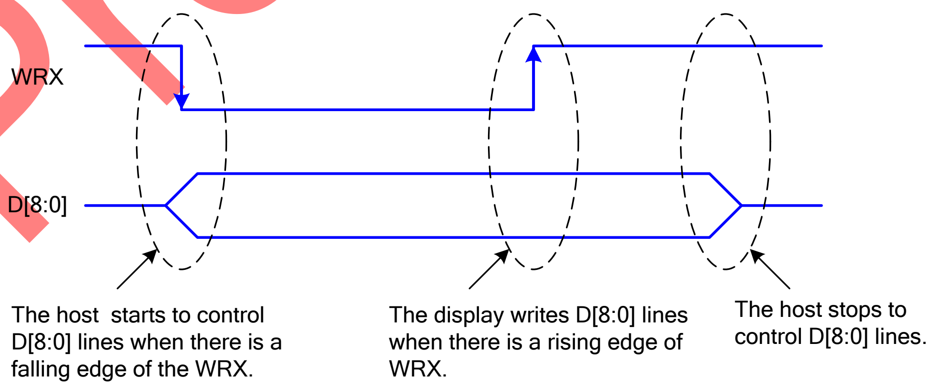


Figure 14 8080-Series WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped).

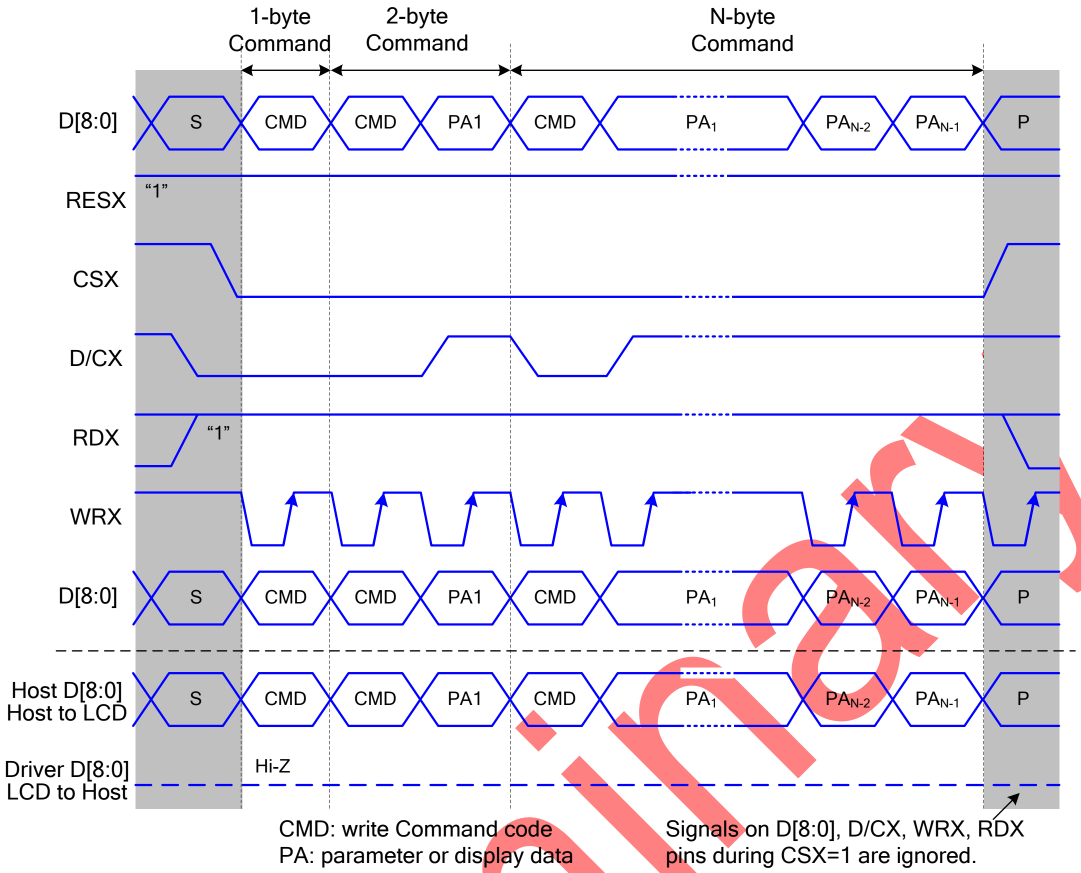


Figure 15 8080-Series Parallel Bus Protocol, Write to Register or Display RAM

8.2.2 Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[8:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

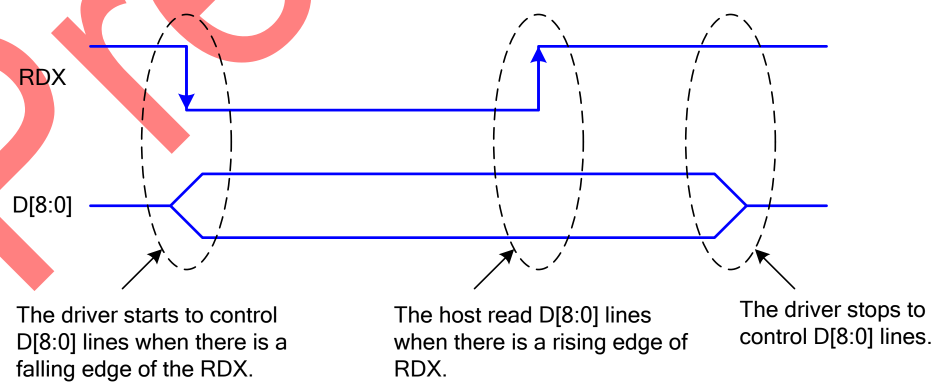


Figure 16 8080-series RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).

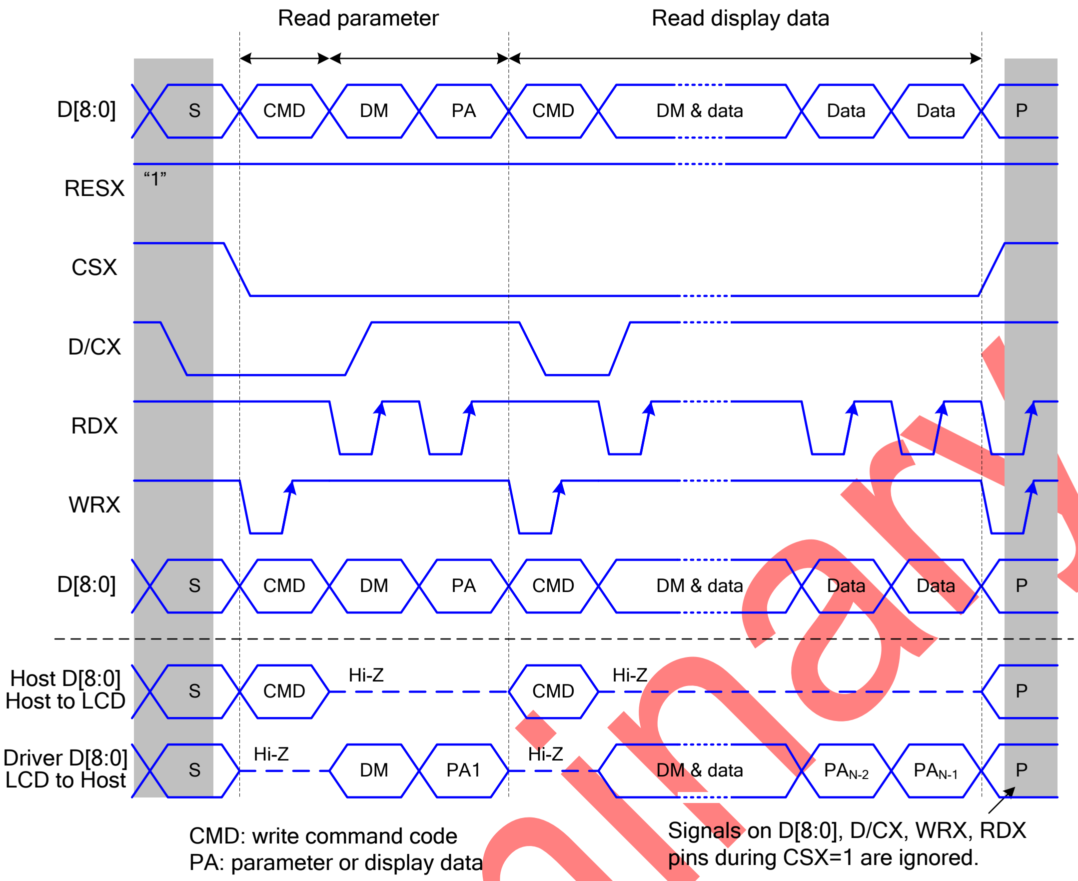


Figure 17 8080-series parallel bus protocol, read data from register or display RAM

8.3 Serial Interface

IM3	IM2	IM1	IM0	Interface	Read back selection
0	1	0	1	3-line serial interface Ⅰ	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
0	1	1	0	4-line serial interface Ⅰ	
1	1	0	1	3-line serial interface Ⅱ	
1	1	1	0	4-line serial interface Ⅱ	

Table 14 Selection of serial interface

The serial interface is either 3-lines/9-bits or 4-lines/8-bits bi-directional interface for communication between the micro controller and the LCD driver. The 3-lines serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-lines serial interface use: CSX (chip enable), D/CX (data/ command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

8.3.1 Pin description

3-line serial interface Ⅰ

Pin Name	Description
CSX	Chip selection signal
DCX	Clock signal
SDA	Serial input/output data

4-line serial interface Ⅰ

Pin Name	Description
CSX	Chip selection signal
WRX	Data is regarded as a command when WRX is low Data is regarded as a parameter or data when WRX is high
DCX	Clock signal
SDA	Serial input/output data

3-line serial interface Ⅱ

Pin Name	Description
CSX	Chip selection signal
DCX	Clock signal
SDA	Serial input data
SDO	Serial output data

4-line serial interface Ⅱ

Pin Name	Description
CSX	Chip selection signal
WRX	Data is regarded as a command when WRX is low Data is regarded as a parameter or data when WRX is high

DCX	Clock signal
SDA	Serial input data
SDO	Serial output data

Table 15 pin description of serial interface

8.3.2 Command write mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. In 4-lines serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

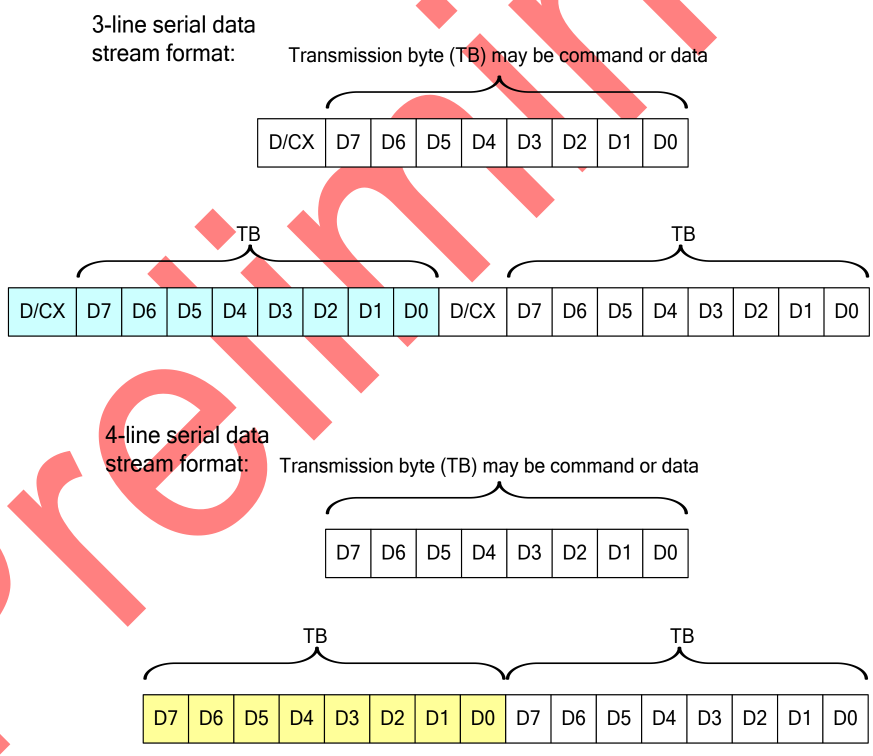


Figure 18 Serial interface data stream format

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX=’0’) or parameter/RAM data (D/CX=’1’). D/CX is sampled when first rising edge of SCL (3-line serial interface) or 8th rising edge of SCL (4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL.

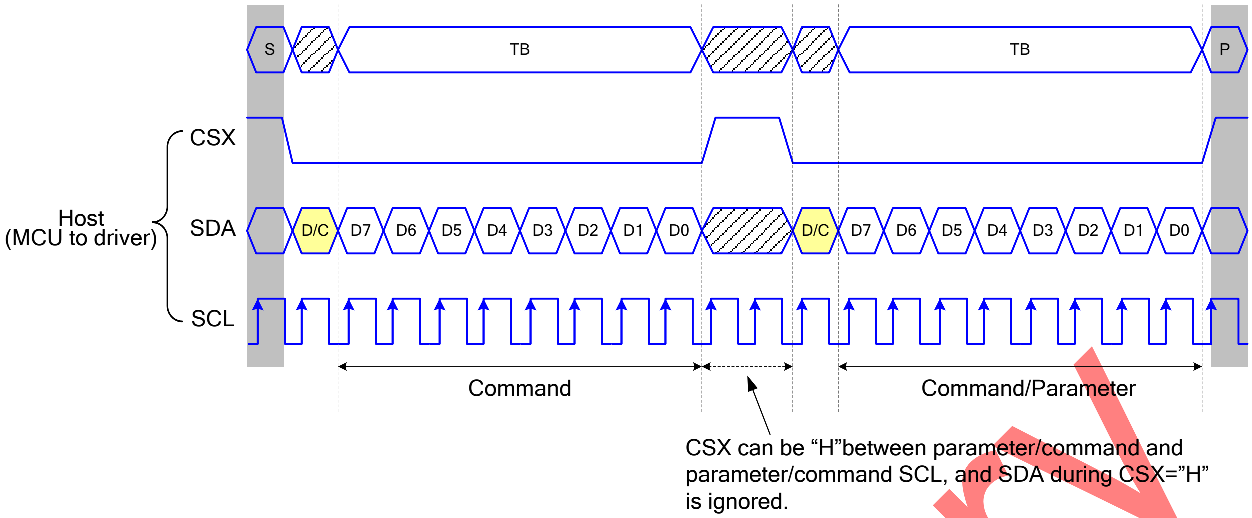


Figure 19 3-line serial interface write protocol (write to register with control bit in transmission)

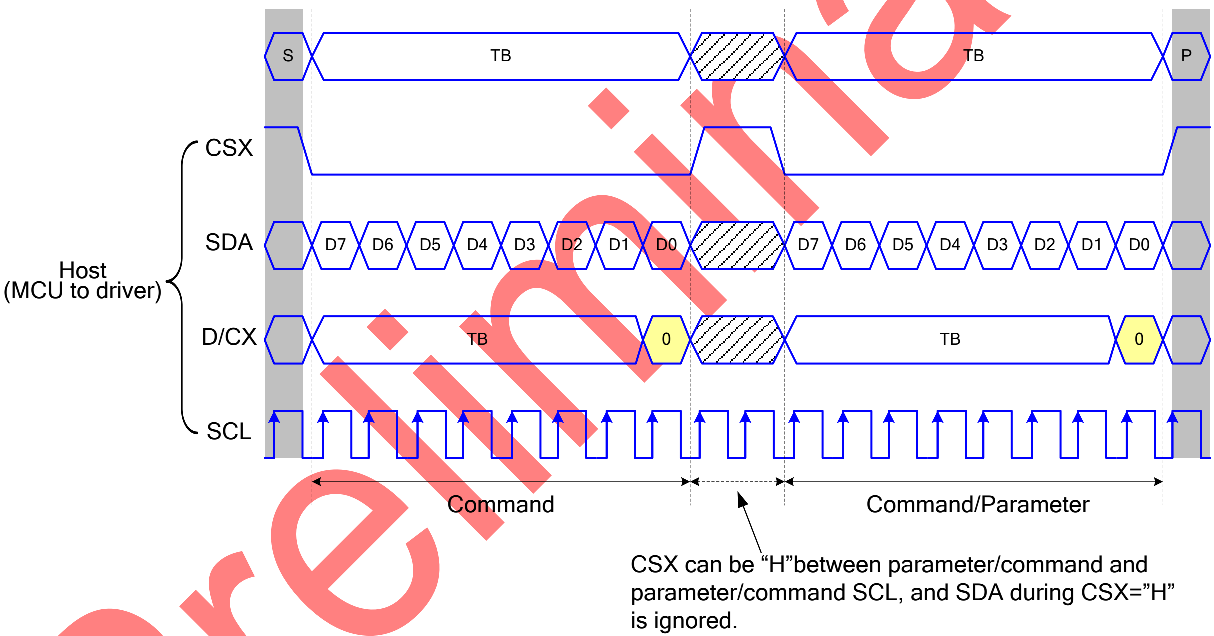


Figure 20 4-line serial interface write protocol (write to register with control bit in transmission)

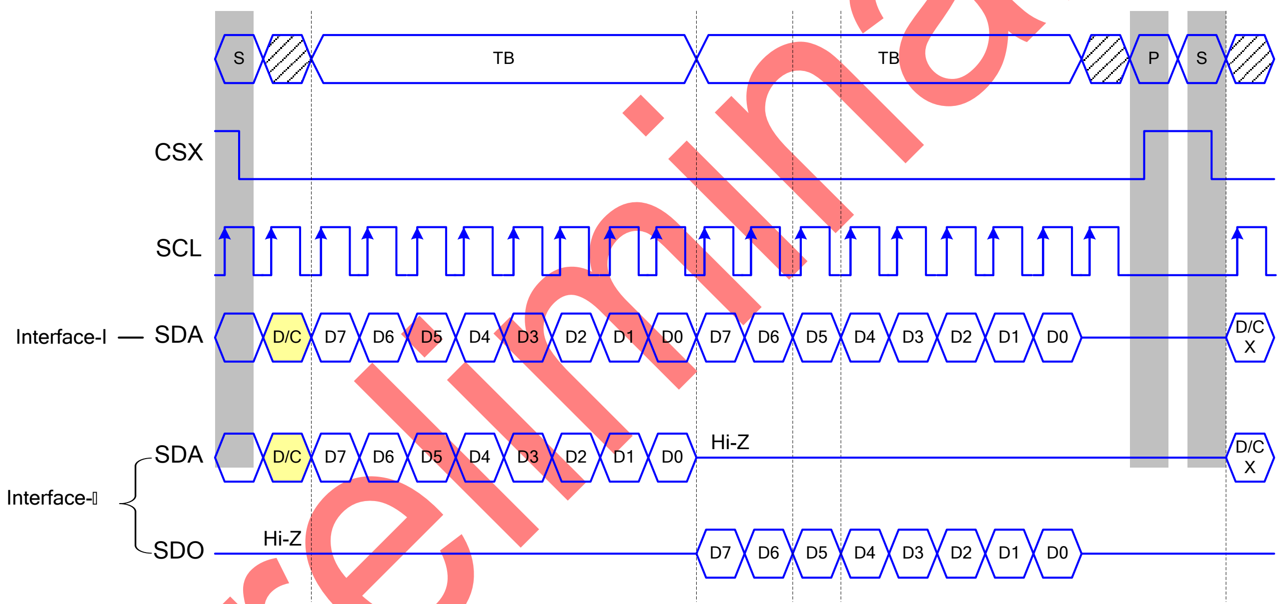
8.3.3 Read function

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

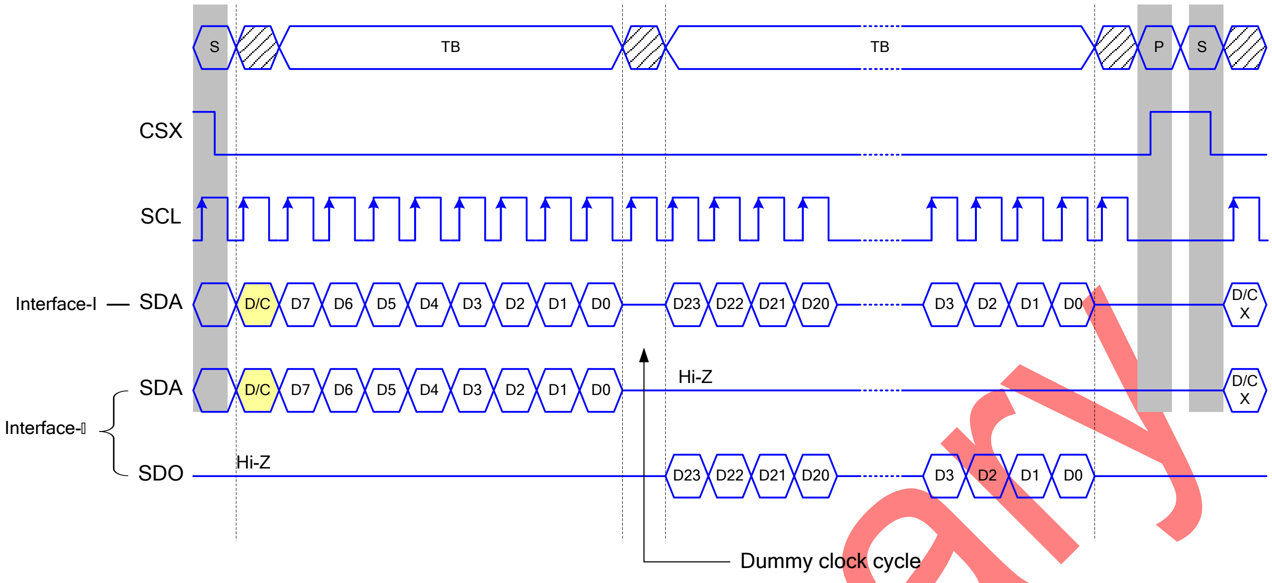
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

8.3.4 3-line serial interface Ⅰ/Ⅱ protocol

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

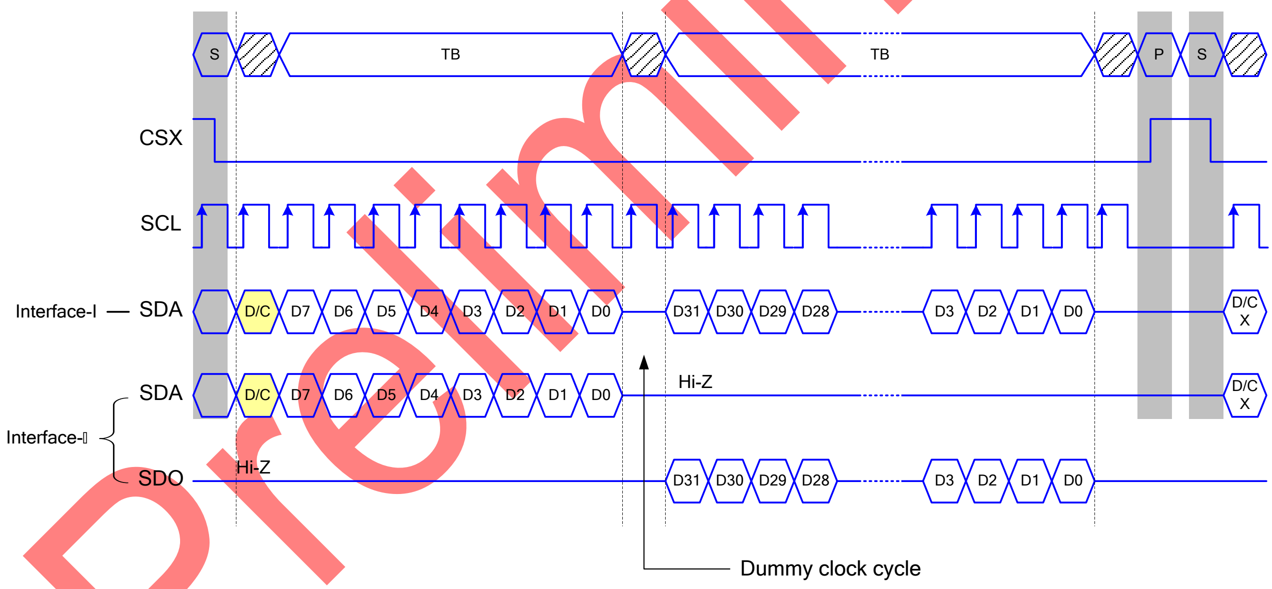
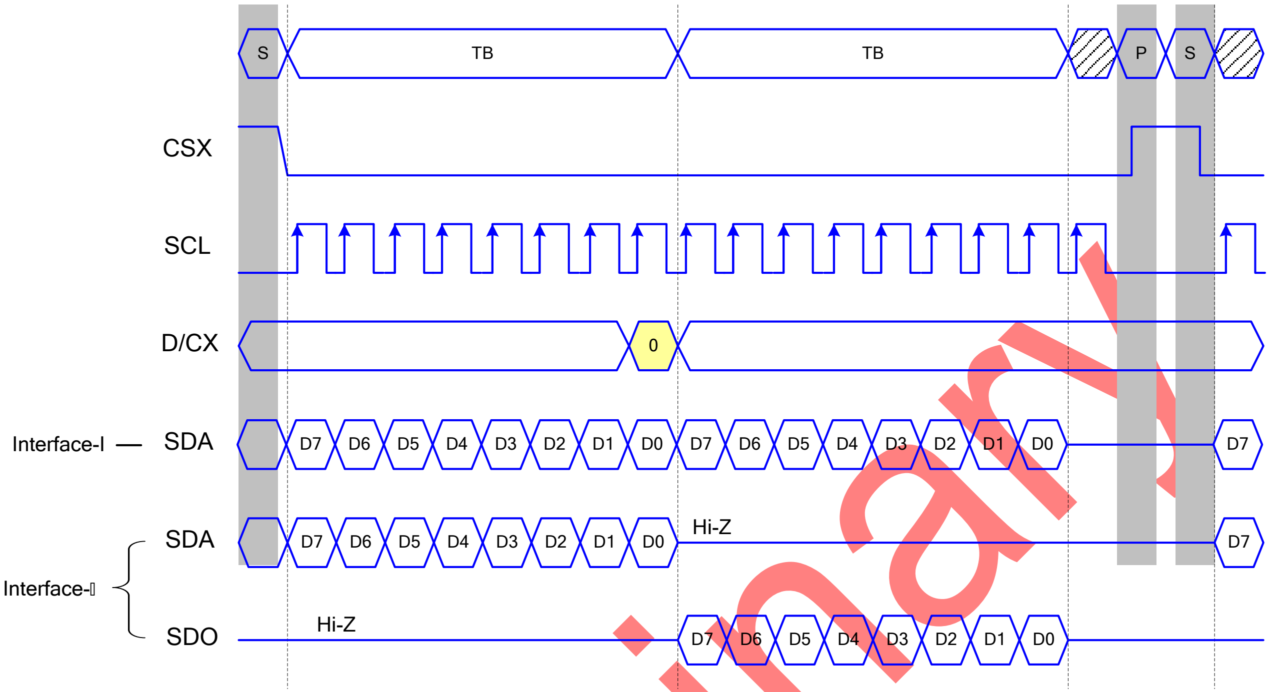


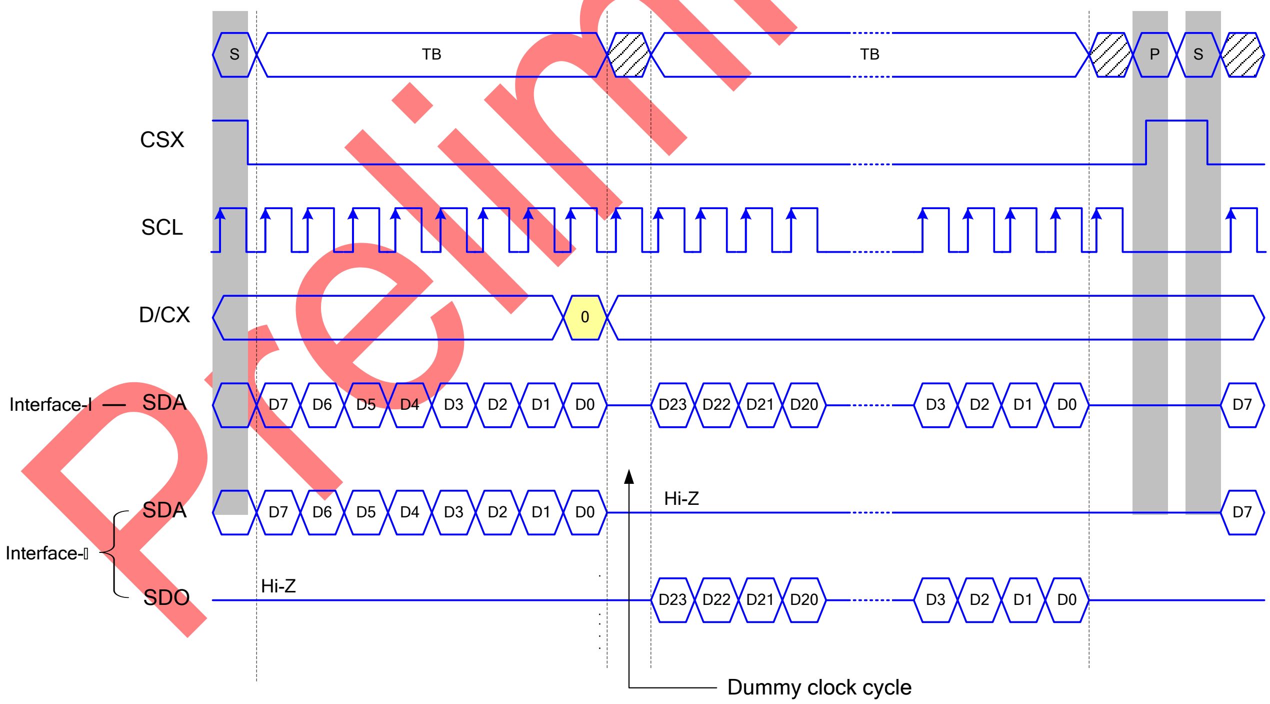
Figure 21 3-line serial interface read protocol

8.3.5 4-line serial protocol

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



4-line serial protocol (for RDDID command: 24-bit read)



4-line Serial Protocol (for RDDST command: 32-bit read)

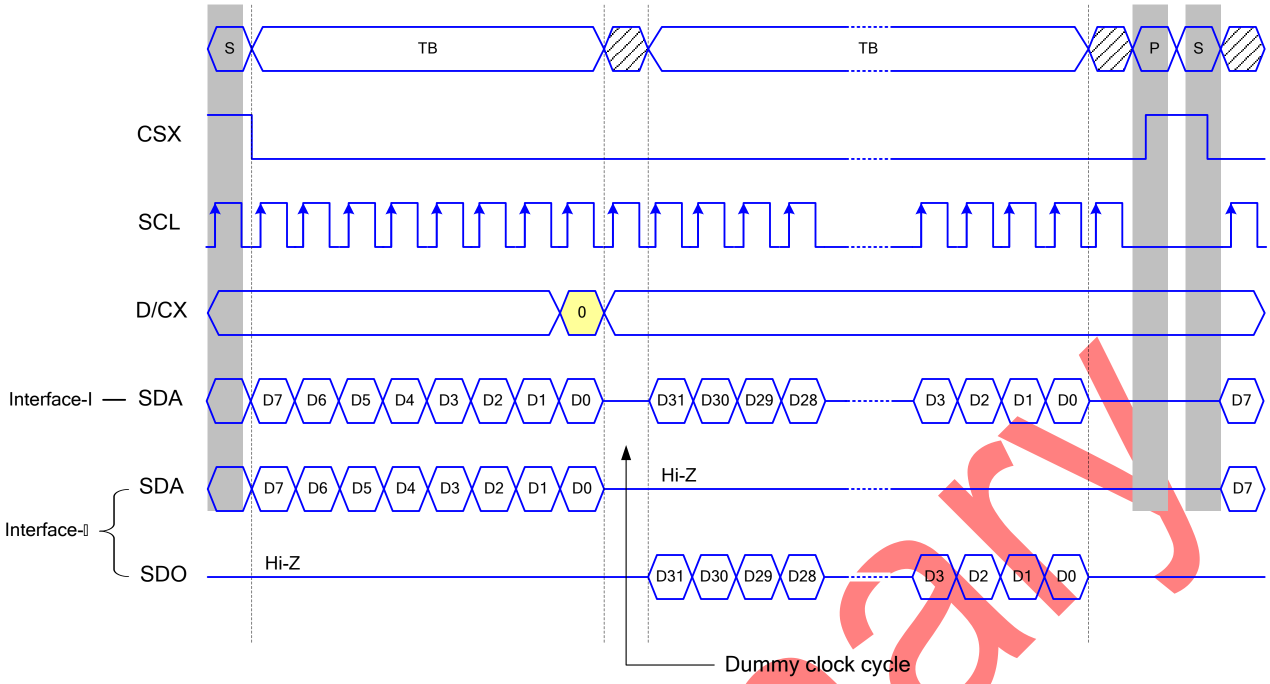


Figure 22 4-line serial interface read protocol

8.3.6 2 data lane serial Interface

Interface selection:

IM3	IM2	IM1	IM0	Interface	Read back selection
0	1	0	1	2 data lane serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read)

Table 16 IM pin selection

2-wire data lane serial interface use: CSX (chip enable), DCX (serial clock) and SDA (serial data input/output 1), and WRX (serial data input 2). To enter this interface, command E7h need set 10h.

2 data lane hardware suggestion and Pin description:

2 data lane serial interface, IM [3:0] = 0101

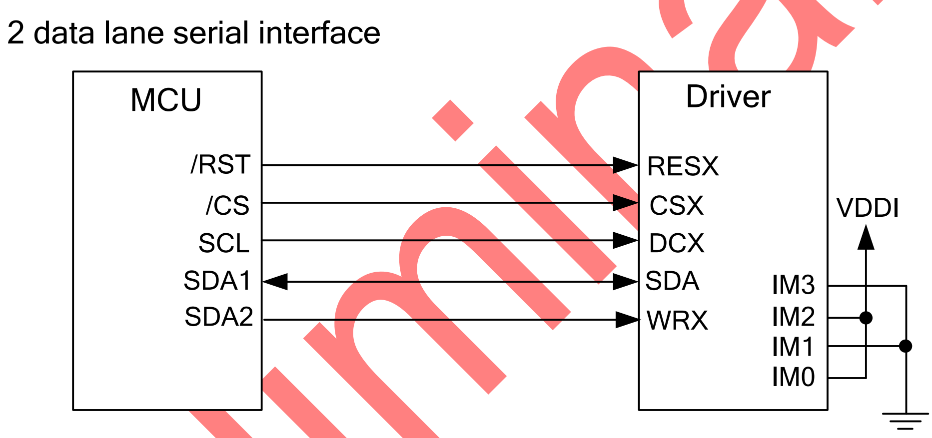


Figure 23 Hardware suggestion of 2 data lane serial interface

Pin Name	Description
CSX	Chip selection signal
DCX	Clock signal
SDA	Serial data input/output1
WRX	Serial data input2

Table 17 Pin description of 2 data lane serial interface

Command write mode:

The command write protocol of 2-wire data lane serial interface is the same with the 3-line serial interface, so users can ignore the input data of WRX.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

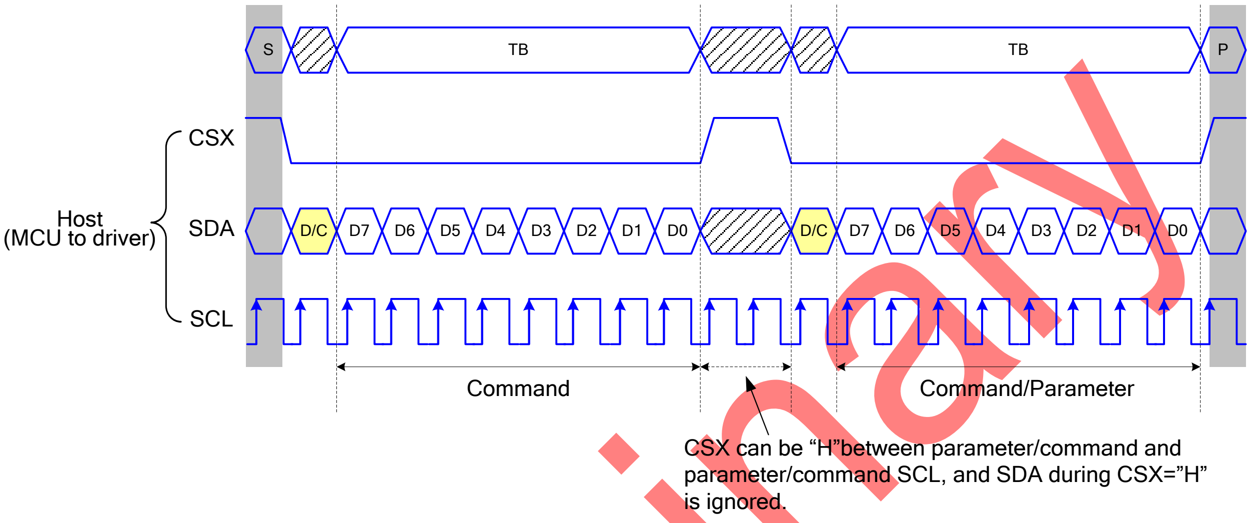


Figure 24 3-line serial interface write protocol (write to register with control bit in transmission)

SRAM write mode:

The SRAM write mode of 2-wire data line serial interface need use SDA pin and WRX pin to be data input pins.

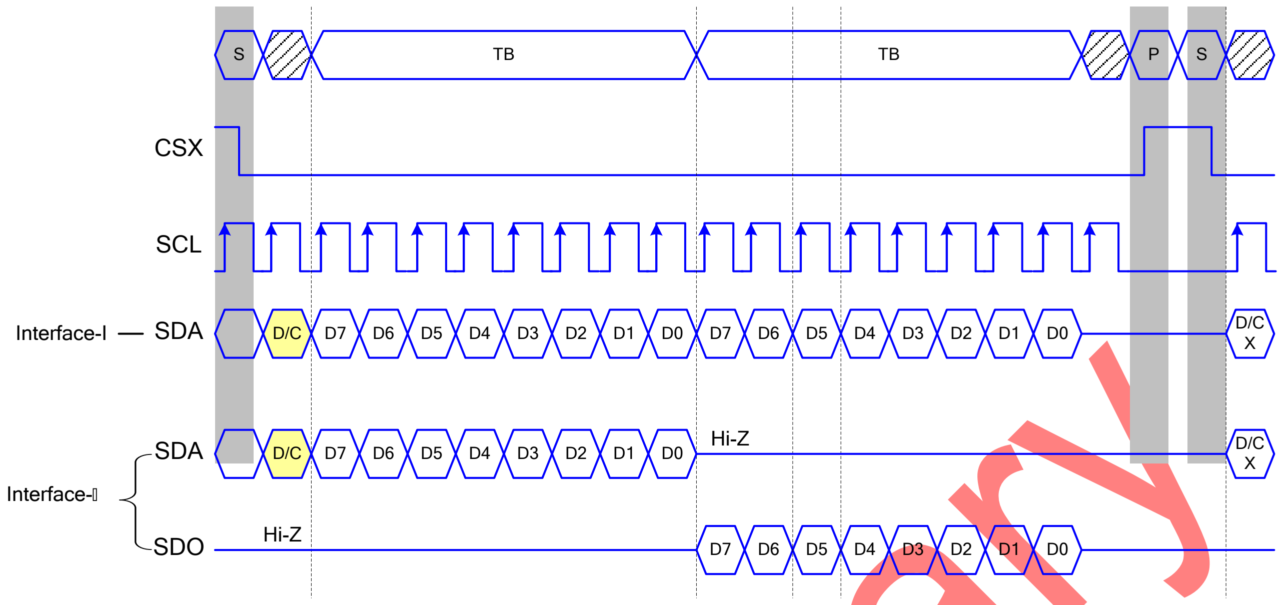
Read function:

The read mode of 2-wire data lane serial interface is the same with the 3-line serial interface and WRX pin can be ignored. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

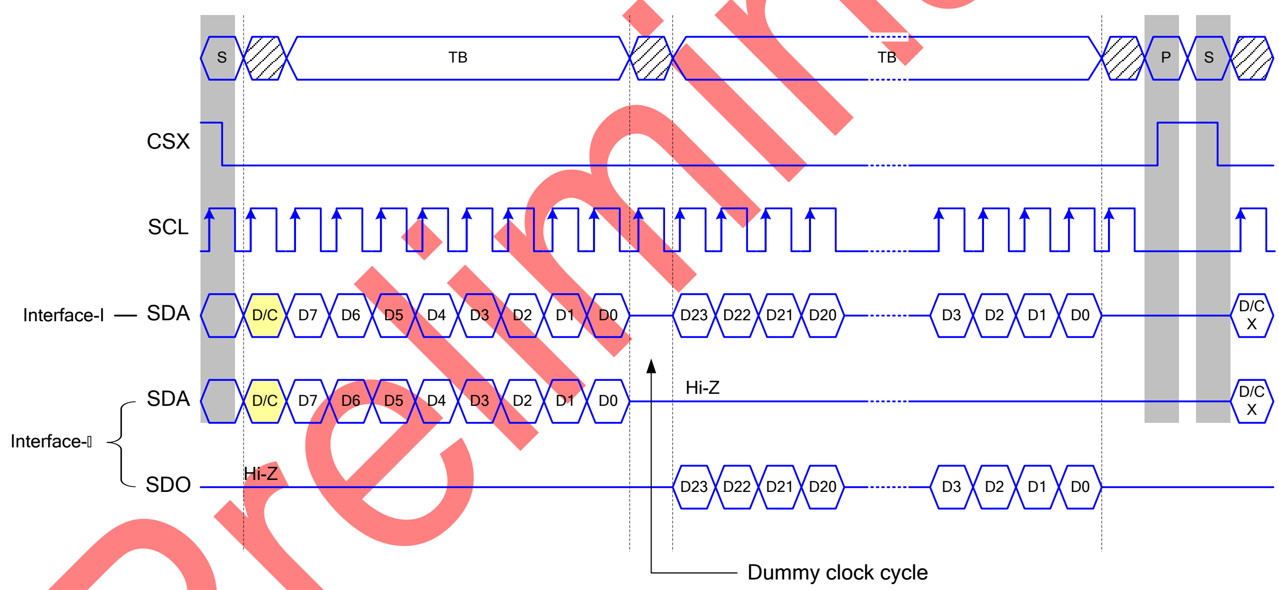
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

3-line serial interface Ⅰ/Ⅱ protocol:

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

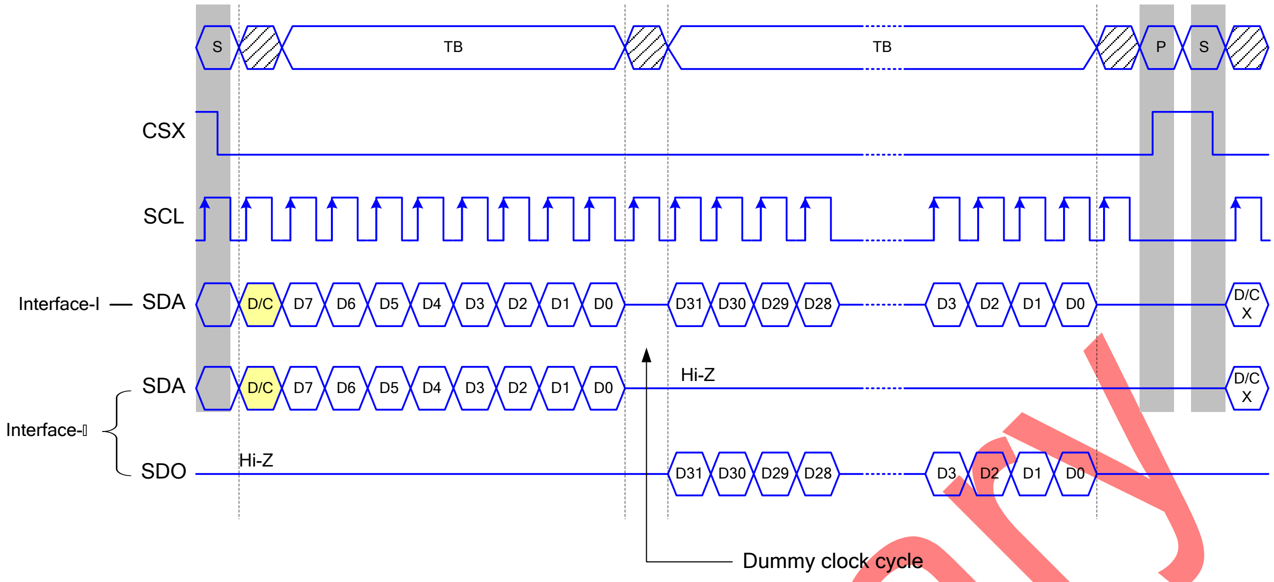


Figure 25 3-line serial interface read protocol

8.4 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state.

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated.

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

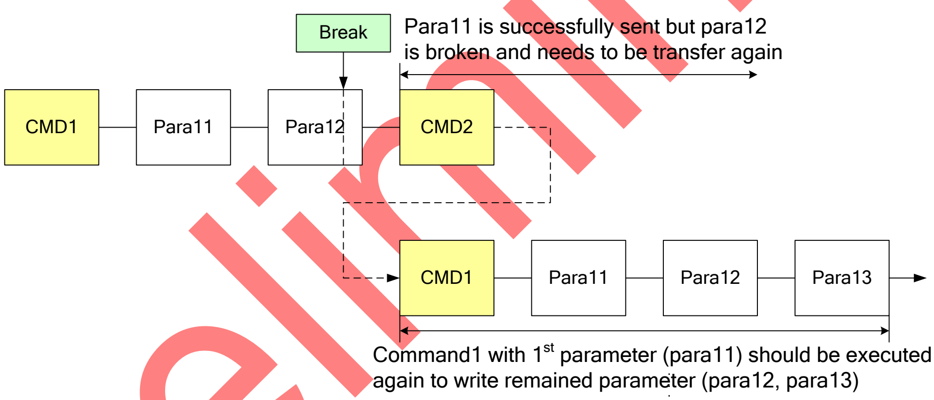


Figure 26 Write interrupts recovery (serial interface)

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

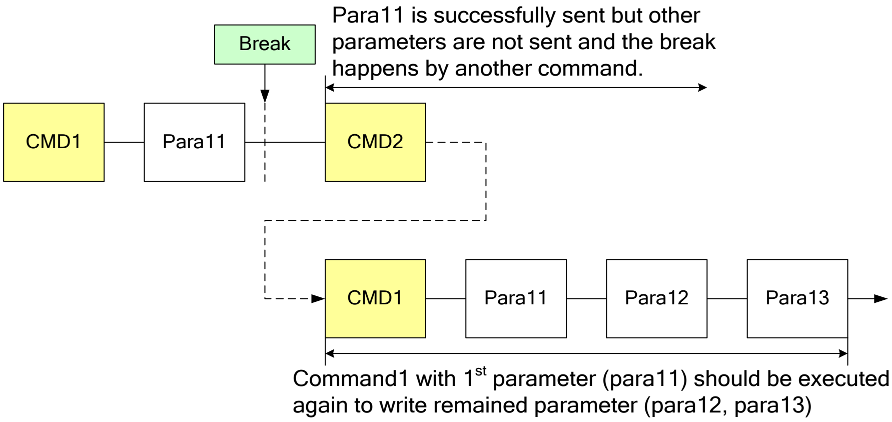


Figure 27 Write interrupts recovery (both serial and parallel Interface)

8.5 Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select Line is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select line is next enabled as shown below.

This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

8.5.1 Parallel interface pause

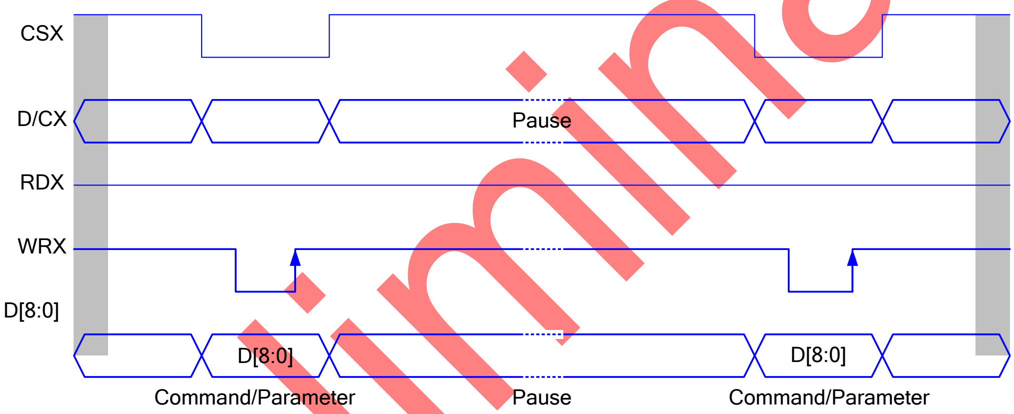


Figure 28 Parallel bus pause protocol (paused by CSX)

8.6 Data Transfer Mode

The module has three kinds color modes for transferring data to the display RAM. These are 12-bit color per pixel, 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

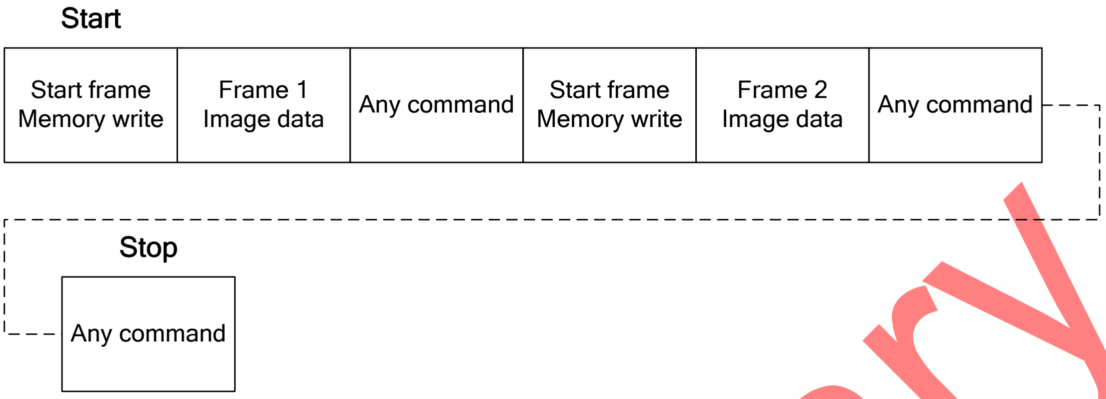
8.6.1 Method 1

The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.

Start					Stop
Start frame Memory write	Frame 1 Image data	Frame 2 Image data	Frame 3 Image data	-------	Any command

8.6.2 Method 2

The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

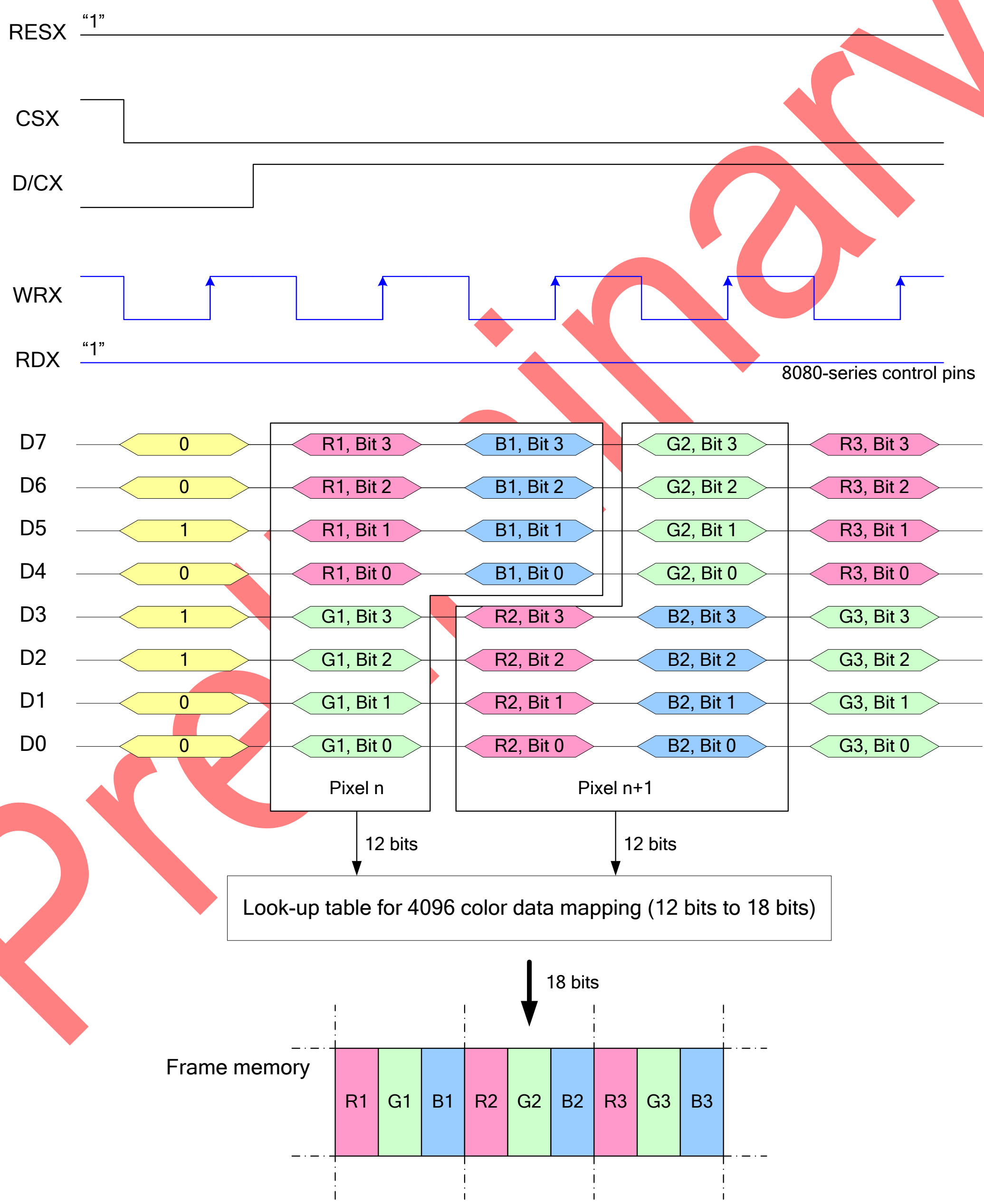
8.7 Data Color Coding

8.7.1 8080 series 8-bit Parallel Interface

The 8080 series 8-bit parallel interface of ST7785M can be used by setting IM[3:0]="0000b". Different display data formats are available for three Colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input.
- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

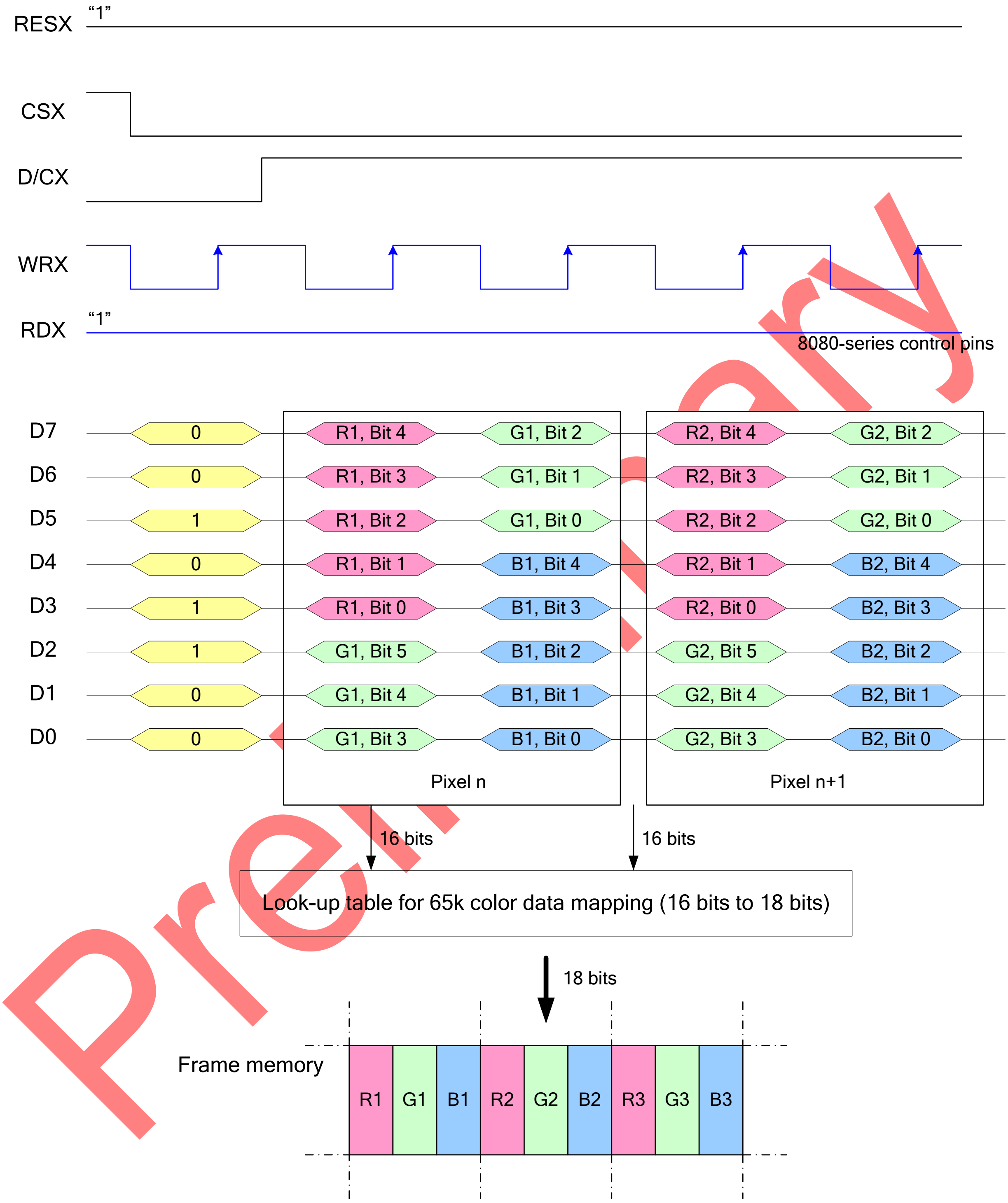
8.7.2 8-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3Ah="03h"



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 3-time transfer is used to transmit 2 pixel data with the 12-bit color depth information.
Note 3: '-' = Don't care – Can be set to '0' or '1'

8.7.3 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah=”05h”

There is 1pixel (3 sub-pixels) per 2-byte



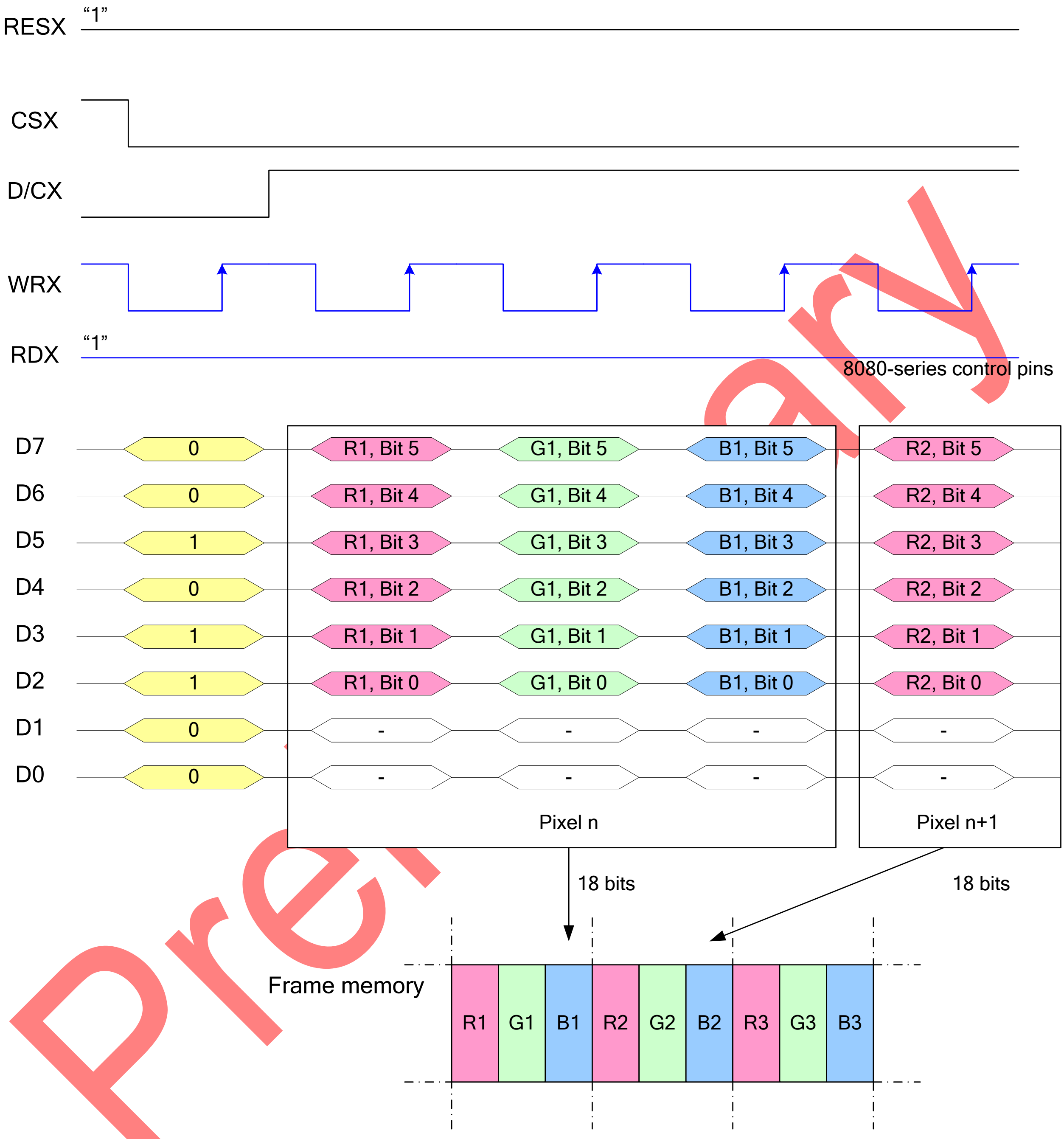
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

8.7.4 8-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah=”06h”

There is 1pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3: ‘-‘ = Don’t care – Can be set to ‘0’ or ‘1’

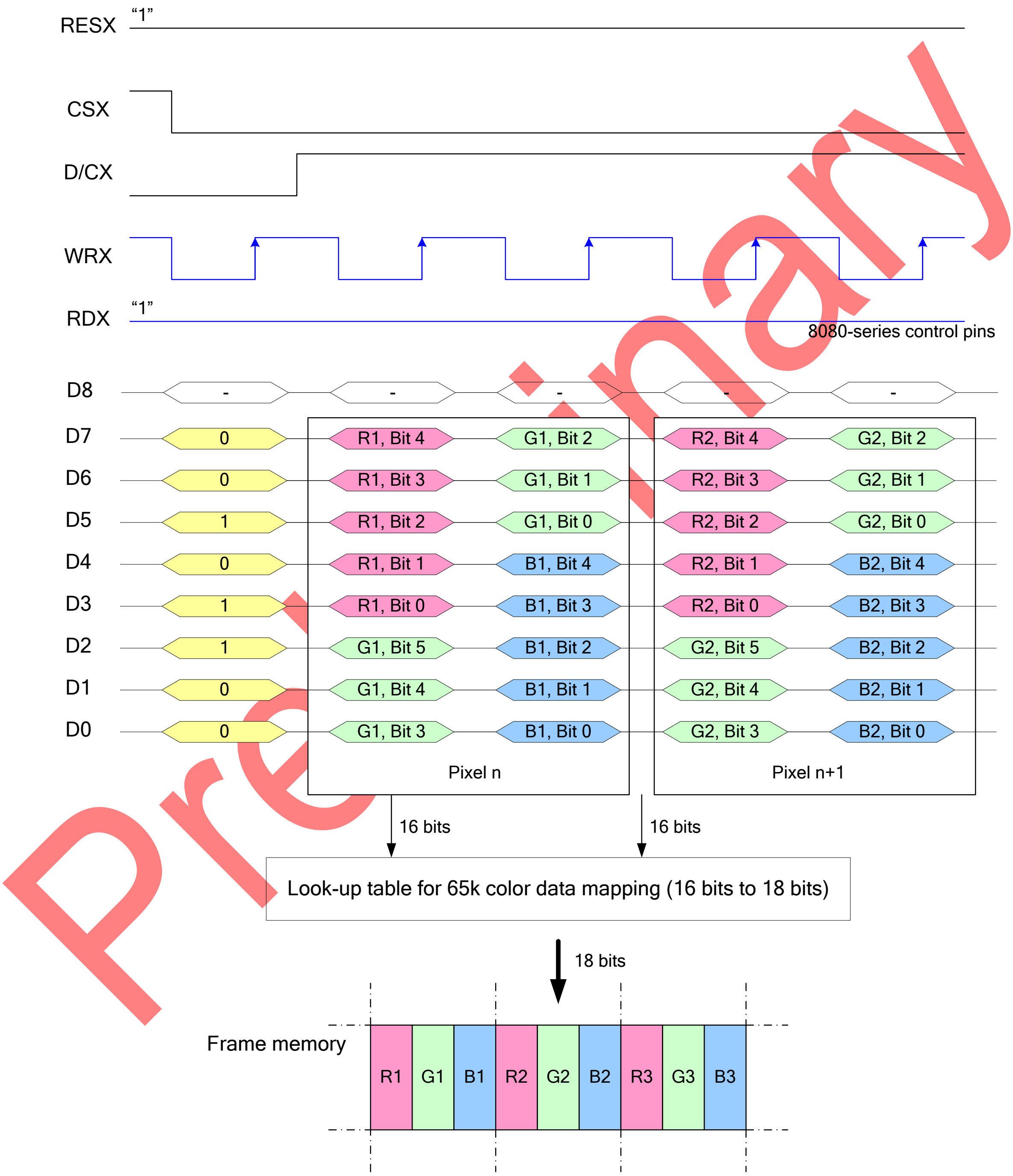
8.7.5 8080 series 9-Bit Parallel Interface

The 8080 series 9-bit parallel interface of ST7785M can be used by setting IM [3:0]="0010b"Different display data formats are available for two colors depth supported by listed below.

-65k colors, RGB 5, 6, 5-bit input

-262k colors, RGB 6, 6, 6-bit input

8.7.6 Write 9-bit data for RGB 5-6-5-bit input (65K-Color), 3Ah="05h"



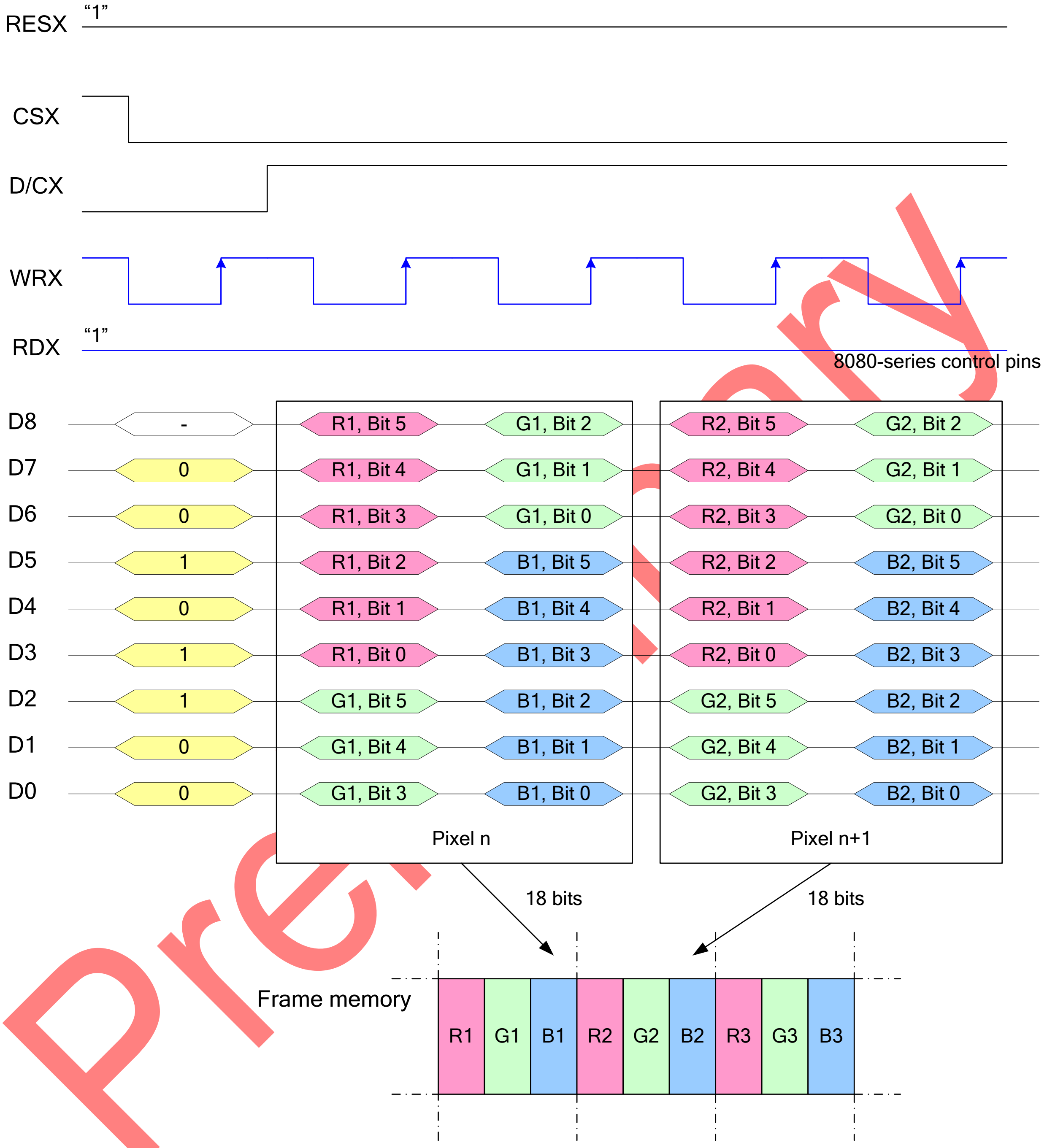
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 4, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

8.7.7 Write 9-bit data for RGB 6-6-6-bit input (262K-Color), 3Ah="06h", MDT [1:0]="00b"

There is 1 pixel (3 sub-pixels) per 2bytes

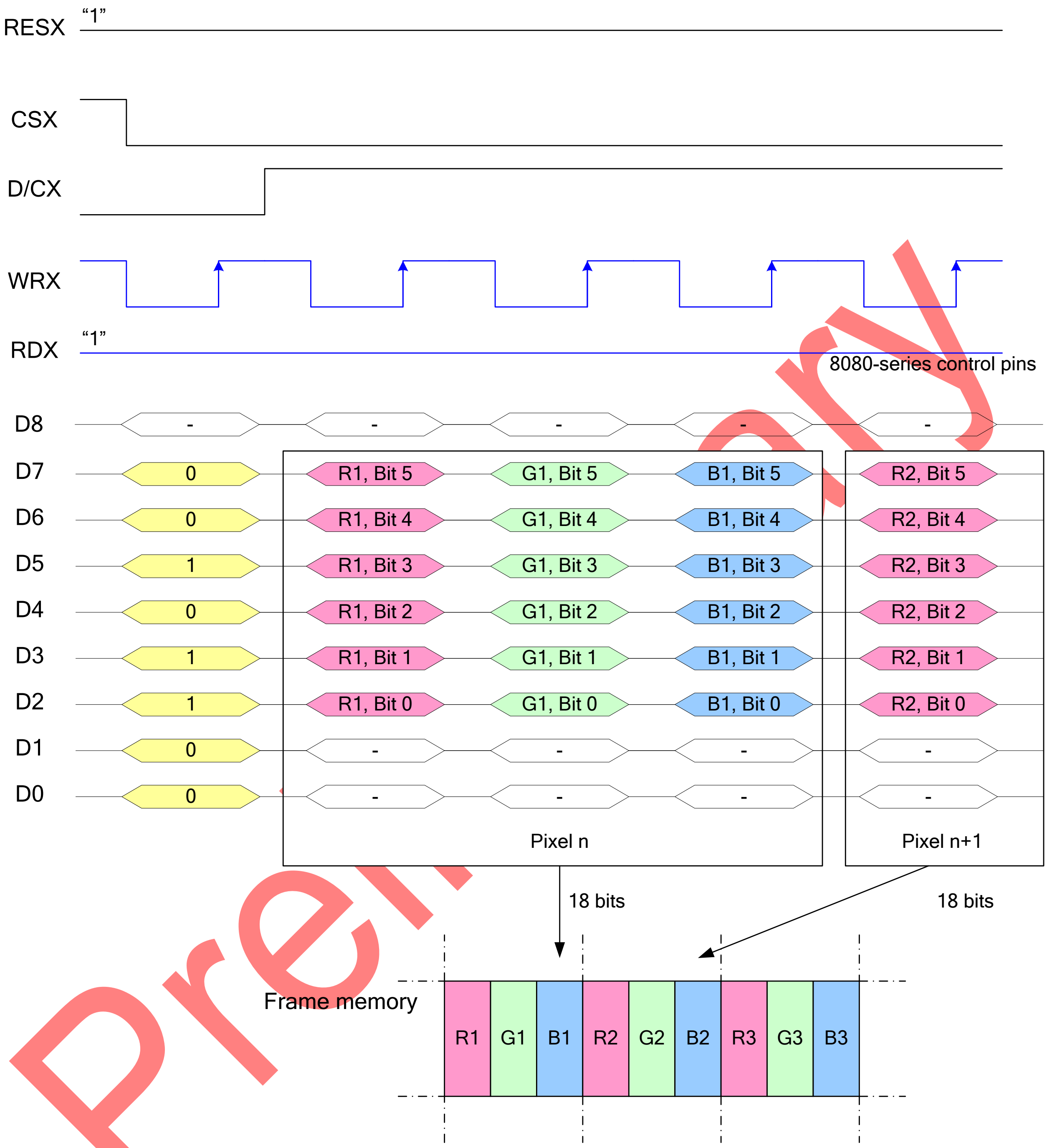


Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 2-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

8.7.8 Write 9-bit data for RGB 6-6-6-bit input (262K-Color), 3Ah="06h", MDT [1:0]="01b"



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 3-time transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3: '-' = Don't care – Can be set to '0' or '1'

8.7.9 3-Line Serial Interface

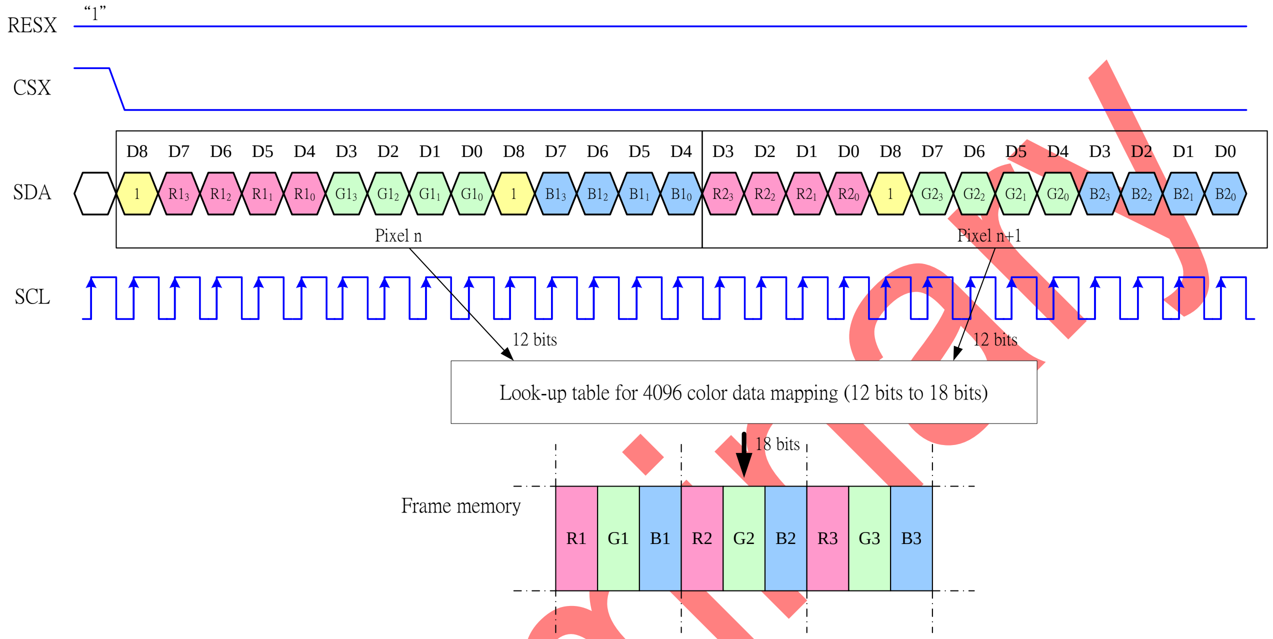
Different display data formats are available for three colors depth supported by the LCM listed below.

4k colors, RGB 4-4-4-bit input

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

8.7.10 Write data for 12-bit/pixel (RGB-4-4-4 bit input), 4K-Colors, 3Ah="03h"

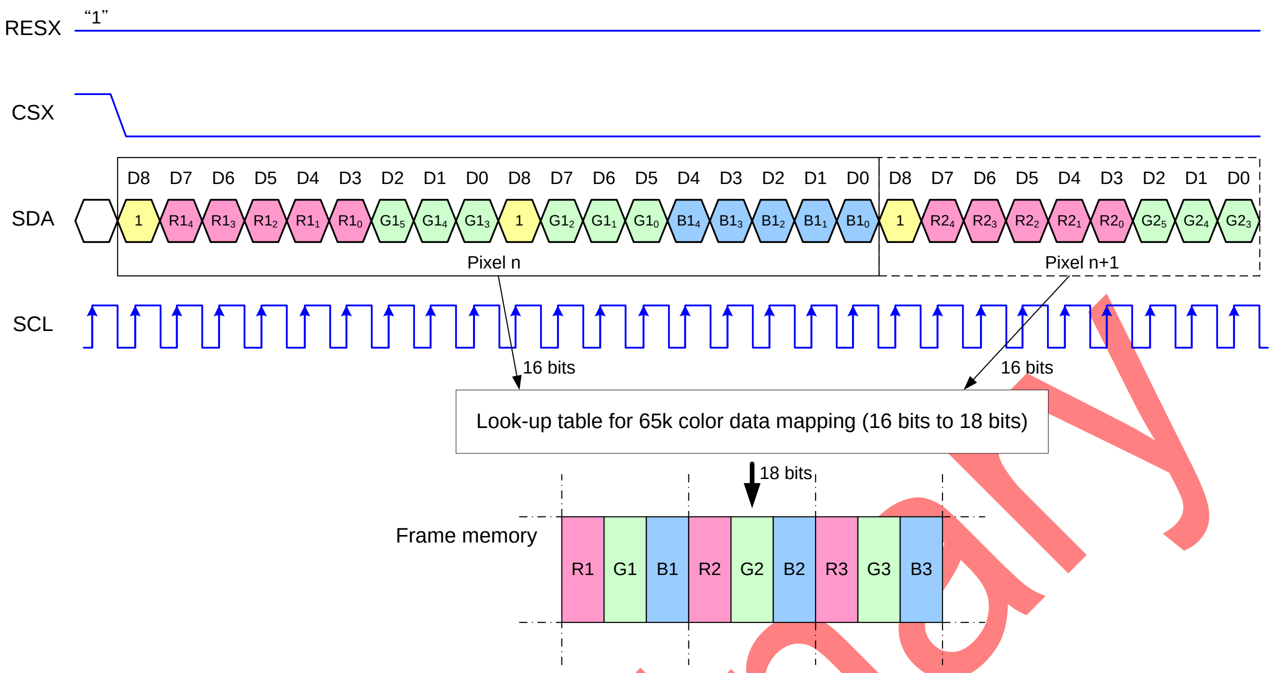


Note 1: Pixel data with the 12-bit color depth information

Note 2: The most significant bits are: Rx3, Gx3 and Bx3

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.7.11 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah=”05h”

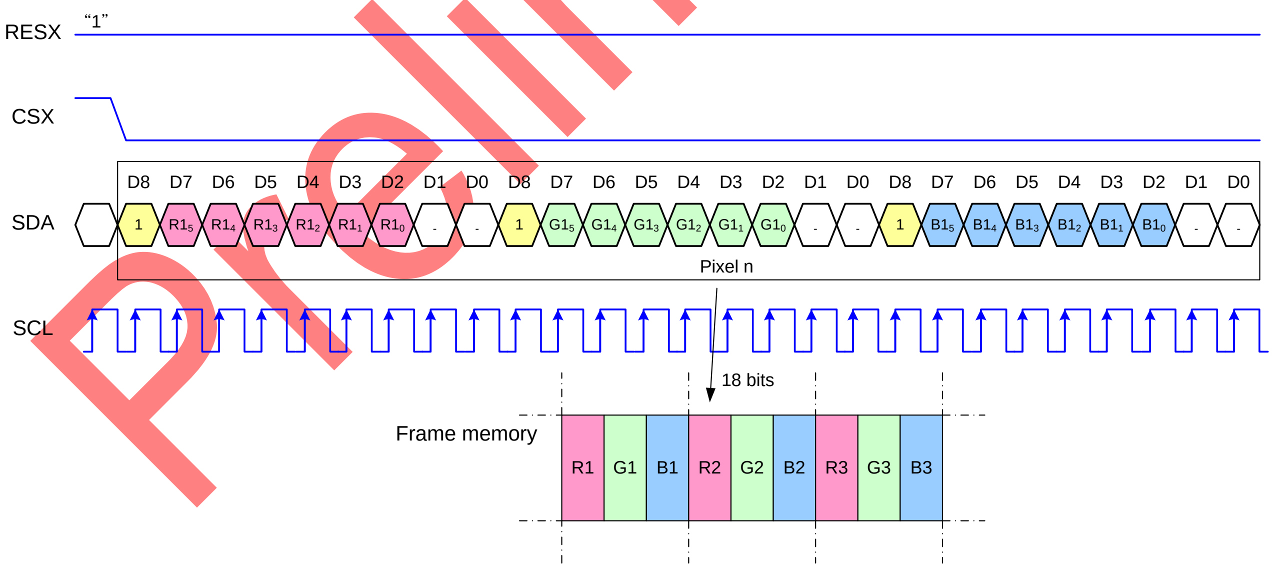


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.7.12 Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah=”06h”



Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.7.13 4-Line Serial Interface

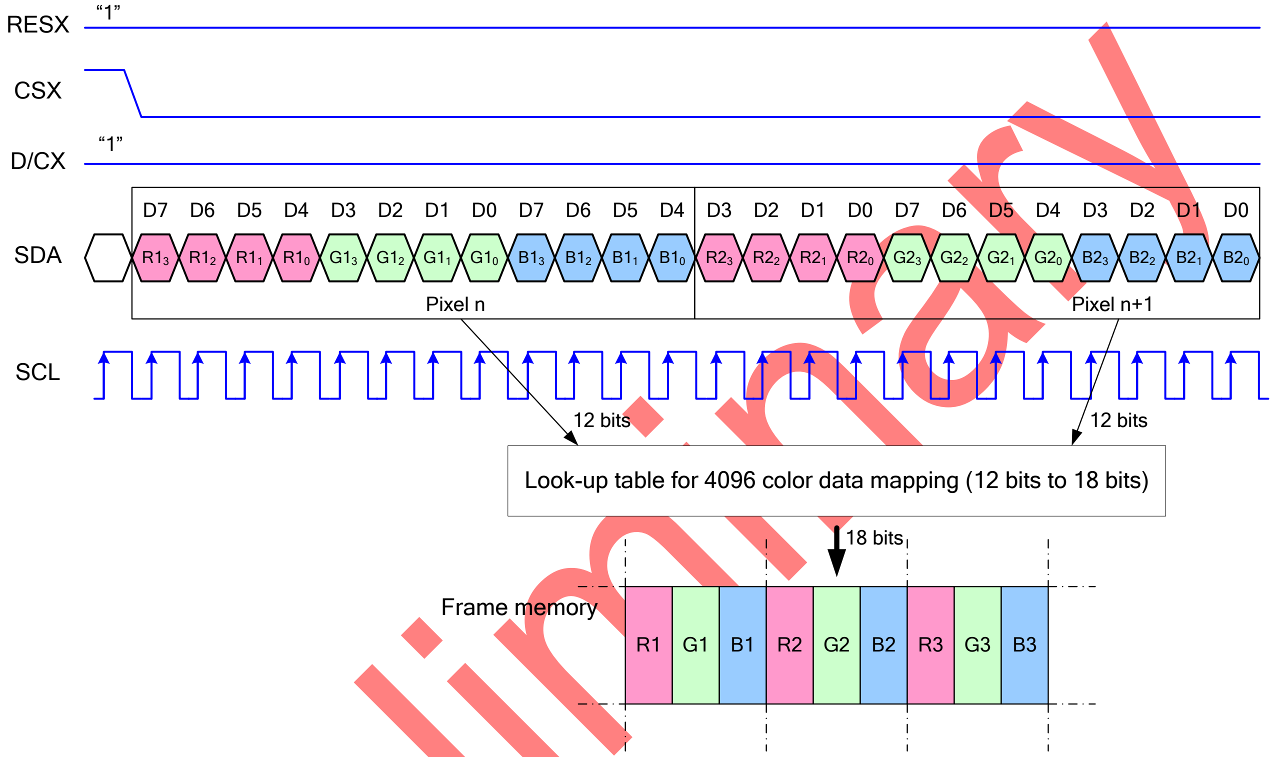
Different display data formats are available for three colors depth supported by the LCM listed below.

4k colors, RGB 4-4-4-bit input

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

8.7.14 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3Ah=”03h”

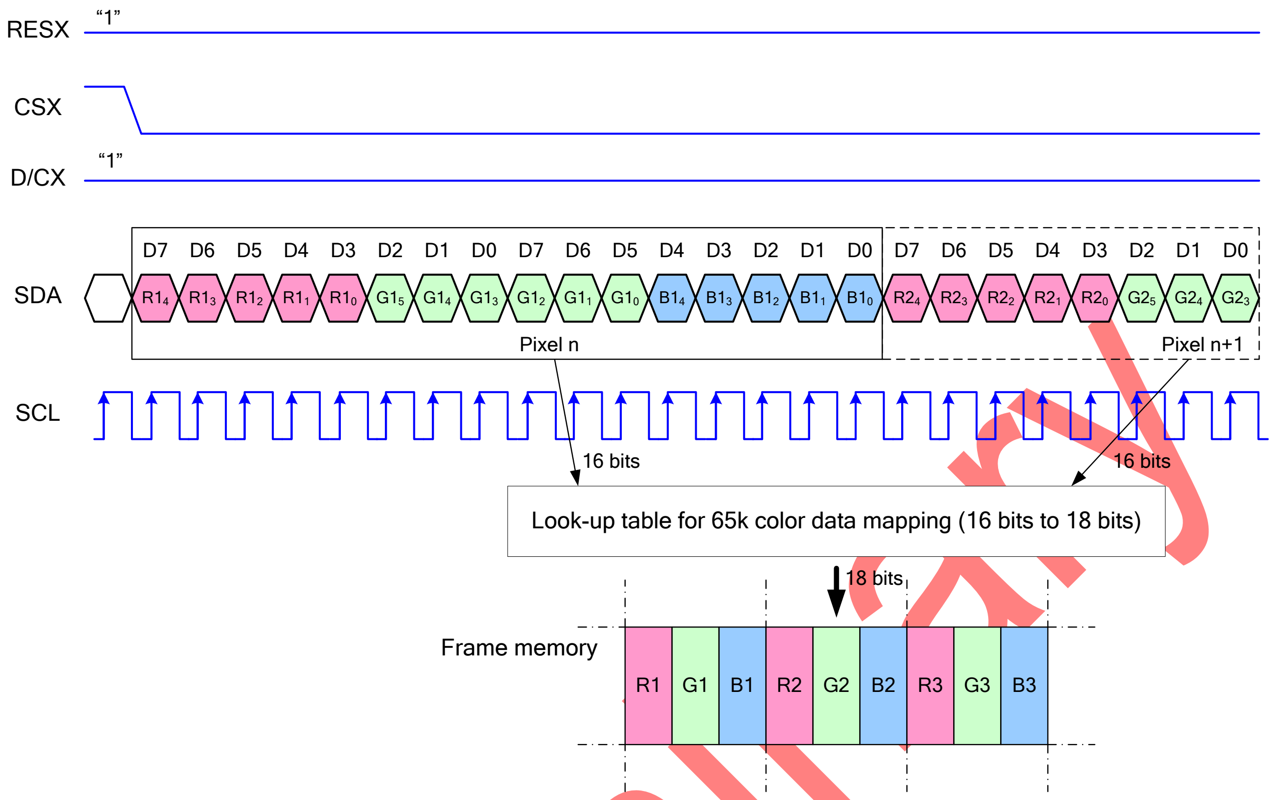


Note 1. pixel data with the 12-bit color depth information

Note 2. The most significant bits are: Rx3, Gx3 and Bx3

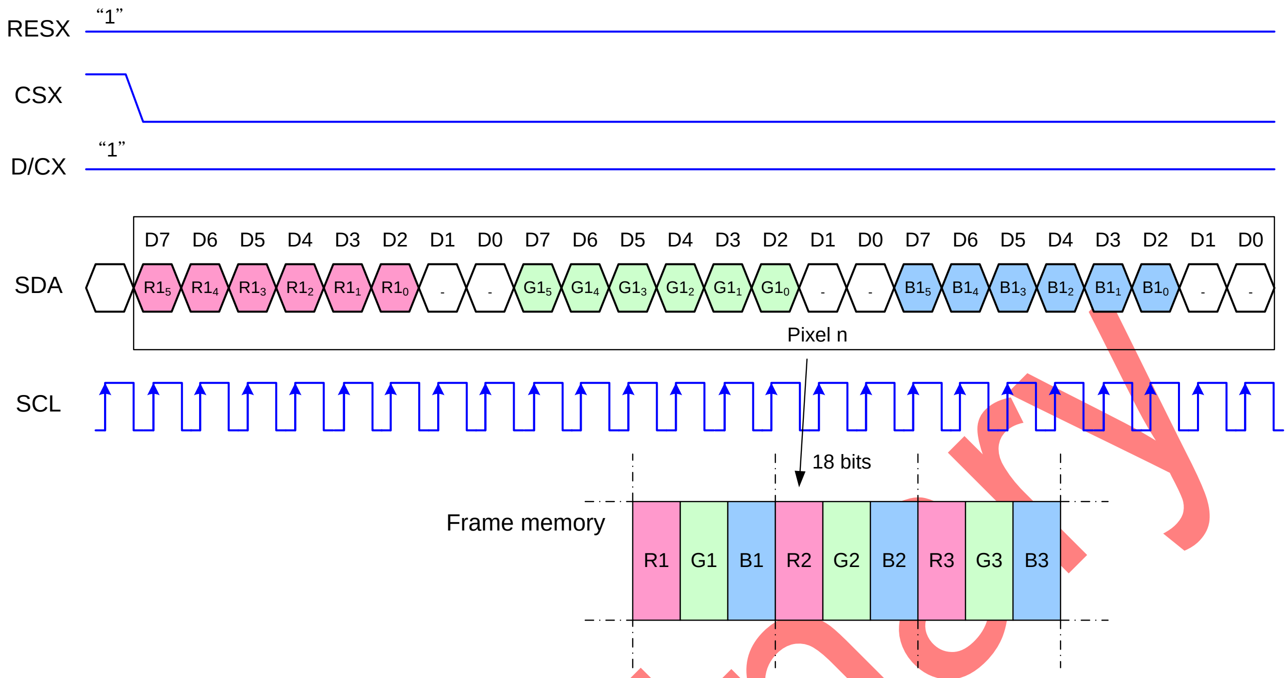
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

8.7.15 Write data for 16-bit/pixel (RGB-5-6-5-bit input), 65K-Colors, 3Ah=”05h”



Note 1. pixel data with the 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

8.7.16 Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah=”06h”



Note 1. Pixel data with the 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

8.8 RGB Interface

8.8.1 RGB Interface Selection

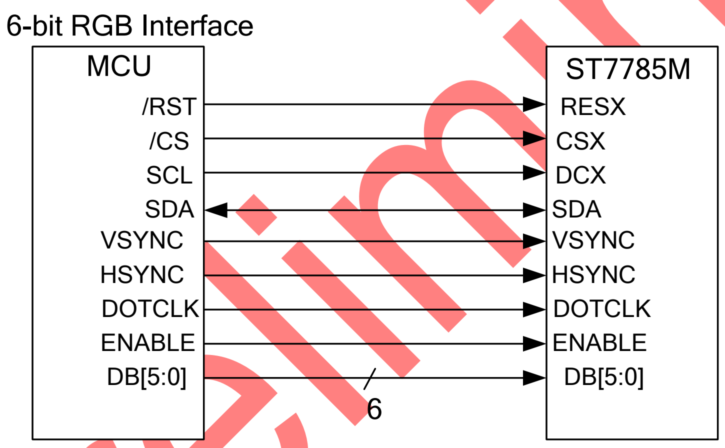
The color format selection of RGB Interface for ST7785M is selected by setting the RIM and command 3Ah, DB [6:4].

RIM	3Ah, DB[6:4]	RGB Interface Mode	Data pins
1	110	6-bit 262K RGB Interface	DB[5:0]
1	101	6-bit 65K RGB Interface	DB[5:0]

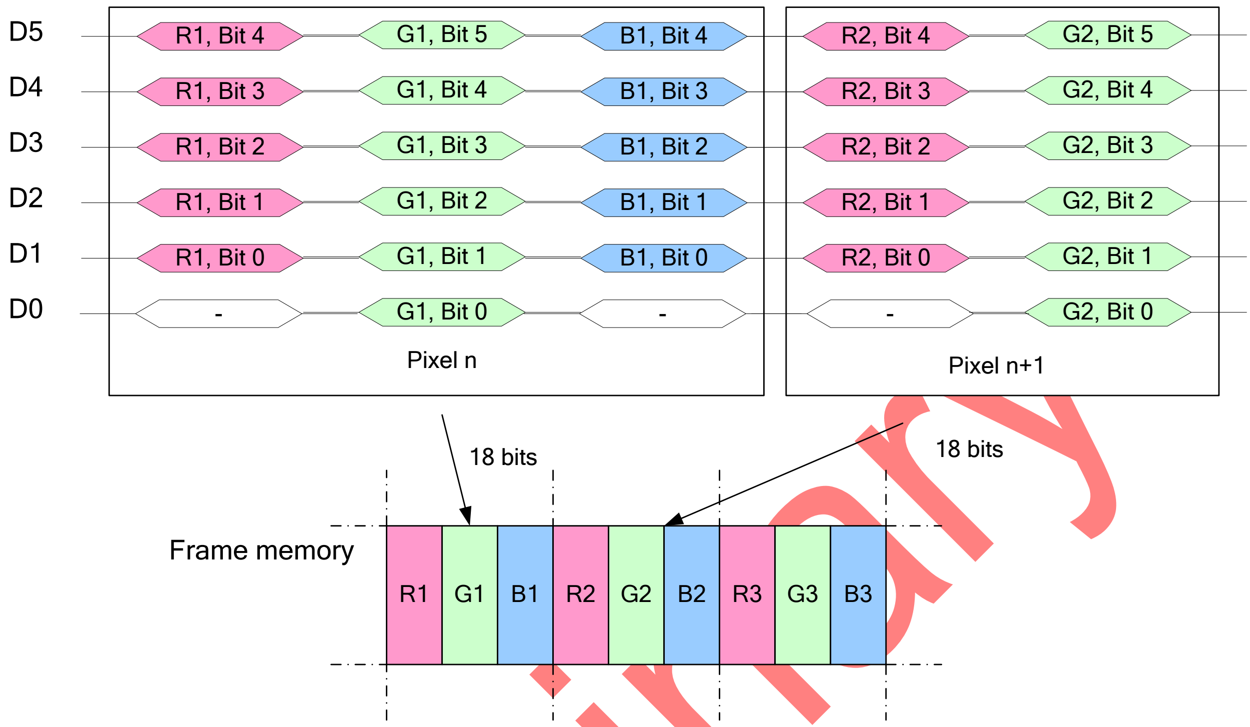
8.8.2 RGB Color Format

ST7785M supports two kinds of RGB interface, DE mode and HV mode, and only 6bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D [5:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D [5:0] pins can be used. When using RGB interface, only serial interface can be selected.

6-bit RGB interface hardware suggestion, IM [3:0]=0101.



Write data for 6-bit/pixel (RGB 5-6-5-bit input), 65K-Colors



Write data for 6-bit/pixel (RGB 6-6-6-bit input), 262K-Colors

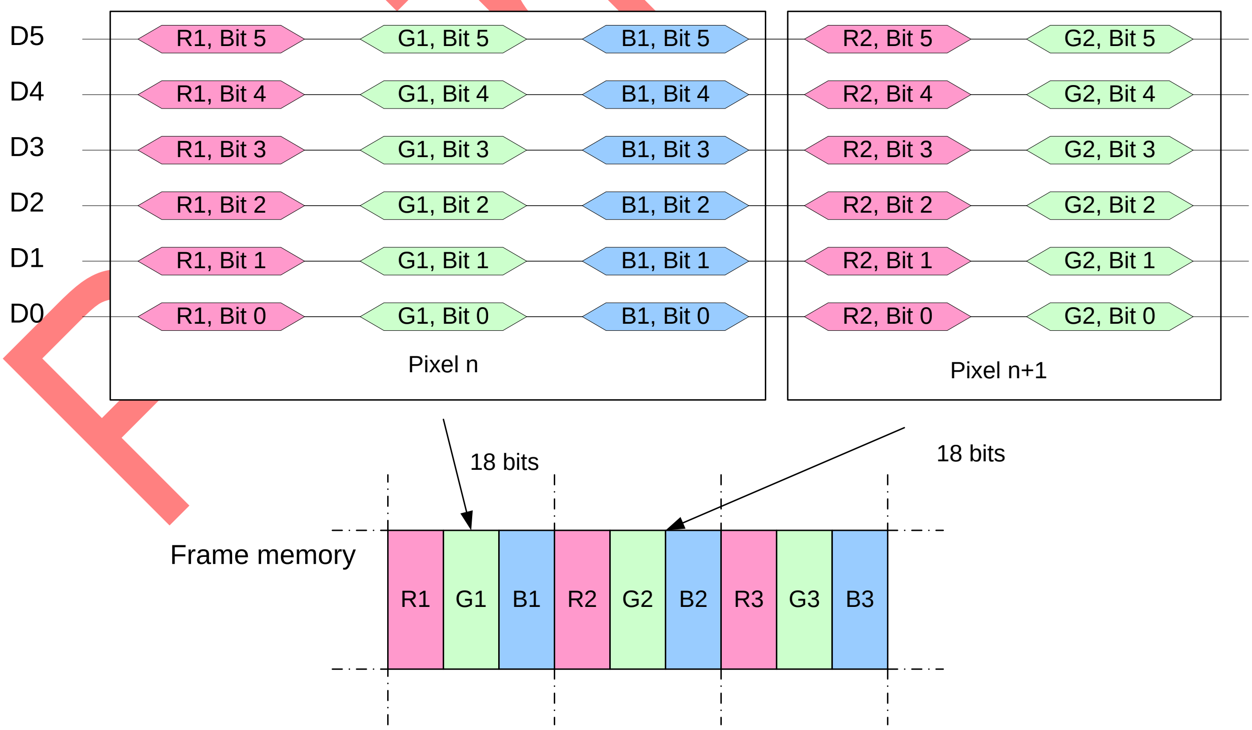


Figure 29 RGB Interface Data Format

8.8.3 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.

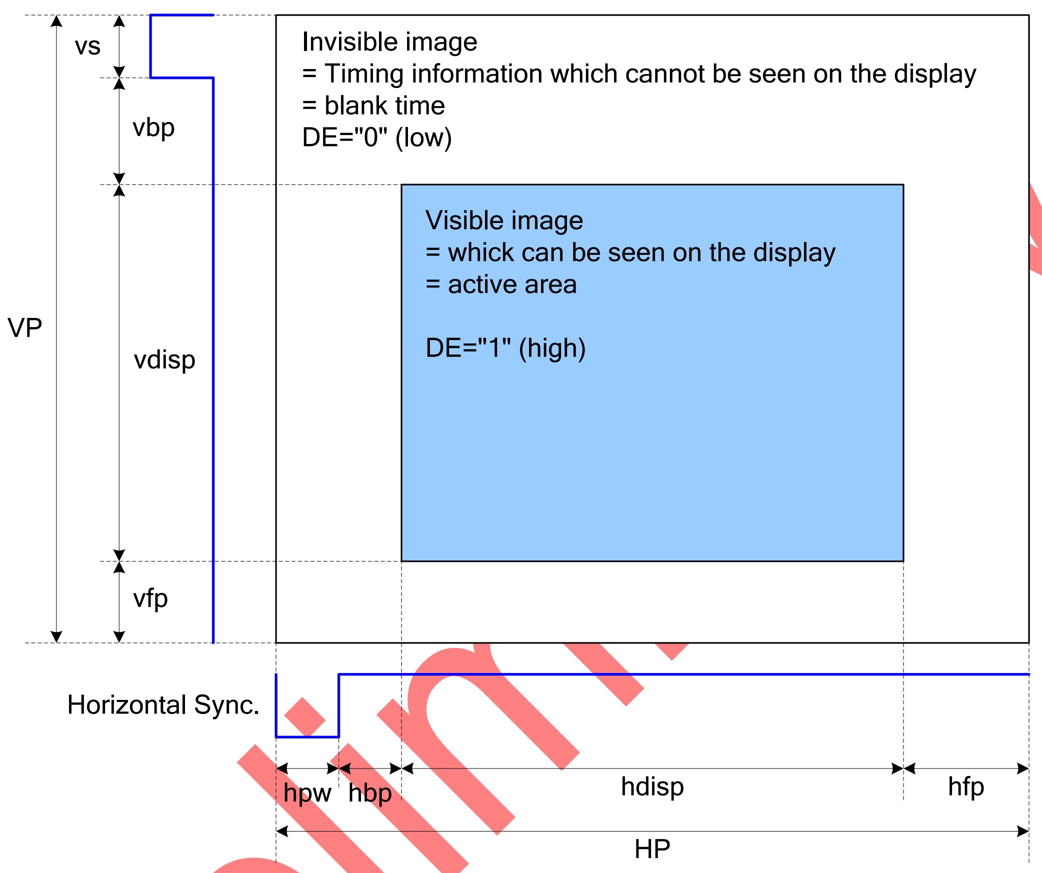


Figure 30 DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

6bit RGB interface:

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	TBD	TBD	TBD	Clock
Horizontal Sync. Back Porch	hbp	TBD	TBD		Clock
Horizontal Sync. Front Porch	hfp	TBD	TBD	TBD	Clock
Vertical Sync. Width	vs	TBD	TBD	TBD	Line
Vertical Sync. Back Porch	vbp	TBD	TBD		Line
Vertical Sync. Front Porch	vfp	TBD	TBD	TBD	Line

Note:

Typical value are related to the setting of dot clock is 17MHz and frame rate is 60Hz..

In with ram mode, hpw+hbp+hfp≧66

In without ram mode, hpw+hbp≧60

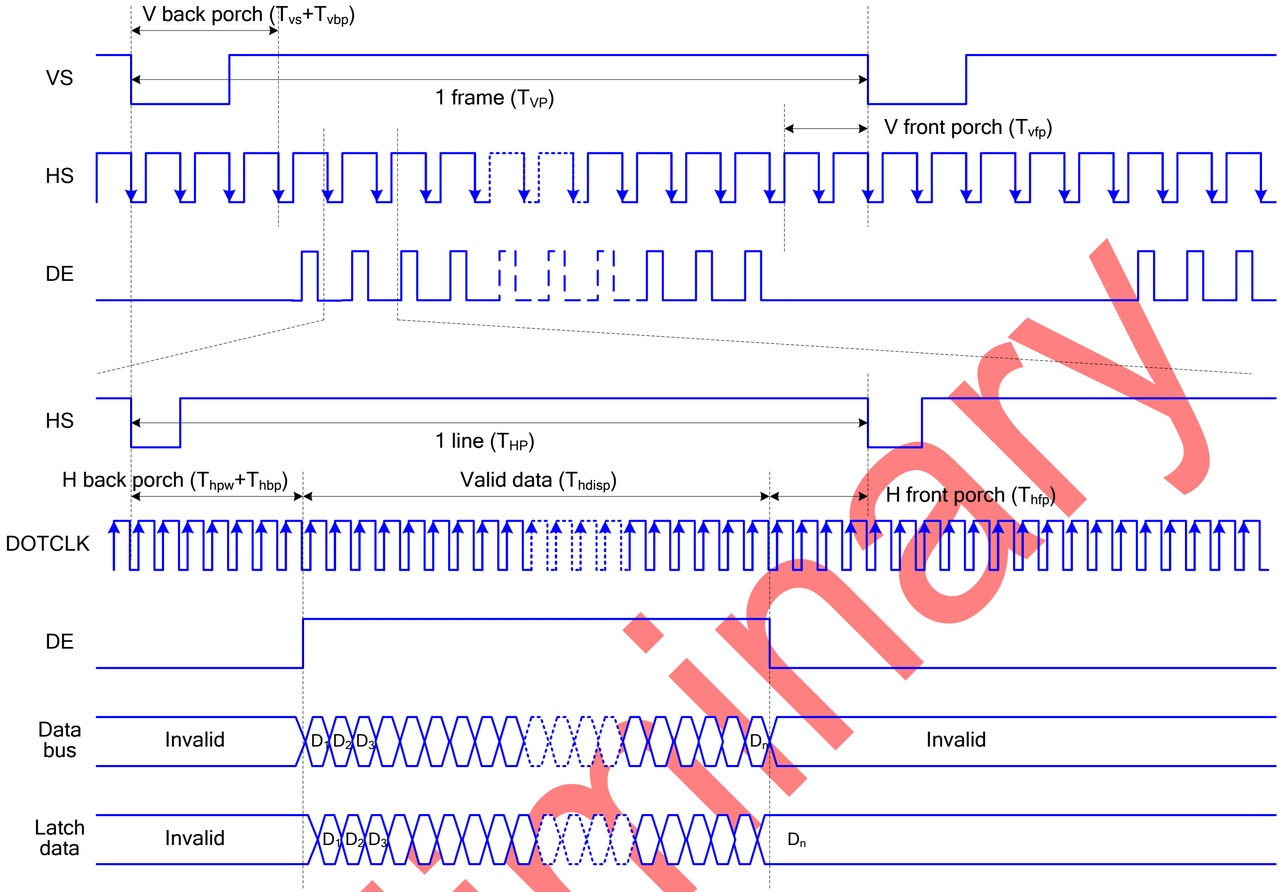
8.8.4 RGB Interface Mode Selection

ST7785M supports two kinds of RGB interface, DE mode and HV mode. Each mode also can select with ram and without ram. The table shown below uses command B1h to select RGB interface mode.

RCM[1:0]	WO	RGB Mode	Data Path
10	0	DE mode	Ram
	1		Shift register (without Ram)
11	0	HV mode	Ram
	1		Shift register (without Ram)

8.8.5 RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Figure 31 Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.

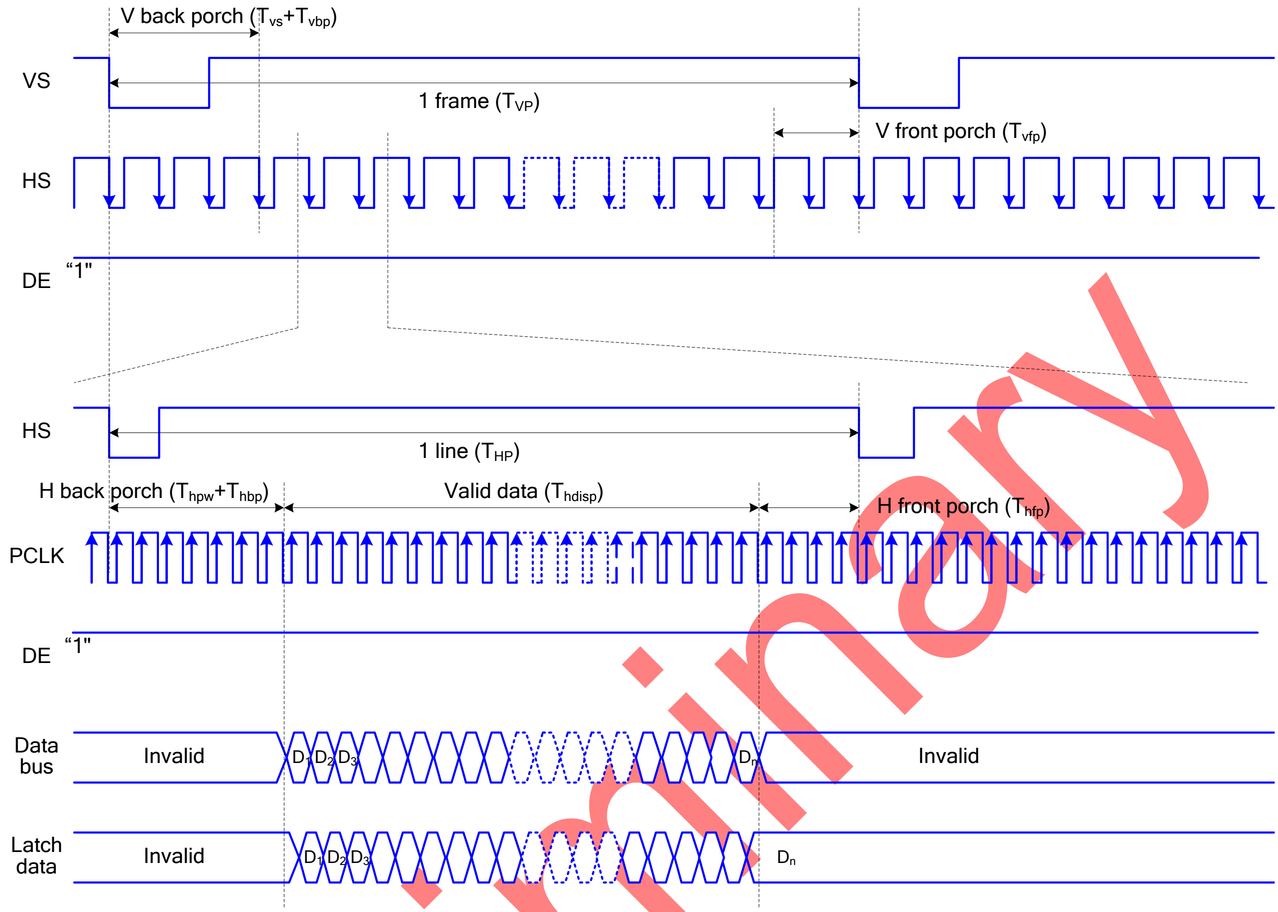


Figure 32 Timing chart of RGB interface HV mod

The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period.

In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

In 6-bit RGB interface mode, each of RGB dots are transferred in synchronization with DOTCLK signals. In other words, one pixel data needs to take three DOTCLKs to transfer.

In 6-bit RGB interface mode, the cycles of VSYNC, HSYNC, ENABLE, DOTCLK signals must be set correctly so that the data transfer is completed in units of pixels.

When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

In RGB interface mode, a RAM address is set in the address counter every frame on the falling edge of VSYNC.

8.9 VSYNC Interface

8.9.1 6-bit RGB Interface

The ST7785M incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables tearing-free display of motion pictures with the conventional interface.

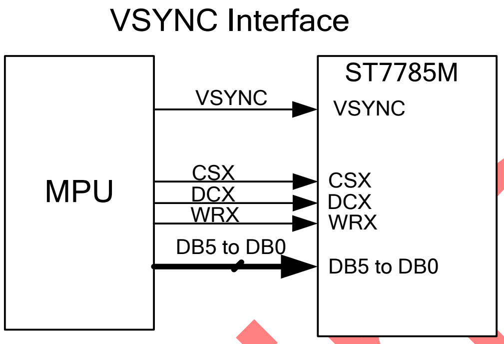


Figure 33 Data transmission through VSYNC interface

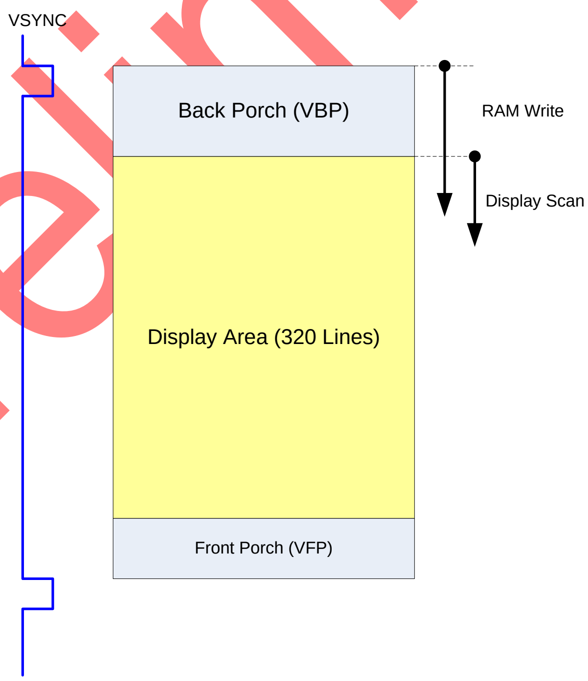


Figure 34 Operation through VSYNC Interface

Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.

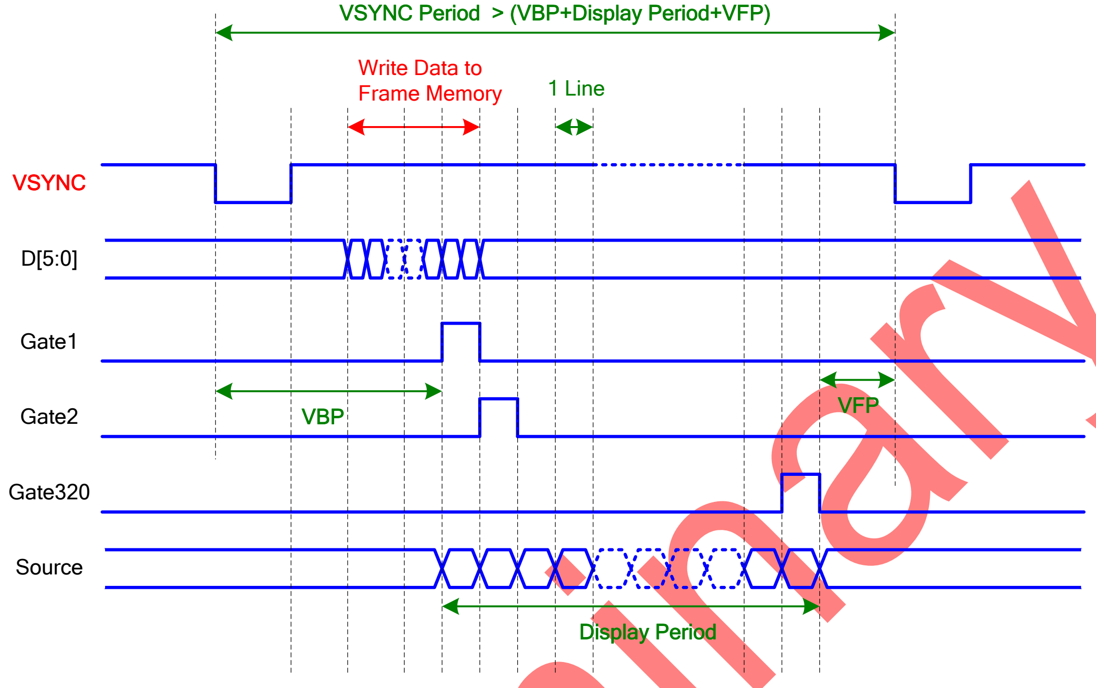


Figure 35 Timing Diagram of VSYNC Interface

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result obtained from the calculation shown below. The internal memory writing address counter is reset by VSYNC. So, insure interval time between VSYNC falling and DRAM data writing.

Note:

1. VSYNC period should always be constant. If not, some degradation of display such as flicker may occur in LCD system.

2. Display data don't need to be written for every VSYNC period. For example, any system is working under 60Hz frame rate and 30-fps motion picture condition. So being written display data for every other frame would be enough.

8.9.2 VSYNC Interface Mode

Leading Mode

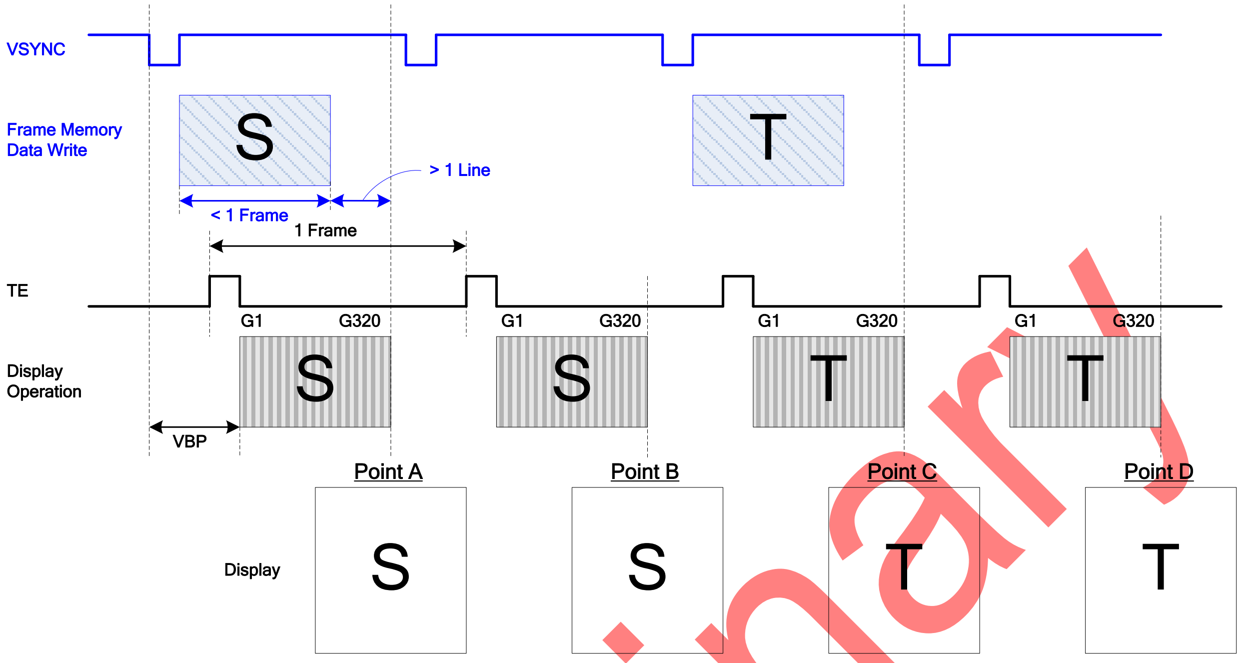


Figure 36 Operation for Leading Mode of VSYNC Interface

Lagging Mode

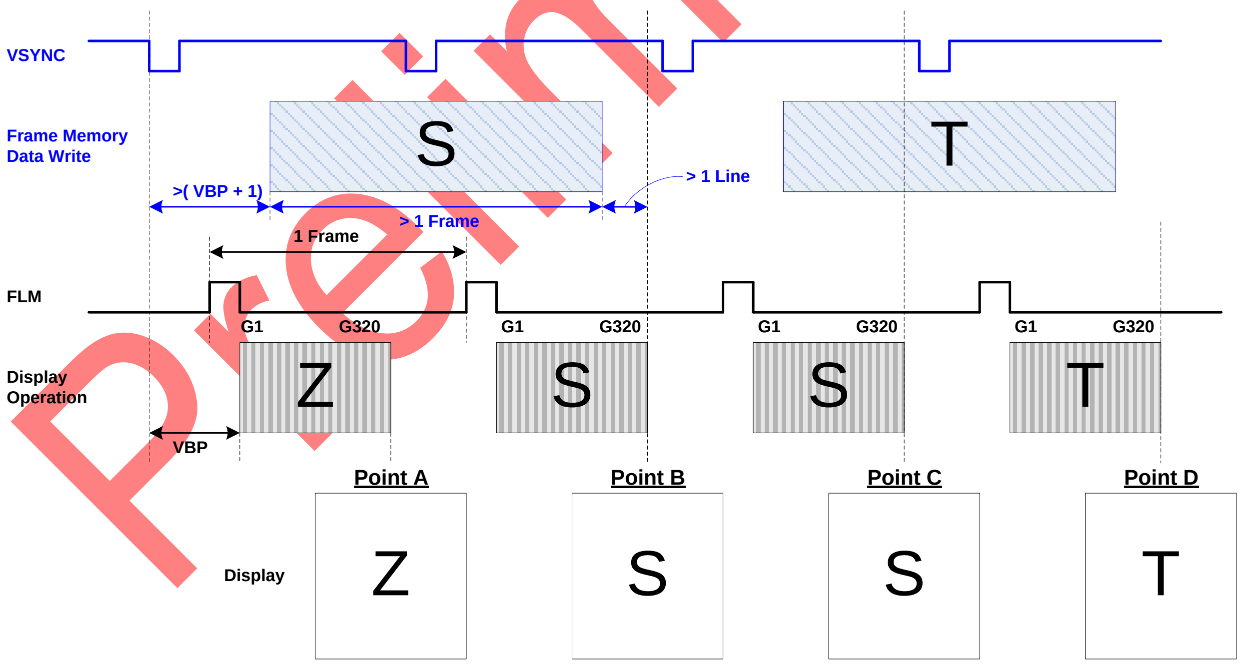


Figure 37 Operation for Lagging Mode of VSYNC Interface

Notes:

1. When RAM writing does not start immediately after the falling edge of VSYNC, the time between the falling edge of VSYNC and the RAM writing start timing must also be considered.

1. The minimum DRAM write speed must be satisfied and the frequency variation must be taken into consideration.

2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.

3. When switching from the internal clock operation mode to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.

4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode and set the AM bit to "0" to transfer display data.

8.10 MIPI-DSI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

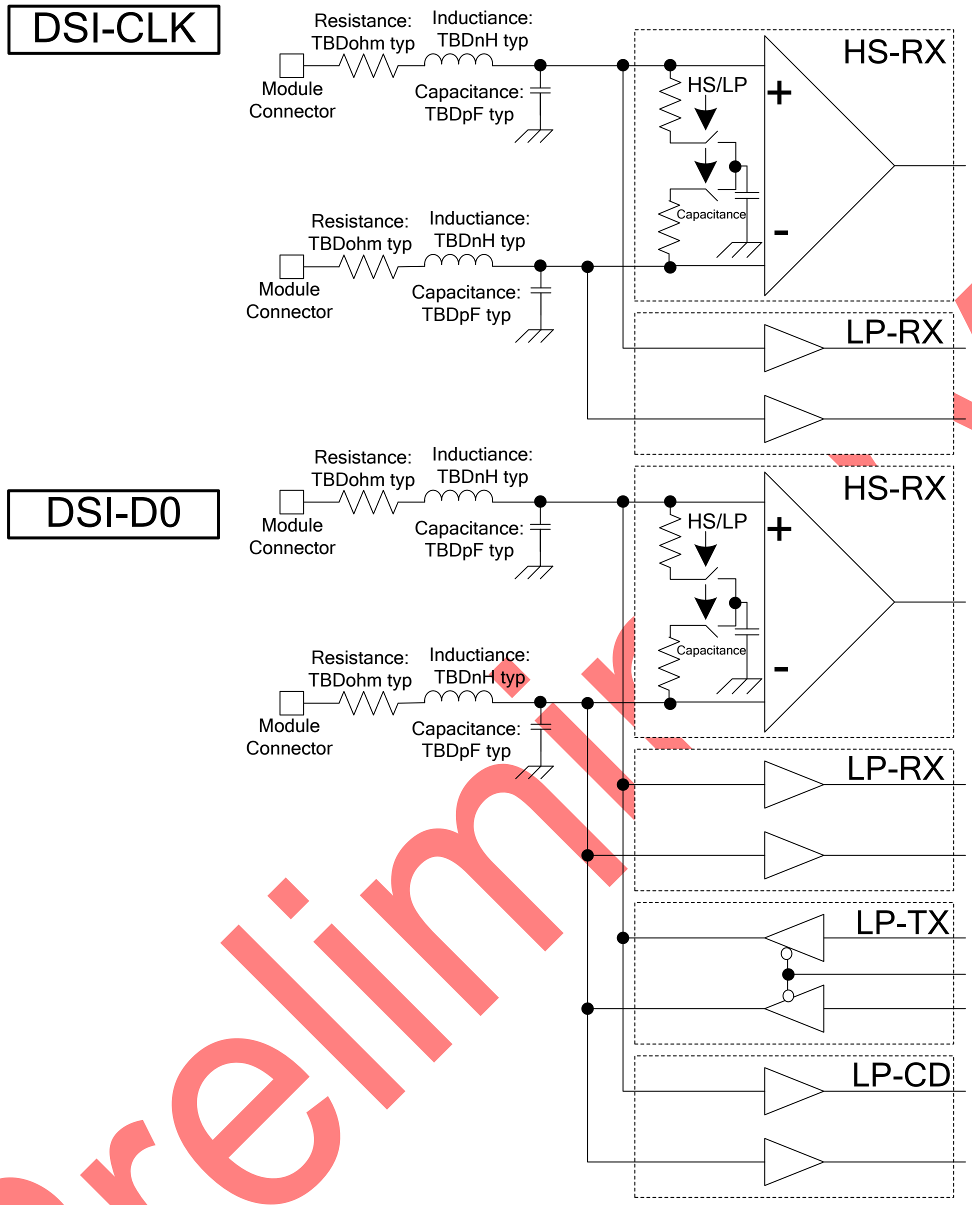
Command Mode refers to operation in which transactions primarily take the form of sending commands to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Configuration:

Lane Pair	MCU (Master)　Display Module (Slave)
Clock Lane	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane 0	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT

8.10.1 Display Module Pin Configuration for DSI



8.10.1 Display Serial Interface (DSI)

8.10.1.1 General description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface level: Low level communication

- Packet level: High level communication

8.10.1.2 Interface level communication

8.10.1.2.1 General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane0 can be driven Low Power (LP) or High Speed (HS) mode.

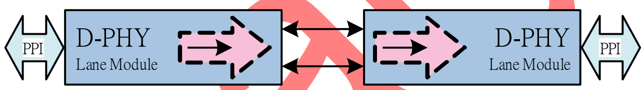
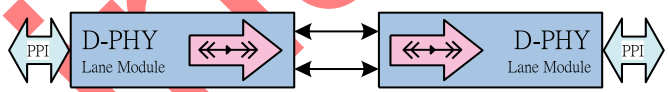
	Lane support mode	
Clock Lane	Unidirectional lane High-Speed Clock only Simplified Escape Mode (ULPS Only)	
Data Lane0	Bi-directional lane Forward high-speed only Bi-directional Escape Mode Bi-direction LPDT	

Table 18 The interface color Lane types and support mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC voltage Levels		High Speed(HS)	Low-Power(LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table 19 High Speed and Low-Power Lane Pair State Descriptions

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

8.10.1.2.2 DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

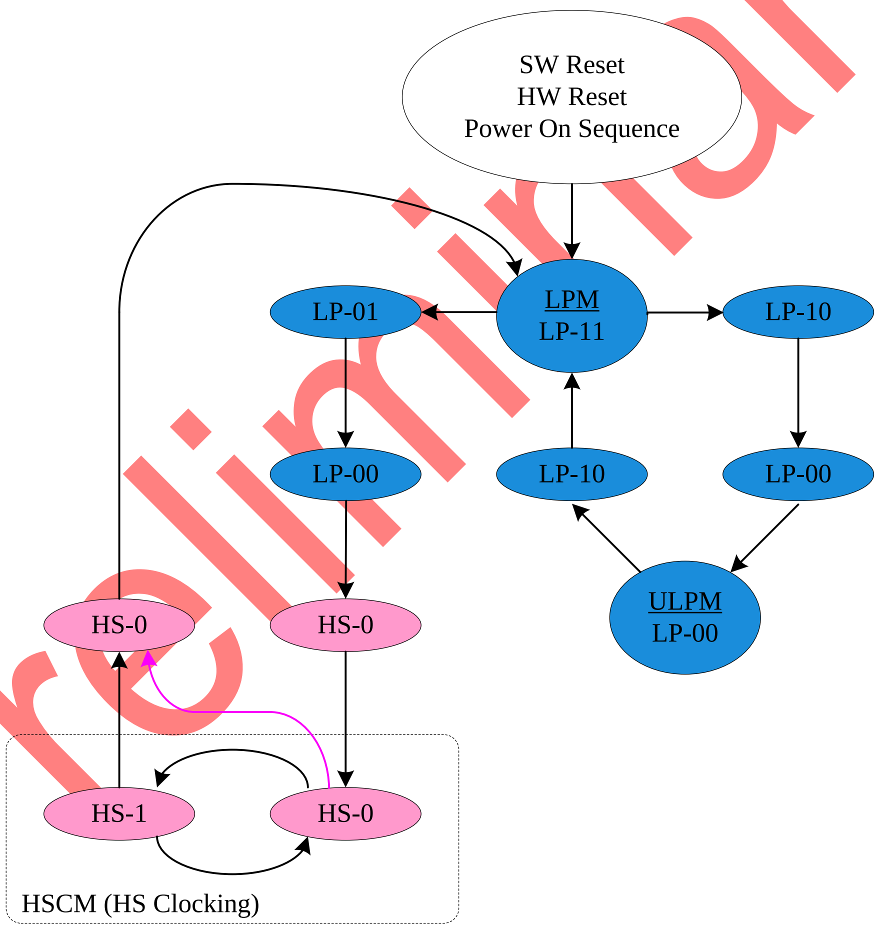


Figure 38 Clock Lanes Power Modes

8.10.1.2.2.1 Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LMP), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

After SW Reset / HW Reset or Power on Sequence=>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM,LP-00 State Code)=>LP10=>LP-11(LPM).

This sequence is illustrated below.

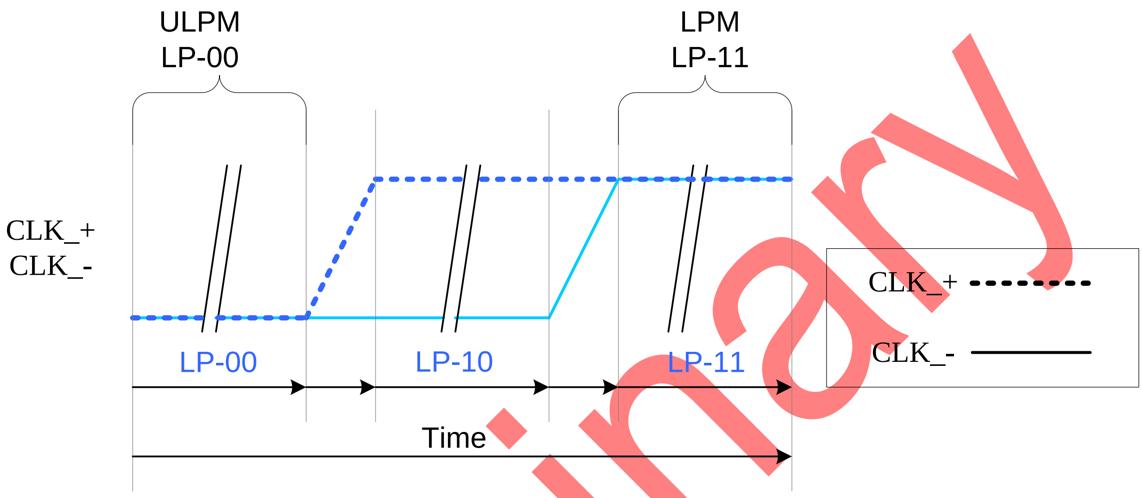


Figure 39 from ULPM to LPM

After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM).

This sequence is illustrated below.

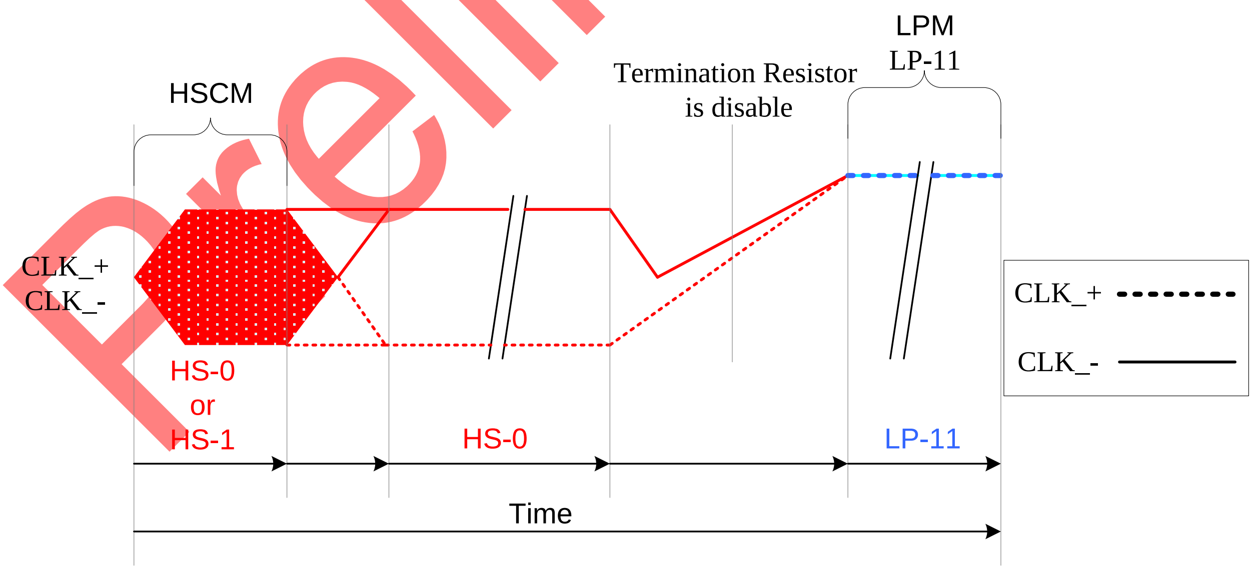


Figure 40 from HSCM to LPM

All three mode changes are illustrated a flow chart below.

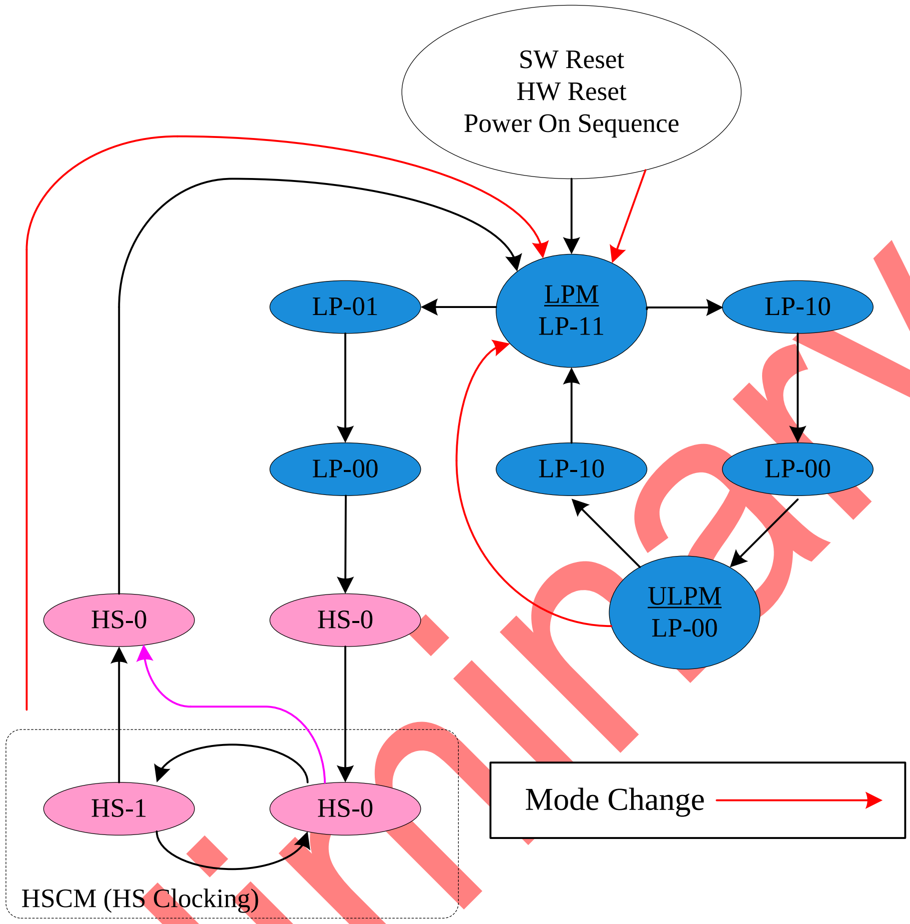


Figure 41 All three mode changes to LPM

8.10.1.2.2.2 Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00(ULPM).

This sequence is illustrated below.

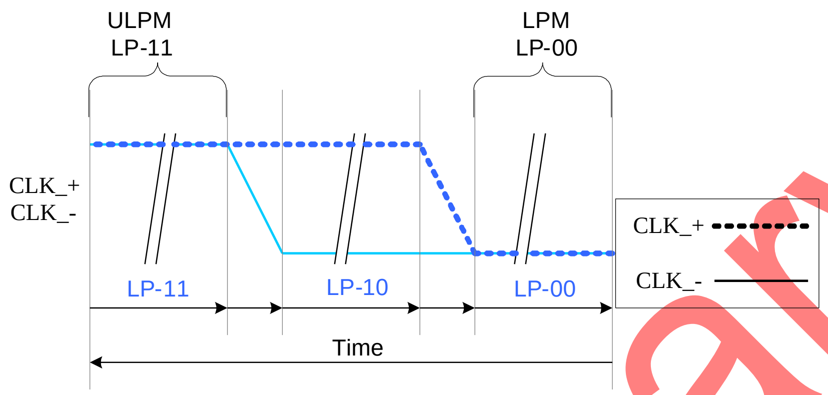


Figure 42 From LPM to UPLM

The mode change is also illustrated below:

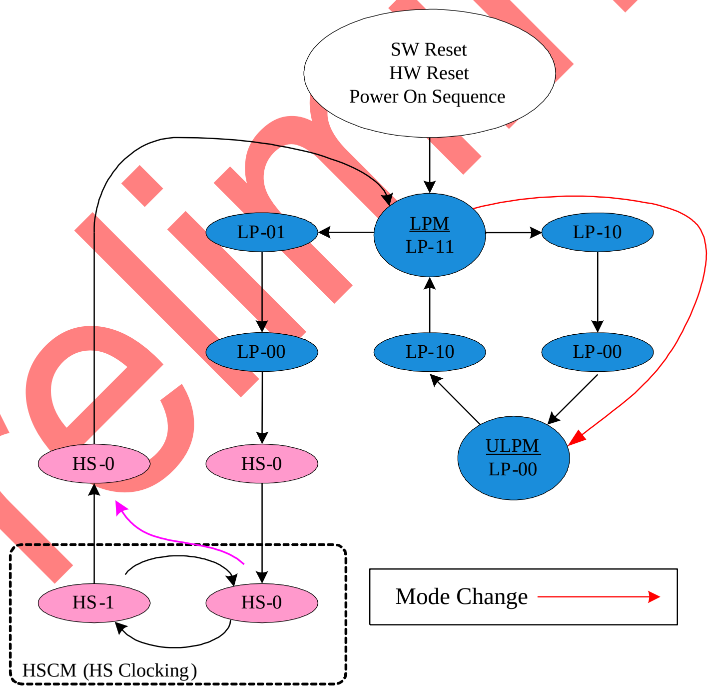


Figure 43 The mode change from LPM to UPLM

8.10.1.2.2.3 High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM).

This sequence is illustrated below.

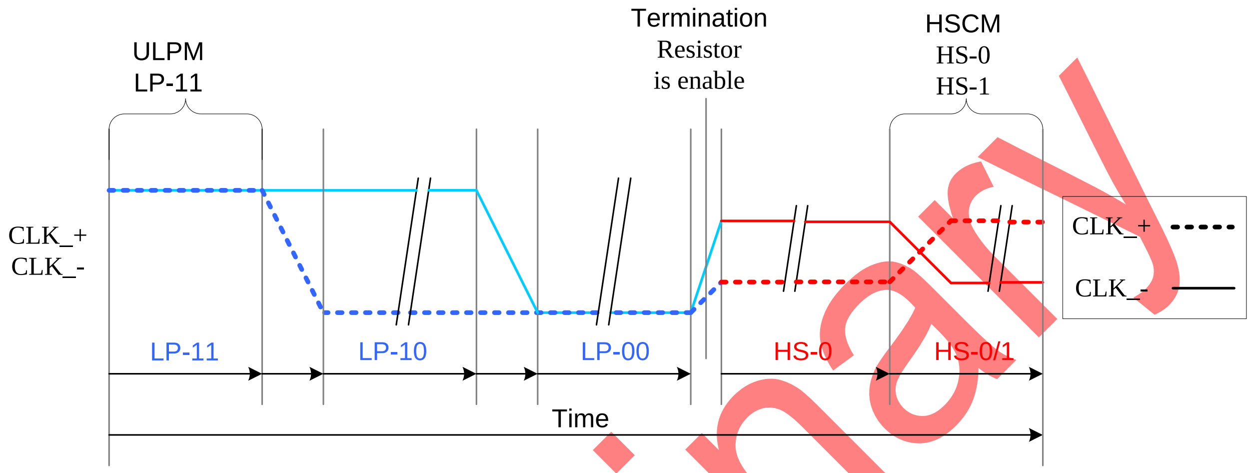


Figure 44 From LPM to HSCM

The mode change is also illustrated below:

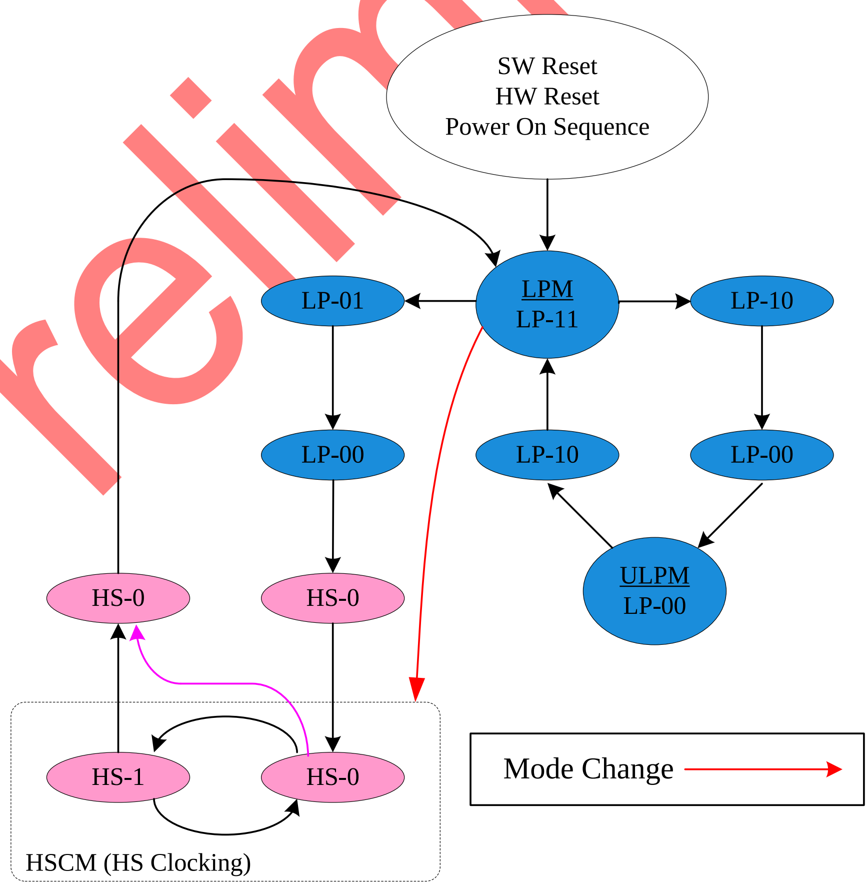


Figure 45 Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

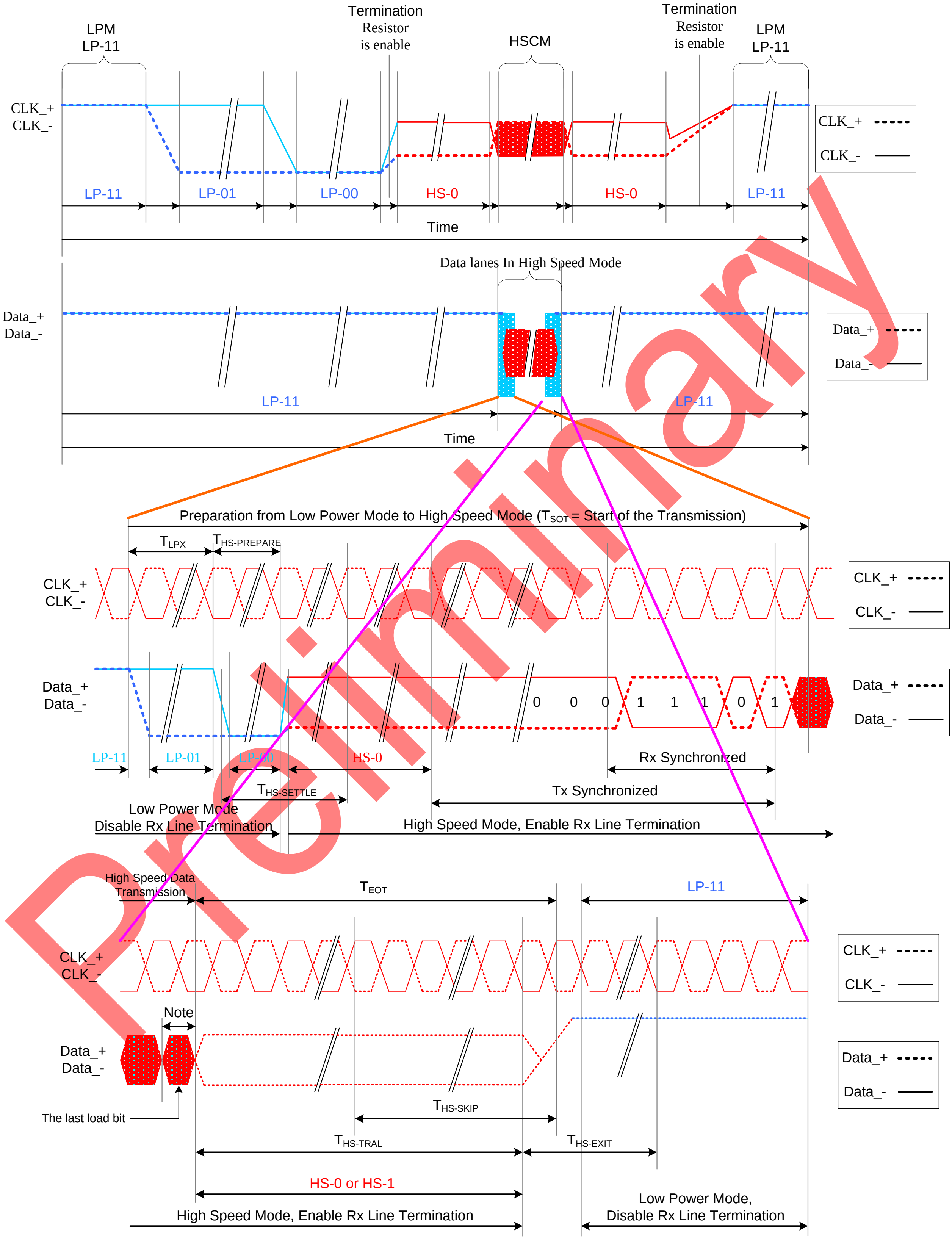


Figure 46 High Speed Clock Burst

8.10.1.2.3 DSI-DATA LANES

8.10.1.2.3.1 GENERAL

DSI-D0+/- Data Lanes can be driven in different modes which are:

• Escape Mode (Only DSI-D0+/- data lanes are used)

• High-Speed Data Transmission (DSI-D1+/- and DSI-D0+/- data lanes are used)

• Bus Turnaround Request (Only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP11(Mark1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z

Notes:

1. Only DSI-D0+/- data lanes are used.

2. DSI-D1+/- and DSI-D0+/- data lanes are used.

3. More information on section “Bus Turnaround (BTA)”

8.10.1.2.3.2 ESCAPE MODE

Data lanes (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

These Escape Modes are used to:

• Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module

• Drive data lanes to “Ultra-Low Power State” (ULPS)

• Indicate “Remote Application Reset” (RAR), which is reset the display module

• Indicate “Tearing Effect” (TEE), which is used for a TE trigger event from the display module to the MCU

• Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.

• A load if it is needed

• Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

• End: LP-11

This basic construction is illustrated below:

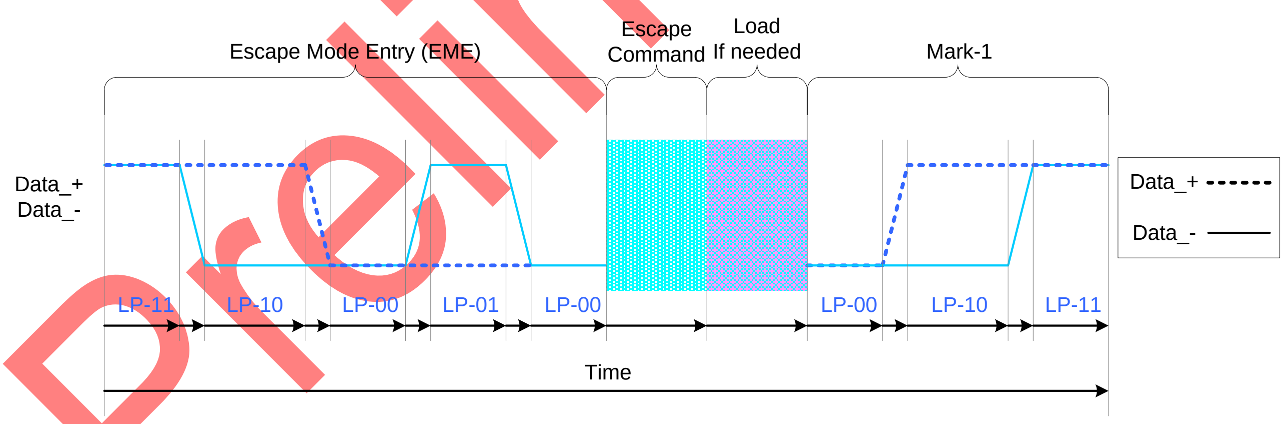


Figure 47 General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Escape commands are defined on the next table.

This basic construction is illustrated below:

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit➔Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 bin	-	○
Ultra-Low Power Mode	Mode	0001 1110 bin	○	○
Underfined-1, Note 1	Mode	1001 1111 bin	-	-
Underfined-2, Note 1	Mode	1101 1110 bin	-	-
Remote Application Reset	Trigger	0110 0010 bin	-	○
Tearing Effect	Trigger	0101 1101 bin	-	-
Acknowledge	Trigger	0010 0001 bin	-	○
Unknow-5,Note 1	Trigger	1010 0000 bin	-	-

Notes:

1. This Escape command support has not been implemented on the display module.

2. n=1.

3. "○"=Supported

4. "-"=Not Supported

5. Tearing Effect Trigger can not be used in MIPI Video mode.

Low-Power Data Transmission (LPDT)

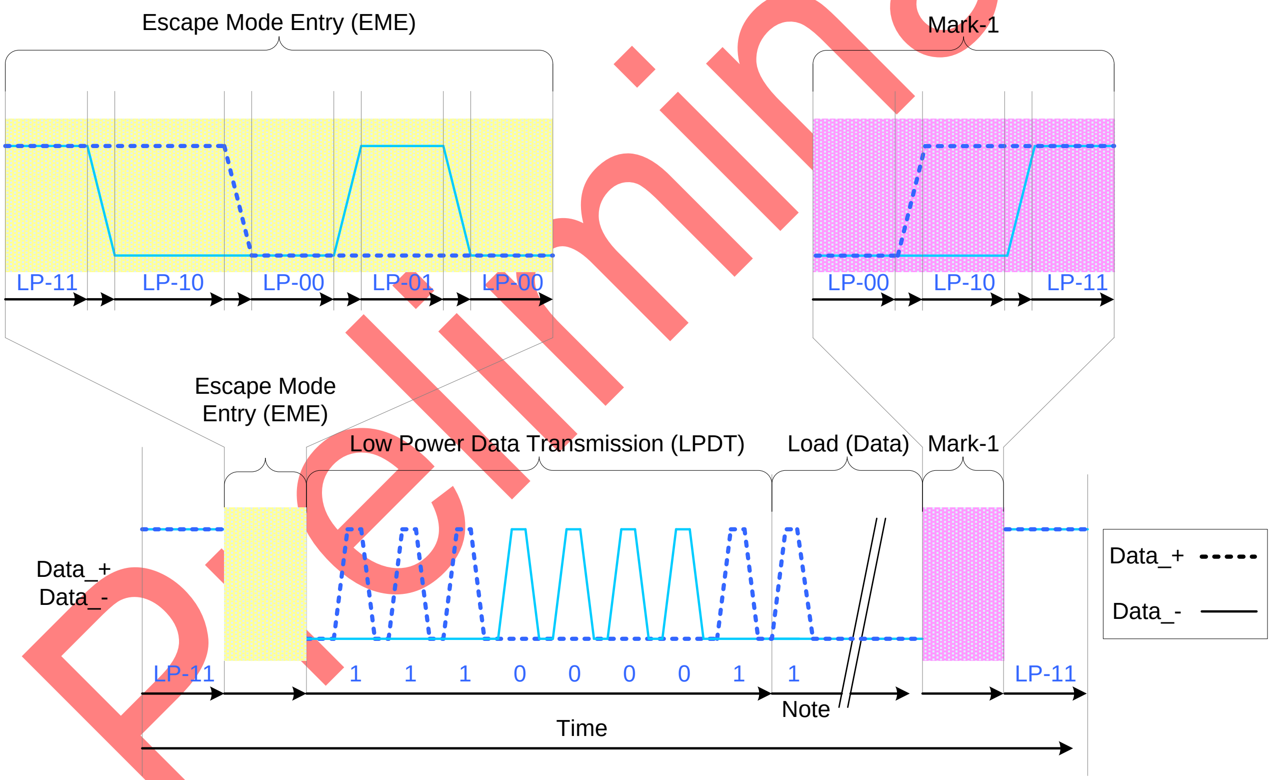
The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data): One or more bytes (8 bits)

  Data lanes are in pause mode when data lanes are stopped (Bothe lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Note : Load (Data) is presenting that the first bit is logical "1" in this Exsample

Figure 48 Low-Power Data Transmission (LPDT)

Notes:

Load (Data) is presenting that the first bit is logical '1' in this example

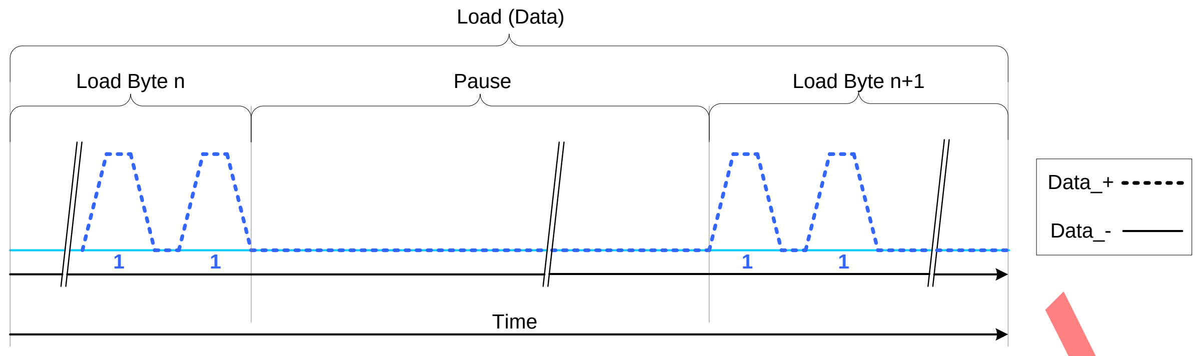


Figure 49 Pause (Example)

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)

• Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

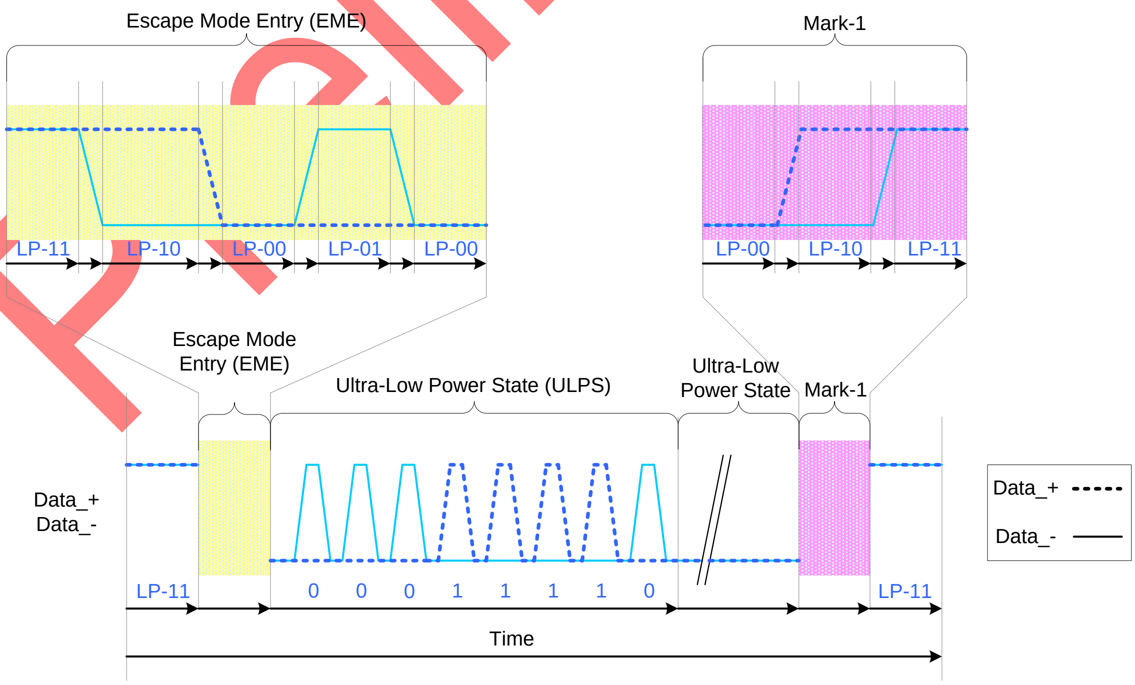


Figure 50 Ultra-Low Power State (ULPS)

Remote Application Reset (RAP)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

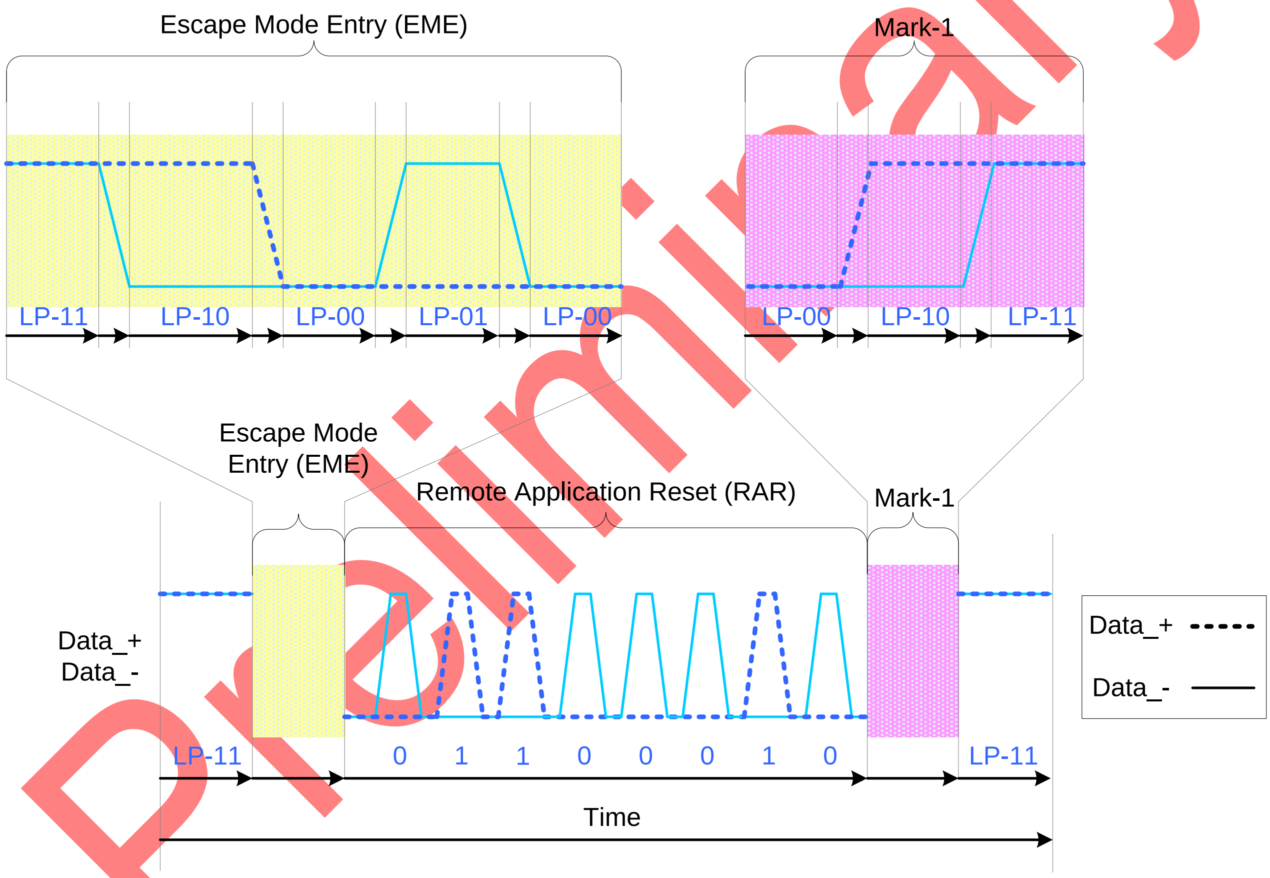


Figure 51 Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

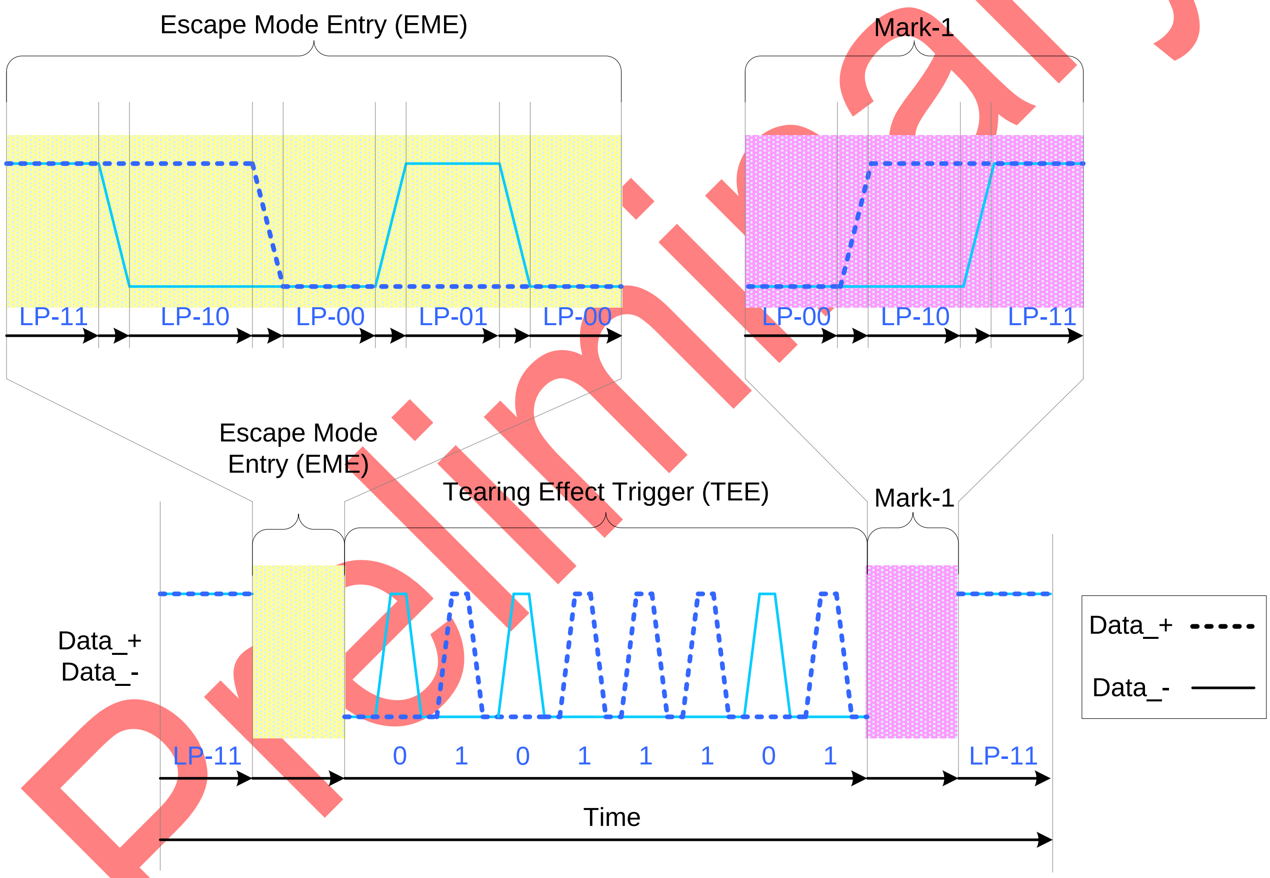


Figure 52 Tearing Effect (TEE)

Note: Tearing Effect (TEE) cannot be used in MIPI Video Mode

Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

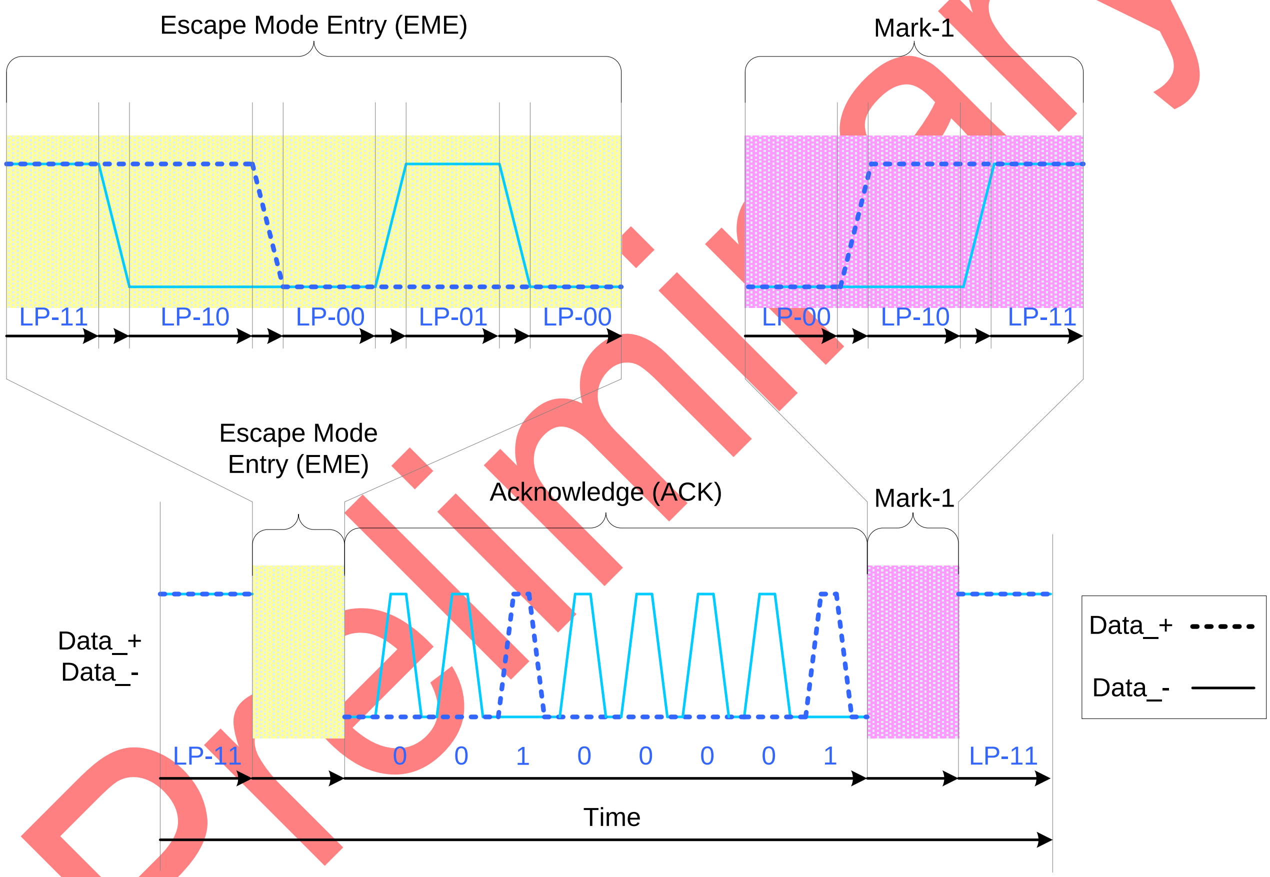


Figure 53 Acknowledge (ACK)

8.10.1.2.3.3 HIGH SPEED DATA TRANSMISSION (HSDT)

Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “8.8.2.2.2.3 High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are entering (TSOT) in the High-Speed Data Transmission (HSDT) as follows

• Start: LP-11

• HS-Request: LP-01

• HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)

• Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)

• End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below

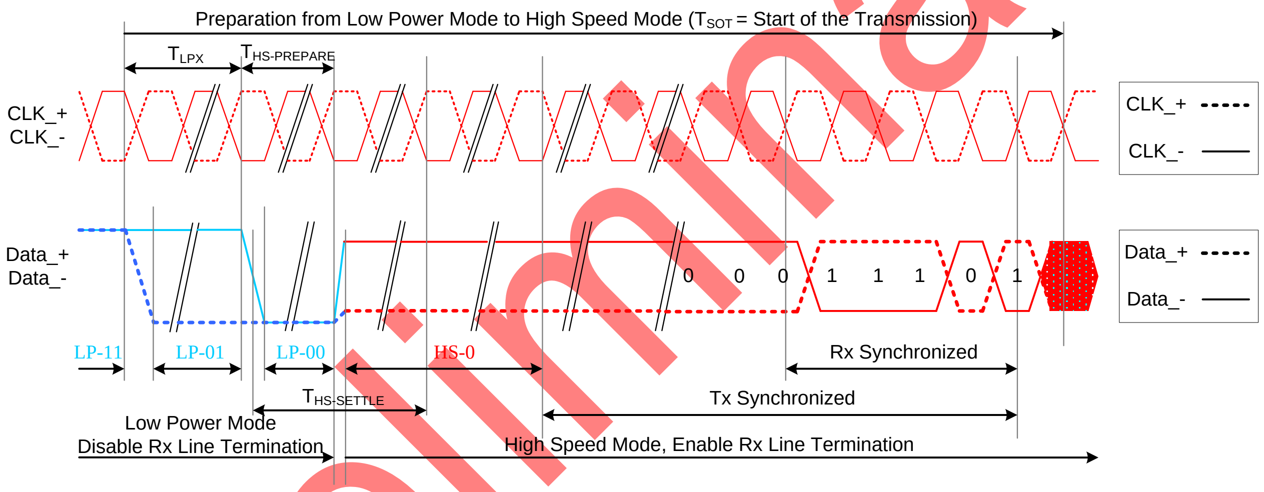


Figure 54 Entering High-Speed Data transmission (T_{SOT} of HSDT)

Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode.

See more information on chapter "5.3.2.2.2.3 High-Speed Clock Mode (HSCM)".

Data lanes of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
- MCU changes to HS-1, if the last load bit is HS-0
- MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below

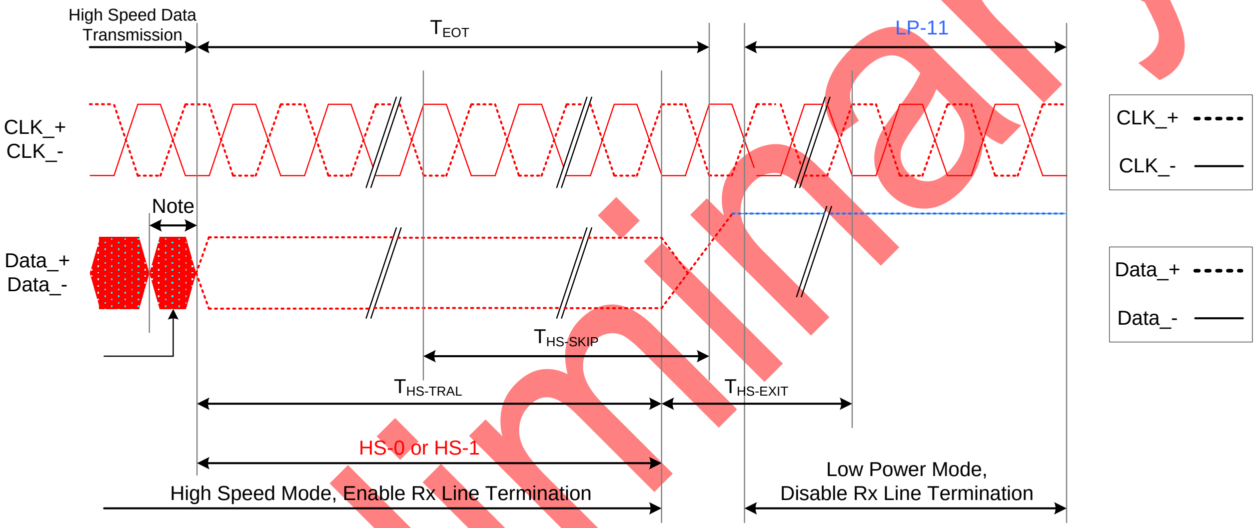


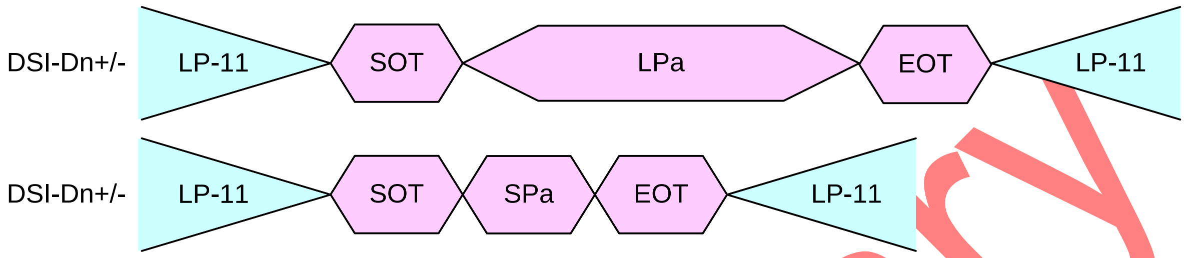
Figure 55 Leaving High-Speed data Transmission (T_{EOT} of HSDT)

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

Single Packet in High Speed Data Transmission



Multiple Packets in High Speed Data Transmission

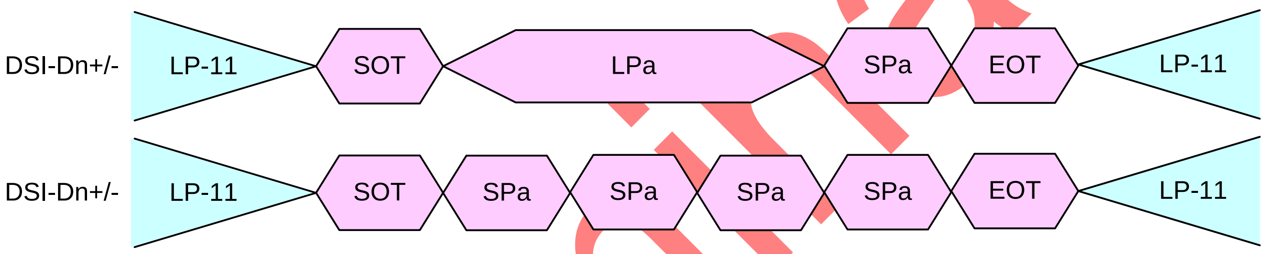
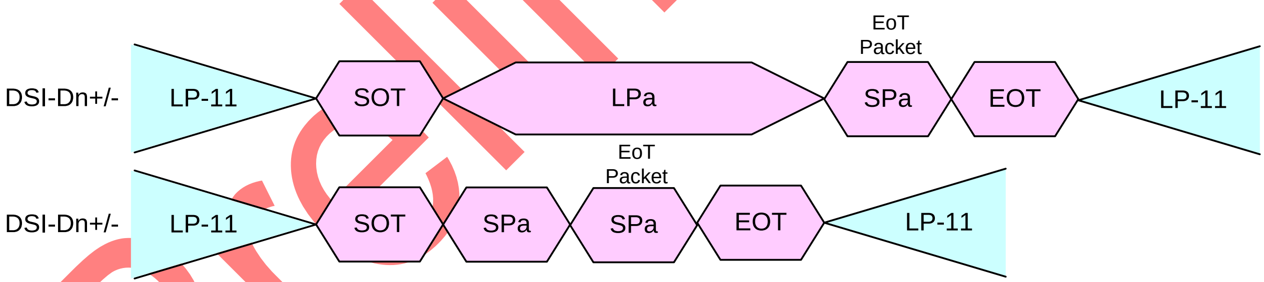


Figure 56   HS Transmission Example with EoT packet disabled

Single Packet in High Speed Data Transmission



Multiple Packets in High Speed Data Transmission

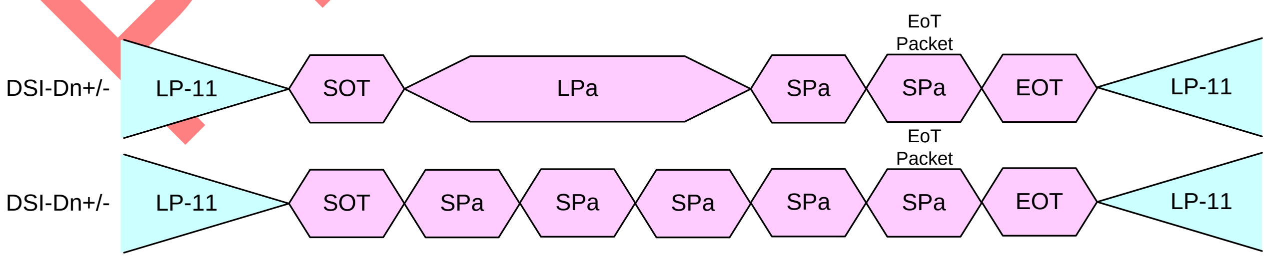


Figure 57   HS Transmission Example with EoT packet enable

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Data lanes are'1's (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

- Start (MCU):LP-11
- Turnaround Request (MCU): LP-11 _ LP-10 _ LP-00 _ LP-10 _ LP-00
- The MCU wait until the display module is starting to control DSI-D0+/- data lanes and the MCU stop to control DSI-D0+/- data lanes (=High-Z)
- The display module changes to the stop mode: LP-00 _ LP-10 _ LP-11

The same bus turnaround .procedure (From the MCU to the display module) is illustrated below.

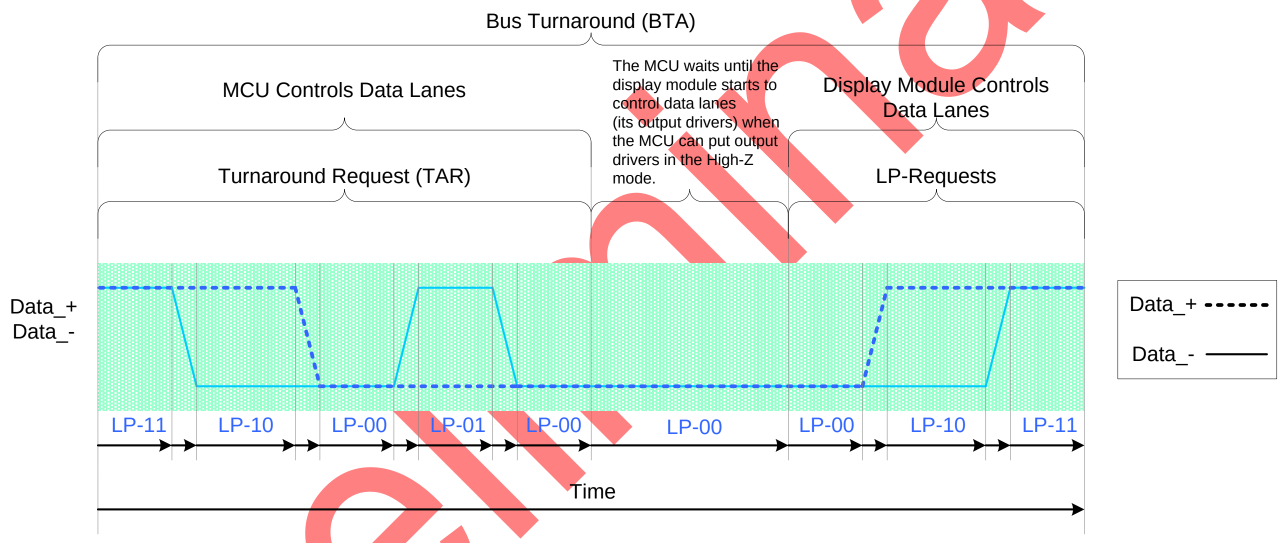


Figure 58 Bus Turnaround Procedure

MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU.

8.10.1.3 Packet Level Communication

8.10.1.3.1 Short Packet (SPA) and Long Packet (LPA) Structure

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

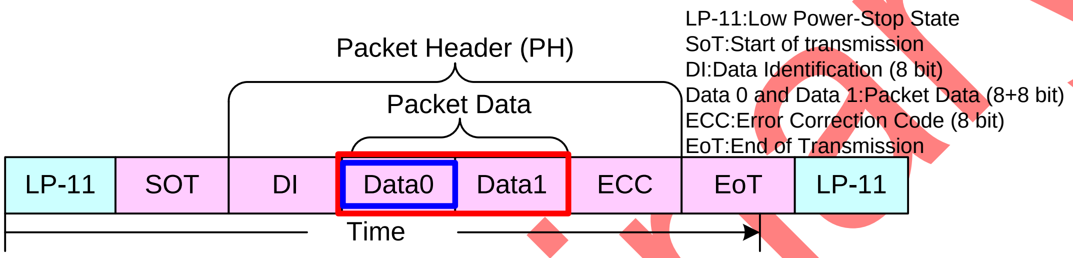
The lengths of the packets are

• Short Packet (SPa): 4 bytes

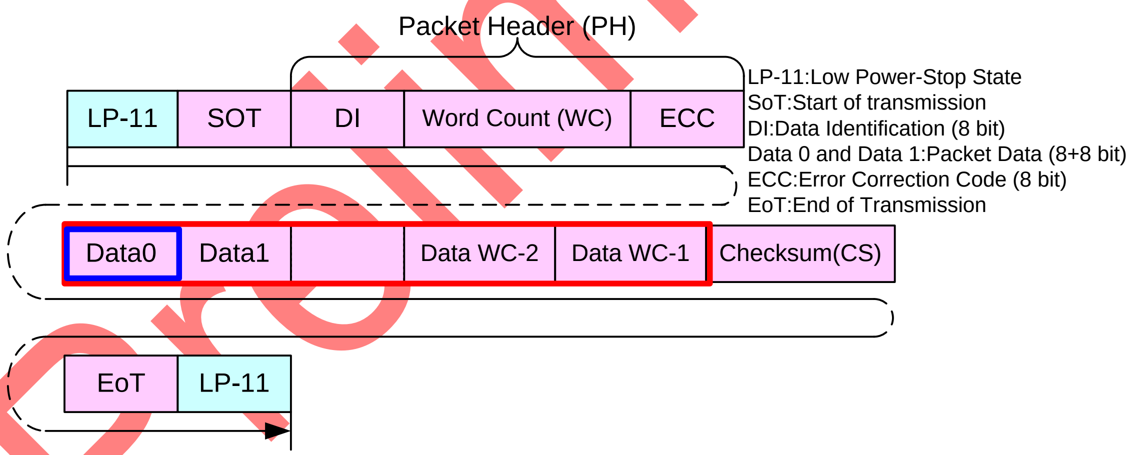
• Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

Short Packet (Spa) Structure:



Long Packet (Spa) Structure:



Note:

Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sendings).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

** LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11*

** LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11*

** LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11*

8.10.1.3.1.1 Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.

DI								WC (LSB)								WC (MSB)								ECC							
29 hex								01 hex								00 hex								06 hex							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time →

Figure 59 Bit Order of Byte on Packets

8.10.1.3.1.2 Bit Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

WC (LSB)								WC (MSB)							
01 hex								00 hex							
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB

Time →

Figure 60 Byte Order of the Multiple Byte on Packets

8.10.1.3.1.3 Pack Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

• 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)

• 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1

• 4th byte: Error Correction Code (ECC)

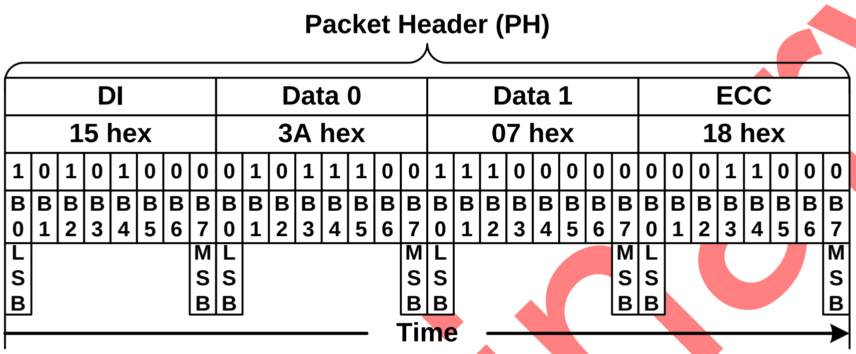


Figure 61 Packet Header (PH) on Short Packet (Spa)

Long Packet (LPa):

• 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

• 2nd and 3rd bytes: Word Count (WC)

• 4th byte: Error Correction Code (ECC)

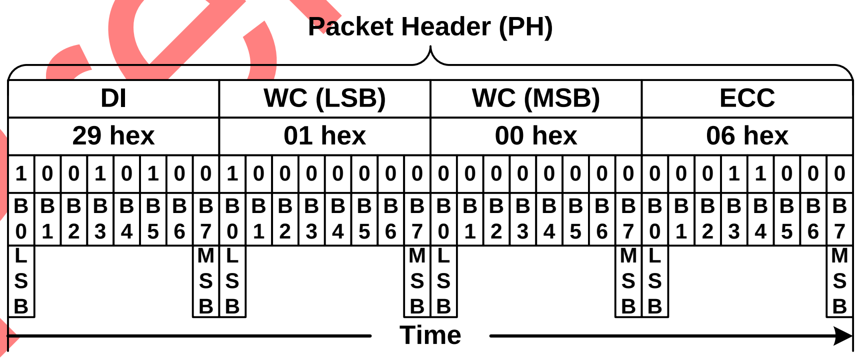


Figure 62 Packet Header (PH) on Long Packet (LPa)

Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5…0]

The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Figure 63 Data Identification (DI) Structure

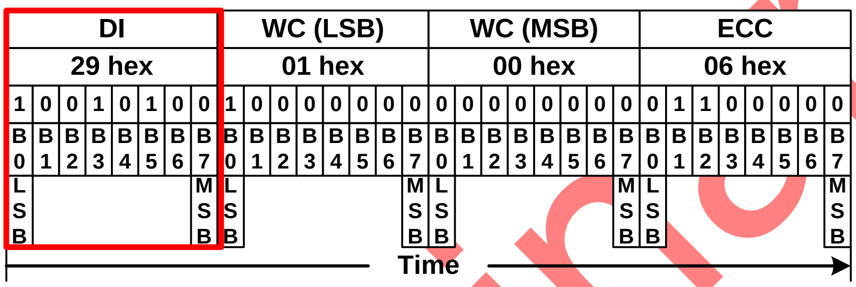


Figure 64 Data Identification (DI) on the Packet Header (PH)

Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI [7…6]) structure and it is used to address where a packet is wanted to send from the MCU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

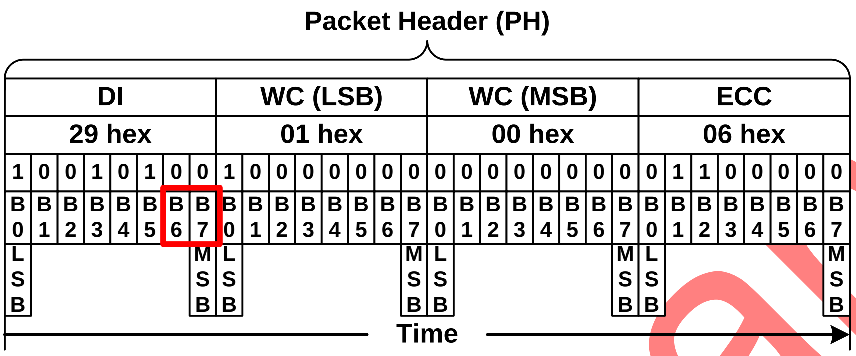
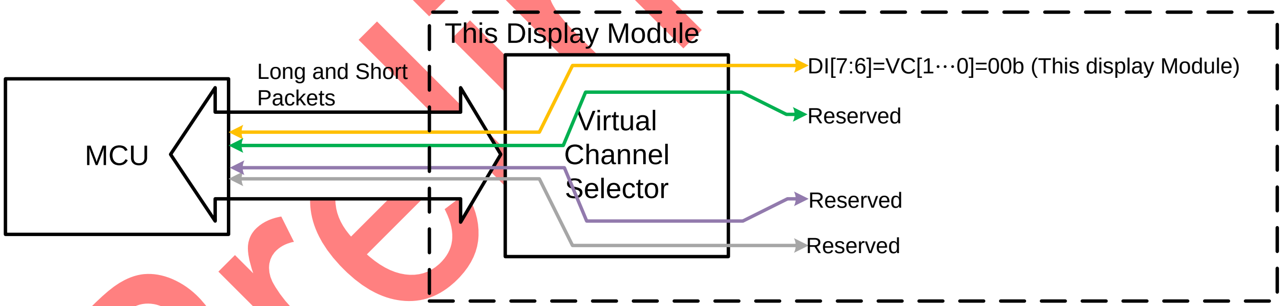


Figure 65 Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.



Virtual Channel (VC) Configuration

Virtual Channel (VC) always 0 (D[7...6]=VC[1…0]00b) when the MCU is sending "End of Transmission Packet" to the display module. See section "End of Transmission Packet (EoTP)

This display module is not supporting the virtual channel selector for other device (1 to 3) when only possible virtual channel (VC[1…0]) is 00b for this display module.

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

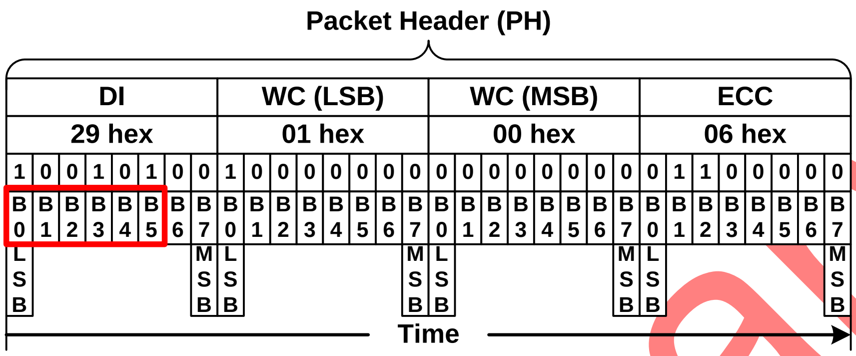


Figure 66 Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Data Type Hex	Data Type Binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start.	Short
11h	01 0001	Sync Event, V Sync End.	Short
21h	10 0001	Sync Event, H Sync Start.	Short
31h	11 0001	Sync Event, H Sync End.	Short
08h	00 1000	End of Transmission (EoT) packet.	Short
02h	00 0010	Color Mode (CM) Off Command.	Short
12h	01 0010	Color Mode (CM) On Command.	Short
22h	10 0010	Shut Down Peripheral Command.	Short
32h	11 0010	Turn On Peripheral Command.	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter.	Short
23h	10 0011	Generic Short WRITE, 2 parameters.	Short
04h	00 0100	Generic READ, no parameters.	Short
14h	01 0100	Generic READ, 1 parameter.	Short
24h	10 0100	Generic READ, 2 parameters.	Short
05h	00 0101	DCS WRITE, no parameter.	Short
15h	01 0101	DCS WRITE, 1 parameter.	Short
06h	00 0110	DCS READ, no parameter.	Short
37h	11 0111	Set Maximum Return Packet Size.	Short
09h	00 1001	Null Packet, no data.	Long
19h	01 1001	Blanking Packet, no data.	Long
29h	10 1001	Generic Long Write.	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet.	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB,5-6-5 Format.	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB,6-6-6 Format.	Long
2Eh	10 1110	Loosely Packed Pixel Stream,18-bit RGB,6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream,24-bit RGB,8-8-8 Format.	Long

Table 20 Data Type (DT) from MCU to the Display Module (or Other Devices)

From the Display Module (or Other Devices) to the MCU									
Hex	B 5	B 4	B 3	B 2	B 1	B 0	Description	Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge with Error Report	Short	AwER
1Ch	0	1	1	1	0	0	DCS Read Long Response	Short	DCSRR_L
21h	1	0	0	0	0	1	DCS Read Short Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Read Short Response, 2 byte returned	Short	DCSRR2_S
1Ah	0	1	1	0	1	0	Generic Read Long Response	Short	GENRR-L
11h	0	1	0	0	0	1	Generic Read Short Response,1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Read Short Response,2 byte returned	Short	GENRR2-S

Table 21 Data Type (DT) from the Display Module (or Other Devices) to the MCU

The receiver will ignore other Data Type (DT) if they are not defined on tables: "Data Type (DT) from the MCU to the Display Module (or Other Devices)" or "Data Type (DT) from the Display Module (or Other Devices) to the MCU".

Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet of Packet Data (PD) send after the Packet Header.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

• Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS's parameter)

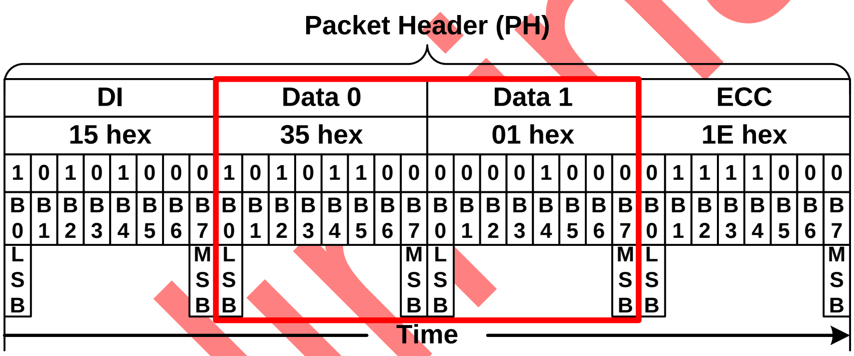


Figure 67 Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)

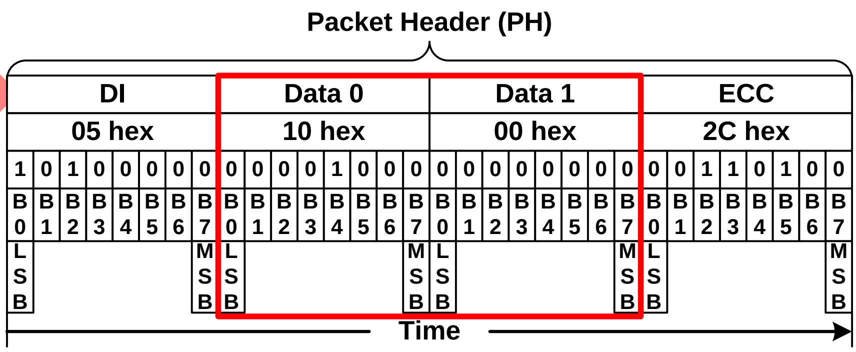


Figure 68 Packet Data(PD) for Short Packet (Spa), 1 Bytes Information

Word Count (WC) on the Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

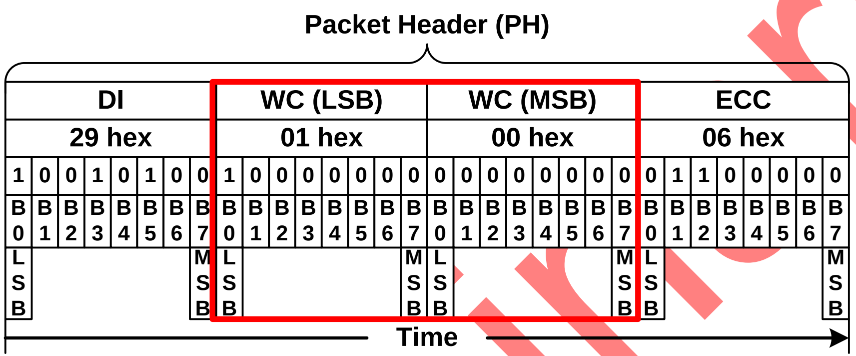
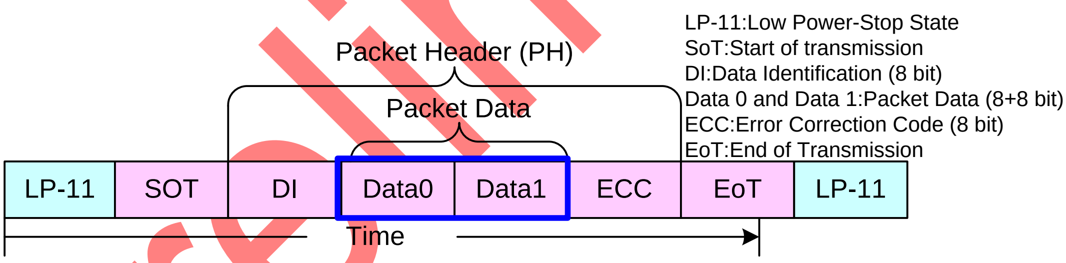
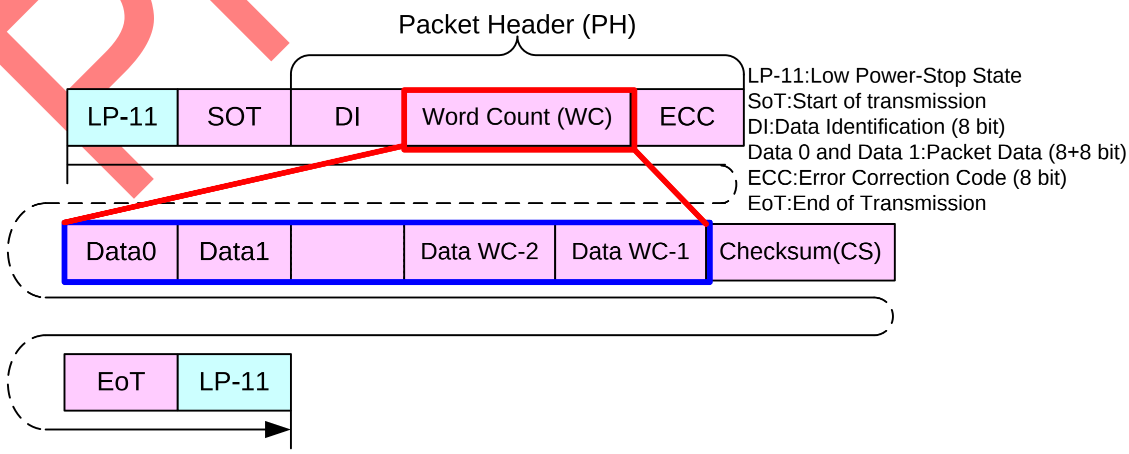


Figure 69 Word Count (WC) on the Long Packet (LPa)

Short Packet:



Long Packet:



Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH):

The ECC protects the following field”

• Short Packet (SPa): Data Identification (DI) byte (8 bits, D[0...7]), Packet Data (PD) bytes (16 bits, D[8...23]) and ECC(8 bits: P[0…7])

• Long Packet (LPa): Data Identification (DI) byte (8 bits, D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits, P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.

Packet Header (PH)

DI	Data 0	Data 1	ECC
05 hex	10 hex	00 hex	2C hex
1 0 1 0 0 0 0 0	0 0 0 0 1 0 0 0	0 0 0 0 0 0 0 0	0 0 1 1 0 1 0 0
D0 D1 D2 D3 D4 D5 D6 D7	D8 D9 D10 D11 D12 D13 D14 D15	D16 D17 D18 D19 D20 D21 D22 D23	P0 P1 P2 P3 P4 P5 P6 P7
B0 B1 B2 B3 B4 B5 B6 B7	B0 B1 B2 B3 B4 B5 B6 B7	B0 B1 B2 B3 B4 B5 B6 B7	B0 B1 B2 B3 B4 B5 B6 B7
LSB … MSB	LSB … MSB	LSB … MSB	LSB … MSB

Time →

D[23..0] and P[7⋯0] on the Short Packet (SPa)

Packet Header (PH)

DI	WC (LSB)	WC (MSB)	ECC
29 hex	01 hex	00 hex	06 hex
1 0 0 1 0 1 0 0	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0
D0 D1 D2 D3 D4 D5 D6 D7	D8 D9 D10 D11 D12 D13 D14 D15	D16 D17 D18 D19 D20 D21 D22 D23	P0 P1 P2 P3 P4 P5 P6 P7
B0 B1 B2 B3 B4 B5 B6 B7	B0 B1 B2 B3 B4 B5 B6 B7	B0 B1 B2 B3 B4 B5 B6 B7	B0 B1 B2 B3 B4 B5 B6 B7
LSB … MSB	LSB … MSB	LSB … MSB	LSB … MSB

Time →

D[23⋯0] and P[7⋯0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

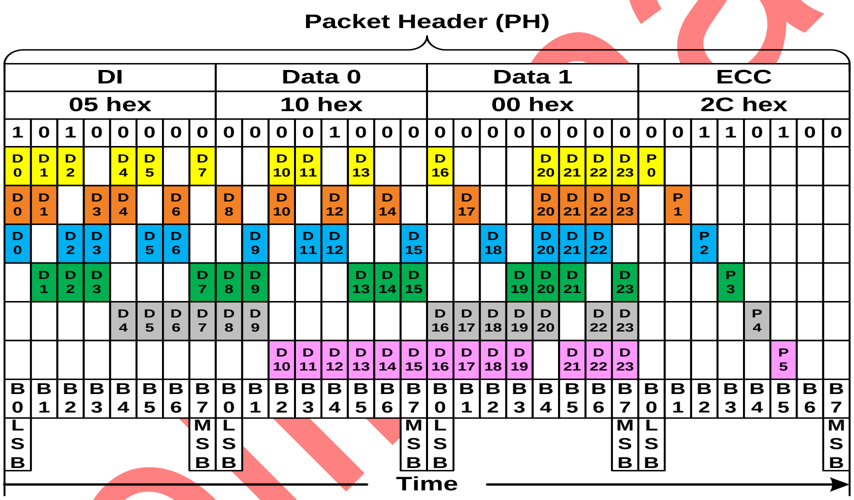
• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

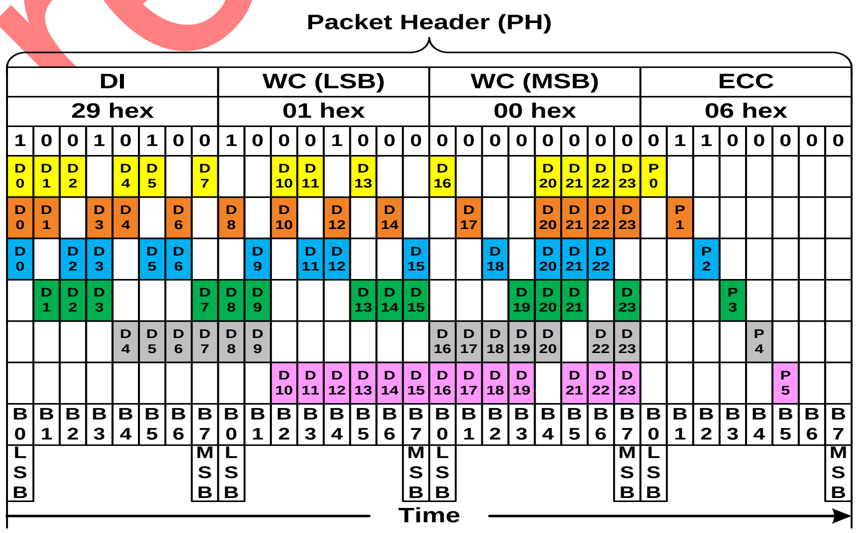
• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).



XOR Functionality on the Short Packet (SPa)



XOR Functionality on the Long Packet (LPa)

The transmitter (The MCU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

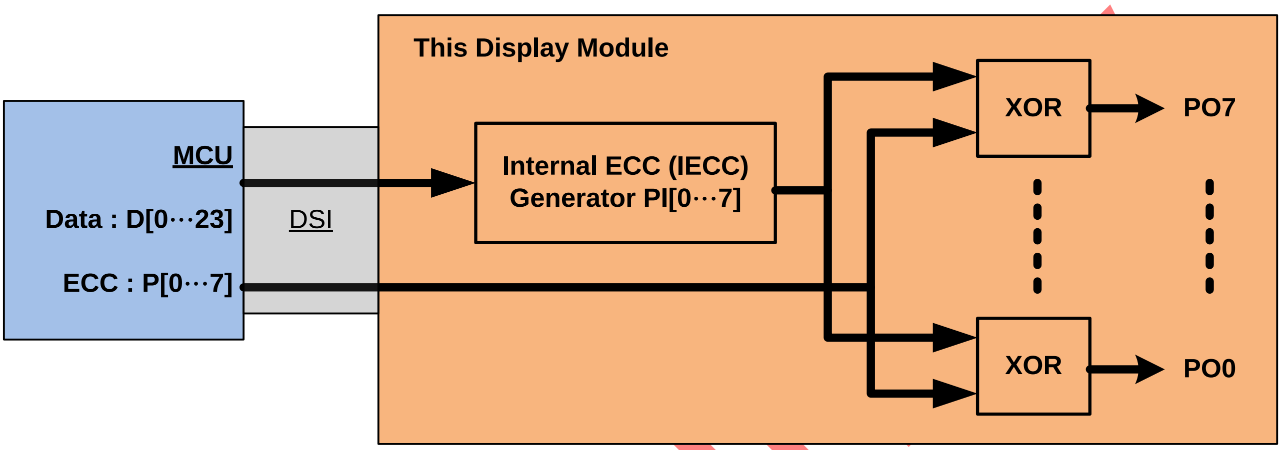


Figure 70 Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC)	0	0	0	0	0	0	0	0	=00h=>No Error
=>PO[7…0]									
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values-No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC)	0	0	1	1	0	0	0	0	=0Ch=> Error
=>PO[7…0]									
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values- Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7…0] is on : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO[7…0] = 0Eh
- The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

8.10.1.3.1.4 Packet Data (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

8.10.1.3.1.5 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

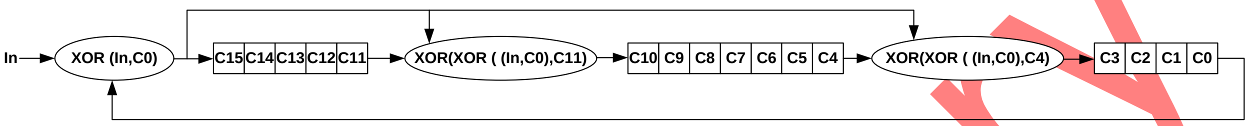
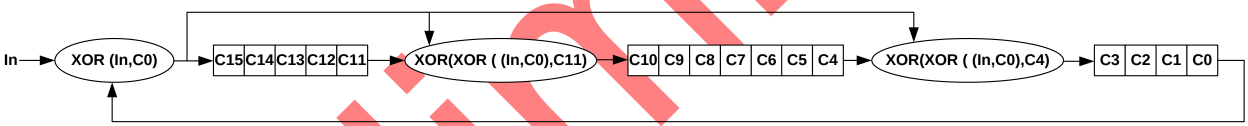


Figure 71 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Stop	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 Byte	CRC Resoult	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			LSB																	LSB	

Figure 72 CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.

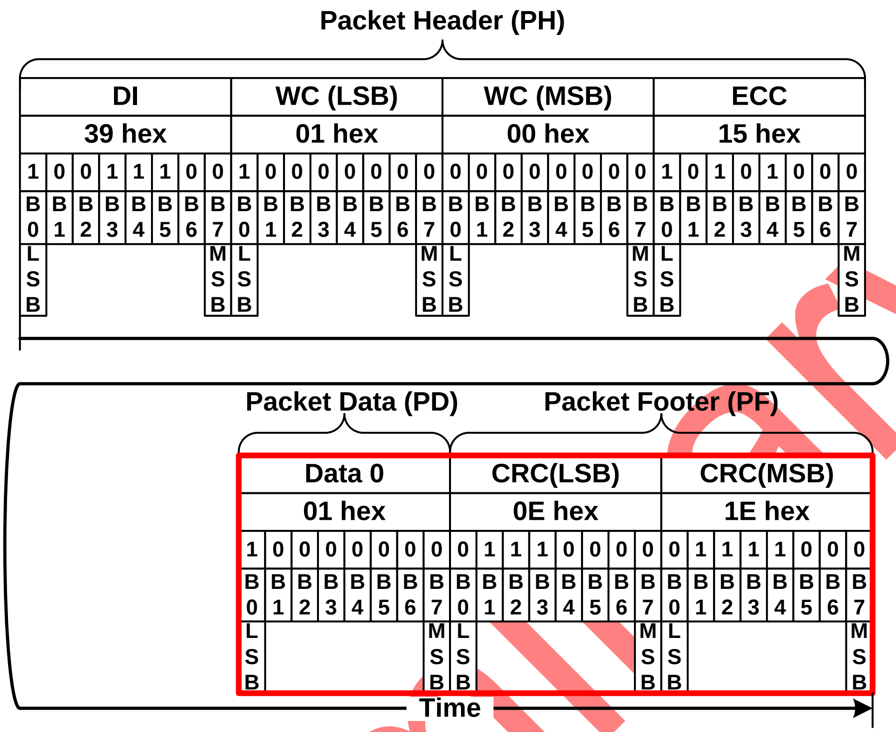


Figure 73 Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

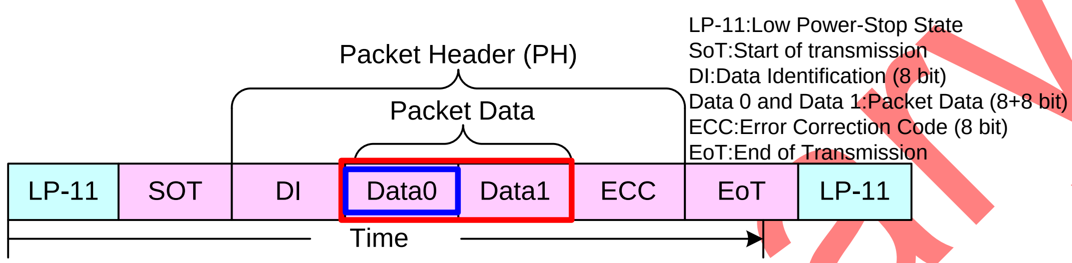
8.10.1.3.2 Packet Transmissions

8.10.1.3.2.1 Packet from the MCU to the Display Module

Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter "9 Instruction Description", is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

Short Packet



Long Packet:

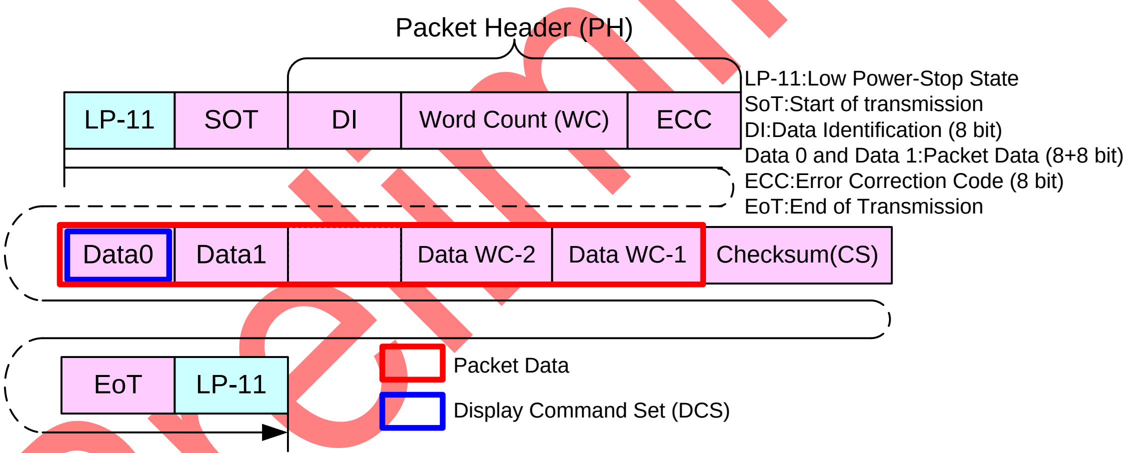


Figure 74 Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

Generic Write, 1 Parameter (GENW1-S), Data Type = 01 0011 (13h)

"Generic Write, 1 Parameter" (GENW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0011b), from the MCU to the display module. The content of 2 payload bytes is "command" and 00h.

These commands are defined on a table (See chapter "9 Instruction Description") below

Command
NOP (00h)
SWRESET (01h)
SLPIN (10H)
SLPOUT (11h)
PTLON (12h)
NORON (13h)
INVOFF (20h)
INVON (21h)
ALLPOFF (22h)
ALLPON (23h)
DISPOFF (28h)
DISPON (29h)
IDMOFF (38h)
IDMON (39h)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 01 0011b
- Packet Data (PD)
    - Data 0: "Sleep In (10h)", Display Command Set (DCS)
    - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

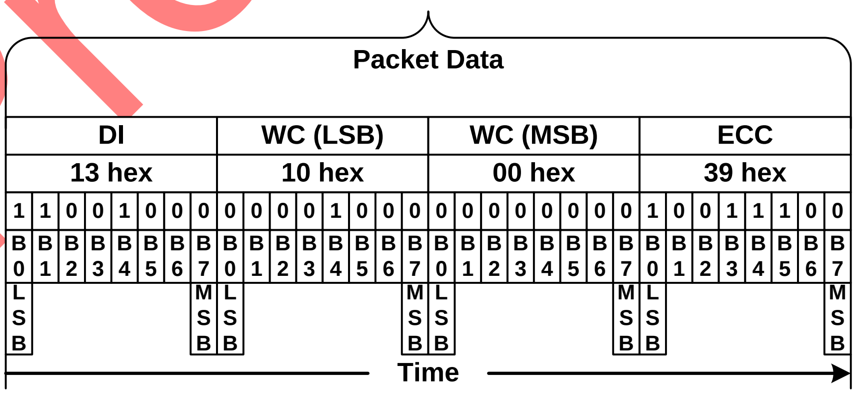


Figure 75 Generic Write, 1 Parameter (GENW1-S)-Example

Generic Write, 2 Parameter (GENW2-S), Data Type = 10 0011 (23h)

“Generic Write, 2 Parameter” (GENW2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0011b), from the MCU to the display module. The content of 2 payload bytes is “command” and “parameter”. These commands are defined on a table (See chapter “6 Instruction Description”) below.

Command
GAMSET (26h)
COLMOD (3Ah)
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 10 0011b
- Packet Data (PD)
    - Data 0: “PMCSET (3Ah)”, Display Command Set (DCS)
    - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

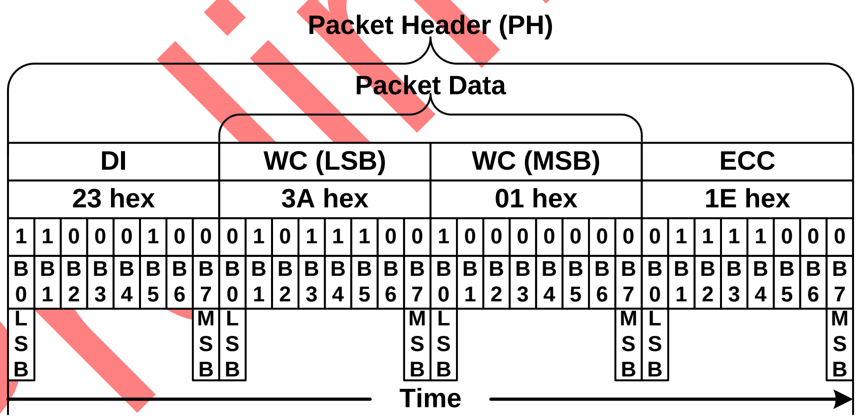


Figure 76 Generic Write, 2 Parameter (GENW2-S) – Example

Generic Write Long (GENW-L) , Data Type = 10 1001 (29h)

"Generic Write Long" (GENW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 10 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "6 Instruction Description") below.

Command		
NOP (00h) , Note1	INVON (21h) , Note1	IDMOFF (38h) , Note1
SWRESET (01h) , Note1	ALLPOFF (22h)	IDMON (39h) , Note1
SLPIN (10H) , Note1	ALLPON (23h)	COLMOD (3Ah) , Note2
SLPOUT (11h) , Note1	GAMSET (26h), , Note2	WRDISBV (51h) , Note2
PTLON (12h) , Note1	DISPOFF (28h) , Note1	WRCTRLD (53h) , Note2
NORON (13h) , Note1	DISPON (29h) , Note1	WRCABC (55h) , Note2
INVOFF (20h) , Note1	PARLINES (C5h)	WRCABCMB (5E) , Note2

Notes : 1. Also Short Packet (SPa) can be used; See Generic Write, 1 Parameter.
2. Also Short Packet (SPa) can be used; See Generic Write, 2 Parameter.c

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 10 1001b
- Word Count (WC)
    - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

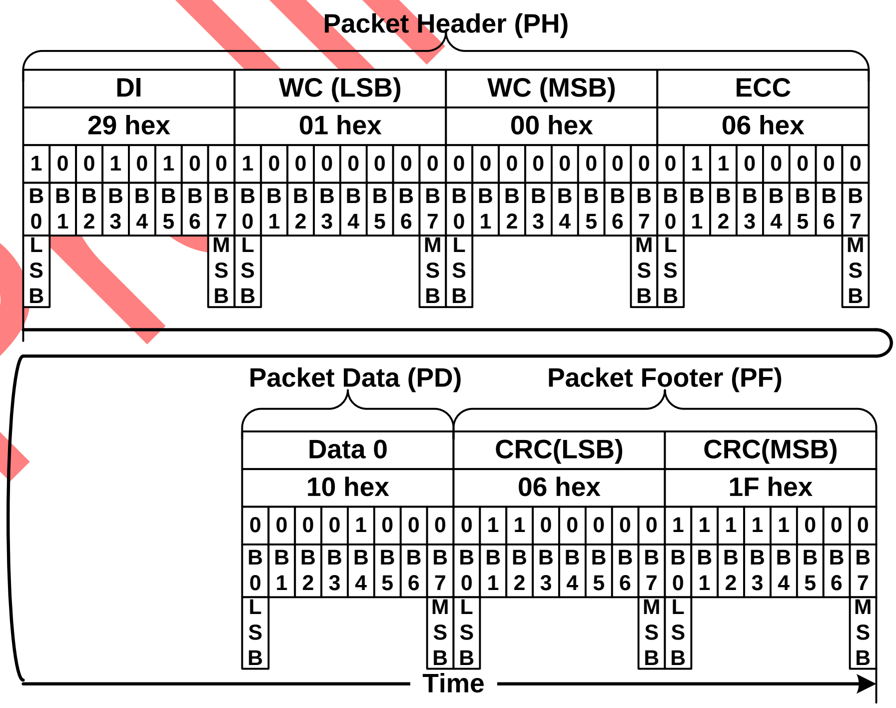


Figure 77 Generic Long Write (GENW-L) with DCS Only – Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 10 1001b
- Word Count (WC)
  - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Gamma Set (3Ah)”, Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

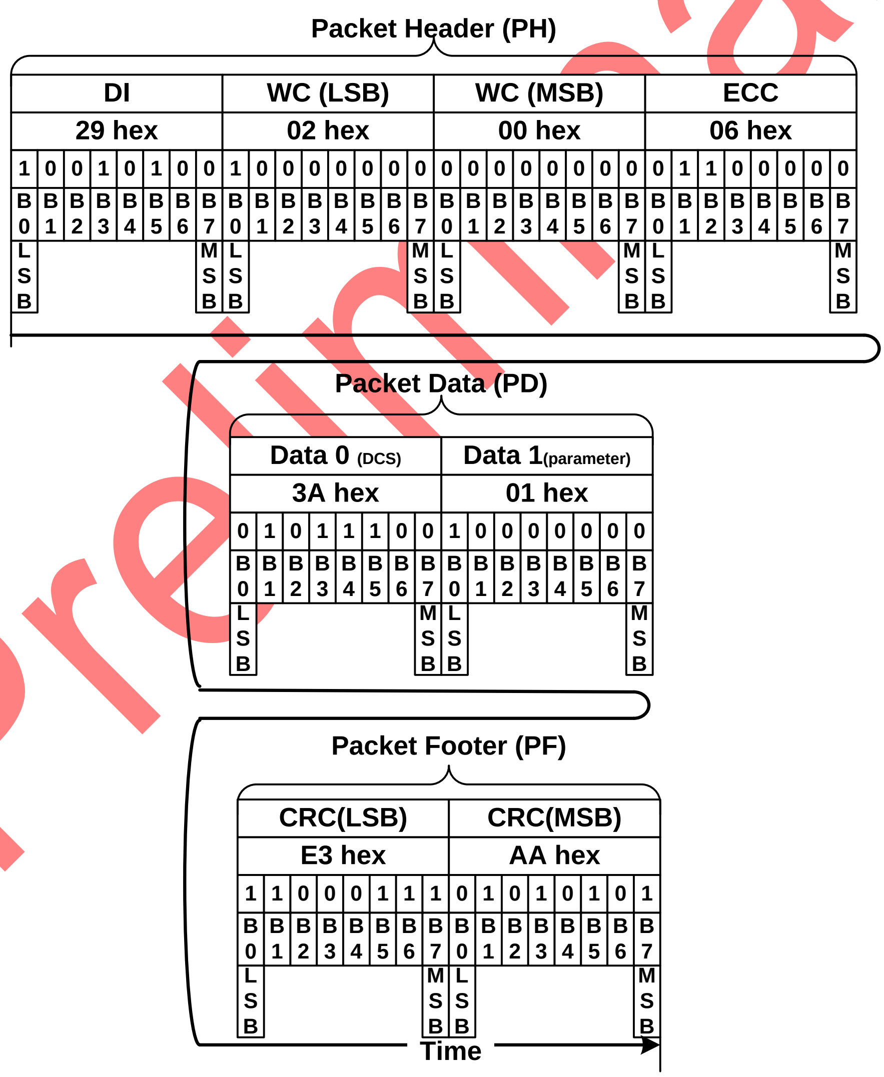


Figure 78 Generic Long Write (GENW-L) with DCS and 1 Parameter-Example

Long Packet (Lpa), when a Write (4 parameters) was sent, is defined e.g.

- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 10 1001b
- Word Count (WC)
    - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
    - Data 0: "PARLINES (30h)", Display Command Set (DCS)
    - Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15…8]
    - Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7…0]
    - Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15…8]
    - Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7…0]
- Packet Footer (PF)

This is defined on the Long Packet (Lpa) as follows.

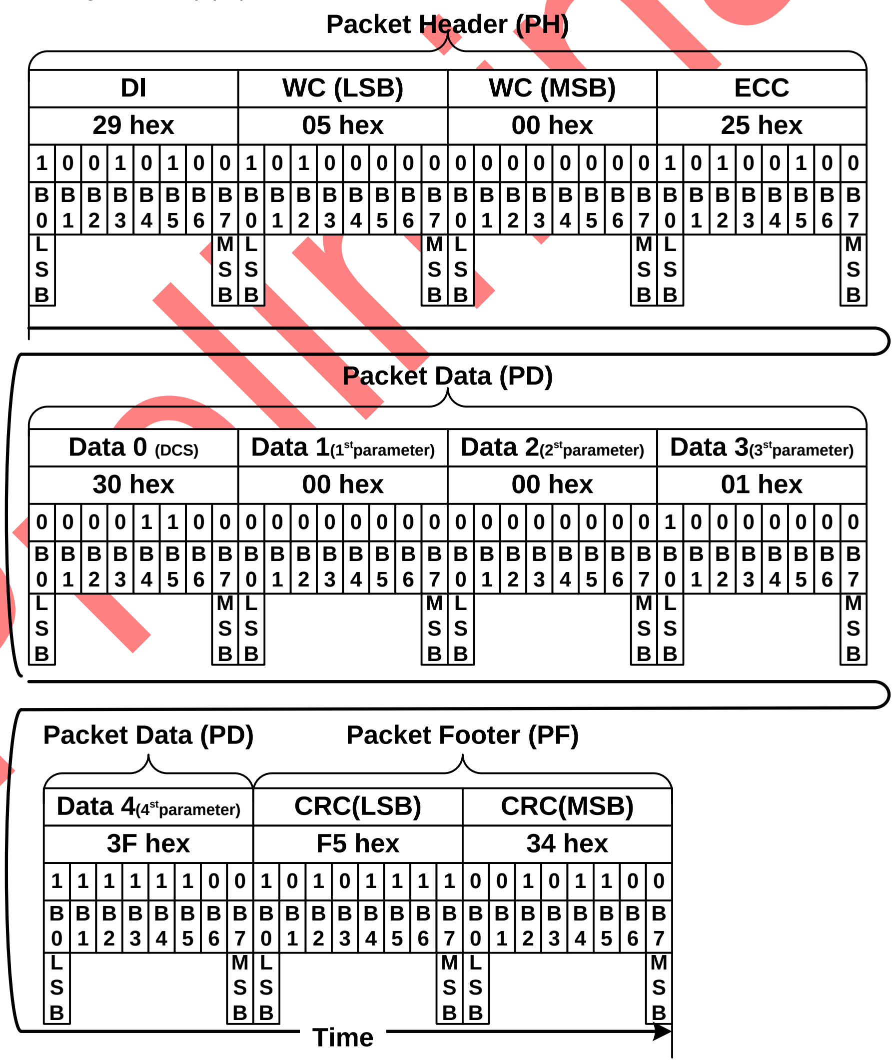


Figure 79 Generic Write Long (GENW-L) with DCS and 4 Parameters-Example

Generic Read, 1 Parameter (GENR1-S) , Data Type = 01 0100 (14h)

"Generic Read, 1 Parameter (GENR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT,01 0100b), from the MCU to the display module. This command is defined on a table (See chapter "9 Instruction Description") below.

Command	
RDDID (04h)	RDDSM (0Eh)
RDNUMED (05h)	RDDSDR (0Fh)
RDRED (06h)	RDDISBV (52h)
RDGREEN (07h)	RDCTRLD (54h)
RDBLUE (08h)	RDCABC (56h)
RDDPM (0Ah)	RDCABCMB (5Fh)
RDDMADCTR (0Bh)	RDID1 (DAh)
RDDCOLMOD (0Ch)	RDID2 (DBh)
RDDIM (0Dh)	RDID3 (DCh)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

• The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 11 0111b

• Maximum Return Packet Size (MRPS)

  • Data 0: 01hex

  • Data 1: 00hex

• Error Correction Code (ECC)

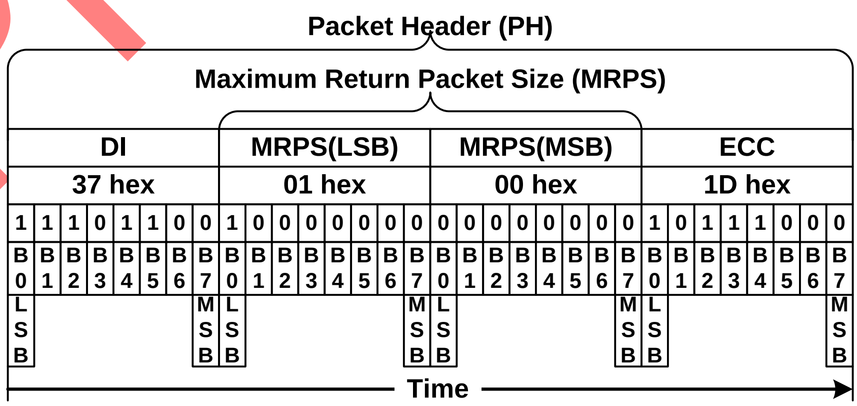


Figure 80 Set Maximum Return Packet Size (SMRPS-S)- Example

Step 2:

• The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Generic Read, 1 Parameter” to the display module

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 01 0100b

• Packet Data (PD)

  • Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)

  • Data 1: Always 00hex

• Error Correction Code (ECC)

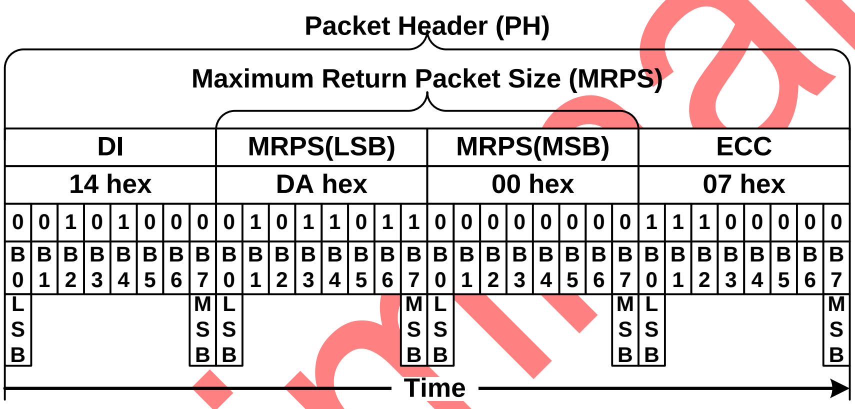


Figure 81 Generic Read, 1 Parameter (GENR1-S) – Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section “Acknowledge with Error Report (AwER)”.

2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

Display Command Set (DCS) Write, No Parameter (DCSWN-S) , Data Type = 00 0101 (05h)

"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to the display module. These commands are defined on a table (See chapter "9 Instruction Description") below.

Command	
NOP (00h)	INVON (21h)
SWRESET (01h)	ALLPOFF (22h)
SLPIN (10h)	ALLPON (23h)
SLPOUT (11h)	DISPOFF (28h)
PTLON (12h)	DISPON (29h)
NORON (13h)	IDMOFF (38h)
INVOFF (20h)	IDMON (39h)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 00 0101b
- Packet Data (PD)
    - Data 0: "Sleep In (10h)", Display Command Set (DCS)
    - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

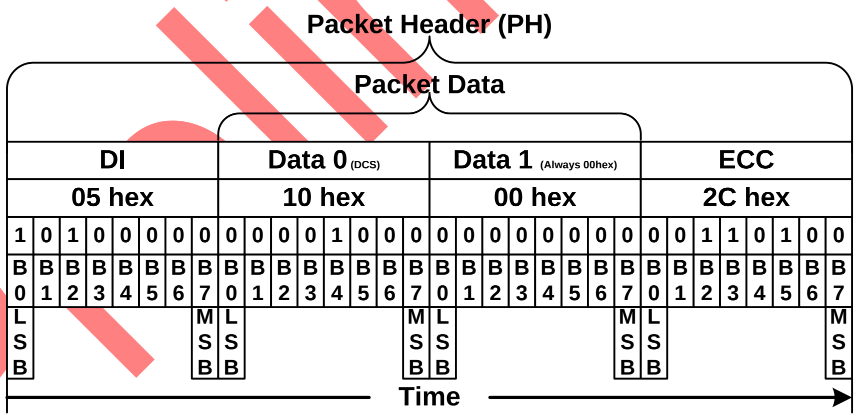


Figure 82 Display Command Set (DCS) Write,No Parameter(DCSWN-S)-Example

Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) , Data Type = 01 0101 (15h)

“Display Command Set (DCS) Write, 1 Parameter” (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to the display module. These commands are defined on a table (See chapter “9 Instruction Description”) below.

Command
GAMSET (26h)
COLMOD (3Ah)
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 0101b
- Packet Data (PD)
  - Data 0: “PMCSET (3Ah)”, Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

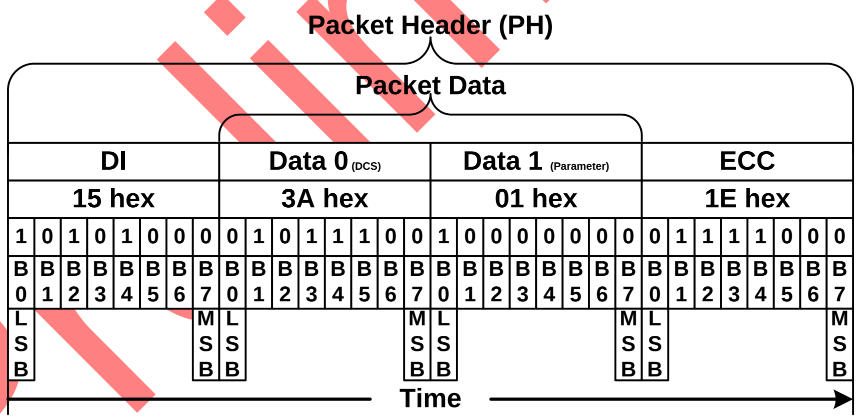


Figure 83 Display Command Set (DCS) Write,1 Parameter (DCSW1-S)-Example

Display Command Set (DCS) Write Long (DCSW-L) , Data Type = 11 1001 (39h)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "9 Instruction Description") below

Command		
NOP (00h) , Note1	INVON (21h) , Note1	COLMOD (3Ah) , Note2
SWRESET (01h) , Note1	GAMSET (26h) , Note2	WRDISBV (51h), Note2
SLPIN (10h) , Note1	DISPOFF (28h) , Note1	WRCTRLD (53h)
SLPOUT (11h) , Note1	DISPON (29h), Note1	WRCABC (55h) , Note2
PTLON (12h) , Note1	PARLINES (30h)	WRCABCMB (5Eh)
NORON (13h), Note1	IDMOFF (38h) , Note1	
INVOFF (20h), Note1	IDMON (39h) , Note1	

Notes : 1. Also Short Packet (SPa) can be used; See_Display Command Set (DCS) Write, No Parameter.

2. Also Short Packet (SPa) can be used; See Display Command Set (DCS) Write, 1 Parameter.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

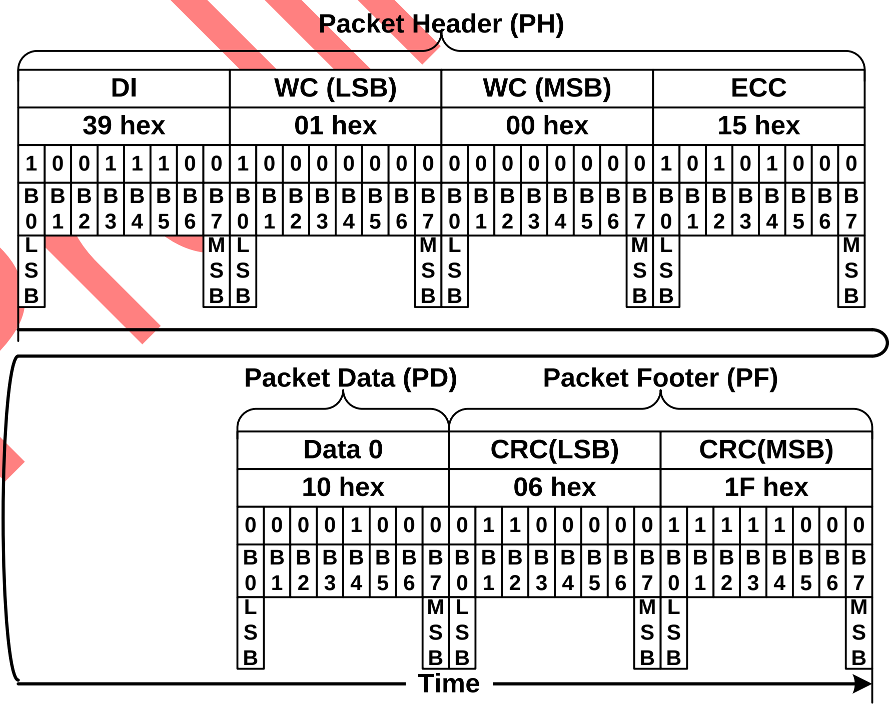


Figure 84 Display Command Set (DCS) Write Long (DCSW-L) with DCS Only-Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

  • Word Count (WC): 0002h

• Error Correction Code (ECC)

• Packet Data (PD):

  • Data 0: “Gamma Set (26h)”, Display Command Set (DCS)

  • Data 1: 01hex, Parameter of the DCS

• Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows

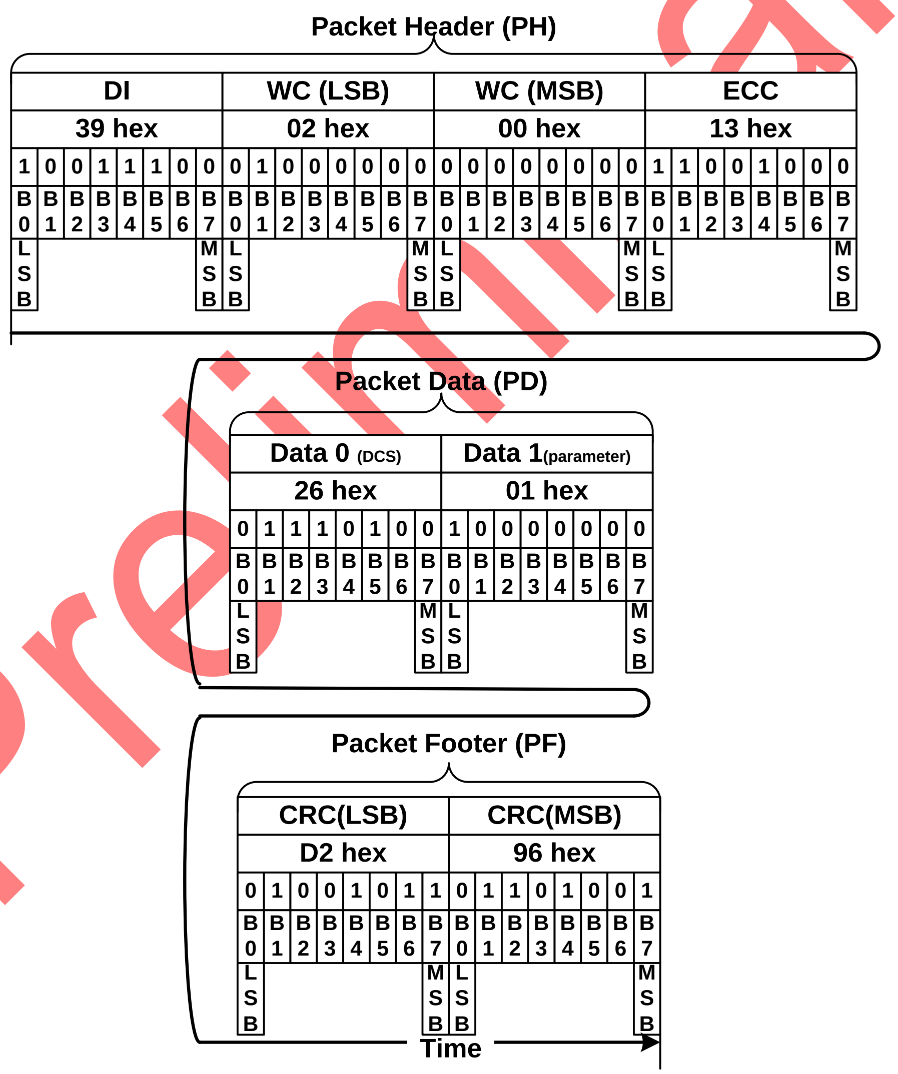


Figure 85 Display Command Set (DCS) Write Long with DCS and 1 Parameter-Example

Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
    - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
    - Data 0: “PARLINES (30h)”, Display Command Set (DCS)
    - Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15…8]
    - Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7…0]
    - Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15…8]
    - Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7…0]
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

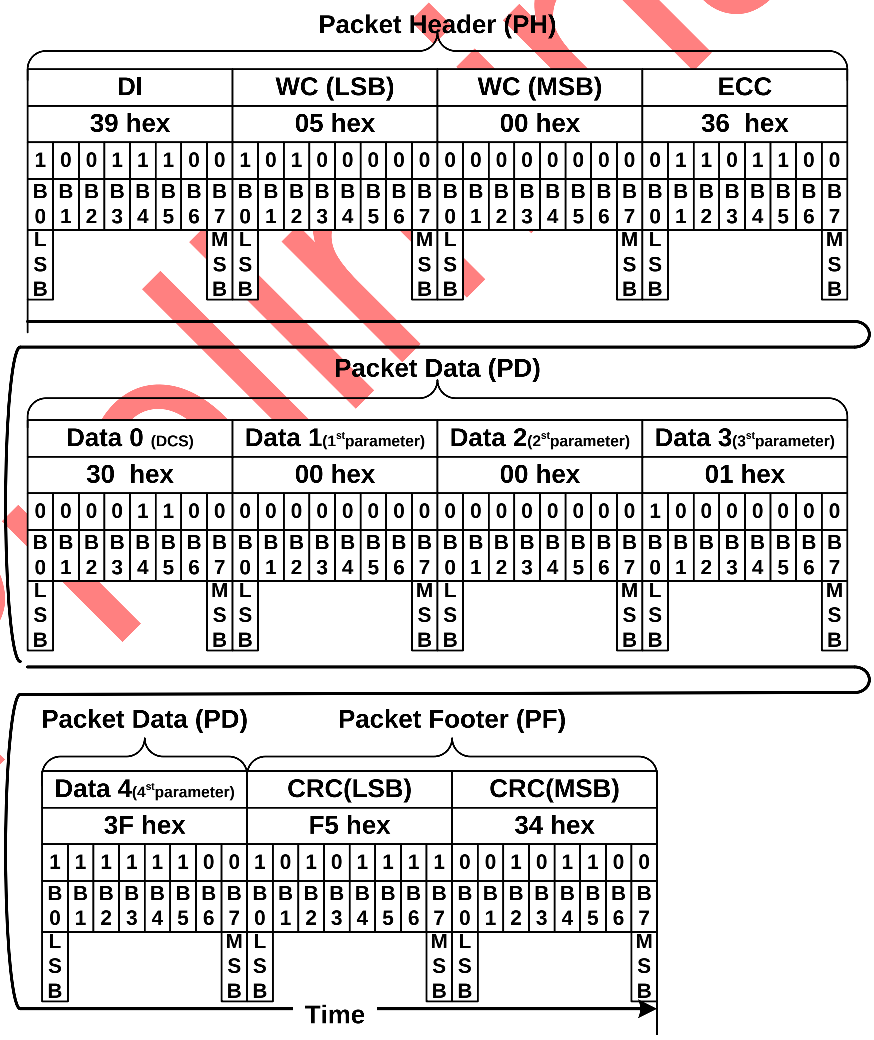


Figure 86 Display Command Set (DCS) Write Long with DCS and 4 Parameters-Example

Display Command Set (DCS) Read, No Parameter (DCSRN-S), Data Type = 00 0110 (06h)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to the display module. These commands are defined on a table (See chapter "9 Instruction Description") below.

Command	
RDDID (04h)	RDDSM (0Eh)
RDNUMED (05h)	RDDSDR (0Fh)
RDRED (06h)	RDDISBV (52h)
RDGREEN (07h)	RDCTRLD (54h)
RDBLUE (08h)	RDCABC (56h)
RDDPM (0Ah)	RDCABCMB (5Fh)
RDDMADCTR (0Bh)	RDID1 (DAh)
RDDCOLMOD (0Ch)	RDID2 (DBh)
RDDIM (0Dh)	RDID3 (DCh)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

• The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 11 0111b

• Maximum Return Packet Size (MRPS)

  • Data 0: 01hex

  • Data 1: 00hex

• Error Correction Code (ECC)

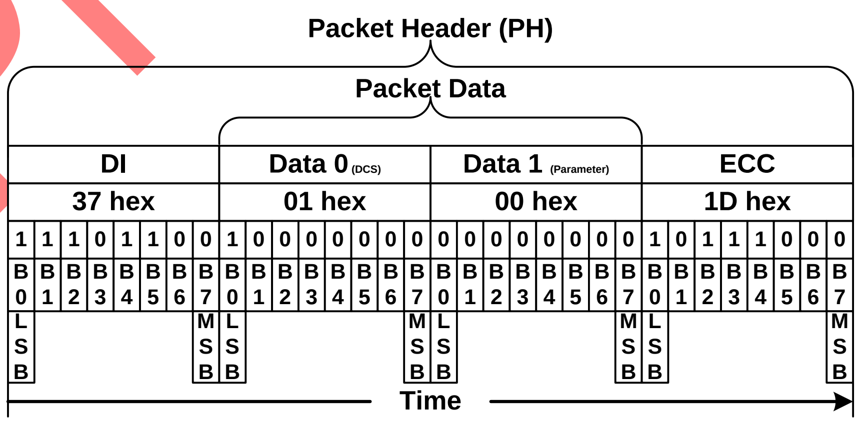


Figure 87 Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

• The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to the display module

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 00 0110b

• Packet Data (PD)

  • Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)

  • Data 1: Always 00hex

• Error Correction Code (ECC)

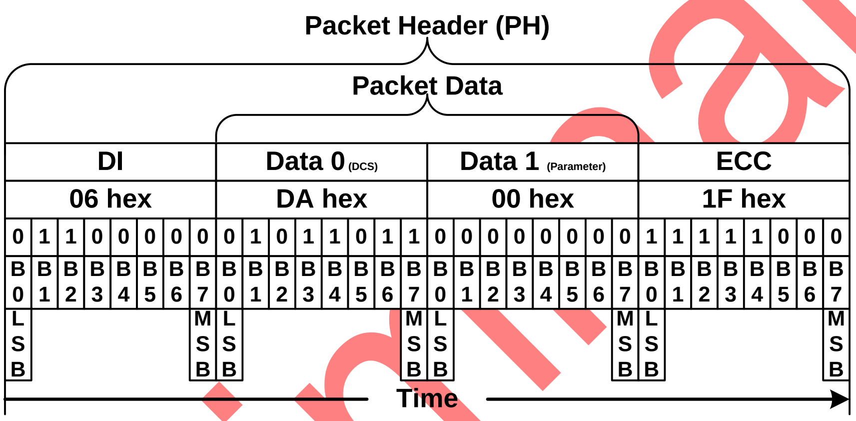


Figure 88 Display Command Set (DCS) Read, No Parameter (DCSRN-S) – Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section “Acknowledge with Error Report (AwER)”.

2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

Null Packet, No Data (NP-L) , Data Type = 00 1001 (09h)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b),from the MCU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. The display module is ignored Packet Data (PD) what the MCU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 1001b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89h (Random data)
  - Data 1: 23h (Random data)
  - Data 2: 12h (Random data)
  - Data 3: A2h (Random data)
  - Data 4: E2h (Random data)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

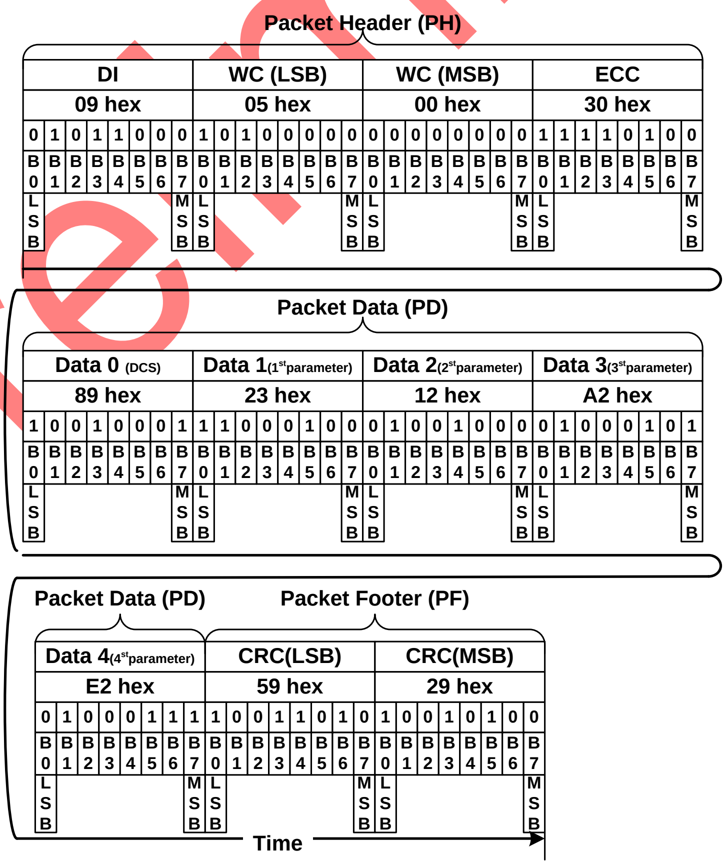


Figure 89 Null Packet, No Data (NP-L)-Example

End of Transmission Packet (EoTP), Data Type = 00 1000 (08h)

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 001000b), from the MCU to the display module. The purpose of this command is terminated the high speed mode (HPDT) properly when there is added this extra packet after the last payload packet before "End of Transmission" (EoT), which is an interface level functionality.

The MCU can decide if it want to use the "End of Transmission Packet" (EoTP) or not. The ST7701S has the capability to support both: i.e. If MCU applies the EoTP, it shall report the "DSI Protocol Violation" error when the EoTP is not detected in the high speed (HS). This error reporting can be enable/disable by bit DIS_EoTP_HS of command B100h (page 0).

The display module is or isn't receiving "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Marked-1" (=leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send "End of Transmission Packet" (EoTP) to MCU during the Low Power Data Transmission (LPDT) mode.

The summary of the receiving and transmitting EoTP is listed below.

Direction	Display Module (DM) in High Speed Data Transmission (HPDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU=>Display Driver	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Driver=>MCU	HS Mode is not available (EoTP is not available)	EoTP can not be sent by the Display Driver

Table 22 Receiving and Transmitting EoTP during LPDT

Short Packet (SPa) is using a fixed format as follow

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 00 1000b

• Packet Data (PD):

  • Data 0: 0Fh

  • Data 1: 0Fh

• Error Correction Code (ECC)

• ECC: 01h

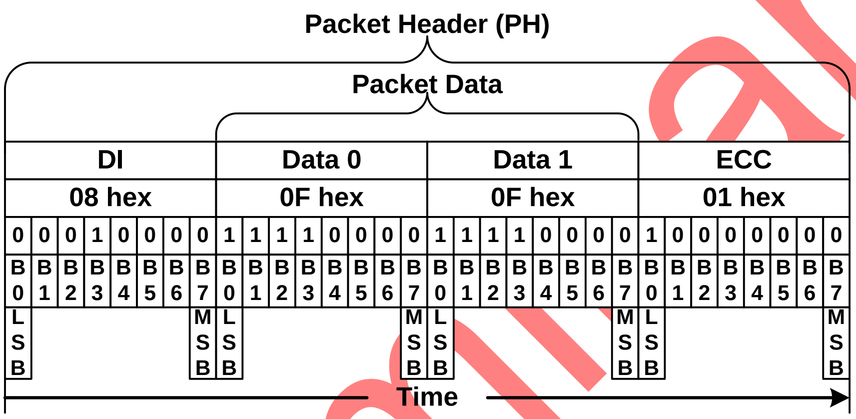


Figure 90 End of Transmission Packet (EoTP)

Some use case of the “End of Transmission Packet” (EoTP) are illustrated only for reference purpose below.

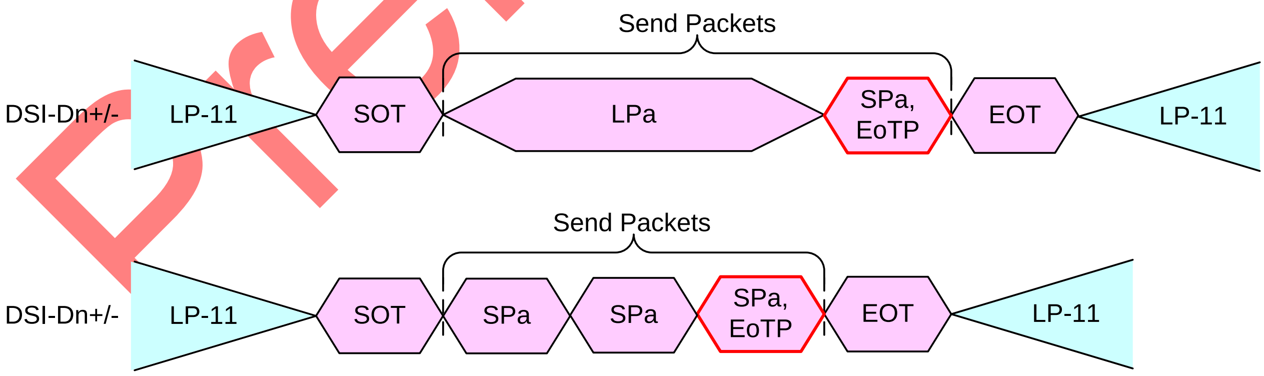


Figure 91 End of Transmission Packet (EoTP)-Example

Sync Event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the peripheral. The Sync Events are defined as follows:

- Data Type = 00 0001 (01h) V Sync Start
- Data Type = 01 0001 (11h) V Sync End
- Data Type = 10 0001 (21h) H Sync Start
- Data Type = 11 0001 (31h) H Sync End

In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA.

Sync events should occur in pairs, Sync Start and Sync End, if accurate 1054 pulse-length information needs to be conveyed. Alternatively, if only a single point (event) in time is required, a single sync event (normally, Sync Start) may be transmitted to the peripheral. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode, however. Display modules that do not need traditional sync/blanking/pixel timing should transmit pixel data in a high-speed burst then put the bus in Low Power Mode, for reduced power consumption. The recommended burst size is a scan line of pixels, which may be temporarily stored in a line buffer on the display module.

Color Mode On Command, and, Data Type = 01 0010 (12h)

Color Mode On is a Short packet command that switches a Video Mode display module to 8-colors mode for power saving.

Color Mode Off Command, Data Type = 00 0010 (02h)

Color Mode Off is a Short packet command that returns a Video Mode display module from 8-colors mode to normal display operation.

Shutdown Peripheral Command, Data Type = 10 0010 (22h)

Shutdown Peripheral command is a Short packet command that turns off the display in a Video Mode display module for power saving. Note the interface shall remain powered in order to receive the turn-on, or wake-up, command.

Turn On Peripheral Command, Data Type = 11 0010 (32h)

Turn On Peripheral command is Short packet command that turns on the display in a Video Mode display module for normal display operation.

Blanking Packet (Long), Data Type = 01 1001 (19h)

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload. The Blanking packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte checksum.

Packed Pixel Stream, 16-bit Format, Long packet, Data Type = 00 1110 (0Eh)

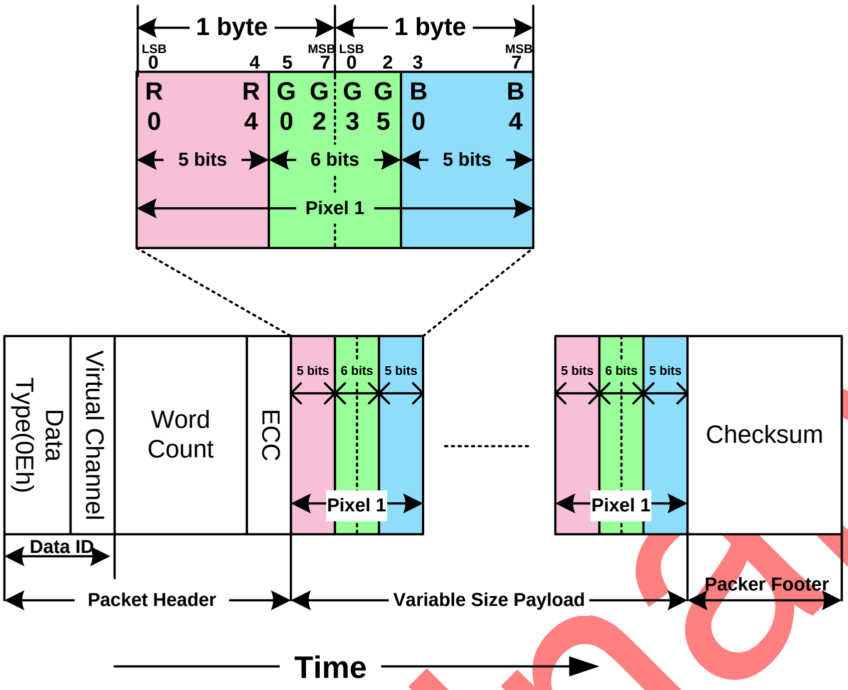


Figure 92 16-bit per Pixel-RGB Color Format, Long packet

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

Packed Pixel Stream, 18-bit Format, Long packet, Data type = 01 1110 (1Eh)

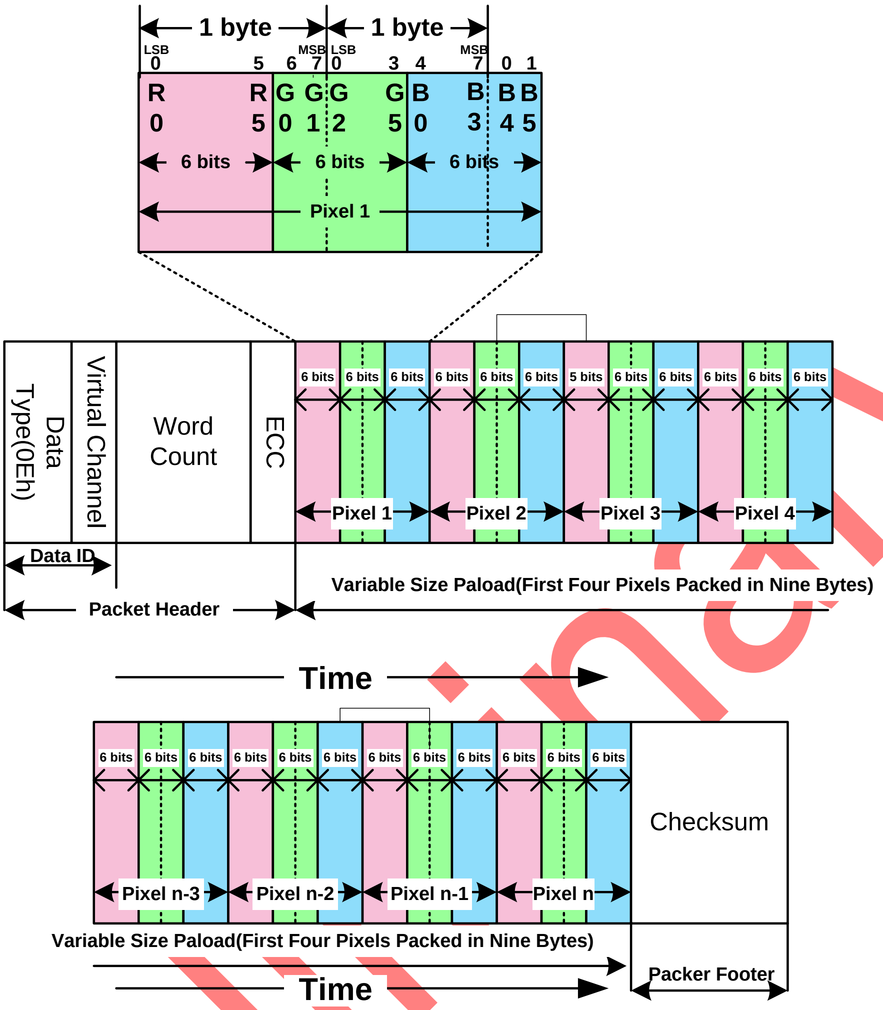


Figure 93 18-bit per Pixel-RGB Color Format, Long pack

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

Pixel Stream, 18-bit Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)

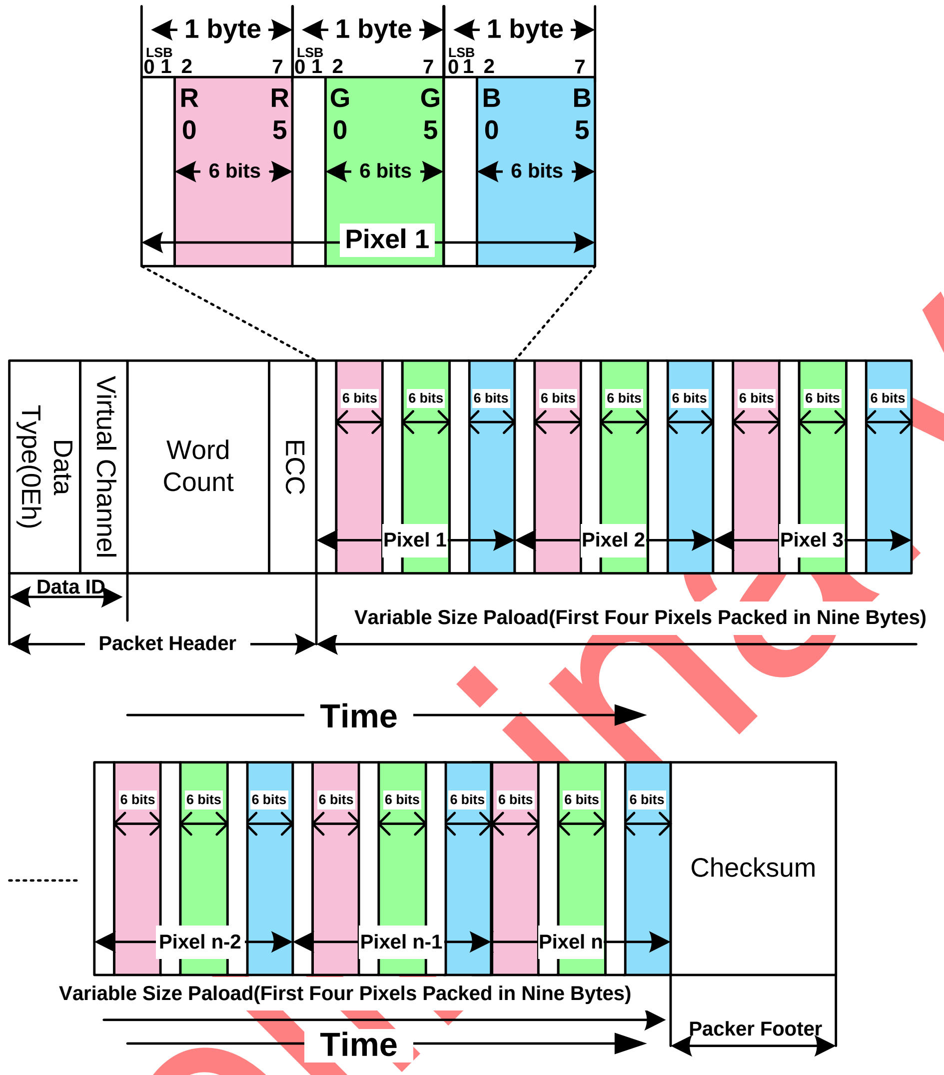


Figure 94 18-bit per Pixel (Loosely Packed)-RGB Color Format, Long pack

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the "packed" format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

Packed Pixel Stream, 24-bit Format, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

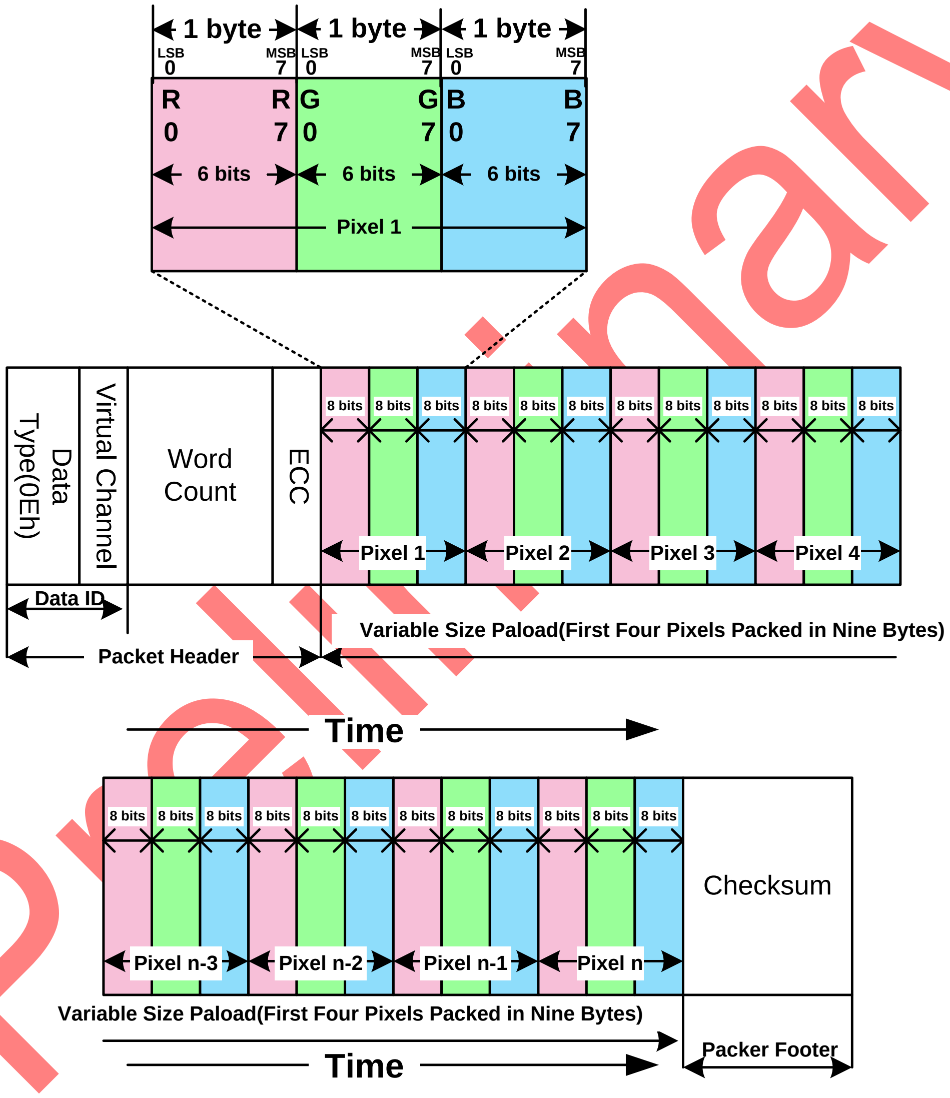


Figure 95 24-bit per Pixel -RGB Color Format, Long packet

8.10.1.3.2.2 PACKET FROM THE DISPLAY MODULE TO THE MCU

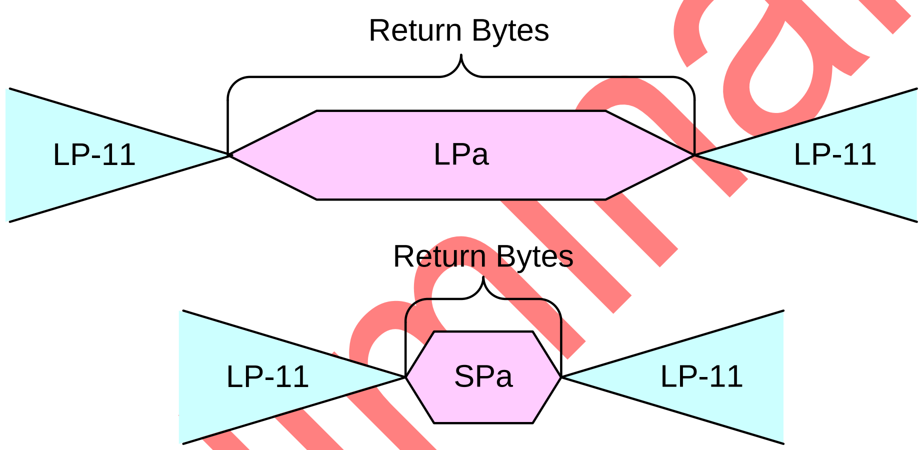
Used Packet Types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) Read, No Parameter",(DCSRN-S)) or an Acknowledge with Error Report .The used packet type is defined on Data Type (DT)..

A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

Both cases are illustrated for reference purposes below.

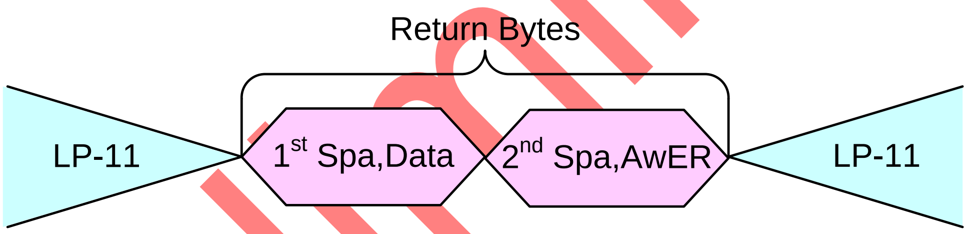


Return Bytes on Signal Packet

Data Type Hex	Data Type Binary	Symbol	Description	Packet Size
02h	00 0010	AwER	Acknowledge & Error Report	Short
1Ch	01 1100	DCSRR-L	DCS Long Read Response	Long
21h	10 0001	SCSRR1-S	DCS Short Read Response, 1 Byte returned	Short
22h	01 0010	DCSRR2-S	DCS Short Read Response, 2 Byte returned	Short
1Ah	01 1010	GENRR-L	Generic Long Read Response	Long
11h	01 0001	GENRR1-S	Generic Long Read Response, 1 Byte returned	Short
12h	01 0010	GENRR2-S	Generic Long Read Response, 2 Byte returned	Short

Table 23 Data Type for Display Module-sourced Packets

The display module is return 2 packets (1st packet: Data, 2nd packet Acknowledge with Error Report) to the MCU when the display module has received a read command. See section "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" where has been detected and corrected a single bit error by the EEC (See bit 8 on Table" Acknowledge with Error Report (AwER) for Short Packet (SPa) Response"). This return packets are illustrated for reference purpose below.



Exception When Return Bytes on Several Packet

AwER=Acknowledge with Error Report

Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT,00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1',as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Table 24 Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Set to "0" internally (Only for Long Packet (LP))
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Table 25 Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

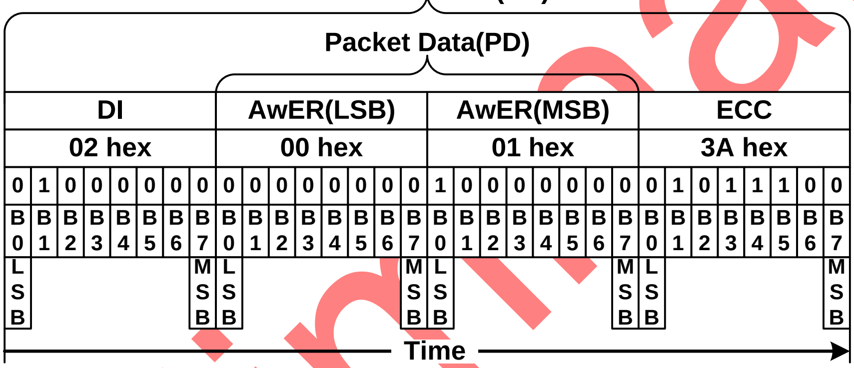
These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

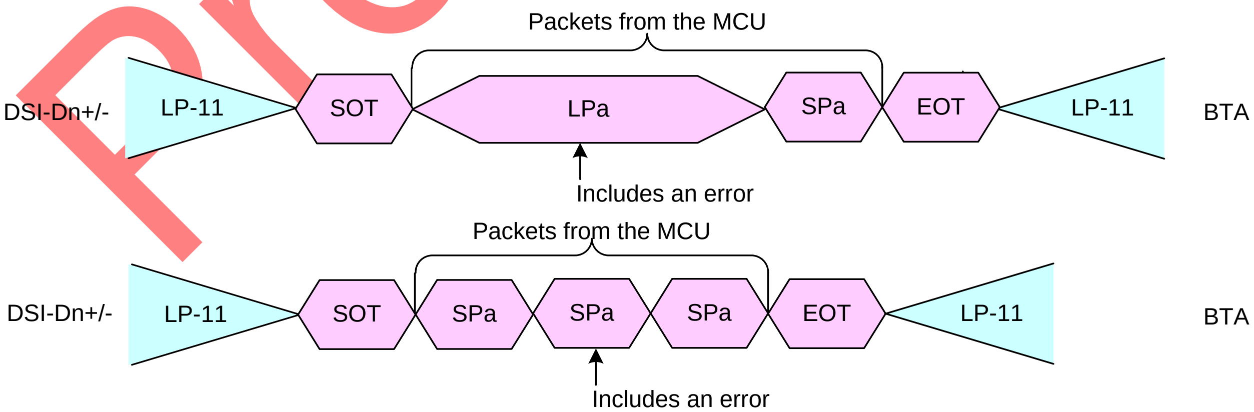
- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 00 0010b
- Packet Data (PD):
    - Bit 8: ECC Error, single-bit (detected and corrected)
    - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Acknowledge with Error Report (AwER)-Example

It is possible that the display module receivers several packets, which include error, from the MPU before the MPU performs the Bus Turnaround (BTA).Some examples are illustrated below for reference purpose.



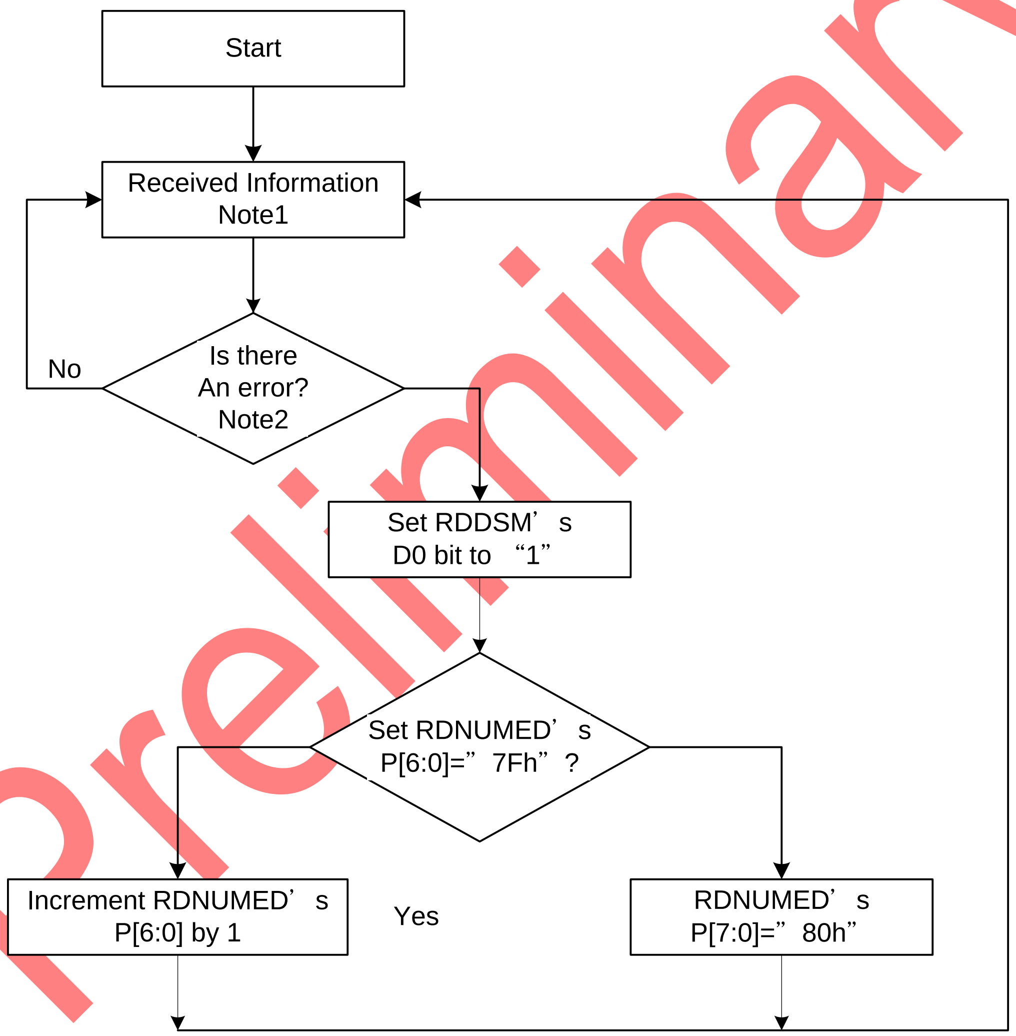
Error Packet

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)”commands.

The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Notes:

1. This information can Interface or Packet Level Communication but it is always from the MCU to the display module in this case.

2. CRC or ECC error.

DCS Read Long Response (DCSRR-L), Data Type = 01 1100(1Ch)

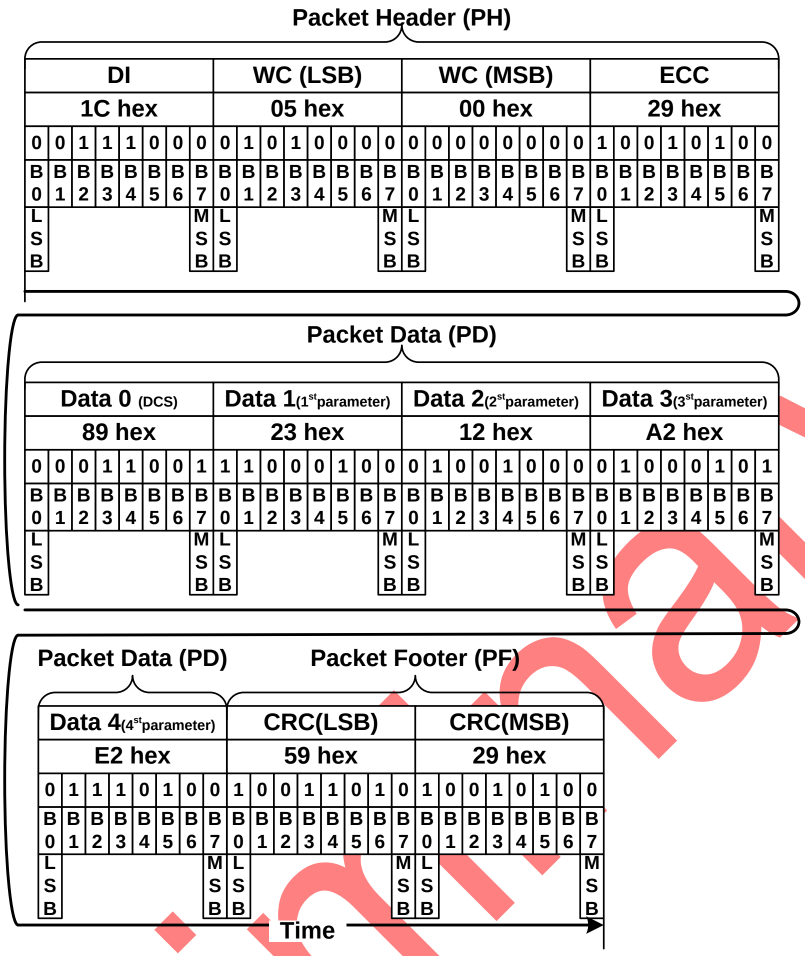
"DCS Read Long Response" (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT,01 1100b), from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

"DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 01 1100b
- Word Count (WC)
    - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
    - Data 0: 89h
    - Data 1: 23h
    - Data 2: 12h
    - Data 3: A2h
    - Data 4: E2h
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



DCS Read Long Response(DCSRR-L)-Example

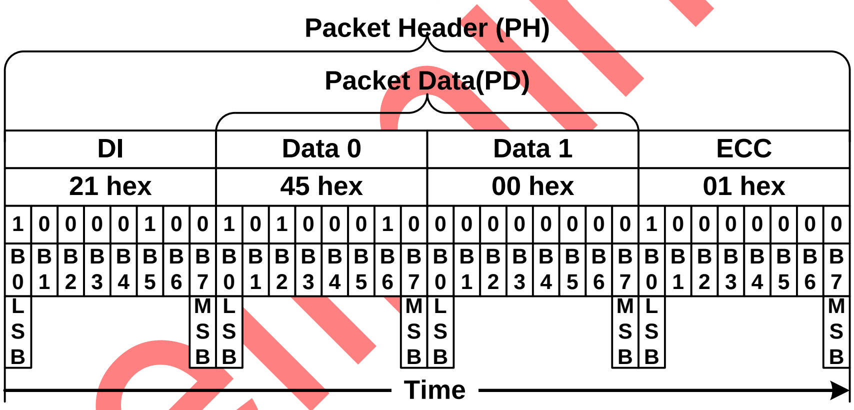
DCS Read Short Response, 1 Byte Returned (DCSRR1-S), Data Type = 10 0001(21h)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 10 0001b
- Packet Data (PD):
    - Data 0: 45h
    - Data 1: 00h (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



DCS Read Short Response, 1 Byte Returned(DCSRR1-S)-Example

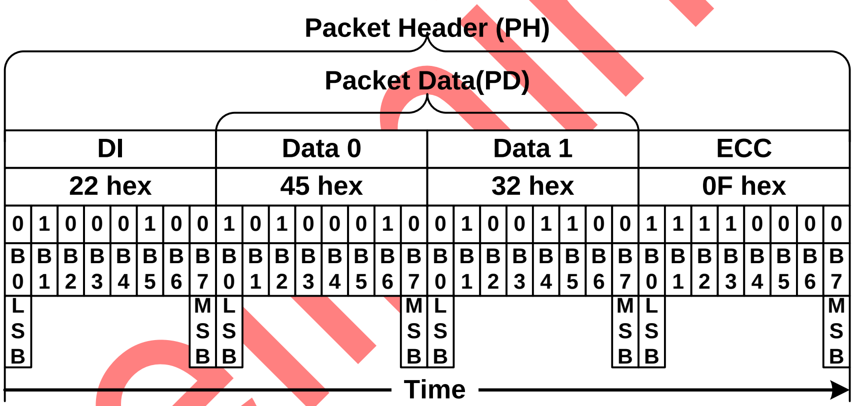
DCS Read Short Response, 2 Bytes Returned (DCSRR2-S), Data Type = 10 0010(22h)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 10 0010b
- Packet Data (PD):
  - Data 0: 45h
  - Data 1: 32h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



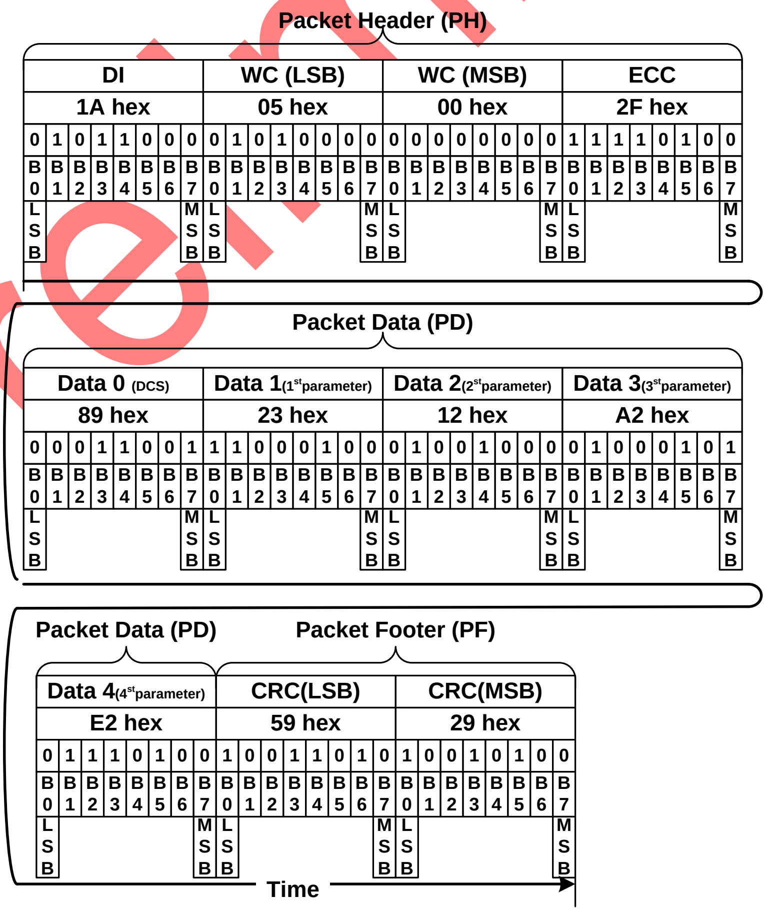
DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) -Example

Generic Read Long Response (GENRR-L), Data Type = 01 1010(1Ah)

“Generic Read Long Response” (GENRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1010b), from the display module to the MCU. “Generic Read Long Response” (GENRR-L) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module. Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 01 1010b
- Word Count (WC)
    - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
    - Data 0: 89h
    - Data 1: 23h
    - Data 2: 12h
    - Data 3: A2h
    - Data 4: E2h
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



Generic Read Short Response, 1 Byte Returned (GENRR1-S), Data Type = 01 0001(11h)

“Generic Read Short Response, 1 Byte Returned” (GENRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0001b), from the display module to the MCU. “Generic Read Short Response, 1 Byte Returned” (GENRR1-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 01 0001b
- Packet Data (PD):
    - Data 0: 45h
    - Data 1: 00h (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

Packet Header (PH)

Packet Data(PD)

DI								Data 0								Data 1								ECC							
22 hex								45 hex								32 hex								0F hex							
0	1	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	1	0	0	1	1	0	0	1	1	1	1	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time →

Generic Read Short Response, 1 Byte Returned (GENRR1-S)-Example

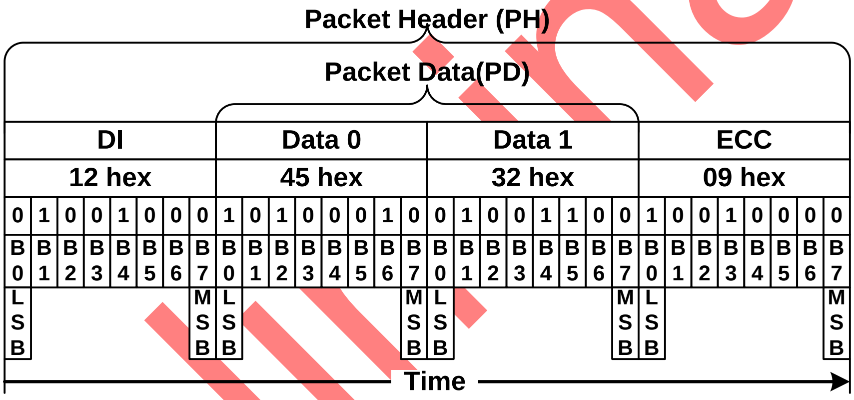
Generic Read Short Response, 2 Bytes Returned (GENRR2-S), Data Type = 01 0010(12h)

"Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0010b), from the display module to the MCU. "Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 01 0010b
- Packet Data (PD):
    - Data 0: 45h
    - Data 1: 32h
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



Generic Read Short Response, 2 Bytes Returned (GENRR2-S)-Example

8.10.1.3.3 COMMUNICATION SEQUENCES

8.10.1.3.3.1 GENERAL

The communication sequences can be done on interface or packet levels between the MCU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”.

This communication sequence description is for DSI data lanes and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.

Functions of the interface level communication is described on the following table.

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop state
	LPDT	Low power data transmission
	ULPS	Ultra-Low power state
	RAR	Remote application reset
	TEE	Tearing effect event
	ACK	Acknowledge (No error)
	BTA	Bus turnaround
High Speed	HSDT	High speed data transmission

Table 26 Interface Level Communication

Functions of the packet level communication are described on the following table.

Packet Sender	Abbreviation	Packet Size	Packet Description
MCU	DCSW1-S	SPa	DCS Write,1 Parameter
	DCSWN-S	SPa	DCS Write, No parameter
	DCSW-L	LPa	DCS Write,Long
	DCSRN-S	SPa	DCS Read,No Parameter
	SMRPS-S	SPa	Set maximum return packet size
	NP-L	LPa	Null packet, No data
Display Module	AwER	SPa	Acknowledge with error report
	DCSRR-L	LPa	DCS Read, Long Response
	DCSRR1-S	SPa	DCS Read, Short Response
	DCSRR2-S	SPa	DCS Read, Short Response

Table 27 Packet Level Communication

8.10.1.3.3.2 SEQUENCES

DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write, 1 Parameter Sequence – Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence – Example2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error=>goto line8 If error=goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" is defined on chapter "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Write, No Parameter Sequence-Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence – Example2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error=>goto line8 If error=goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Sequence-Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, Long Sequence – Example2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error=>goto line8 If error=goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined on chapter "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence – Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>		-	Start
2	SMRPS-S	HSDT	=>		-	Define how many data byte is wanted to read: 1 byte
3	DCSRN-S	HSDT	=>		-	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	=>		-	End of Transmission Packet
5	-	LP-11	=>		-	
6	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
7	-	-	<=	LP-11	-	If no error=>goto line 9 If error=> goto line 14 If error is corrected by ECC =>go to line 19
8						
9	-	-	<=	LPDT	DCSRR1-S	Responsed 1 byte return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the Display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface Control change from the Display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	DCSRR1-S	Responsed 1 byte return
20	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
21	-	-	<=	LP-11	-	
22	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
23	-	LP-11	=>	-	-	End

Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and example sequences, how this packet is used, is described on following tables.

Null Packet, No Parameter Sequence - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission Is used
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoT)” is defined on chapter “End of Transmission Packet (EoT)” and an example sequences, how this packet is used, is described on following tables.

End of Transmission Packet – Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission Is used
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

8.10.1.4 Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

8.10.1.4.1 TRANSMISSION PACKET SEQUENCES

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

• Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

• Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.

• Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

During the BLLP the DSI Link may do any of the following:

• Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX

• Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode

• Transmit one or more non-video packets from the host processor to the peripheral using HS Mode

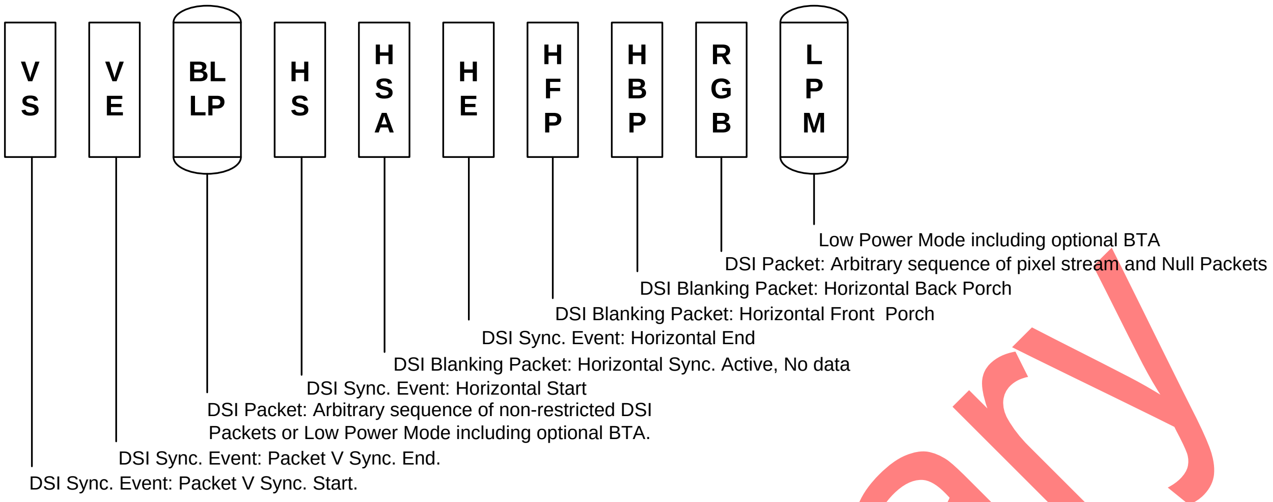
• If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode

• Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.



DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

There are two limitation for MIPI Video mode 2 Lane:

(1) The packet number for H-porch or 1-line data should be even.

(2) Packet Pixel Stream should be start at Lane0.

8.10.1.4.2 NON-BURST MODE WITH SYNC PULSES

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.

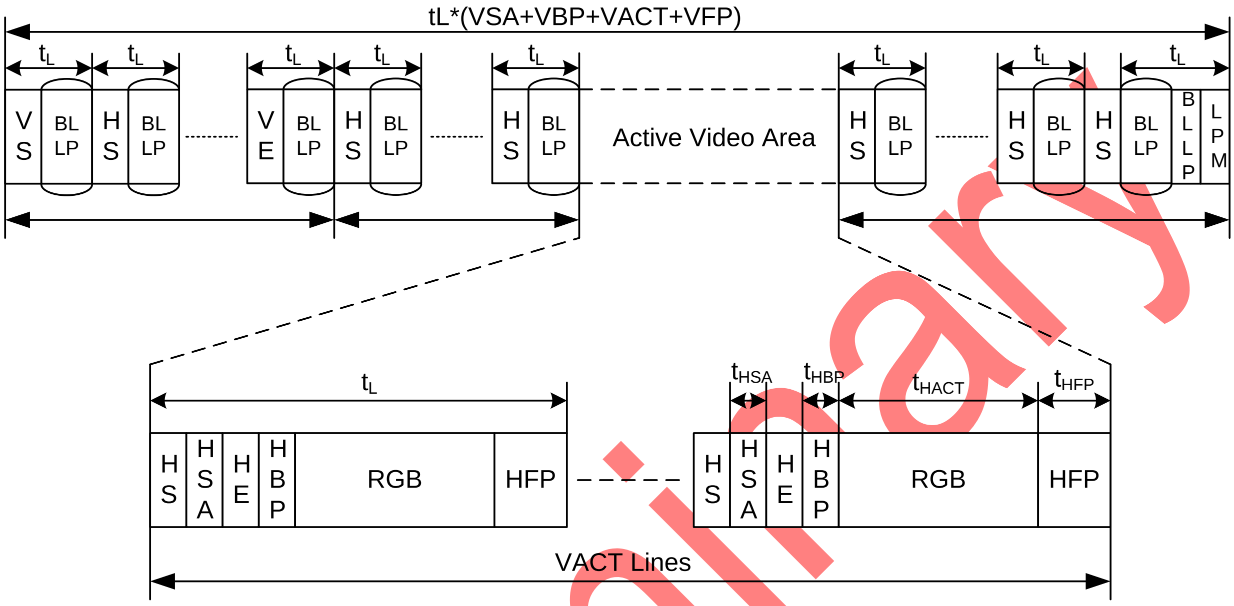


Figure 96 DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.10.1.4.3 NON-BURST MODE

This mode is a simplification of the format described in section 5.3.2.4.2 “Non-Burst Mode with Sync Pulse” .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.

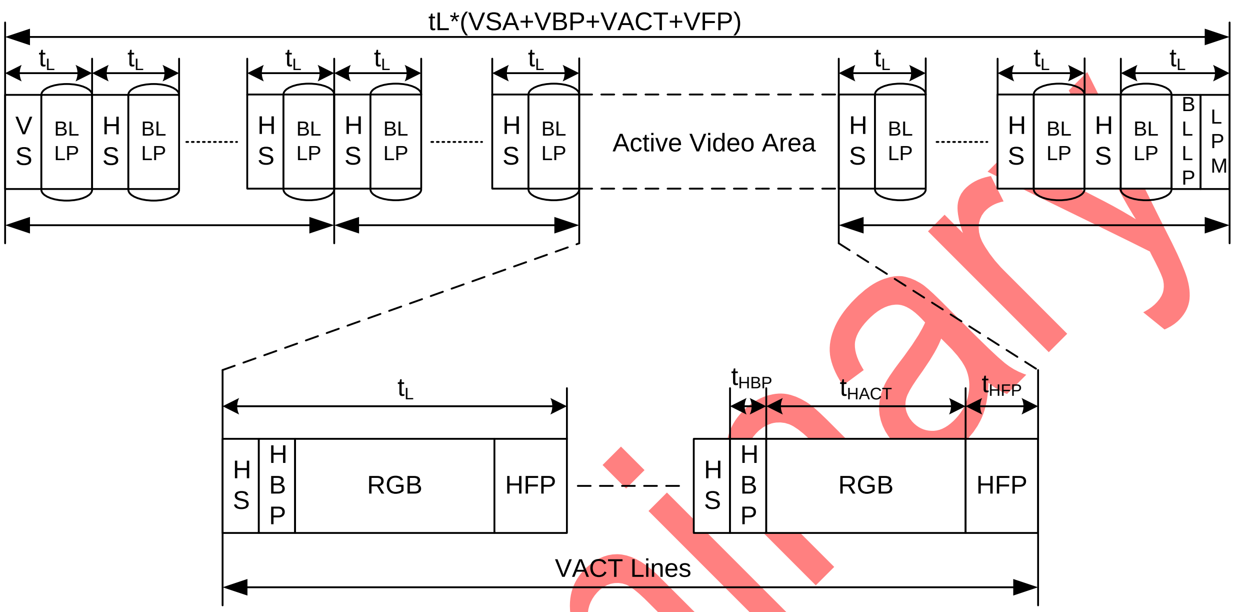


Figure 97 DSI Video Mode Interface Timing: Non-burst Transmission

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.10.1.4.4 BURST MODE

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.

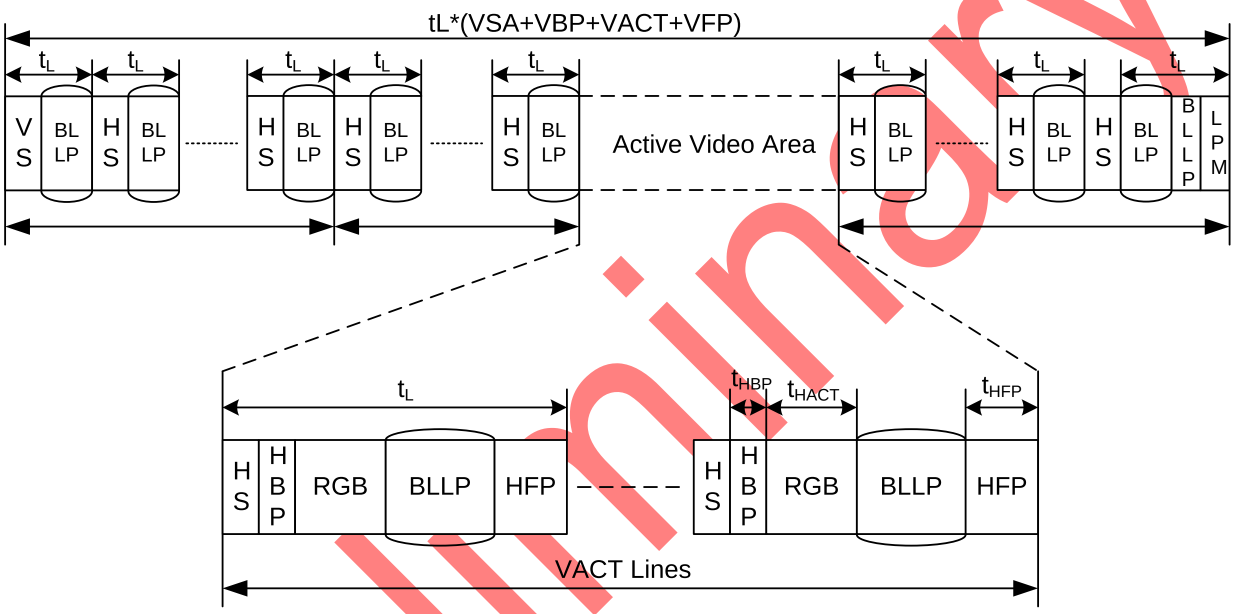


Figure 98 DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.11 Display Data RAM

8.11.1 Configuration

The display module has an integrated 240x320x18-bit graphic type static RAM. This 1382400-bit memory allows storing on-chip a 240xRGBx320 image with an 18-bpp resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

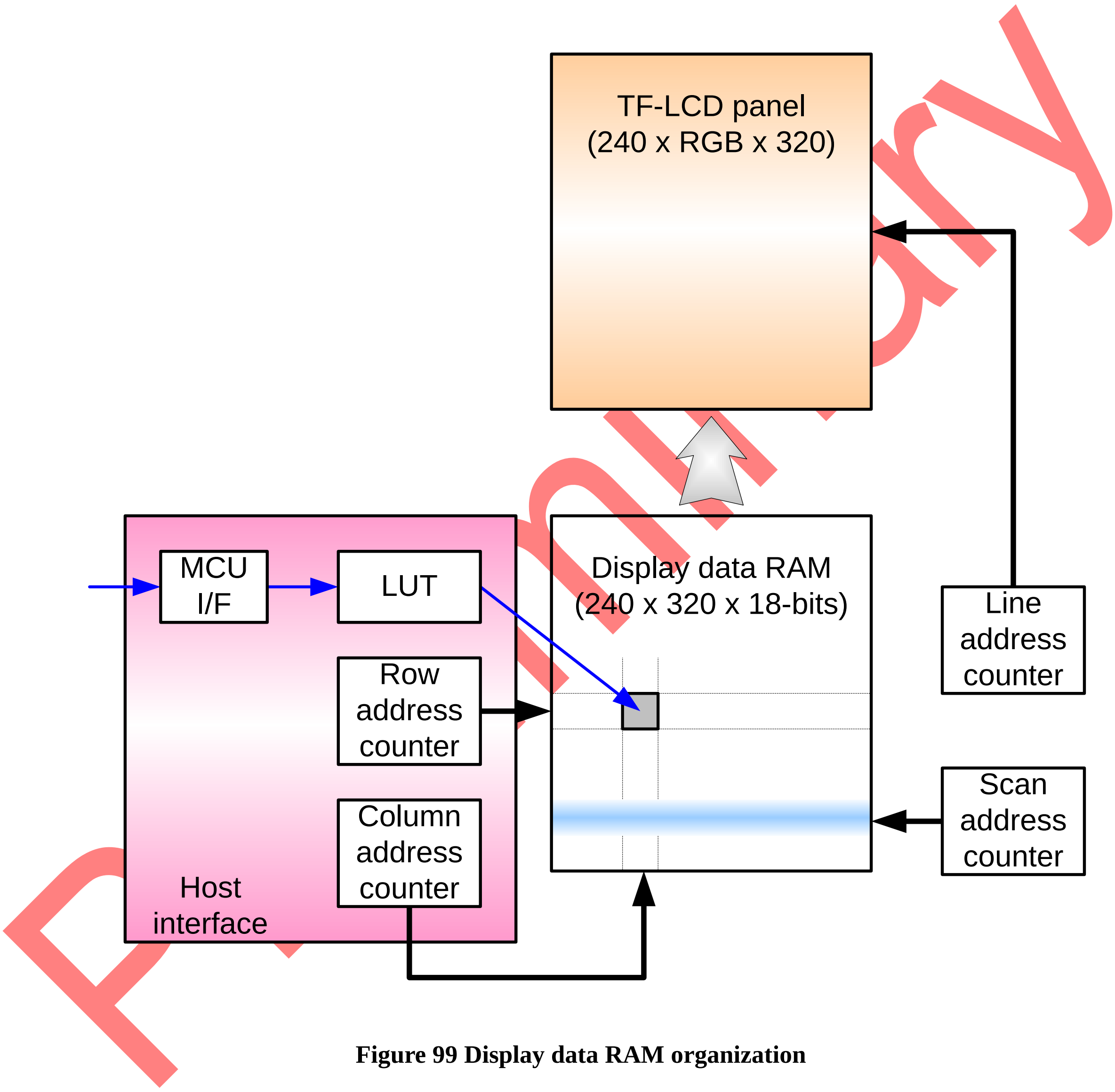


Figure 99 Display data RAM organization

8.11.2 Memory to display address mapping

RGB alignment											
Data control command		Column									
(MADCTR) MX=0		0			1				239		
(MADCTR) MX=1		239			238				0		
Color		R	G	B	R	G	B		R	G	B
Page \ Data											
(MADCTR) MY=0	(MADCTR) MY=1										
0	319										
1	318										
2	317										
3	316										
4	315										
5	314										
6	313										
7	312										
:	:										
312	7										
313	6										
314	5										
315	4										
316	3										
317	2										
318	1										
319	0										
Source output		0	1	2	3	4	5		717	718	719

8.12 Address Control

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=239 (EFh) and Y=0 to Y=319 (13Fh). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=239 (EFh), YE=319 (13Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET and MADCTL", define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 8.12 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

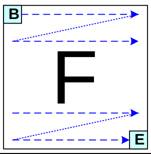
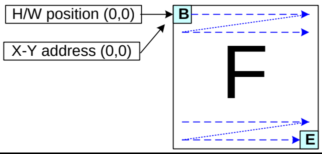
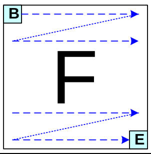
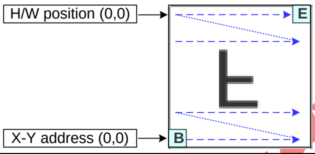
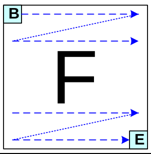
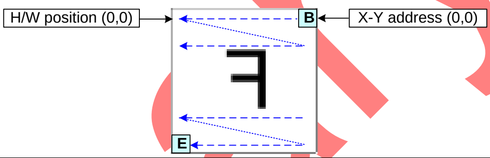
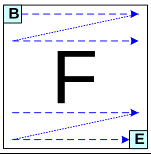
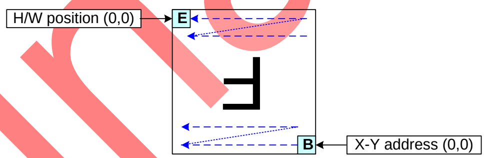
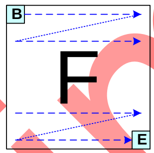
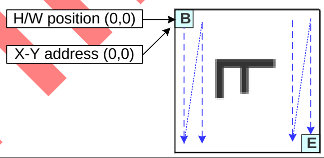
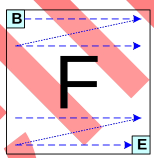
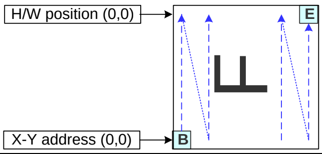
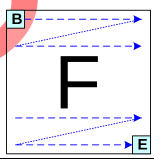
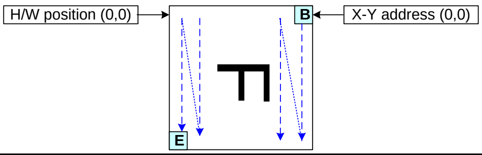
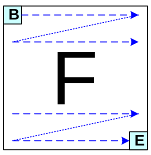
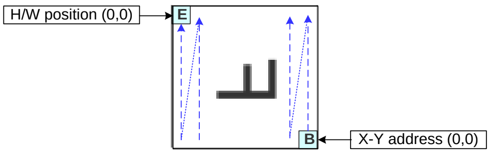
Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 100 Display data RAM organization

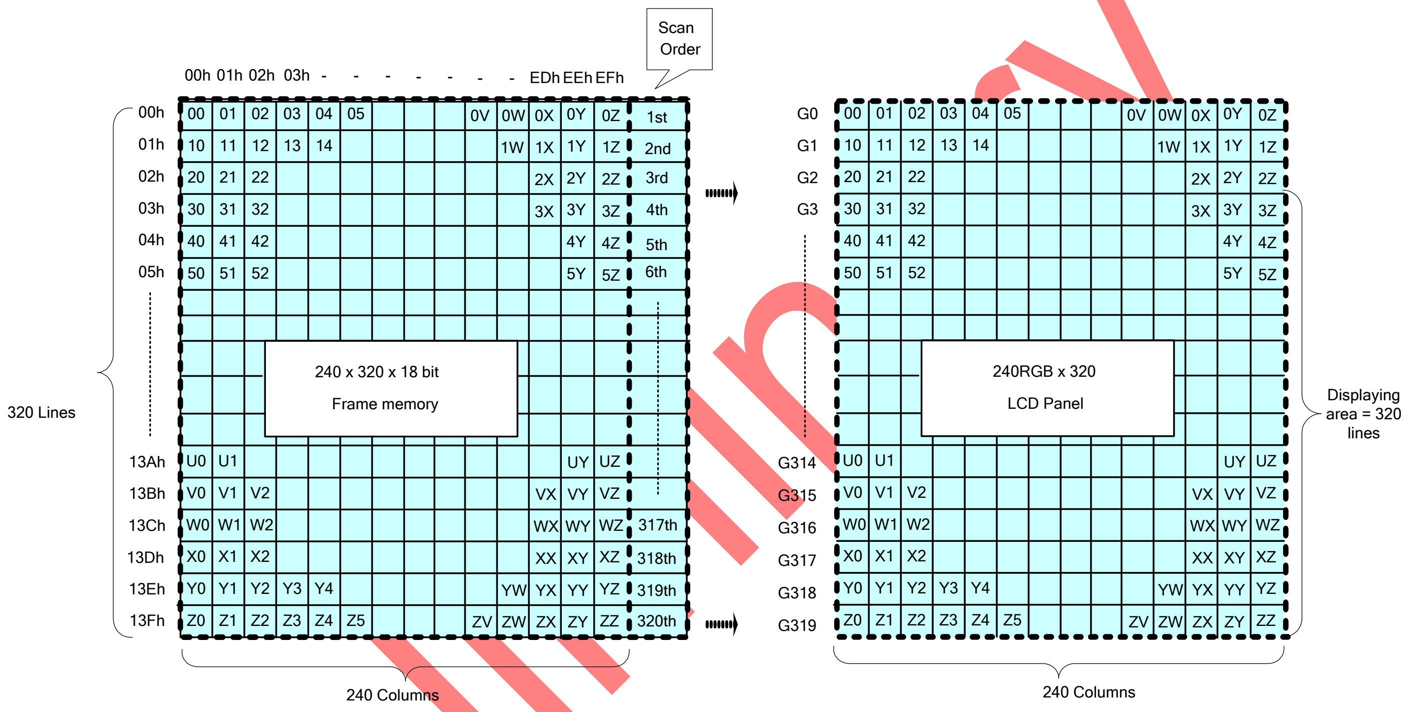
8.13 Normal Display On or Partial Mode On, Vertical Scroll Off

In this mode, contents of the frame memory within an area where column address is 00h to 83h and row address is 00h to

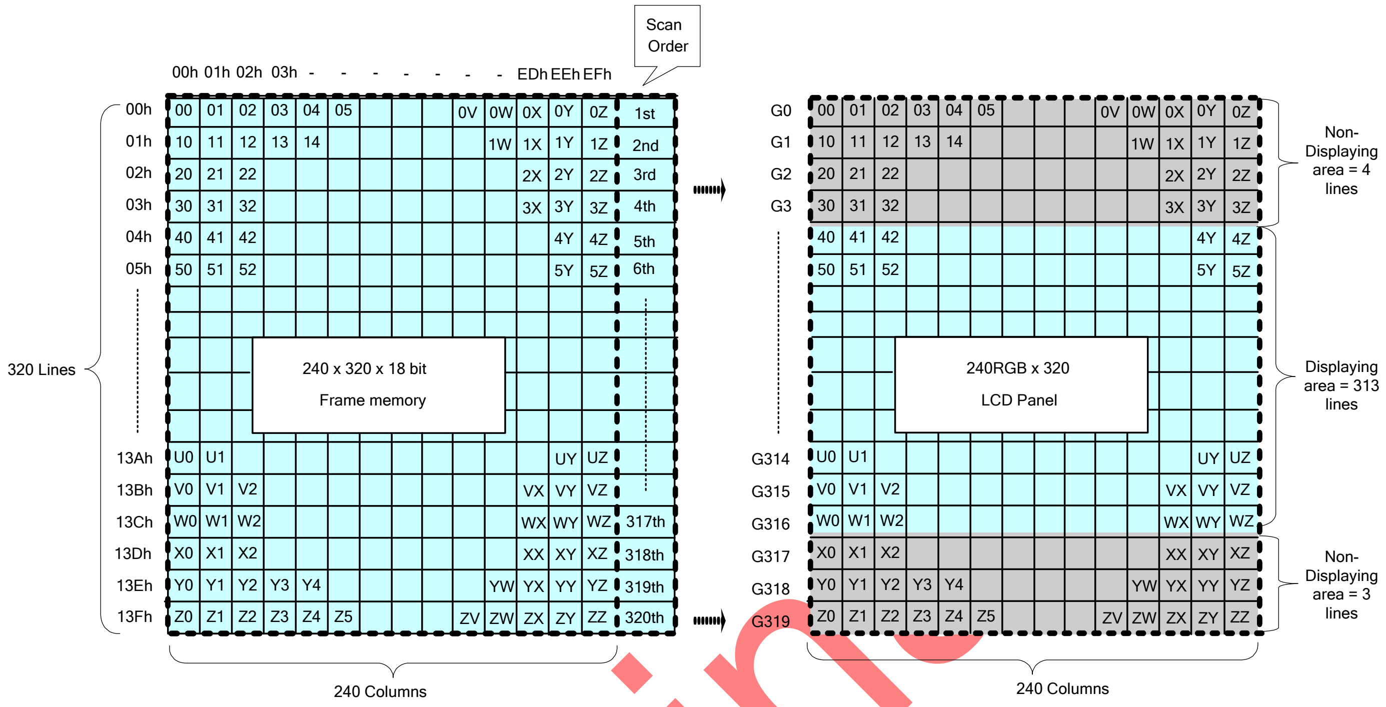
83h is displayed.

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).

Example1) Normal Display On



Example2) Partial Display On: PSL[15:0] = 0004h, PEL[15:0] = 013Ch, MADCTR (ML)=0


Scan Order
00h 01h 02h 03h - - - - - - - EDh EEh EFh
320 Lines
240 x 320 x 18 bit
Frame memory
1st
2nd
3rd
4th
5th
6th
317th
318th
319th
320th
240 Columns
G0
G1
G2
G3
G314
G315
G316
G317
G318
G319
240RGB x 320
LCD Panel
Non-Displaying area = 4 lines
Displaying area = 313 lines
Non-Displaying area = 3 lines
240 Columns

8.14 Vertical Scroll Mode

8.14.1 Rolling scroll

There is just one types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

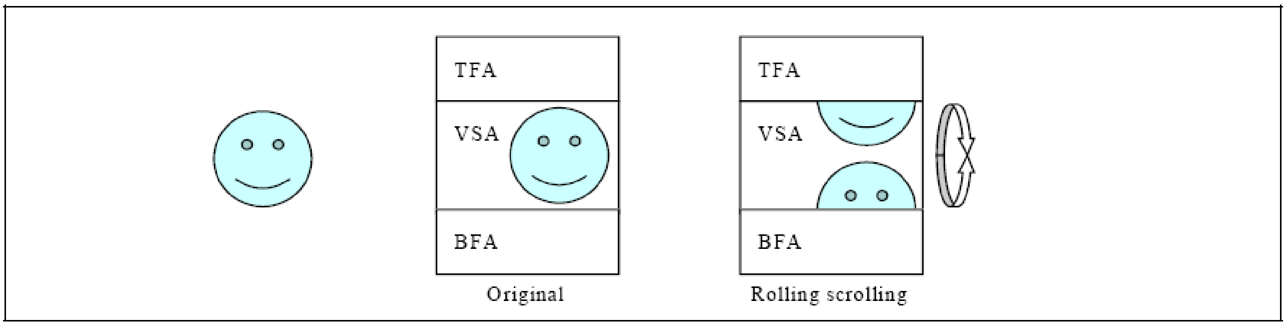
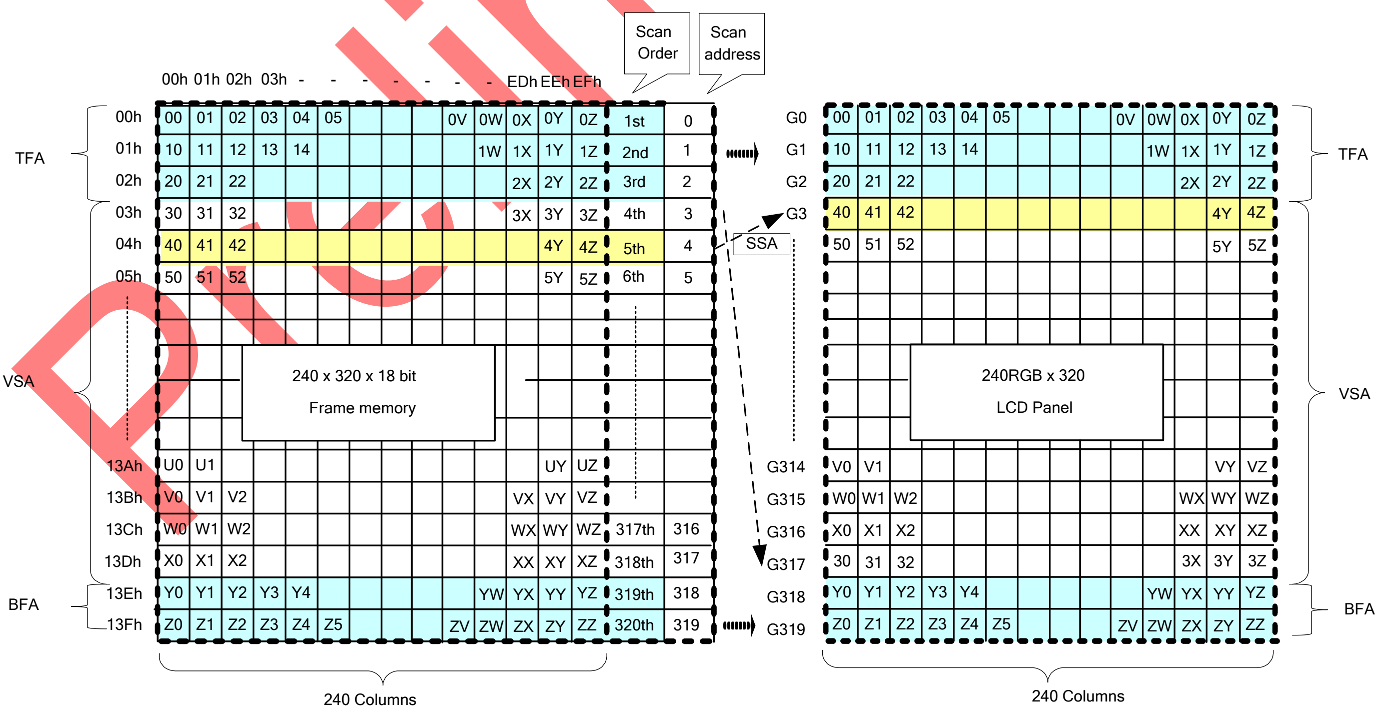


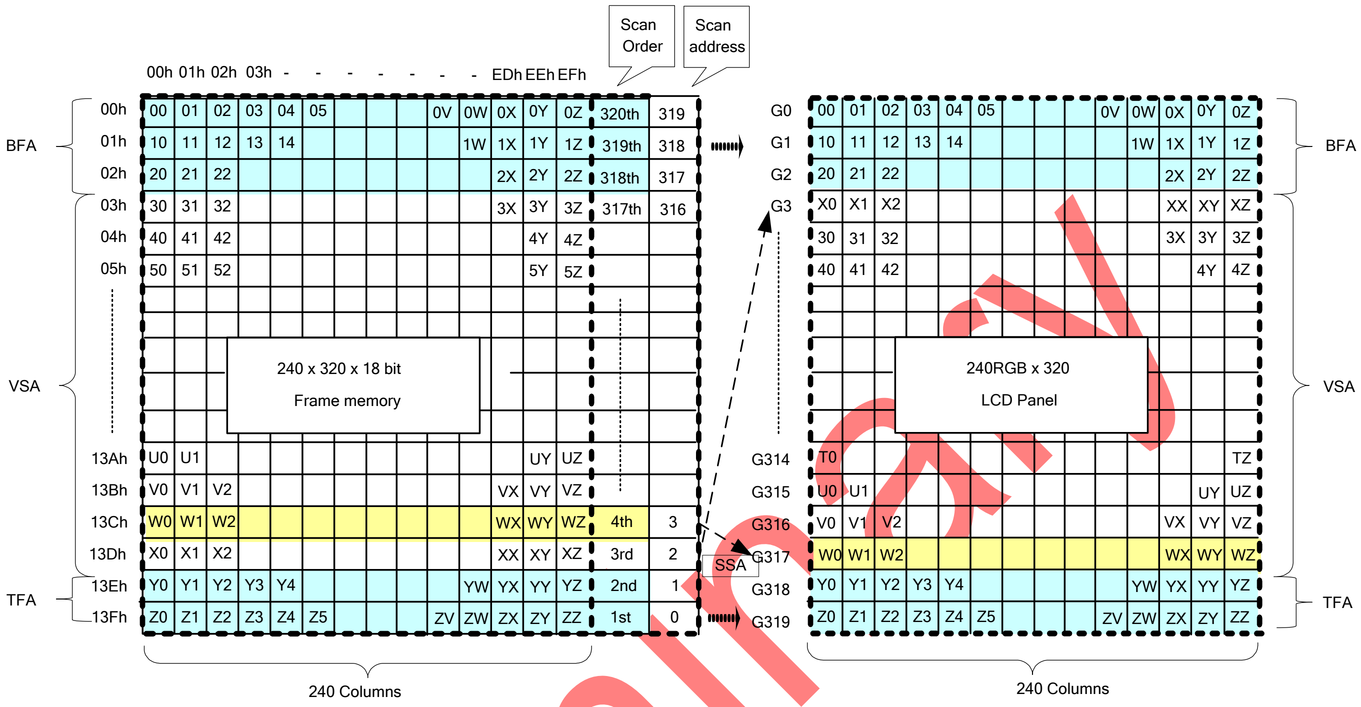
Figure 101 Rolling Scroll Definition

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =320. In this case, ‘rolling’ scrolling is applied as shown below. All the memory contents will be used.

Example1) Panel size=240 x 320, TFA =3, VSA=315, BFA=2, SSA=4, MADCTR ML=0: Rolling Scroll



Example2) Panel size=132 x 132, TFA =2, VSA=315, BFA=3, SSA=4, MADCTR ML=1: Rolling Scroll (TFA and BFA are exchanged)



8.14.2 Vertical Scroll Example

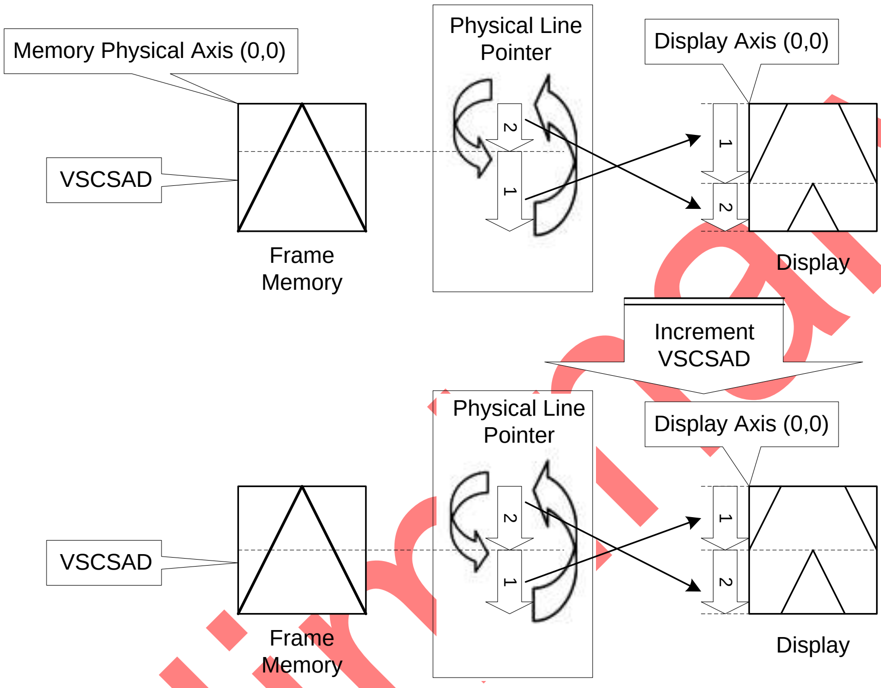
There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA<320

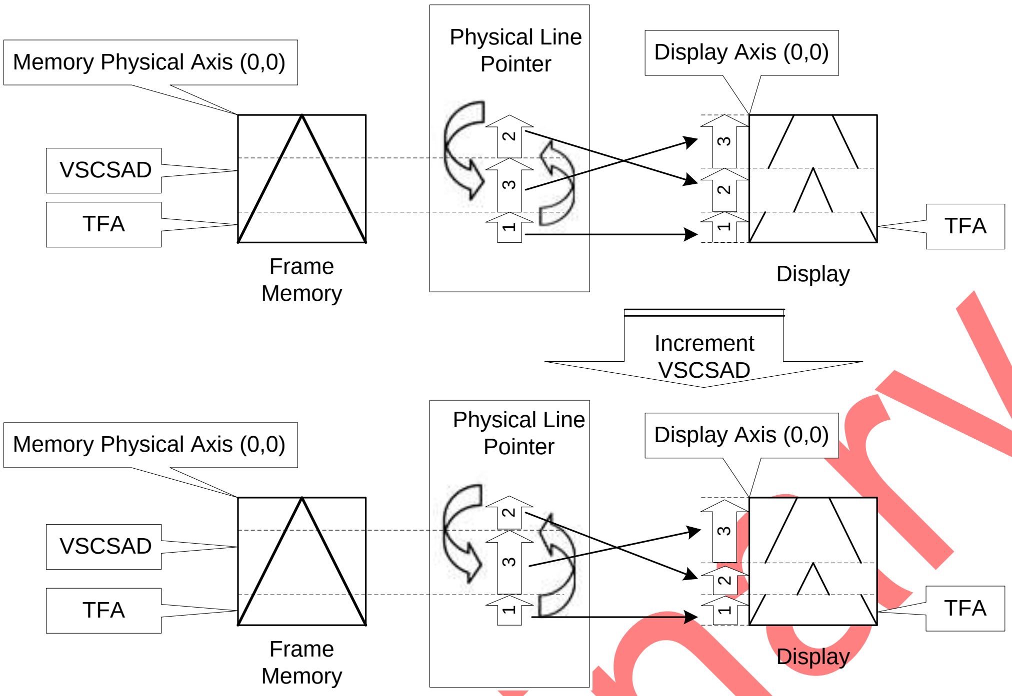
N/A. Do not set TFA + VSA + BFA<320. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=320 (Rolling Scrolling)

Example1) When MADCTR parameter ML=”0”, TFA=0, VSA=320, BFA=0 and VSCSAD=40.



Example2) When MADCTR parameter ML="1", TFA=10, VSA=310, BFA=0 and VSCSAD=30.

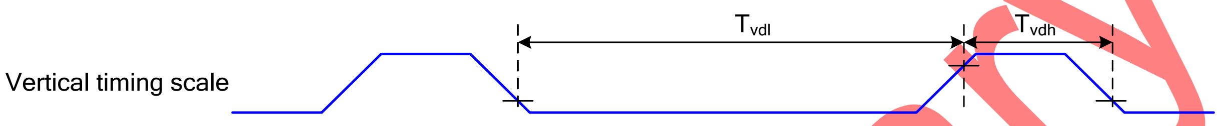


8.15 Tearing Effect

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

8.15.1 Tearing effect line modes

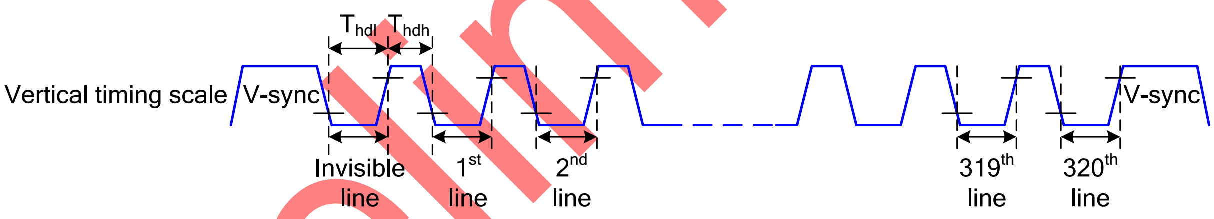
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



tvdh= The LCD display is not updated from the Frame Memory

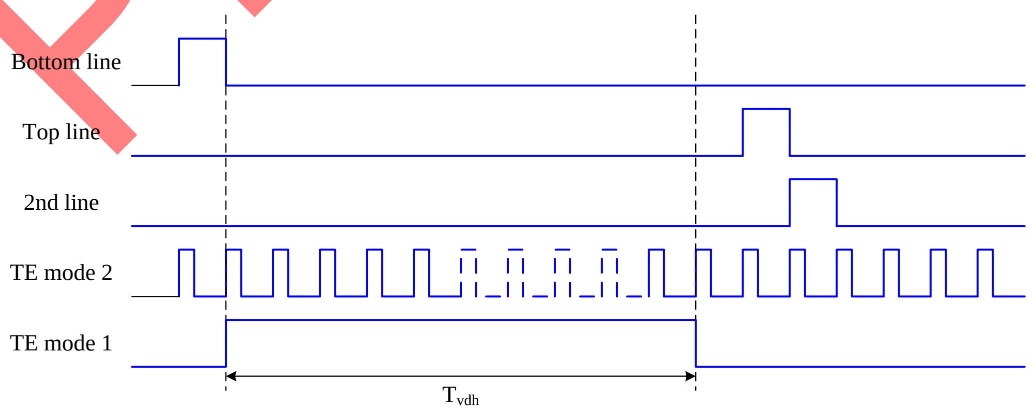
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.



thdh= The LCD display is not updated from the Frame Memory

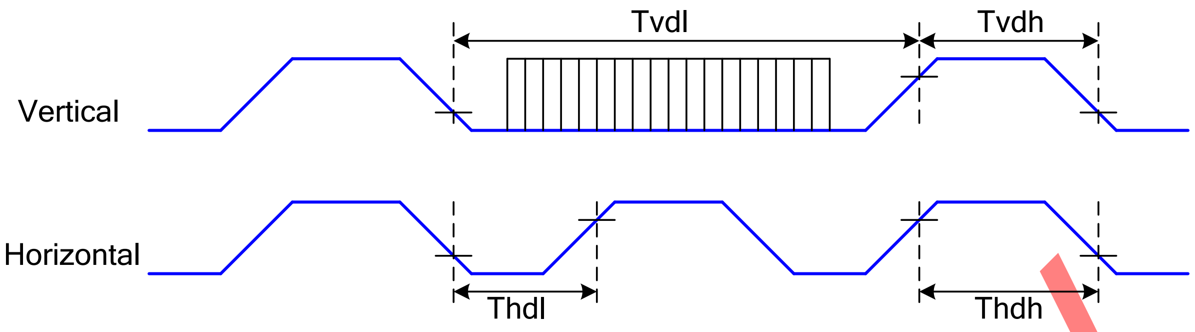
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

8.15.2 Tearing effect line timings

The Tearing Effect signal is described below:

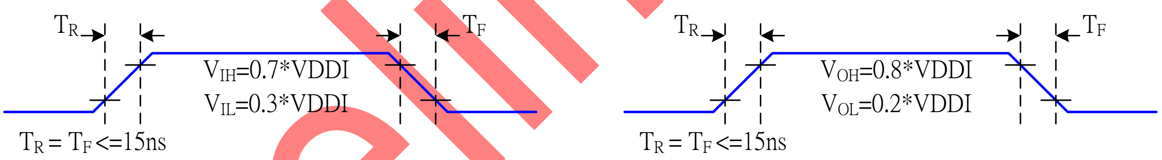


Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	33	-	µs	
thdh	Horizontal Timing Low Duration	25	500	µs	

Table 28 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25°C)

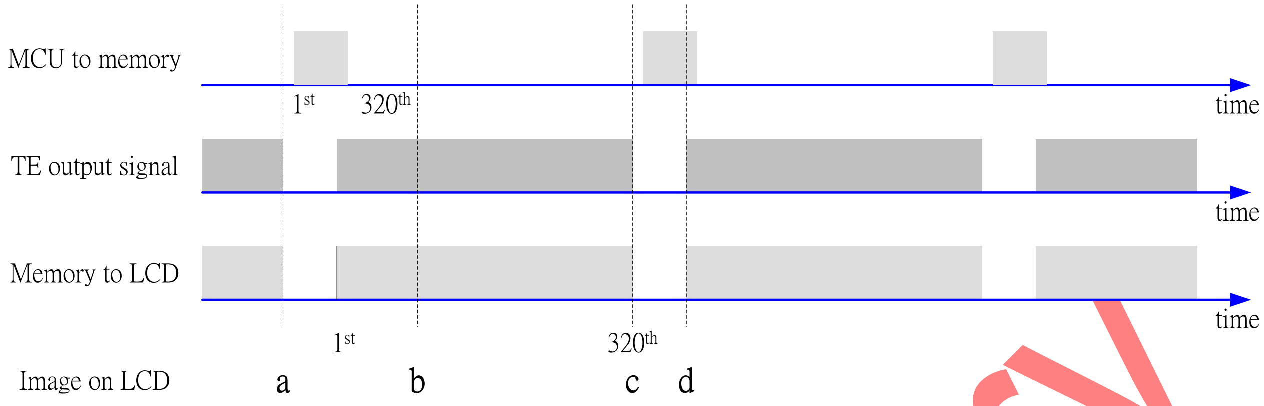
Note: The timings in Table 15 apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

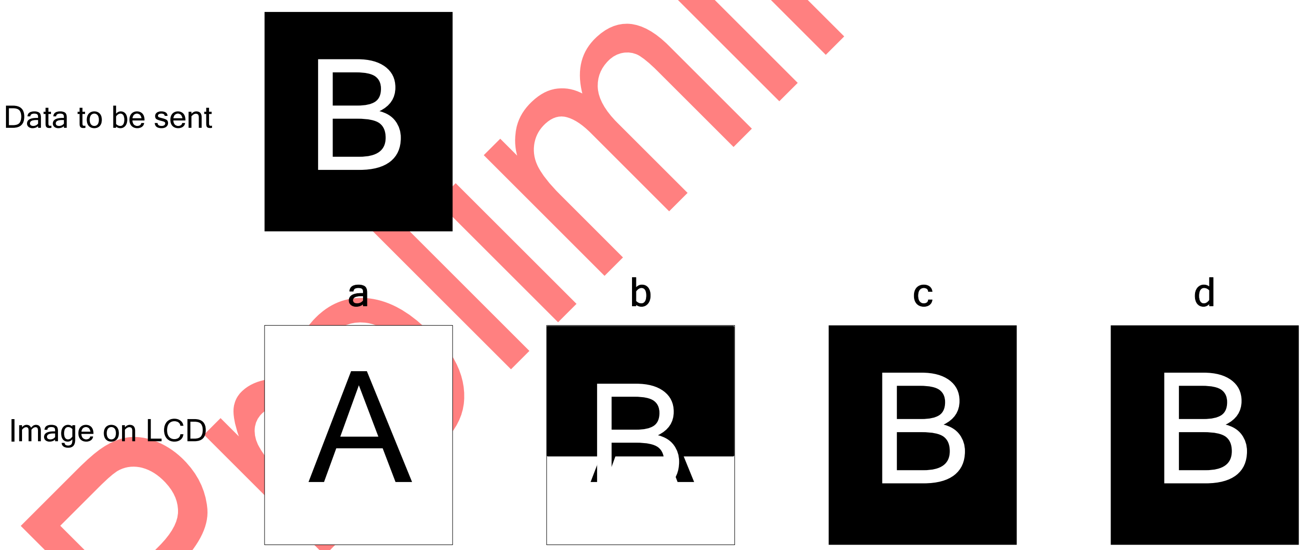


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

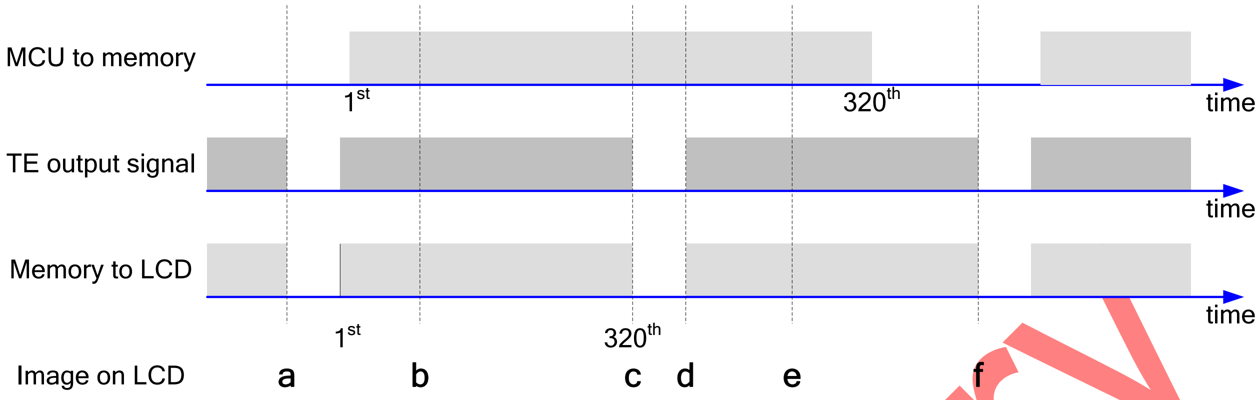
8.15.3 Example 1: MPU Write is faster than panel read



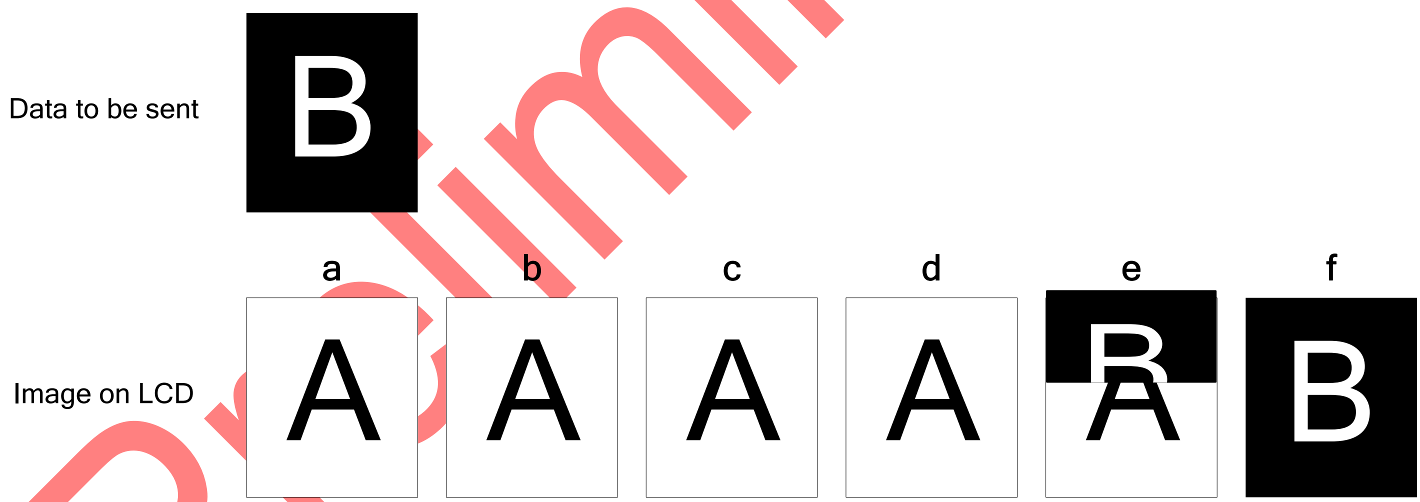
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



8.15.4 Example 2: MPU write is slower than panel read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



8.16 Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

In CABC function application, VDDI power on need delay 5ms after VDD has been supplied.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

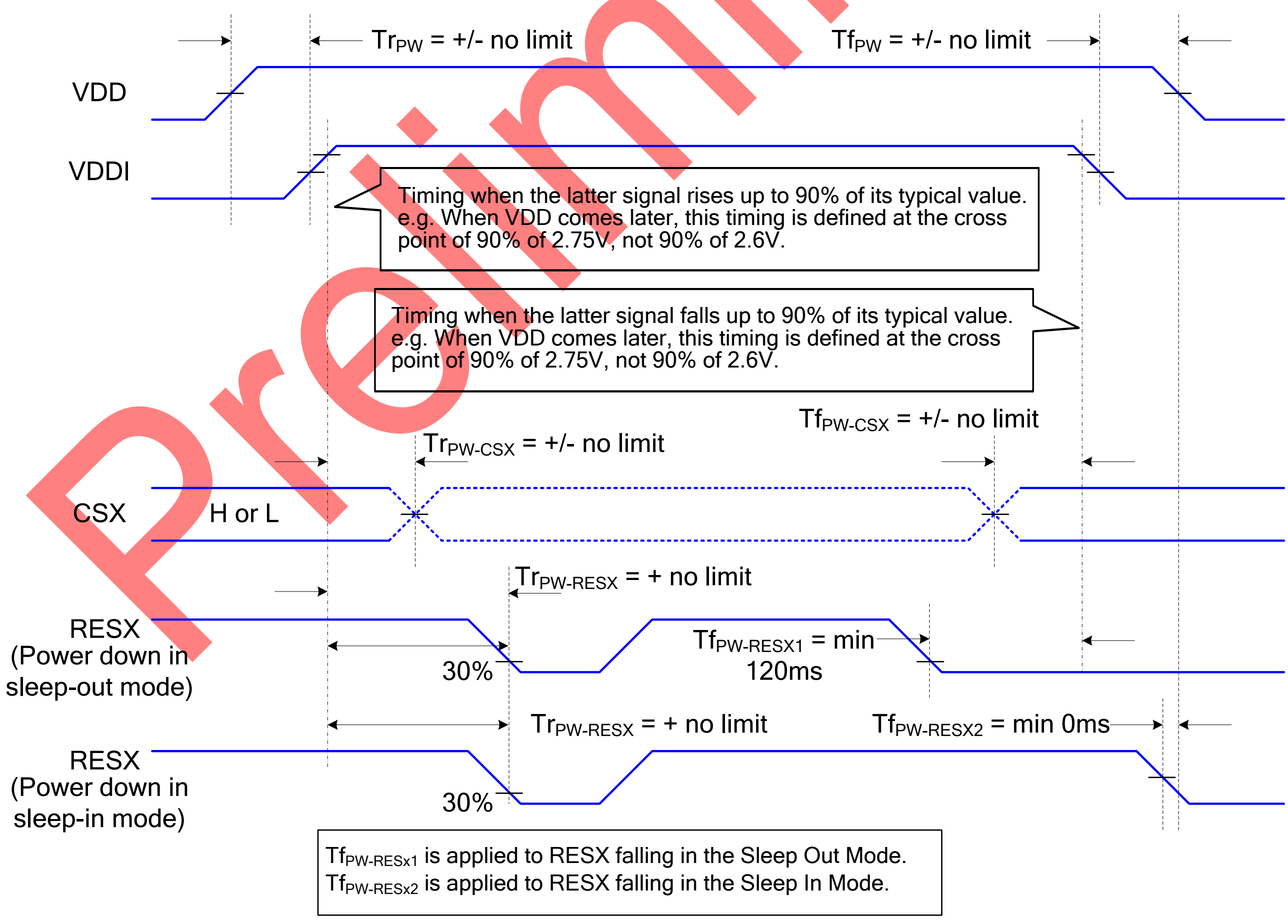
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



8.16.1 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.

8.17 Power Level Definition

8.17.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

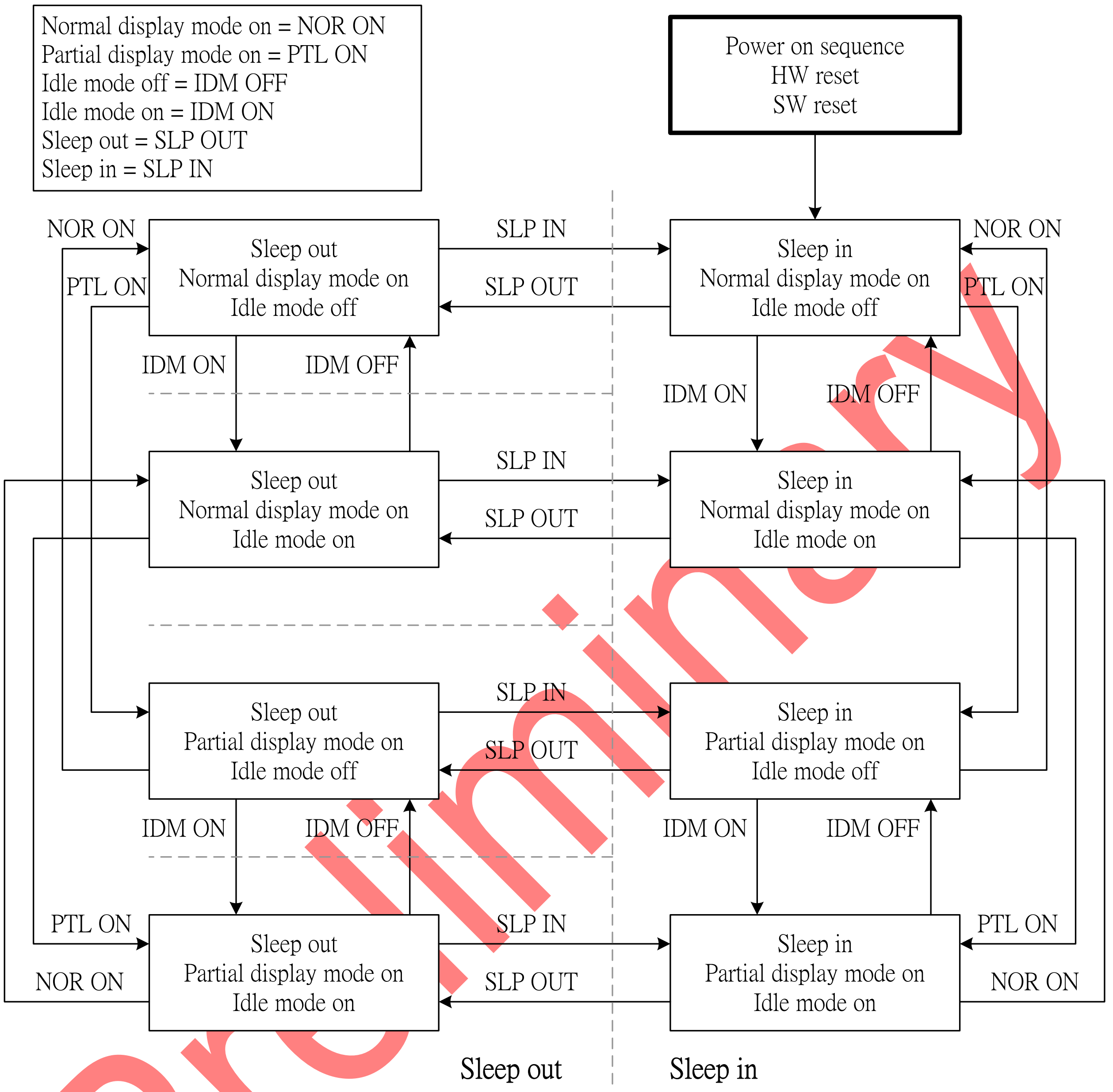
In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode

In this mode, the DC: DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

8.18 Power Flow Chart



8.19 Gamma Correction

ST7785M incorporate the gamma correction function to display 262,244 colors for the LCD panel. The gamma correction is performed with 3 groups of registers, which are gradient adjustment, contrast adjustment and fine- adjustment registers for positive and negative polarities, and RGB can be adjusted individually.

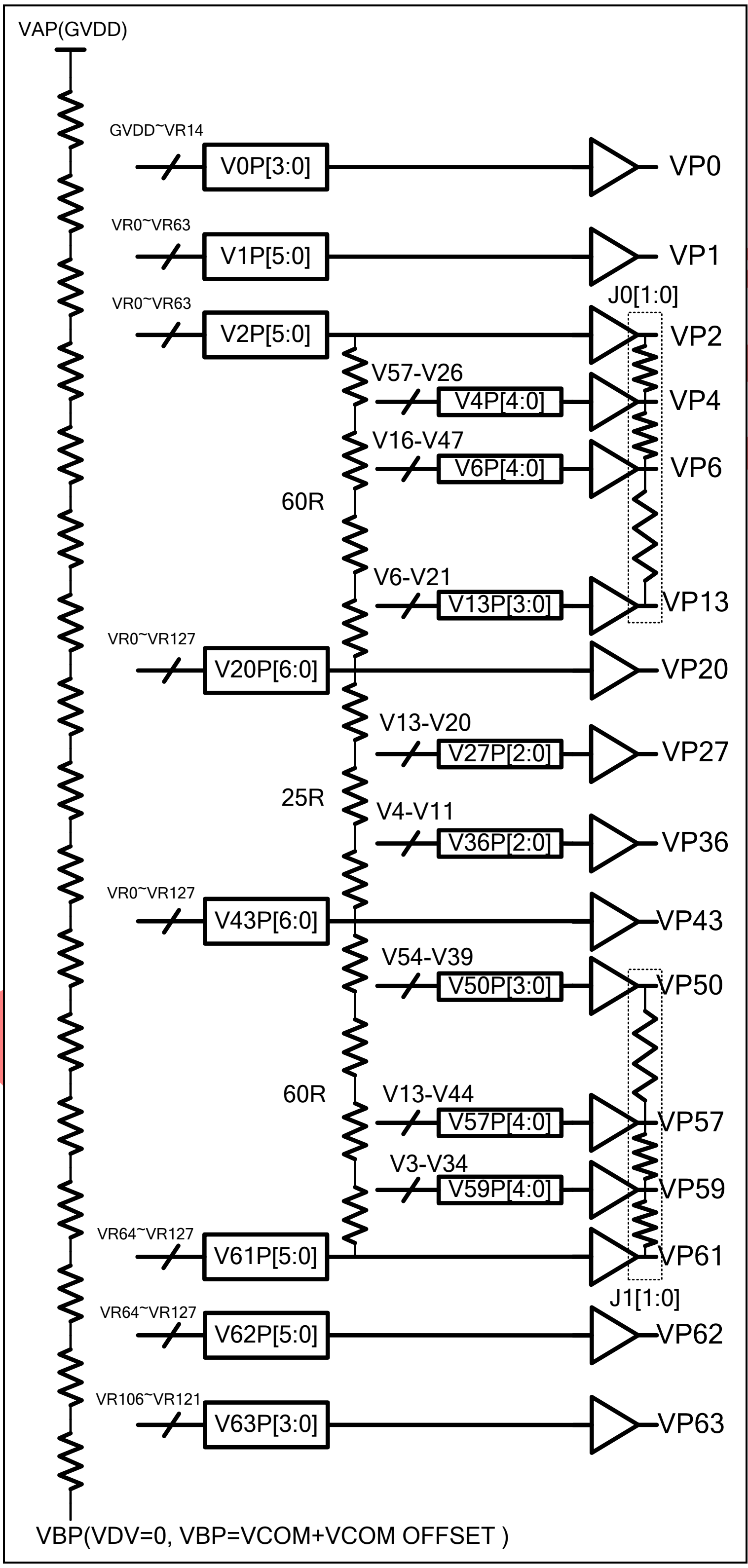


Figure 102 Gray scale Voltage Generation (Positive)

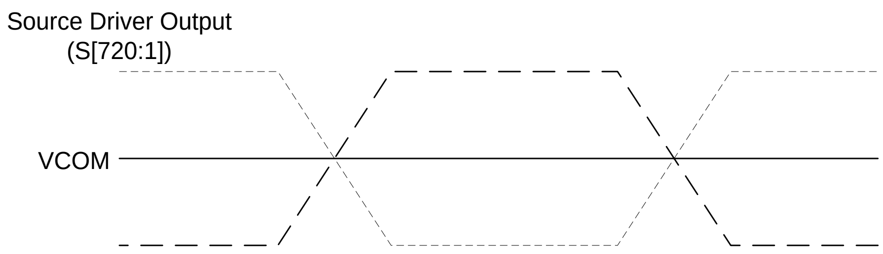


Figure 103 Relationship between Source Output and VCOM

Percentage adjustment:

J0P[1:0], J1P[1:0], J0N[1:0], J1N[1:0] these register are used to adjust the voltage level of interpolation point. The following table is the detail description.

J0P[1:0]/J0N[1:0]:

	00h	01h	02h	03h
VP3/VN3	50%	56%	50%	60%
VP5/VN5	50%	44%	50%	42%
VP7/VN7	86%	71%	80%	66%
VP8/VN8	71%	57%	63%	49%
VP9/VN9	57%	40%	49%	34%
VP10/VN10	43%	29%	34%	23%
VP11/VN11	29%	17%	20%	14%
VP12/VN12	14%	6%	9%	6%

J1P[1:0]/J1N[1:0]:

	00h	01h	02h	03h
VP51/VN51	86%	86%	86%	89%
VP52/VN52	71%	71%	77%	80%
VP53/VN53	57%	60%	63%	69%
VP54/VN54	43%	46%	46%	51%
VP55/VN55	29%	34%	31%	37%
VP56/VN56	14%	17%	14%	20%
VP58/VN58	50%	56%	47%	47%
VP60/VN60	50%	50%	50%	53%

Table 29 voltage level percentage adjustment description

Source voltage of positive gamma level

Gamma level	Related Register	Formula
VP0	V0P[3:0]	(VAP-VBP)*(129R-V0P[3:0]R)/129R+VBP
VP1	V1P[5:0]	(VAP-VBP)*(128R-V1P[5:0]R)/129R+VBP
VP2	V2P[5:0]	(VAP-VBP)*(128R-V2P[5:0]R)/129R+VBP
VP3	J0P[1:0]	(VP2-VP4)*J0P[1:0]+VP4
VP4	V4P[4:0]	(VP2-VP20)*(57R-V4P[4:0])/60R+VP20
VP5	J0P[1:0]	(VP4-VP6)*J0P[1:0]+VP6
VP6	V6P[4:0]	(VP2-VP20)*(47R-V6P[4:0])/60R+VP20
VP7	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP8	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP9	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP10	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP11	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP12	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP13	V13P[3:0]	(VP2-VP20)*(21R-V13P[3:0])/60R+VP20
VP14	--	(VP13-VP20)/(20-13)*(20-14)+VP20
VP15	--	(VP13-VP20)/(20-13)*(20-15)+VP20
VP16	--	(VP13-VP20)/(20-13)*(20-16)+VP20
VP17	--	(VP13-VP20)/(20-13)*(20-17)+VP20
VP18	--	(VP13-VP20)/(20-13)*(20-18)+VP20
VP19	--	(VP13-VP20)/(20-13)*(20-19)+VP20
VP20	V20P[6:0]	(VAP-VBP)*(128R-V20P[6:0]R)/129R+VBP
VP21	--	(VP20-VP27)/(27-20)*(27-21)+VP27
VP22	--	(VP20-VP27)/(27-20)*(27-22)+VP27
VP23	--	(VP20-VP27)/(27-20)*(27-23)+VP27
VP24	--	(VP20-VP27)/(27-20)*(27-24)+VP27
VP25	--	(VP20-VP27)/(27-20)*(27-25)+VP27
VP26	--	(VP20-VP27)/(27-20)*(27-26)+VP27
VP27	V27P[2:0]	(VP20-VP43)*(20R-V27P[2:0])/25R+VP43
VP28	--	(VP27-VP36)/(36-27)*(36-28)+VP36
VP29	--	(VP27-VP36)/(36-27)*(36-29)+VP36
VP30	--	(VP27-VP36)/(36-27)*(36-30)+VP36
VP31	--	(VP27-VP36)/(36-27)*(36-31)+VP36
VP32	--	(VP27-VP36)/(36-27)*(36-32)+VP36
VP33	--	(VP27-VP36)/(36-27)*(36-33)+VP36
VP34	--	(VP27-VP36)/(36-27)*(36-34)+VP36
VP35	--	(VP27-VP36)/(36-27)*(36-35)+VP36
VP36	V36P[2:0]	(VP20-VP43)*(11R-V36P[2:0])/25R+VP43
VP37	--	(VP36-VP43)/(43-36)*(43-37)+VP43
VP38	--	(VP36-VP43)/(43-36)*(43-38)+VP43
VP39	--	(VP36-VP43)/(43-36)*(43-39)+VP43
VP40	--	(VP36-VP43)/(43-36)*(43-40)+VP43
VP41	--	(VP36-VP43)/(43-36)*(43-41)+VP43
VP42	--	(VP36-VP43)/(43-36)*(43-42)+VP43
VP43	V43P[6:0]	(VAP-VBP)*(128R-V43P[6:0]R)/129R+VBP
VP44	--	(VP43-VP50)/(50-43)*(50-44)+VP50
VP45	--	(VP43-VP50)/(50-43)*(50-45)+VP50
VP46	--	(VP43-VP50)/(50-43)*(50-46)+VP50
VP47	--	(VP43-VP50)/(50-43)*(50-47)+VP50
VP48	--	(VP43-VP50)/(50-43)*(50-48)+VP50
VP49	--	(VP43-VP50)/(50-43)*(50-49)+VP50
VP50	V50P[3:0]	(VP43-VP61)*(54R-V50P[3:0])/60R+VP61
VP51	J1P[1:0]	(V5P0-VP57)*J1P[1:0]+VP57
VP52	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57

VP53	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP54	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP55	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP56	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP57	V57P[4:0]	(VP43-VP61)*(44R-V57P[4:0])/60R+VP61
VP58	J1P[1:0]	(VP57-VP59)*J1P[1:0]+VP59
VP59	V59P[4:0]	(VP43-VP61)*(34R-V59P[4:0])/60R+VP61
VP60	J1P[1:0]	(VP59-VP61)*J1P[1:0]+VP61
VP61	V61P[5:0]	(VAP-VBP)*(64R-V61P[5:0]R)/129R+VBP
VP62	V62P[5:0]	(VAP-VBP)*(64R-V62P[5:0]R)/129R+VBP
VP63	V63P[3:0]	(VAP-VBP)*(23R-V63P[3:0]R)/129R+VBP

Source voltage of negative gamma level

Gamma level	Related Register	Formula
VN0	V0N[3:0]	VBN-(VBN-VAN)*(129R-V0N[3:0]R)/129R
VN1	V1N[5:0]	VBN-(VBN-VAN)*(128R-V1N[5:0]R)/129R
VN2	V2N[5:0]	VBN-(VBN-VAN)*(128R-V2N[5:0]R)/129R
VN3	J0N[1:0]	(VN2-VN4)*J0N[1:0]+VN4
VN4	V4N[4:0]	(VN2-VN20)*(57R-V4N[4:0])/60R+VN20
VN5	J0N[1:0]	(VN4-VN6)*J0N[1:0]+VN6
VN6	V6N[4:0]	(VN2-VN20)*(47R-V6N[4:0])/60R+VN20
VN7	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN8	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN9	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN10	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN11	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN12	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN13	V13N[3:0]	(VN2-VN20)*(21R-V13N[3:0])/60R+VN20
VN14	--	(VN13-VN20)/(20-13)*(20-14)+VN20
VN15	--	(VN13-VN20)/(20-13)*(20-15)+VN20
VN16	--	(VN13-VN20)/(20-13)*(20-16)+VN20
VN17	--	(VN13-VN20)/(20-13)*(20-17)+VN20
VN18	--	(VN13-VN20)/(20-13)*(20-18)+VN20
VN19	--	(VN13-VN20)/(20-13)*(20-19)+VN20
VN20	V20N[6:0]	VBN-(VBN-VAN)*(128R-V20N[6:0]R)/129R
VN21	--	(VN20-VN27)/(27-20)*(27-21)+VN27
VN22	--	(VN20-VN27)/(27-20)*(27-22)+VN27
VN23	--	(VN20-VN27)/(27-20)*(27-23)+VN27
VN24	--	(VN20-VN27)/(27-20)*(27-24)+VN27
VN25	--	(VN20-VN27)/(27-20)*(27-25)+VN27
VN26	--	(VN20-VN27)/(27-20)*(27-26)+VN27
VN27	V27N[2:0]	(VN20-VN43)*(20R-V27N[2:0])/25R+VN43
VN28	--	(VN27-VN36)/(36-27)*(36-28)+VN36
VN29	--	(VN27-VN36)/(36-27)*(36-29)+VN36
VN30	--	(VN27-VN36)/(36-27)*(36-30)+VN36
VN31	--	(VN27-VN36)/(36-27)*(36-31)+VN36
VN32	--	(VN27-VN36)/(36-27)*(36-32)+VN36
VN33	--	(VN27-VN36)/(36-27)*(36-33)+VN36
VN34	--	(VN27-VN36)/(36-27)*(36-34)+VN36
VN35	--	(VN27-VN36)/(36-27)*(36-35)+VN36
VN36	V36N[2:0]	(VN20-VN43)*(11R-V36N[2:0])/25R+VN43
VN37	--	(VN36-VN43)/(43-36)*(43-37)+VN43
VN38	--	(VN36-VN43)/(43-36)*(43-38)+VN43
VN39	--	(VN36-VN43)/(43-36)*(43-39)+VN43

VN40	--	(VN36-VN43)/(43-36)*(43-40)+VN43
VN41	--	(VN36-VN43)/(43-36)*(43-41)+VN43
VN42	--	(VN36-VN43)/(43-36)*(43-42)+VN43
VN43	V43N[6:0]	VBN-(VBN-VAN)*(128R-V43N[6:0]R)/129R
VN44	--	(VN43-VN50)/(50-43)*(50-44)+VN50
VN45	--	(VN43-VN50)/(50-43)*(50-45)+VN50
VN46	--	(VN43-VN50)/(50-43)*(50-46)+VN50
VN47	--	(VN43-VN50)/(50-43)*(50-47)+VN50
VN48	--	(VN43-VN50)/(50-43)*(50-48)+VN50
VN49	--	(VN43-VN50)/(50-43)*(50-49)+VN50
VN50	V50N[3:0]	(VN43-VN61)*(54R-V50N[3:0])/60R+VN61
VN51	J1N[1:0]	(V5N0-VN57)*J1N[1:0]+VN57
VN52	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN53	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN54	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN55	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN56	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN57	V57N[4:0]	(VN43-VN61)*(44R-V57N[4:0])/60R+VN61
VN58	J1N[1:0]	(VN57-VN59)*J1N[1:0]+VN59
VN59	V59N[4:0]	(VN43-VN61)*(34R-V59N[4:0])/60R+VN61
VN60	J1N[1:0]	(VN59-VN61)*J1N[1:0]+VN61
VN61	V61N[5:0]	VBN-(VBN-VAN)*(64R-V61N[5:0]R)/129R
VN62	V62N[5:0]	VBN-(VBN-VAN)*(64R-V62N[5:0]R)/129R
VN63	V63N[3:0]	VBN-(VBN-VAN)*(23R-V63N[3:0]R)/129R

8.20 Gray voltage generator for digital gamma correction

ST7785M digital gamma function can implement the RGB gamma correction independently. ST7785M utilizes look-up table of digital gamma to change ram data, and then display the changed data from source driver. The following diagram shows the data flow of digital gamma.

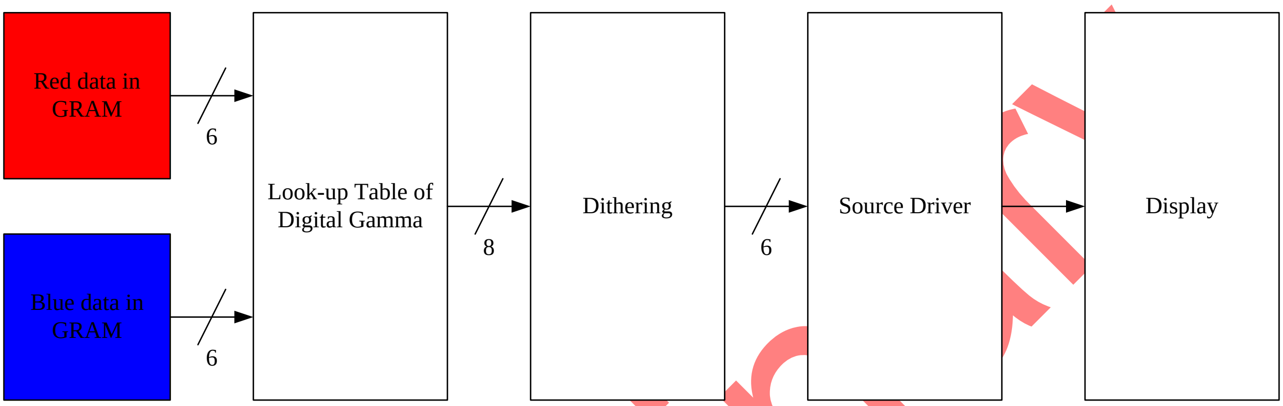


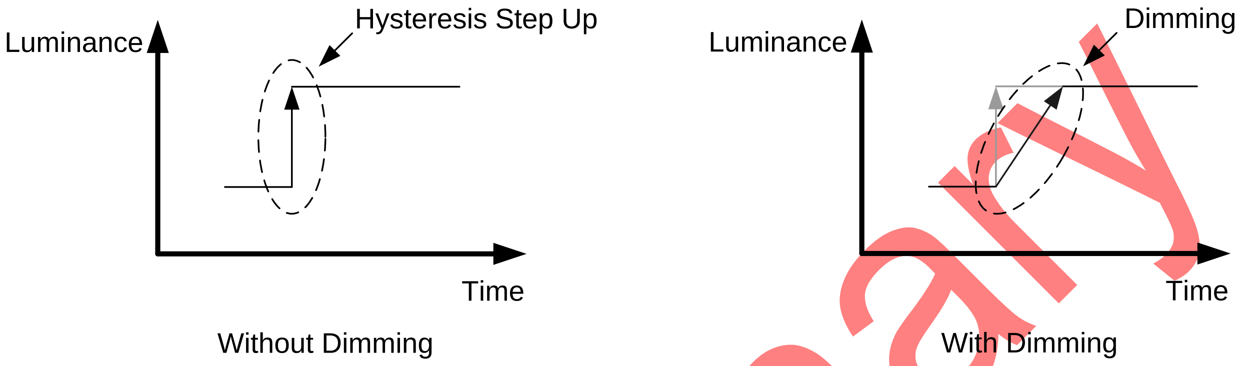
Figure 104 Block diagram of digital gamma

There are 2 registers and each register has 64 bytes to set R, G, B gamma independently. When bit DGMEN be set to 1, R and B gamma will be mapped via look-up table of digital gamma to gray level voltage.

8.21 Display Dimming

8.21.1 General Description

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. This dimming function curve is the same in increment and decrement. The basic idea is described below.



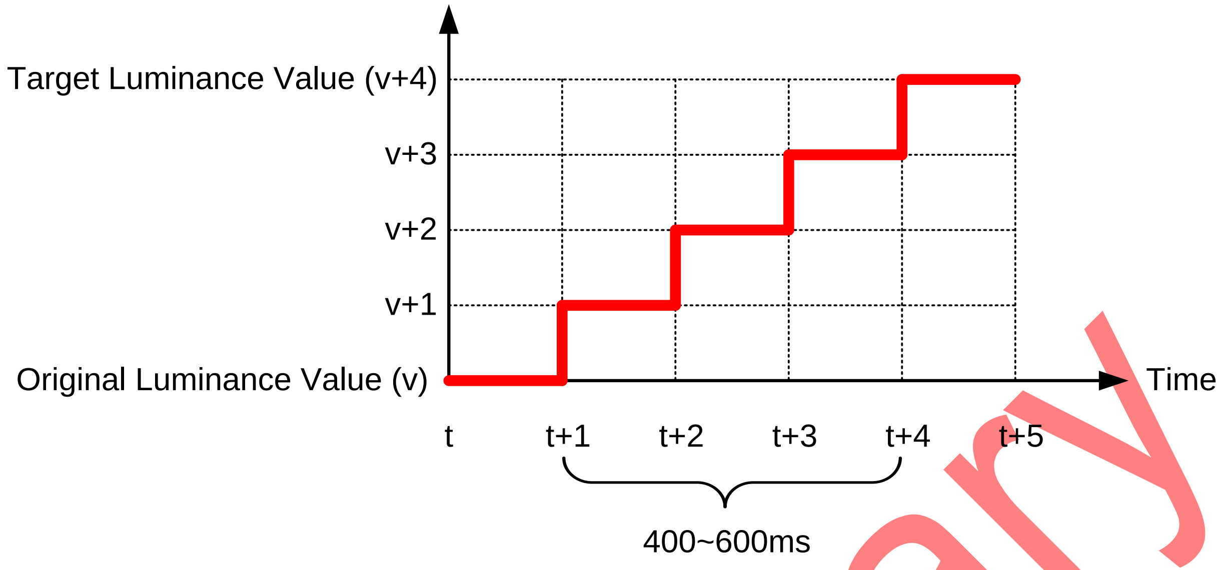
Dimming function can be enable and disable. See "Write CTRL Display (53h)" (bit DD) for more information.

8.21.2 Dimming Requirement

Dimming function in the display module should be implemented so that 400-600ms is used for the transition between the original brightness value and the target brightness value. The transferring time steps between these two brightness values are equal making the transition linear.

The dimming function is working similarly in both upward and downward directions.

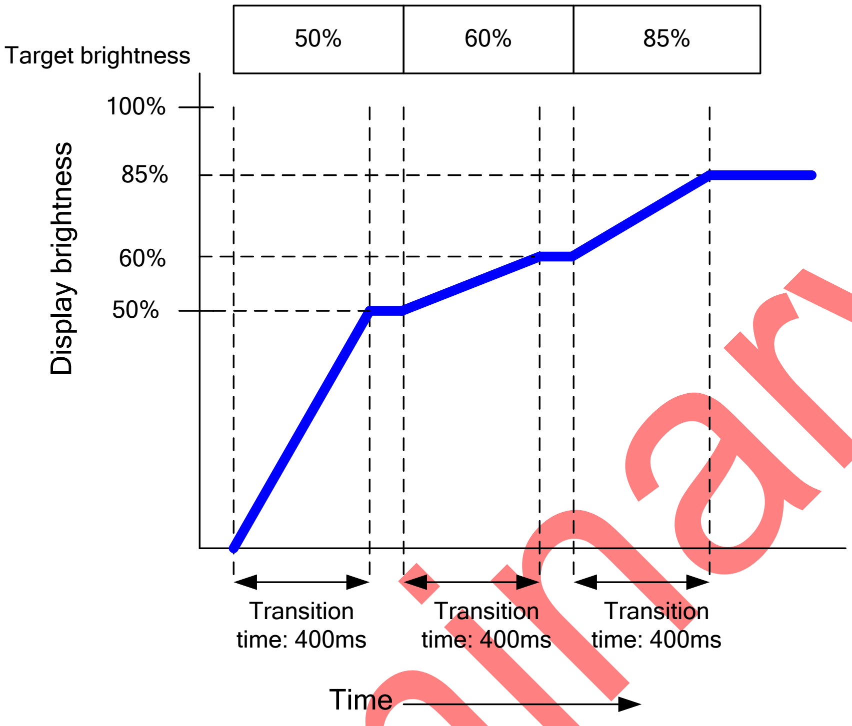
An upward example is illustrate below


Target Luminance Value (v+4)
v+3
v+2
v+1
Original Luminance Value (v)
Time
t
t+1
t+2
t+3
t+4
t+5
400~600ms

8.21.3 Definition of brightness transition time

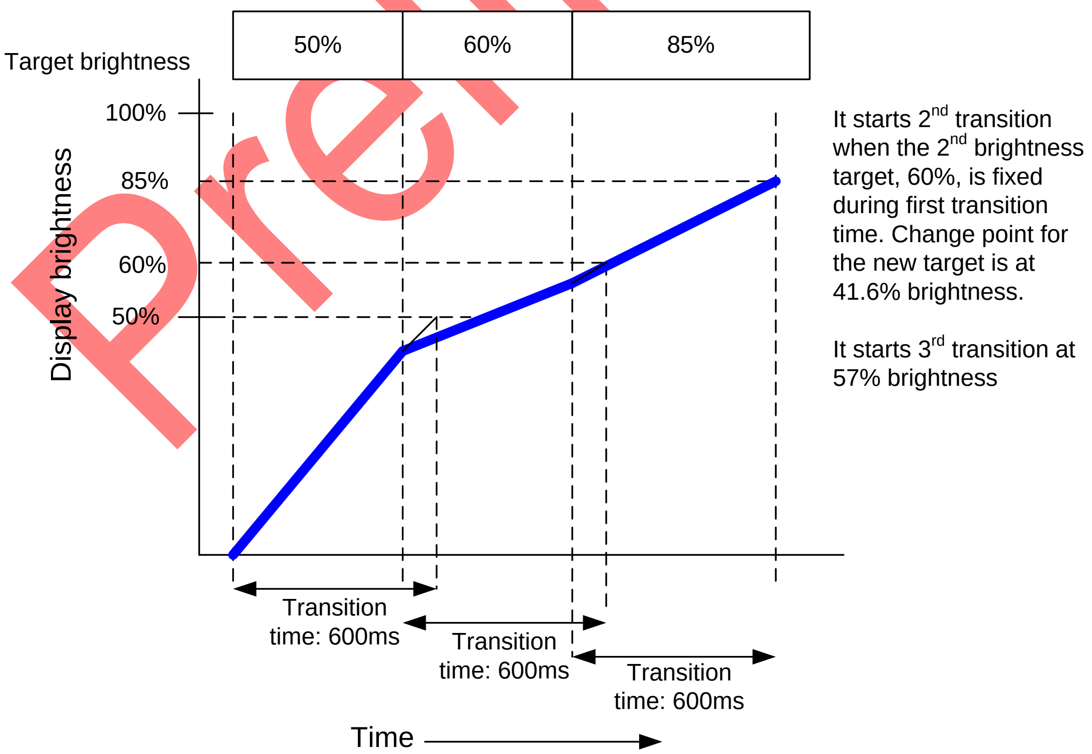
- Shorter transition time than 500ms.

There is some stable time between transitions. Below drawing is for transition time: 400ms.



- Longer transition time than 500ms

There is no any stable time between transitions. Below drawing is for transition time: 600ms.



8.22 Content Adaptive Brightness Control (CABC)

8.22.1 Definition of CABC

A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content gray level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted gray level scale and thus the power consumption reduction

Definition of Modes and target power reduction ratio:

- Off mode: Content Adaptive Brightness Control functionality is totally off.
- UI [User interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less.
- Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%.
- Moving image mode: Optimized for moving image. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%.

Note 1: Updating partial area of the image data should be supported by CABC functionality.
Note 2: Processing power consumption of CABC should be minimized.
Note 3: Customer need program OTP GAMMA when using CABC.

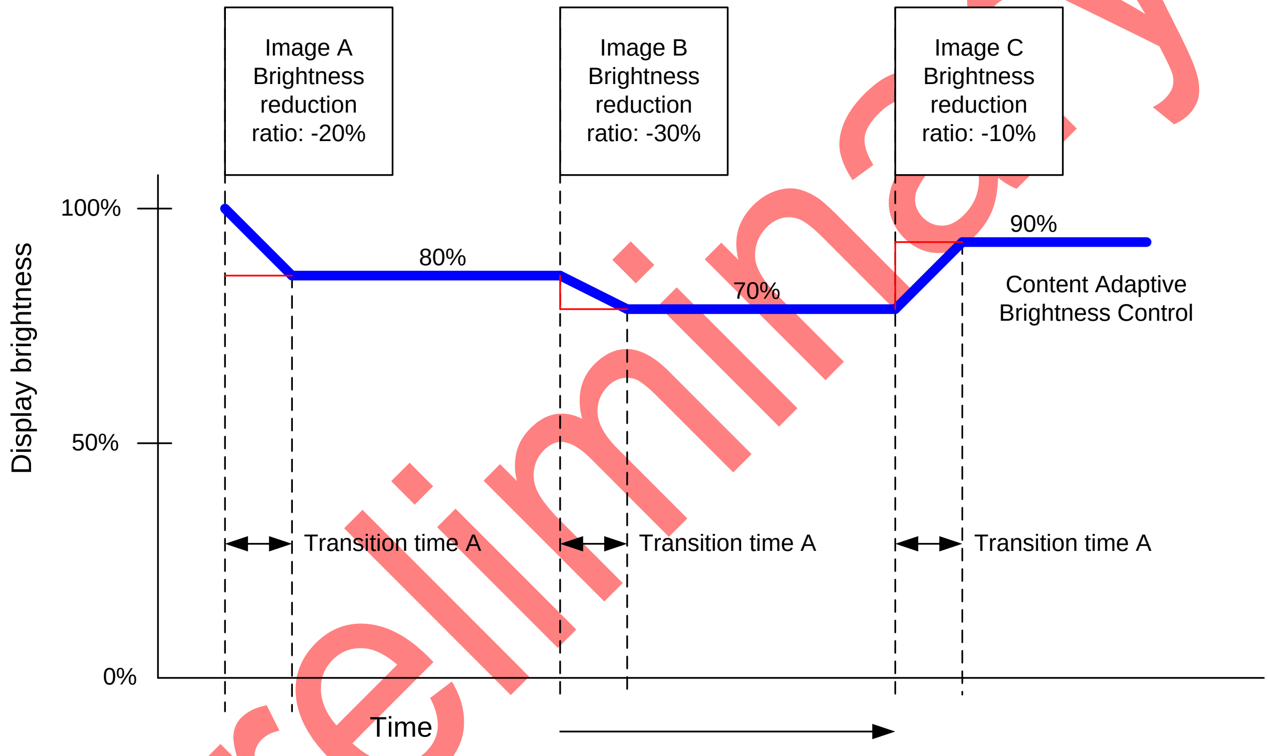
The transition time for dimming function is illustrated below.

- Content Adaptive Brightness Control

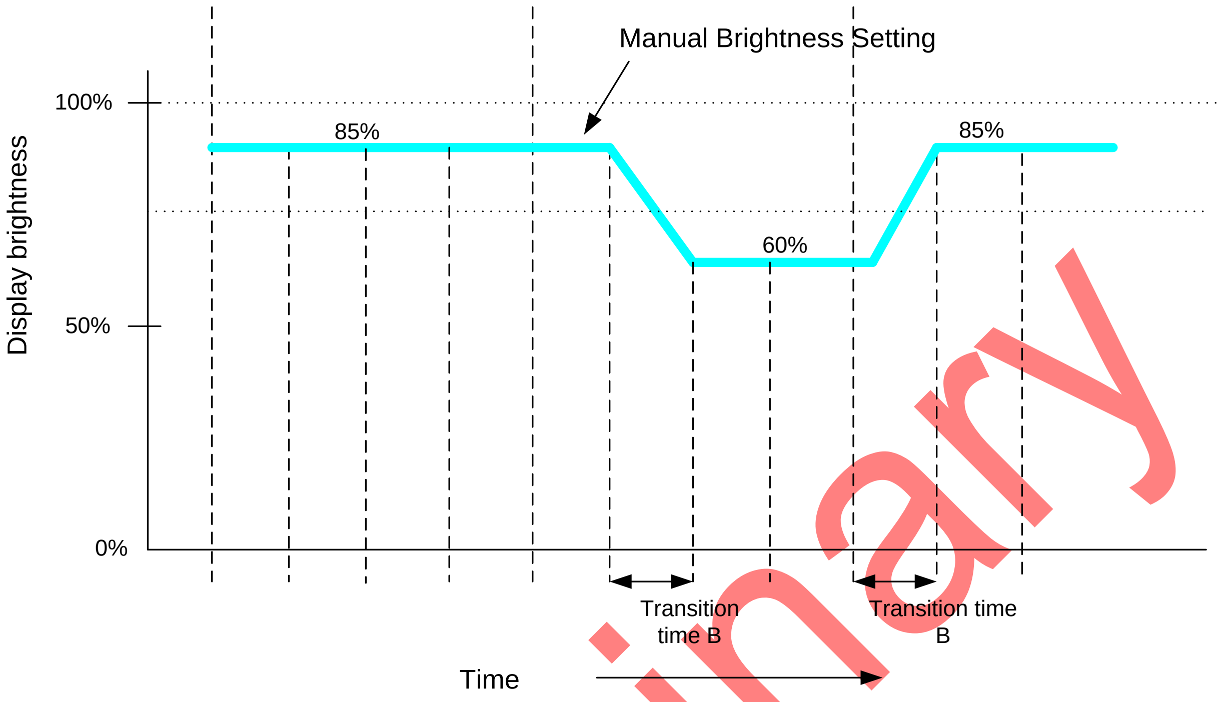
Display brightness is changed, according to the image contents. The following graph mentions the case of displaying three different images.

- Image A: -20% brightness reduction
- Image B: -30% brightness reduction
- Image C: -30% brightness reduction

Transition time from the previous image to the current displayed image is “transition time A”.



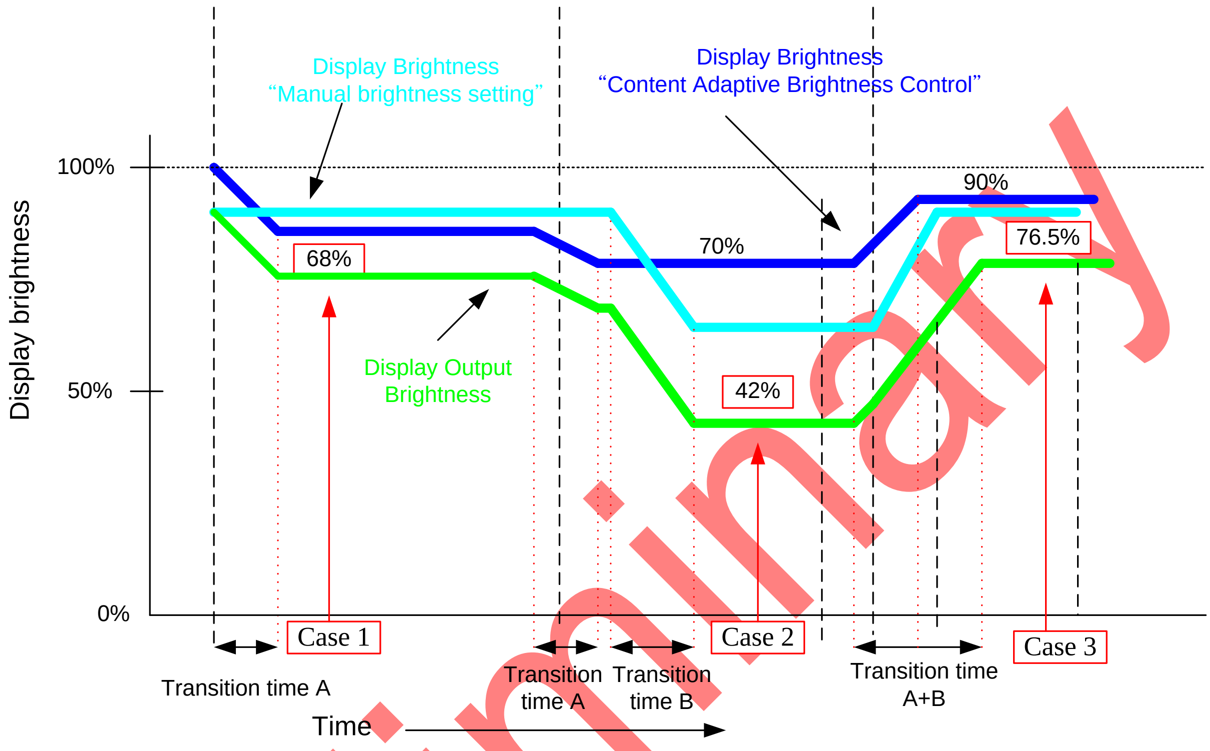
- Manual brightness setting and Dimming function



- Combine Display brightness

Green line in the following graph is for the output brightness of display. It is combined with both display brightness, which are defined in the above graphs.

Maximum transition time is transition time A+B.



Brightness level calculates with the following formula.

Display Output brightness = Manual Brightness setting * CABC brightness ratio

	Manual Brightness setting	Brightness ratio [CABC]	Display Output brightness
Case 1	85%	80%	68%
Case 2	60%	70%	42%
Case 3	85%	90%	76.5%

Transition time from the current brightness to target brightness is A+B in the worst case.

8.22.2 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the LABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting is to avoid too much brightness reduction. When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. If CABC algorithm works without any abnormal visual effect, image processing function can operate even when the brightness cannot be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

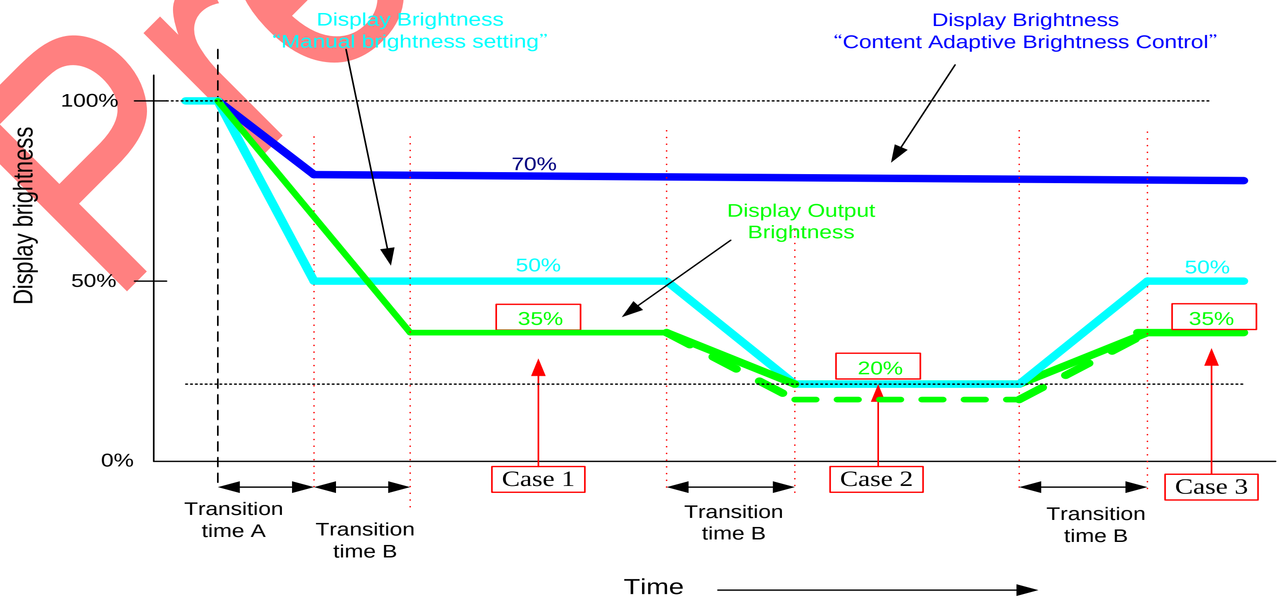
When display brightness is turned off (BCTRL=0 of "9.1.39 Write CTRL Display (53h)"), CABC minimum brightness setting is ignored. "9.1.44 Read CABC minimum brightness (5Fh)" always read the setting value of "9.1.43 Write CABC minimum brightness (5Eh)".

	WRCABC (55h)	Function	RDCABCMB (5Fh)	Image
Sleep-in		NA	WRCABCMB (5Eh)	
CABC off	00b	Disable	WRCABCMB (5Eh)	Original
CABC on	01b/10b/11b	Enable	WRCABCMB (5Eh)	CABC modified

Brightness level calculates with the following formula.

Display Output Brightness = Manual brightness setting * CABC brightness ratio

Below drawing is for the explanation of the CABC minimum brightness setting.



CABC minimum brightness value = 51 (33h: 20% display brightness)

	Display Brightness [manual setting]	Brightness ratio [CABC]	Calculation result of the display brightness formula	Display Output Brightness	Image
Case 1	50%	70%	35%	35%	CABC modified
Case 2	20%	70%	14%	20%	CABC modified
Case 3	50%	70%	35%	35%	CABC modified

At the case 2, the calculation result of the display brightness is 14%. CABC minimum brightness value is set to 20% brightness. Actual display brightness is 20% as the CABC minimum brightness setting.

9 COMMAND

9.1 System Function Command Table 1

Instruction	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No operation
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read display ID
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read display status
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
	1	1	↑	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
	1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read display power
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	0	0		
RDD MADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read display
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	MY	MX	MV	ML	RGB	MH	0	0		-
RDD COLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read display pixel
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0		-
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read display image
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	VSSON	0	INVON	0	0	GC2	GC1	GC0		-
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read display signal
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	TEON	TEM	0	0	0	0	0	0		-

Instruction	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read display self-diagnostic result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	0	0	0	0	0	0		-
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Display inversion on
	1	↑	1	-	0	0	0	0	GC3	GC2	GC1	GC0		
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: 0≦ XS≦ X
	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address start: S≦ XE≦ X
	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: 0≦ YS≦ Y
	1	↑	1		YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
	1	↑	1		YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address start: S≦ YE≦ Y
	1	↑	1		YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Read data

Instruction	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	Dx[8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial start/end address set
	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address: (0, 1,2, ..P)
	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0, 1,2, 3, , P)
	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Vertical scrolling definition
	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		
	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		
	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		
	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect line on
	1	↑	1	-	-	-	-	-	-	-	-	TEM		
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
	1	↑	1	-	MY	MX	MV	ML	RGB	0	0	0		-
VSCRSADD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Vertical scrolling start address
	1	↑	1	-	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8		
	1	↑	1	-	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0		
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
	1	↑	1	-	0	D6	D5	D4	0	D2	D1	D0		Interface format

Instruction	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
RAMWRC	0	↑	1	-	0	0	1	1	1	1	0	0	(3Ch)	Memory write continue
	1	↑	1	D1[8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRDC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)	Memory read continue
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	D1[8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		
	1	1	↑	Dx[8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
TESCAN	0	↑	1	-	0	1	0	0	0	1	0	0	(44h)	Set tear scanline
	1	↑	1	-	N15	N14	N13	N12	N11	N10	N9	N8		
	1	↑	1	-	N7	N6	N5	N4	N3	N2	N1	N0		
RDTESCAN	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)	Get scanline
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	-	-	-	-	-	-	N9	N8		
	1	1	↑	-	N7	N6	N5	N4	N3	N2	N1	N0		
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)	Write display brightness
	1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)	Read display brightness value
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)	Write CTRL display
	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0		
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)	Read CTRL value display
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0		
WRCACE	0	↑	1	-	0	1	0	1	0	1	0	1	(55h)	Write content adaptive brightness control and Color enhancement

Instruction	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	1	-	CECTRL	0	CE1	CE0	0	0	C1	C0		
RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	(56h)	Read content adaptive brightness control
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	CECTRL	0	0	0	0	C1	C0		
WRCABCMB	0	↑	1	-	0	1	0	1	1	1	1	0	(5Eh)	Write CABC minimum brightness
	1	↑	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDCABCMB	0	↑	1	-	0	1	0	1	1	1	1	1	(5Fh)	Read CABC minimum brightness
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDABCSDR	0	↑	1	-	0	1	1	0	1	0	0	0	(68h)	Read Automatic Brightness Control Self-Diagnostic Result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	0	0	0	0	0	0		-
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

Table 30 System Function Command List

Note1: 1. "-": Don't care

2. If host uses high speed mode in MIPI interface, please send one dummy byte before every parameter.

9.1.1 NOP (00h)

00H	NOP (No Operation)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-
Description	This command is empty command.												
Restriction													
Register Availability													
Default													
Flow Chart													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Note: "-"Don't care

9.1.2 SWRESET (01h): Software Reset

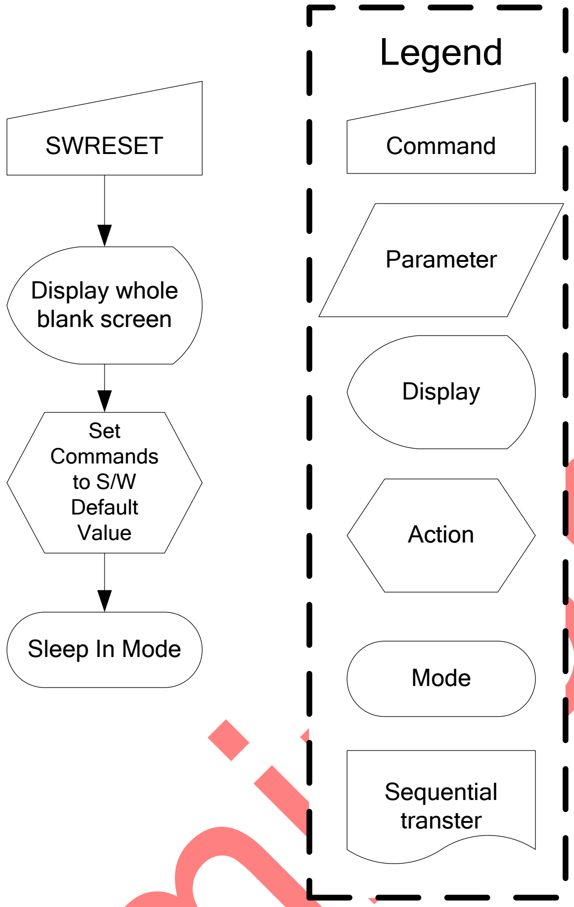
01H	SWRESET (Software Reset)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-
Description	"-" Don't care -The display module performs a software reset, registers are written with their SW reset default values. -Frame memory contents are unaffected by this command.												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5msec. If software reset is sent during sleep in mode, it will be necessary to wait 120msec before sending sleep out command. Software reset command cannot be sent during sleep out sequence.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	SWRESET Display whole blank screen Set Commands to S/W Default Value Sleep In Mode Legend Command Parameter Display Action Mode Sequential transter

9.1.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
3rd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
4th parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

Description

-This read byte returns 24-bit display identification information.

-The 1st parameter is dummy data

-The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID.

-The 3rd parameter (ID26 to ID20): LCD module/driver version ID

-The 4th parameter (ID37 to UD30): LCD module/driver ID.

-Commands RDID1/2/3(Dah, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.

"-" Don't care

Restriction

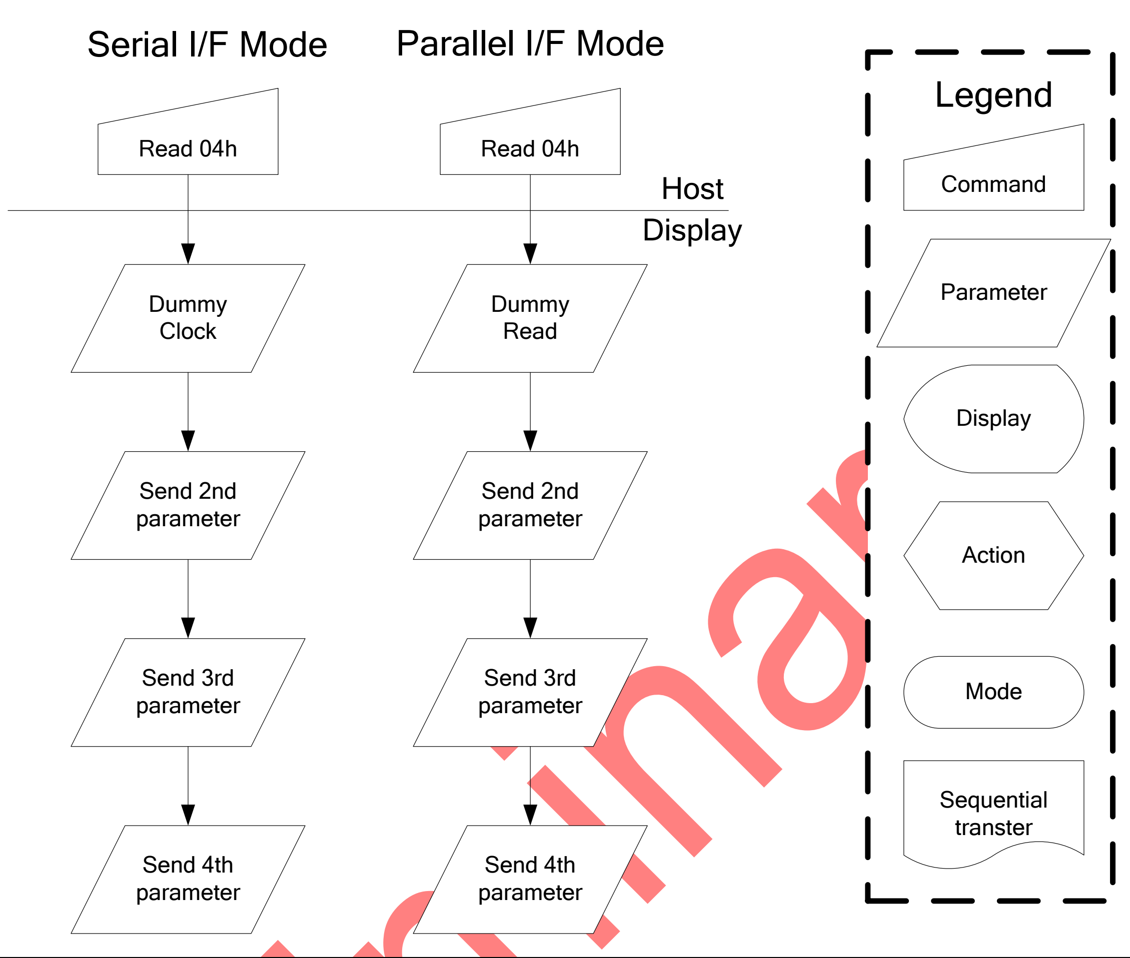
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	0x85	0x85	0x52
S/W Reset	0x85	0x85	0x52
H/W Reset	0x85	0x85	0x52

Flow Chart



Serial I/F Mode
Parallel I/F Mode
Read 04h
Read 04h
Host
Display
Dummy Clock
Dummy Read
Send 2nd parameter
Send 2nd parameter
Send 3rd parameter
Send 3rd parameter
Send 4th parameter
Send 4th parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.4 RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	
3rd parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	
4th parameter	1	1	↑	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	
5th parameter	1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	‘1’ =Booster on, ‘0’ =Booster off
MY	Row Address Order (MY)	‘1’ =Decrement, (Bottom to Top, when MADCTL (36h) D7=’1’) ‘0’ =Increment, (Top to Bottom, when MADCTL (36h) D7=’0’)
MX	Column Address Order (MX)	‘1’ =Decrement, (Right to Left, when MADCTL (36h) D6=’1’) ‘0’ =Increment, (Left to Right, when MADCTL (36h) D6=’0’)
MV	Row/Column Exchange (MV)	‘1’ = Row/column exchange, (when MADCTL (36h) D5=’1’) ‘0’ = Normal, (when MADCTL (36h) D5=’0’
ML	Scan Address Order (ML)	‘0’ =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4=’0’) ‘1’=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4=’1’)
RGB	RGB/ BGR Order (RGB)	‘1’ =BGR, (When MADCTL (36h) D3=’1’) ‘0’ =RGB, (When MADCTL (36h) D3=’0’)
MH	Horizontal Order	‘0’ =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2=’0’) ‘1’ =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2=’1’)
ST24	For Future Use	‘0’
ST23	For Future Use	‘0’
IFPF2 IFPF1 IFPF0	Interface Color Pixel Format Definition	“011” = 12-bit / pixel, “101” = 16-bit / pixel, “110” = 18-bit / pixel, “111” = 16M truncated, others are not defined.
IDMON	Idle Mode On/Off	‘1’ = On, “0” = Off
PTLON	Partial Mode On/Off	‘1’ = On, “0” = Off
SLPOUT	Sleep In/Out	‘1’ = Out, “0” = In

NORON	Display Normal Mode On/Off	‘1’ = Normal Display, ‘0’ = Partial Display
ST15	Vertical Scrolling Status (Not Used)	‘1’ = Scroll on,“0” = Scroll off
ST14	Horizontal Scroll Status (Not Used)	‘0’
INVON	Inversion Status	‘1’ = On, “0” = Off
ST12	All Pixels On (Not Used)	‘0’
ST11	All Pixels Off (Not Used)	‘0’
DISON	Display On/Off	‘1’ = On, “0” = Off
TEON	Tearing effect line on/off	‘1’ = On, “0” = Off
GCSEL2 GCSEL1 GCSEL0	Gamma Curve Selection	“000” = GC0 “001” = GC1 “010” = GC2 “011” = GC3 ”100” to “111” = Not defined
TEM	Tearing effect line mode	‘0’ = mode1, ‘1’ = mode2
ST4	For Future Use	‘0’
ST3	For Future Use	‘0’
ST2	For Future Use	‘0’
ST1	For Future Use	‘0’
ST0	For Future Use	‘0’

“-“ Don’t care

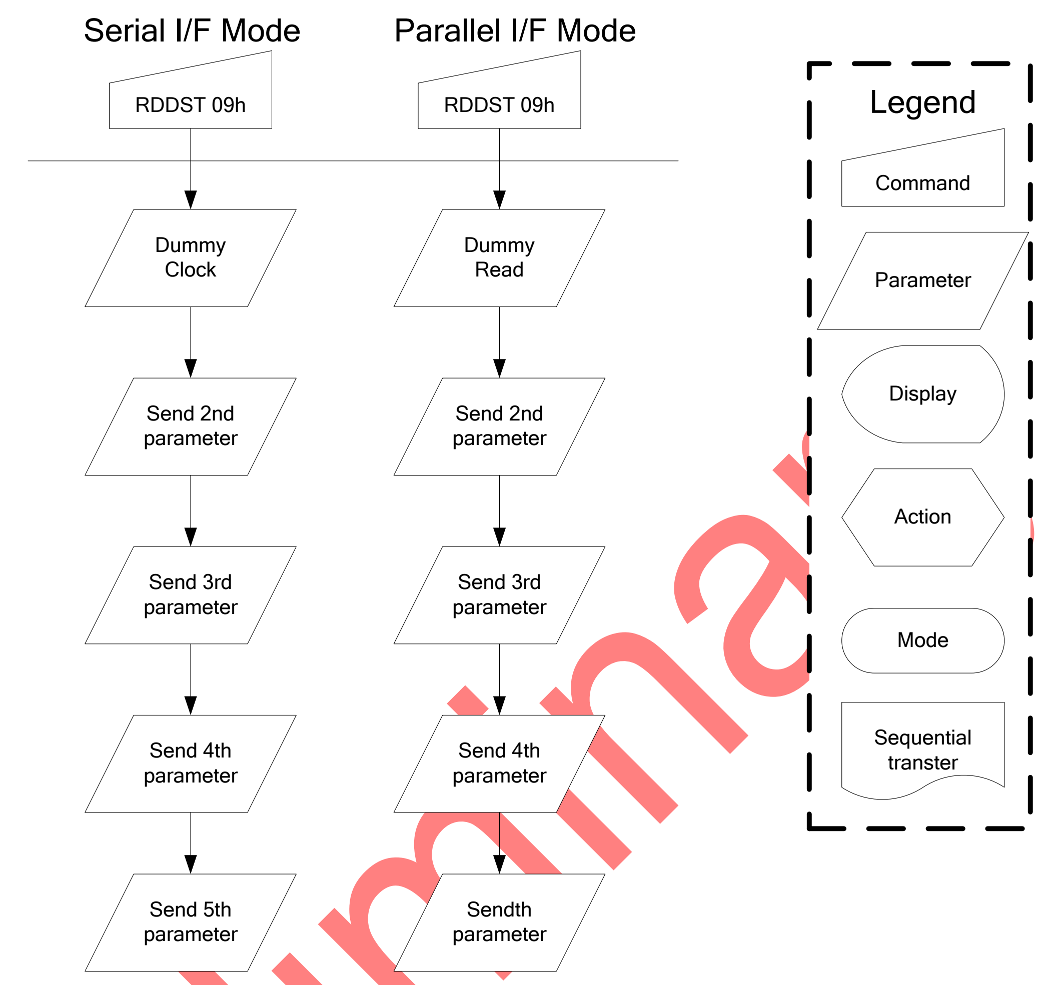
Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (ST31 to ST0)			
	ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]
Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
S/W Reset	0xxx-xx00	0xxx-0001	0000-0000	0000-0000
H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000

Flow Chart	

Serial I/F Mode
Parallel I/F Mode
RDDST 09h
RDDST 09h
Dummy Clock
Dummy Read
Send 2nd parameter
Send 2nd parameter
Send 3rd parameter
Send 3rd parameter
Send 4th parameter
Send 4th parameter
Send 5th parameter
Sendth parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.5 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
IDMON	Idle mode on/off	'1' = Idle Mode On, '0' = Idle Mode Off
PTLON	Partial mode on/off	'1' =Partial mode on, '0' =Partial mode off,
SLPOUT	Sleep in/out	'1' =Sleep out, '0' =Sleep in,
NORON	Display normal mode on/off	'1' = Normal display, '0' = Partial display,
DISON	Display on/off	'1' =Display on, '0' =Display off,
D1	Not Used	"0"
D0	Not Used	"0"

"-" Don't care

Restriction

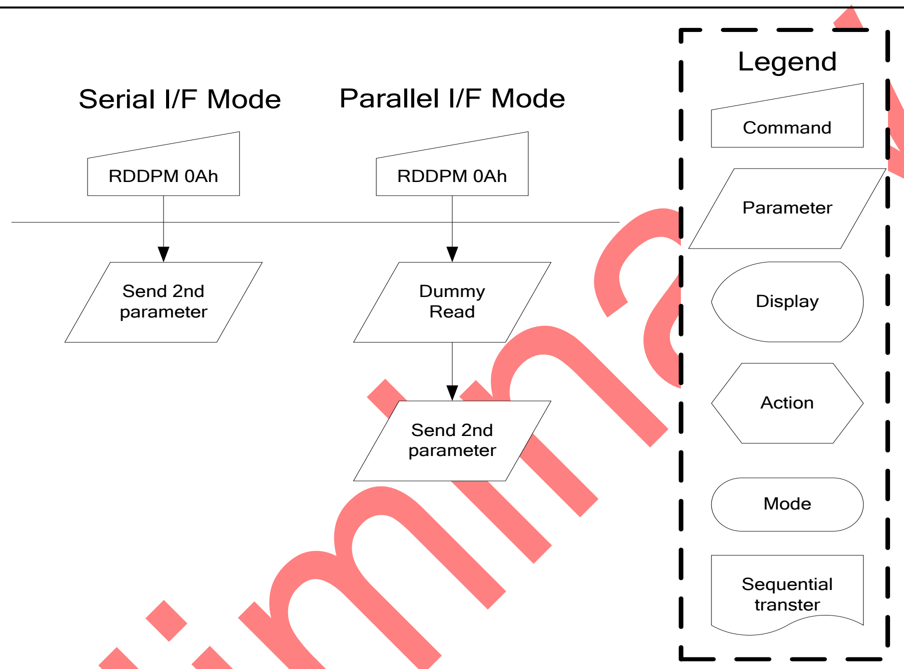
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

<table>
<tr><td>Default</td><td>

Status	Default Value (D7 to D0)
Power On Sequence	0000-1000(08h)
S/W Reset	0000-1000(08h)
H/W Reset	0000-1000(08h)

</td></tr>
<tr><td>Flow Chart</td><td>



</td></tr>
</table>

9.1.6 RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	MY	MX	MV	ML	RGB	MH	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

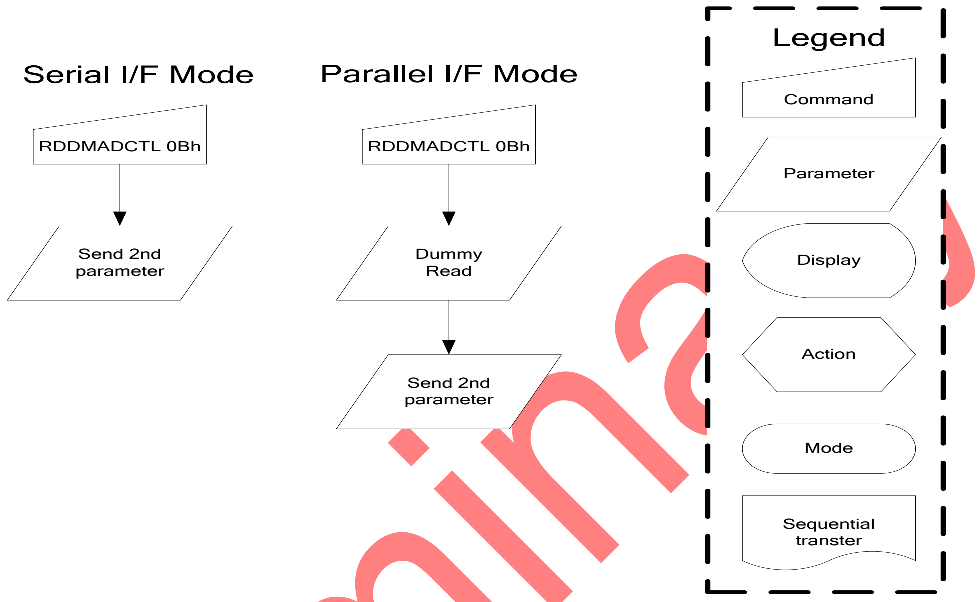
Bit	Description	Value
MY	Row Address Order (MY)	‘1’ =Decrement, (Bottom to Top, when MADCTL (36h) D7=’1’) ‘0’ =Increment, (Top to Bottom, when MADCTL (36h) D7=’0’)
MX	Column Address Order (MX)	‘1’ =Decrement, (Right to Left, when MADCTL (36h) D6=’1’) ‘0’ =Increment, (Left to Right, when MADCTL (36h) D6=’1’)
MV	Row/Column Exchange (MV)	‘1’ = Row/column exchange, (when MADCTL (36h) D5=’1’) ‘0’ = Normal, (when MADCTL (36h) D5=’0’
ML	Scan Address Order (ML)	‘0’ =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4=’0’) ‘1’=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4=’1’)
RGB	RGB/ BGR Order (RGB)	‘1’ =BGR, (When MADCTL (36h) D3=’1’) ‘0’ =RGB, (When MADCTL (36h) D3=’0’)
MH	Horizontal Order	‘0’ =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2=’0’) ‘1’ =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2=’1’)
D1	Not used	‘0’
D0	Not used	‘0’

“-“ Don’t care

Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>0000-0000 (00h)</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>0000-0000 (00h)</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

9.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format

0CH	RDDCOLMOD (Read Display Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	-	Set to '0'
D6	RGB interface color format	'101' = 16 bit/pixel '110' = 18 bit/pixel
D5		
D4		
D3	-	Set to '0'
D2	Control interface color format	'101' = 16 bit/pixel '110' = 18 bit/pixel
D1		
D0		

Others are no define and invalid

"-" Don't care

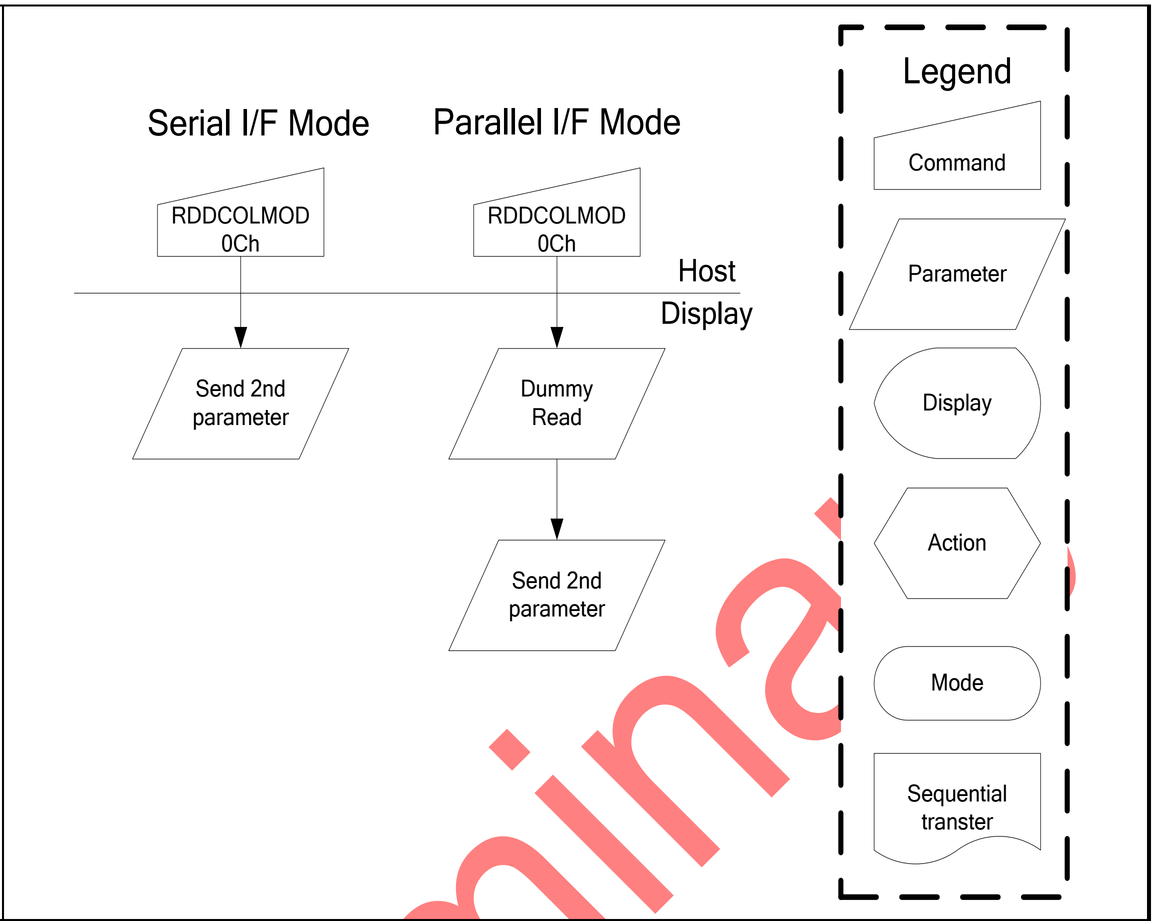
Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0110 (18 bit/pixel)
S/W Reset	No change
H/W Reset	0000-0110 (18 bit/pixel)

Flow Chart	

Serial I/F Mode
Parallel I/F Mode
RDDCOLMOD 0Ch
RDDCOLMOD 0Ch
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.8 RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	VSSON	0	INVON	0	0	GC2	GC1	GC0	

Description

This command indicates the current status of the display as described in the table below:

-VSSON: Vertical scrolling on/off

-INVON: Inversion on/off

Gamma Curve Selection	GC2	GC1	GC0	Gamma set (26h) Parameter
Gamma curve 1	0	0	0	GC0
Gamma curve 2	0	0	1	GC1
Gamma curve 3	0	1	0	GC2
Gamma curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Others are no define and invalid

"-" Don't care

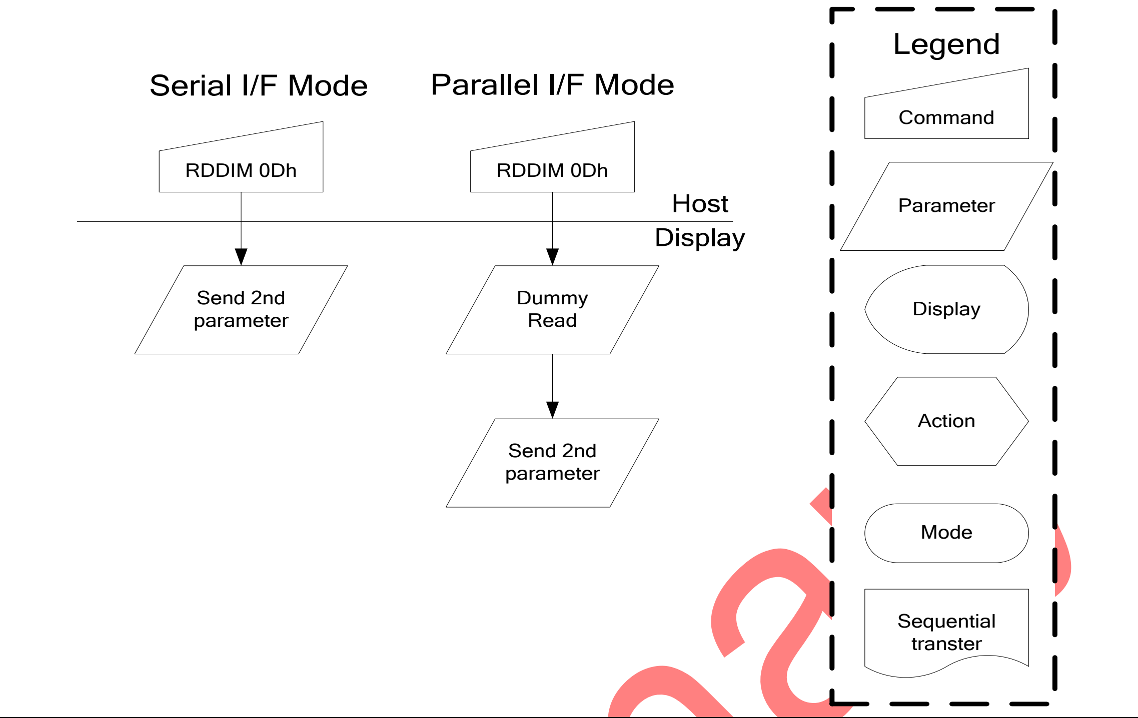
Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

Flow Chart	

Serial I/F Mode
Parallel I/F Mode
RDDIM 0Dh
RDDIM 0Dh
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.9 RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Status)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	TEON	TEM	0	0	0	0	0	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing effect line on/off	'1' = ON, '0' = OFF,
TEM	Tearing effect line mode	'1' = mode2, '0' = mode1,

"-" Don't care

Restriction

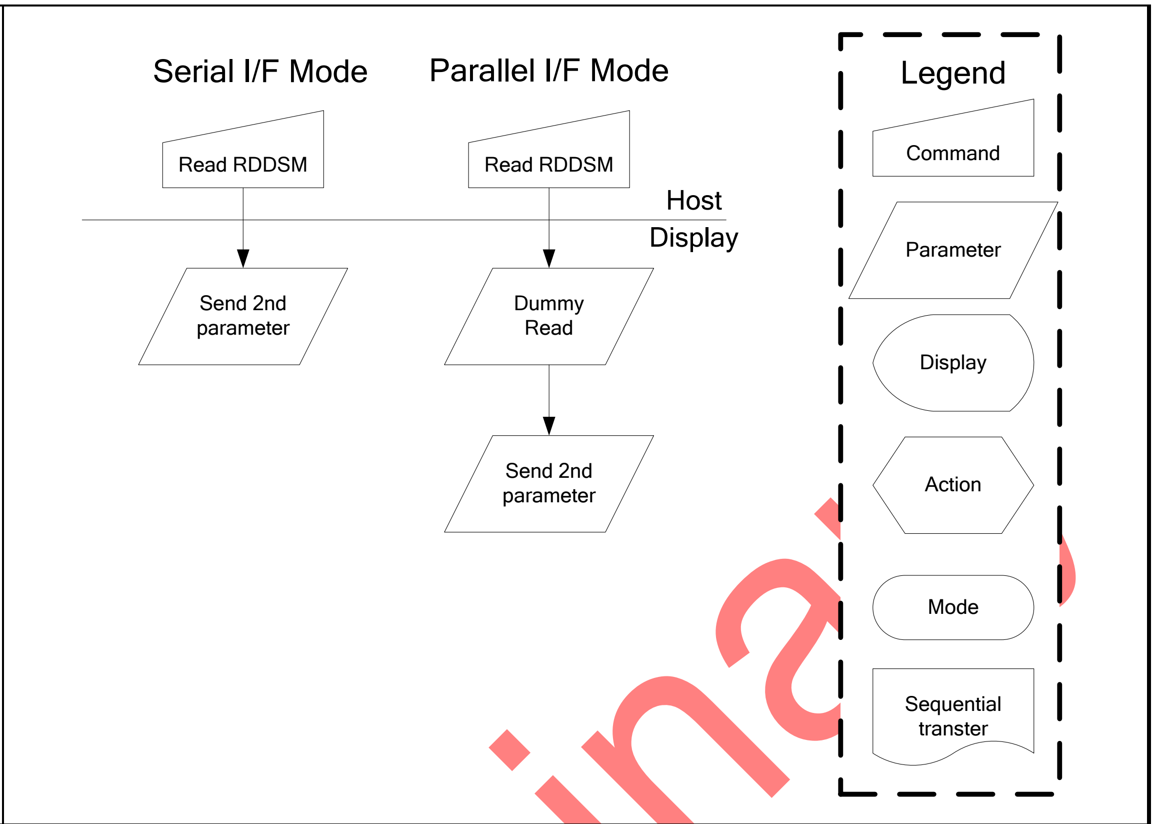
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

Flow Chart



Serial I/F Mode
Parallel I/F Mode
Read RDDSM
Read RDDSM
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.10 RDDSDR (0Fh): Read Display Self-Diagnostic Result

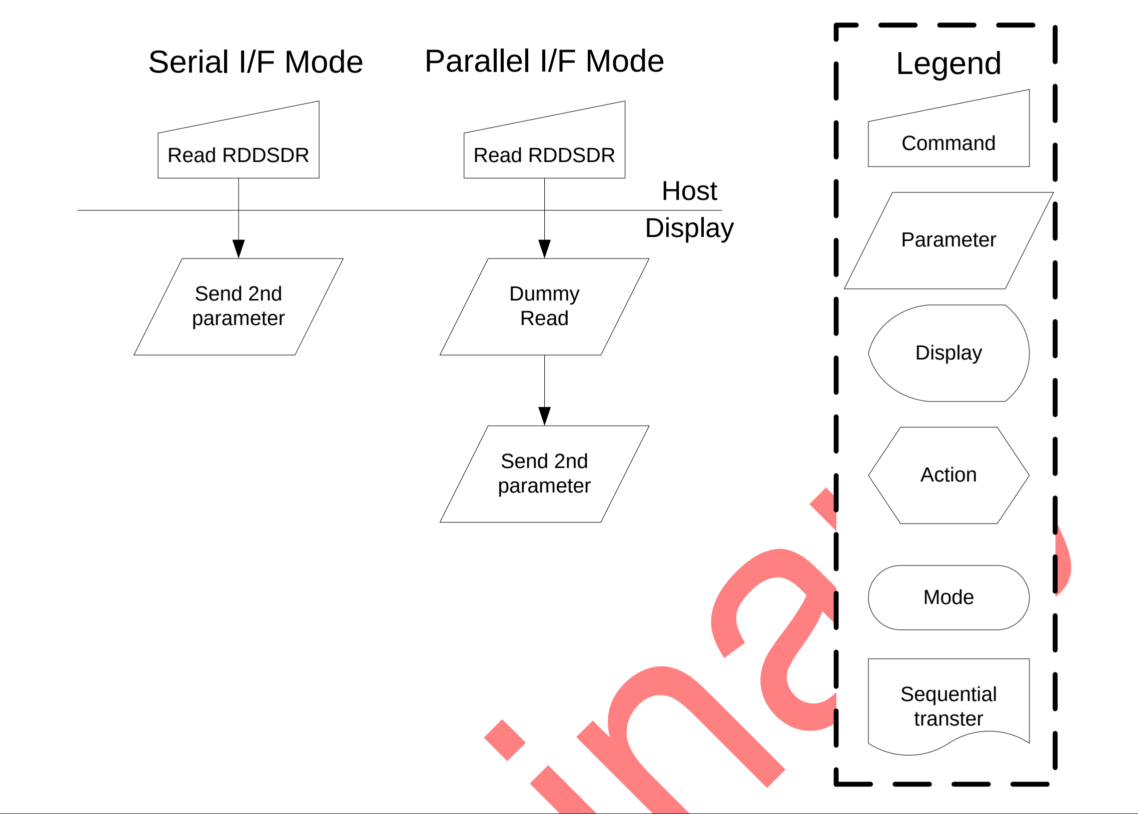
09H	RDDSDR (Read Display Self-Diagnostic Result)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	0	0	0	0	0	0	-
Description	This command indicates the current status of the display self-diagnostic result after sleep out command as described below: -D7: Register loading detection -D6: Functionality detection "-" Don't care												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

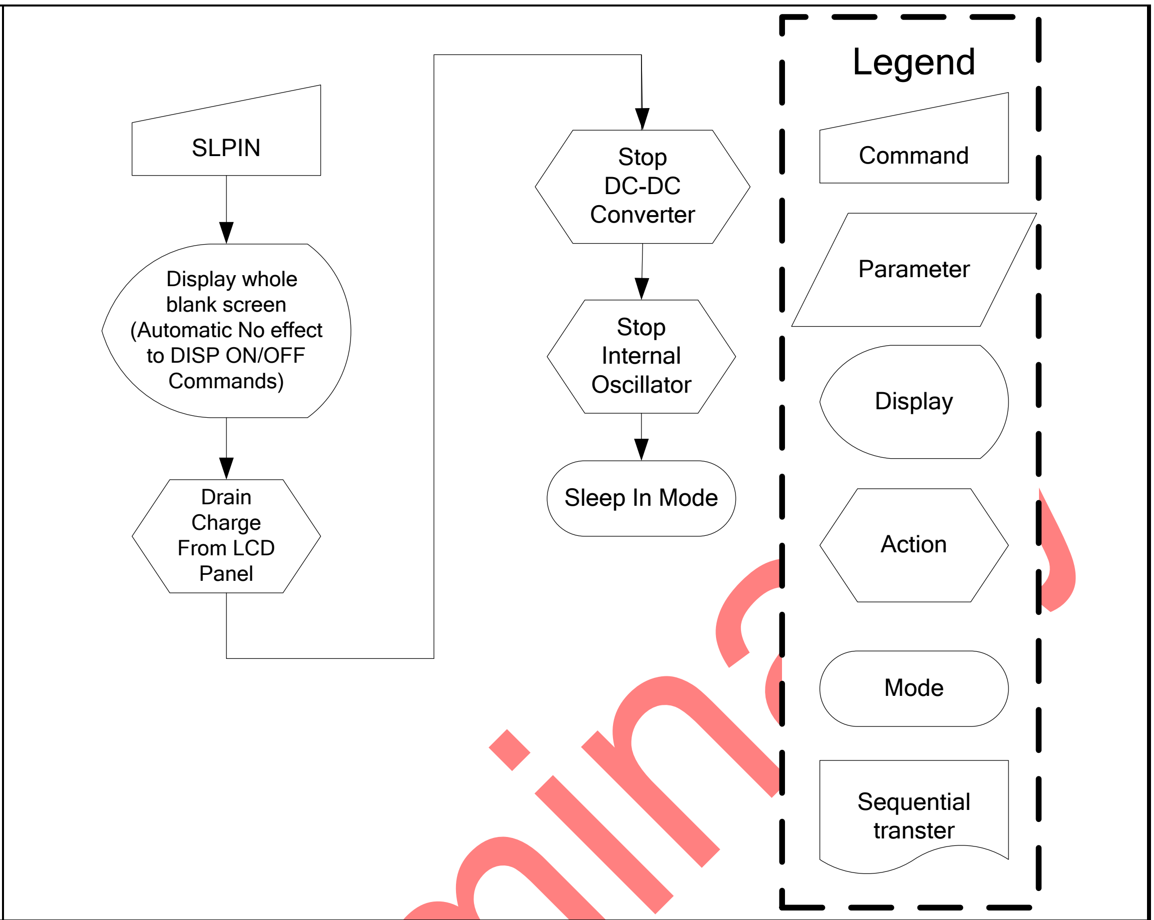
Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

Flow Chart	

Serial I/F Mode
Parallel I/F Mode
Read RDDSDR
Read RDDSDR
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.11 SLPIN (10h): Sleep in

<table>
<tr><td>10H</td><td colspan="13">SLPIN (Sleep In)</td></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>SLPIN</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>(10h)</td></tr>
<tr><td>parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">-This command causes the LCD module to enter the minimum power consumption mode.
-In this mode the DC/DC converter is stopped, internal oscillator is stopped, and panel scanning is stopped.
-MCU interface and memory are still working and the memory keeps its contents.
“-“ Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">-This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h).
-It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize.
-It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.</td></tr>
<tr><td>Register availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep in mode</td></tr><tr><td>S/W Reset</td><td>Sleep in mode</td></tr><tr><td>H/W Reset</td><td>Sleep in mode</td></tr></table></td></tr>
</table>

Flow Chart	

SLPIN
Display whole blank screen (Automatic No effect to DISP ON/OFF Commands)
Drain Charge From LCD Panel
Stop DC-DC Converter
Stop Internal Oscillator
Sleep In Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.12 SLPOUT (11h): Sleep Out

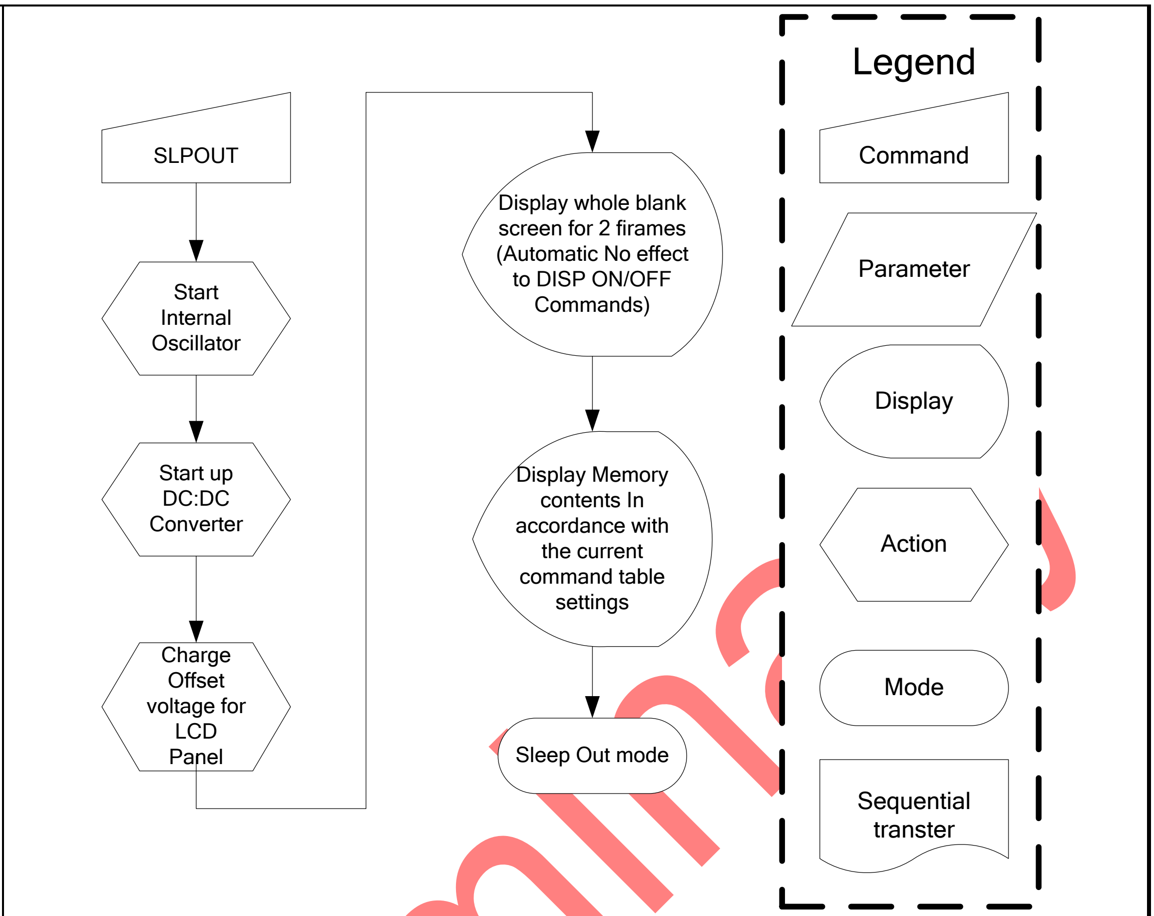
11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
parameter	No Parameter												
Description	-This command turn off sleep mode. -In this mode the DC/DC converter is enable, internal display oscillator is started, and panel scanning is started.												
Restriction	-This command has no effect when module is already in sleep out mode. Sleep out mode can only be left by the sleep in command (10h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command. -The display module runs the self-diagnostic functions after this command is received.												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart	

SLPOUT
Start Internal Oscillator
Start up DC:DC Converter
Charge Offset voltage for LCD Panel
Display whole blank screen for 2 firames (Automatic No effect to DISP ON/OFF Commands)
Display Memory contents In accordance with the current command table settings
Sleep Out mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.13 PTLON (12h): Partial Display Mode On

12H	PTLON (Partial Display Mode On)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
parameter	No Parameter												
Description	-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h) -To leave Partial mode, the Normal Display Mode On command (13h) should be written. "-" Don't care												
Restriction	This command has no effect when partial mode is active.												
Register availability	(see table below)												
Default	(see table below)												
Flow Chart	See Partial Area (30h)												

Register availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	Normal display mode on
S/W Reset	Normal display mode on
H/W Reset	Normal display mode on

9.1.14 NORON (13h): Normal Display Mode On

12H	NORON (Normal Display Mode On)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)
parameter	No Parameter												
Description	-This command turns the display to normal mode. -Normal display mode on means partial mode off. -Exit from NORON by the partial mode on command. "-" Don't care												
Restriction	This command has no effect when normal display mode is active.												
Register availability	(see table below)												
Default	(see table below)												
Flow Chart	See partial area description for details of when to use this command.												

Register availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

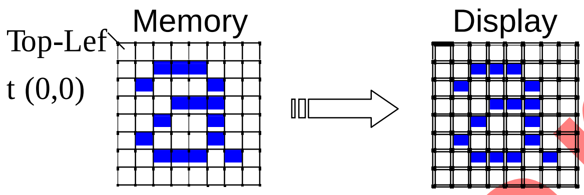
Default:

Status	Default Value
Power On Sequence	Normal display mode on
S/W Reset	Normal display mode on
H/W Reset	Normal display mode on

9.1.15 INVOFF (20h): Display Inversion Off

20H	INVOFF (Display Inversion Off)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
parameter	No Parameter												
Description	-This command is used to recover from display inversion mode. "-" Don't care												
Restriction	This command has no effect when module is already in inversion off mode.												

(Example)

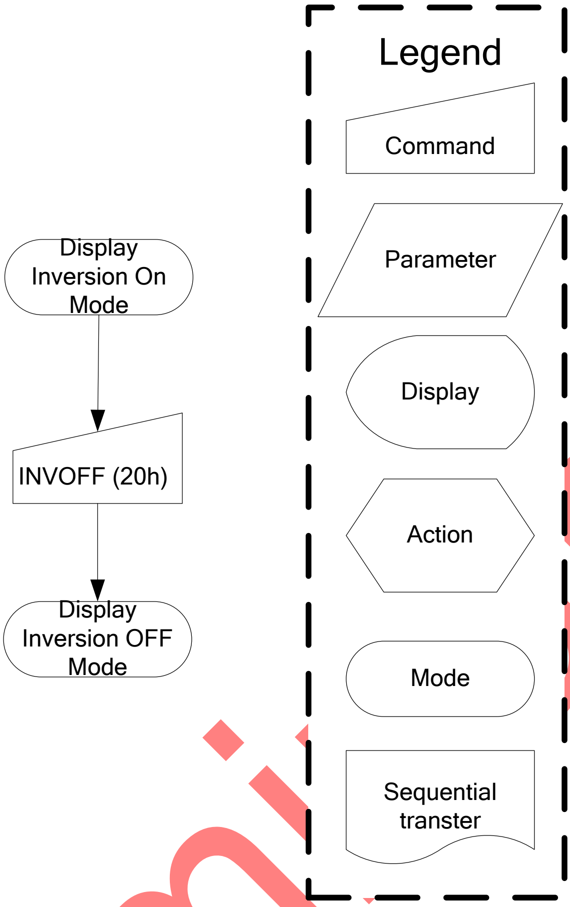


Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

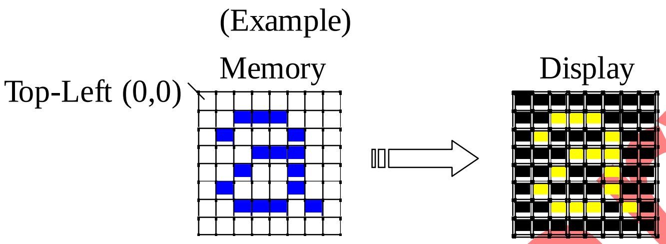
Default

Status	Default Value
Power On Sequence	Display inversion off
S/W Reset	Display inversion off
H/W Reset	Display inversion off

Flow Chart	Display Inversion On Mode INVOFF (20h) Display Inversion OFF Mode Legend Command Parameter Display Action Mode Sequential transter

9.1.16 INVON (21h): Display Inversion On

21H	INVON (Display Inversion On)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
parameter	No Parameter												
Description	-This command is used to recover from display inversion mode. "-" Don't care												
Restriction	This command has no effect when module is already in inversion on mode.												

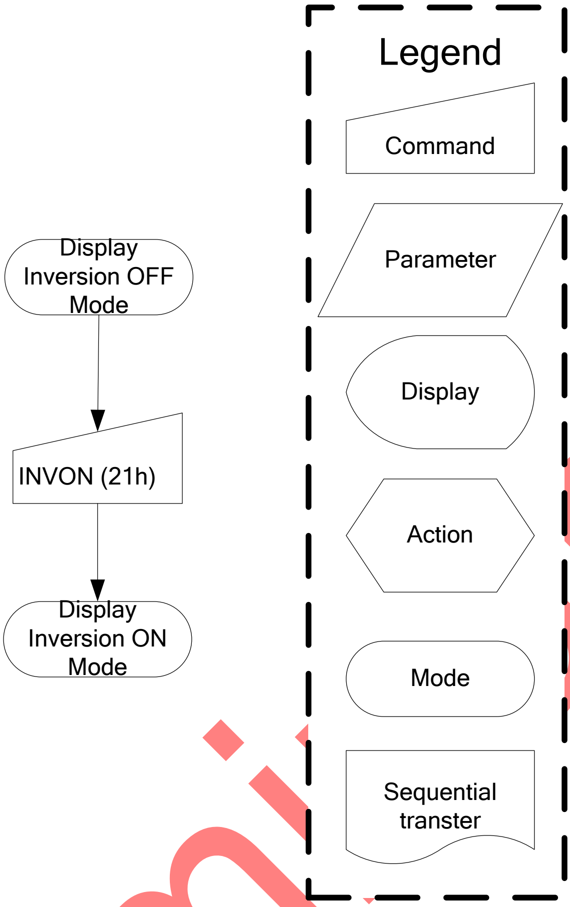


Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display inversion off
S/W Reset	Display inversion off
H/W Reset	Display inversion off

Flow Chart	

Display Inversion OFF Mode
INVON (21h)
Display Inversion ON Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.17 GAMSET (26h): Gamma Set

26H	GAMSET (Gamma Set)												
Inst / Para	D/CX	WRX	RDX	D18	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)
parameter	1	↑	1	-	0	0	0	0	GC3	GC2	GC1	GC0	

1. Description

-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC [7:0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1 (G2.2)
02h	GC1	Gamma Curve 2 (G1.8)
04h	GC2	Gamma Curve 3 (G2.5)
08h	GC3	Gamma Curve 4 (G1.0)

Note: All other values are undefined.

Restriction

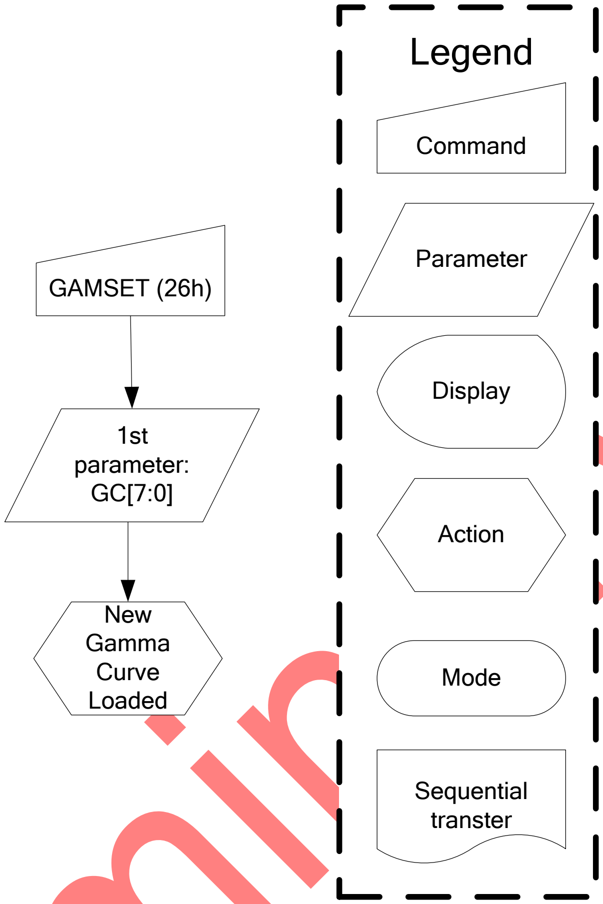
Values of GC[7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0x01
S/W Reset	0x01
H/W Reset	0x01

<table>
<tr><td>Flow Chart</td><td>
</td></tr>
</table>

9.1.18 DISPOFF (28h): Display Off

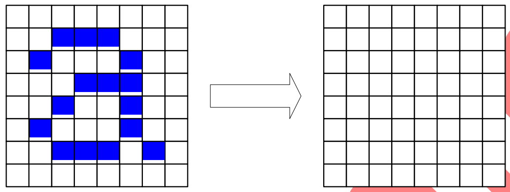
28H	DISPOFF (Display Off)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
parameter	No Parameter												

Description

- This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.
- This command makes no change of contents of frame memory.
- This command does not change any other status.
- There will be no abnormal visible effect on the display.
- Exit from this command by Display On (29h)

(Example)

Memory **Display**



Restriction

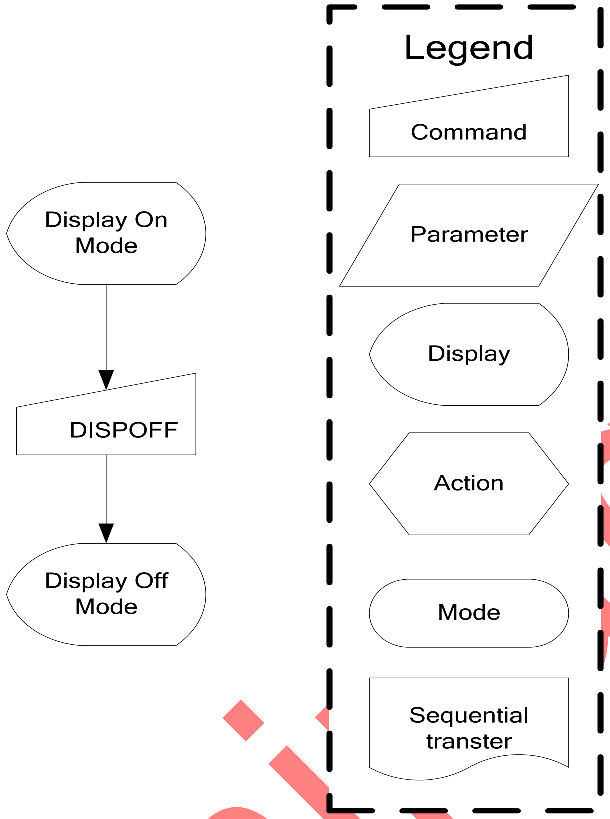
This command has no effect when module is already in display off mode.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart	Display On Mode DISPOFF Display Off Mode Legend Command Parameter Display Action Mode Sequential transter

9.1.19 DISPON (29h): Display On

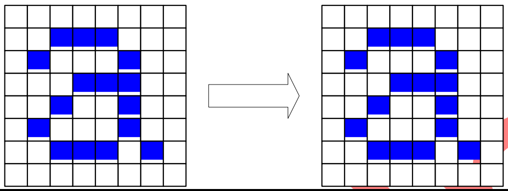
29H	DISPON (Display On)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
parameter	No Parameter												

Description

- This command is used to recover from DISPLAY OFF mode.
- Output from the Frame Memory is enabled.
- This command makes no change of contents of frame memory.
- This command does not change any other status.

(Example)

Memory **Display**



Restriction

This command has no effect when module is already in display on mode.

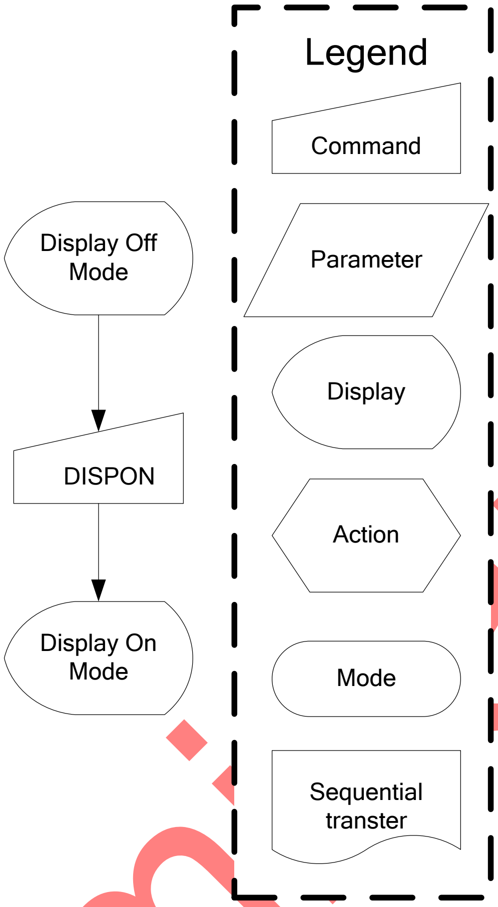
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart


Display Off Mode
DISPON
Display On Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

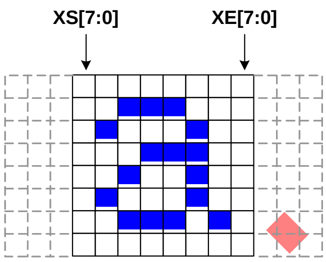
9.1.20 CASET (2Ah): Column Address Set

2AH	CASET (Column Address Set)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)
1st parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
2nd parameter	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
3rd parameter	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
4th parameter	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

2. Description

-The value of XS [7:0] and XE [7:0] are referred when RAMWR command comes.

-Each value represents one column line in the Frame Memory.



Restriction

XS [15:0] always must be equal to or less than XE [15:0]

When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.

(Parameter range: 0 < XS [15:0] < XE [15:0] < 239 (00Efh)): MV="0")

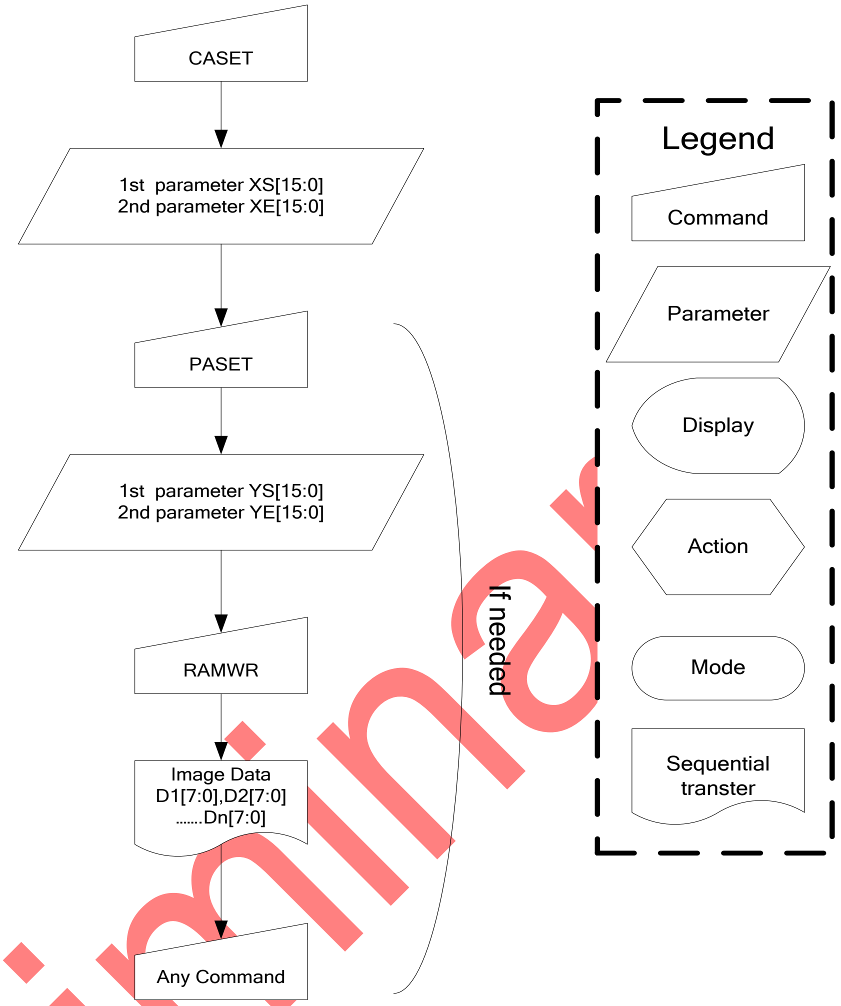
(Parameter range: 0 < XS [15:0] < XE [15:0] < 319 (013Fh)): MV="1")

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	XS[15:0]=0x00	XE[15:0]=0Xef
S/W Reset	XS[15:0]=0x00	When MV=0: XE[15:0]=00Efh, When MV=1: XE[15:0]=013Fh
H/W Reset	XS[15:0]=0x00	XE[15:0]=0Xef

Flow Chart	

CASET
1st parameter XS[15:0]
2nd parameter XE[15:0]
PASET
1st parameter YS[15:0]
2nd parameter YE[15:0]
RAMWR
Image Data
D1[7:0],D2[7:0]
.......Dn[7:0]
Any Command
If needed
Legend
Command
Parameter
Display
Action
Mode
Sequential
transter

9.1.21 RASET (2Bh): Row Address Set

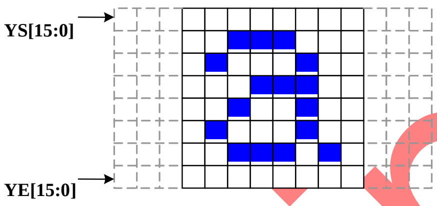
2BH	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
2nd parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
3rd parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
4th parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

3. Description

-This command is used to defined area of frame memory where MCU can access.

-The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes.

-Each value represents one page line in the Frame Memory.



Restriction

YS [15:0] always must be equal to or less than YE [15:0]

When YS [15:0] or YE [15:0] is greater than maximum address like below, data of out of range will be ignored.

(Parameter range: 0 < YS [15:0] < YE [15:0] < 239 (00Efh)): MV="0")

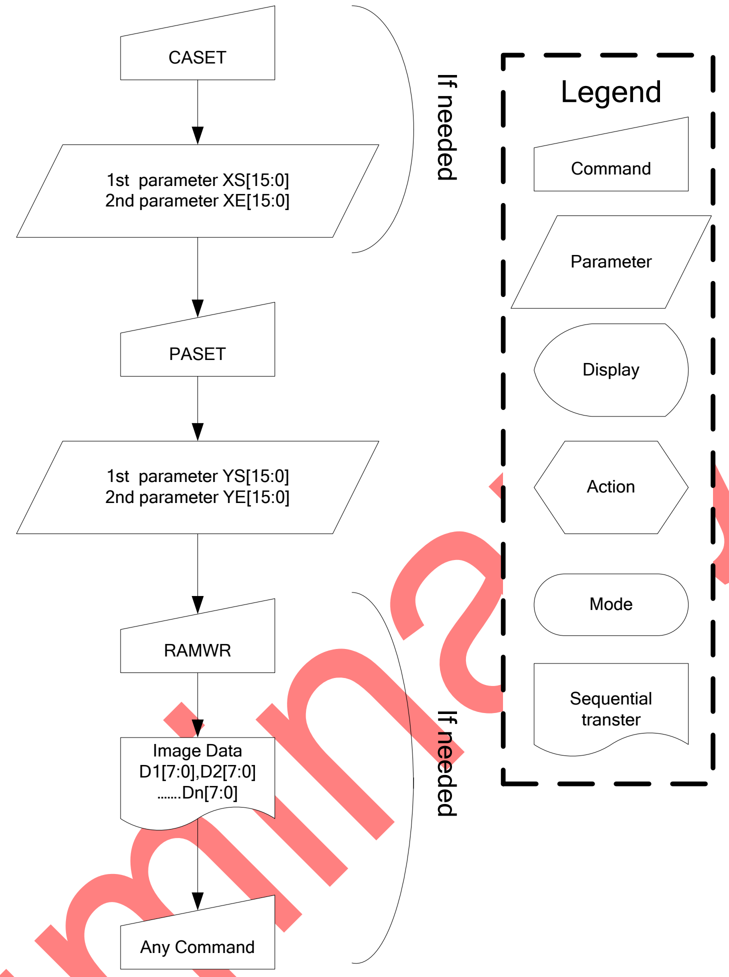
(Parameter range: 0 < YS [15:0] < YE [15:0] < 319 (013Fh)): MV="1")

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	YS[15:0]=0000h	YE[15:0]=013Fh
S/W Reset	YS[15:0]=0000h	When MV=0: YE[15:0]=013Fh, When MV=1: YE[15:0]=00Efh
H/W Reset	YS[15:0]=0000h	YE[15:0]=013Fh

Flow Chart	

CASET
1st parameter XS[15:0]
2nd parameter XE[15:0]
PASET
1st parameter YS[15:0]
2nd parameter YE[15:0]
RAMWR
Image Data
D1[7:0],D2[7:0]
.......Dn[7:0]
Any Command
If needed
If needed
Legend
Command
Parameter
Display
Action
Mode
Sequential
transter

9.1.22 RAMWR (2Ch): Memory Write

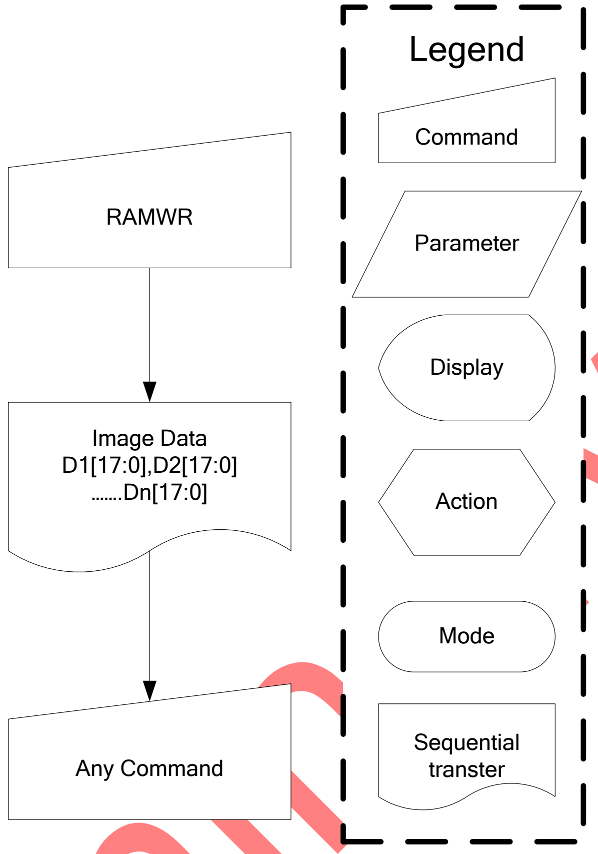
2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st parameter	1	↑	1	D1[8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
…	1	↑	1	Dx[8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
N parameter	1	↑	1	Dn[8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	
Description	-This command is used to transfer data from MCU to frame memory. -When this command is accepted, the column register and the page register are reset to the start column/start page positions. -The start column/start page positions are different in accordance with MADCTL setting. -Sending any other command can stop frame write.												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

<table>
<tr>
<td>Flow Chart</td>
<td>
</td>
</tr>
</table>

9.1.23 RAMRD (2Eh): Memory Read

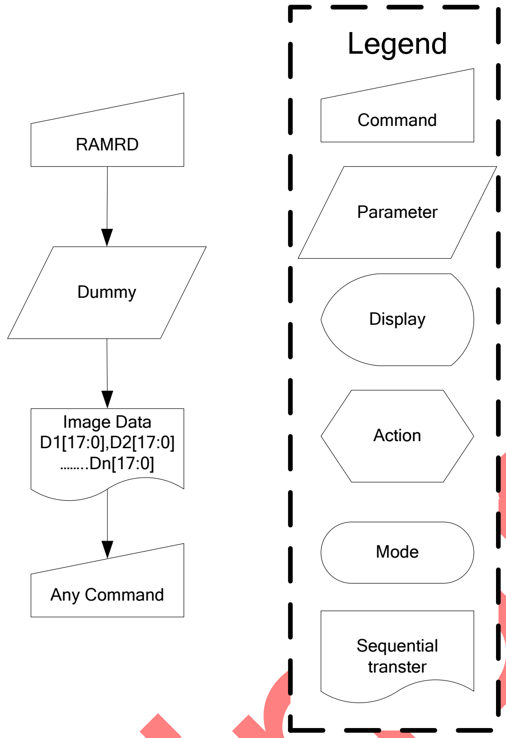
2EH	RAMRD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	D8	D7	D6	D5	D4	D3	D2	D1	D0	
:	1	1	↑	:	:	:	:	:	:	:	:	:	
(N+1)th parameter	1	1	↑	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Description	-This command is used to transfer data from frame memory to MCU. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTL setting. -Then D[8:0] is read back from the frame memory and the column register and the row register incremented -Frame Read can be cancelled by sending any other command. -The data color coding is fixed to 18-bit in reading function. Please see section 9.8 "Data color coding" for color coding (18-bit cases), when there is used 8, 9 data lines for image data. Note1: The Command 3Ah should be set to 66h when reading pixel data from frame memory.												
Restriction													
Register availability	(see table below)												
Default	(see table below)												

Register availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart	 RAMRD Dummy Image Data D1[17:0],D2[17:0] ....Dn[17:0] Any Command Legend Command Parameter Display Action Mode Sequential transter

9.1.24 PTLAR (30h): Partial Area

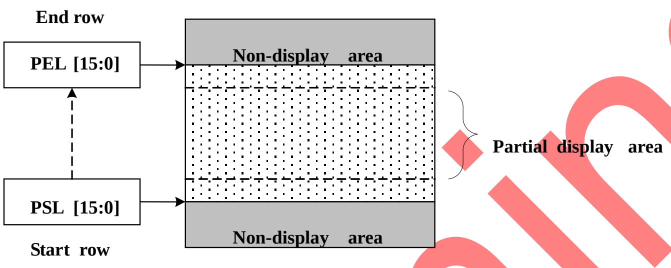
30H	PTLAR (Partial Area)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1st parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	
2nd parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
3rd parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
4th parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	

Description

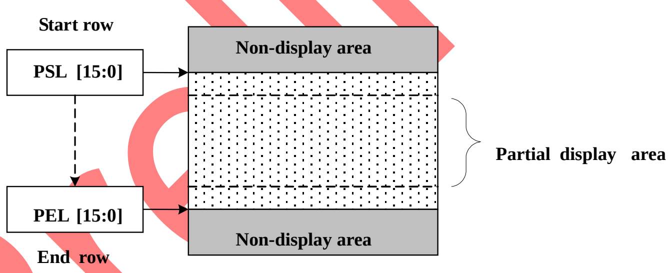
-This command defines the partial mode's display area.

-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

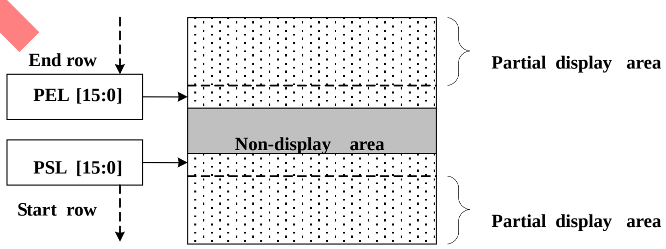
-If End Row > Start Row, when MADCTL ML='1'



-If End Row > Start Row, when MADCTL ML='0'



-If End Row < Start Row, when MADCTL ML='0'



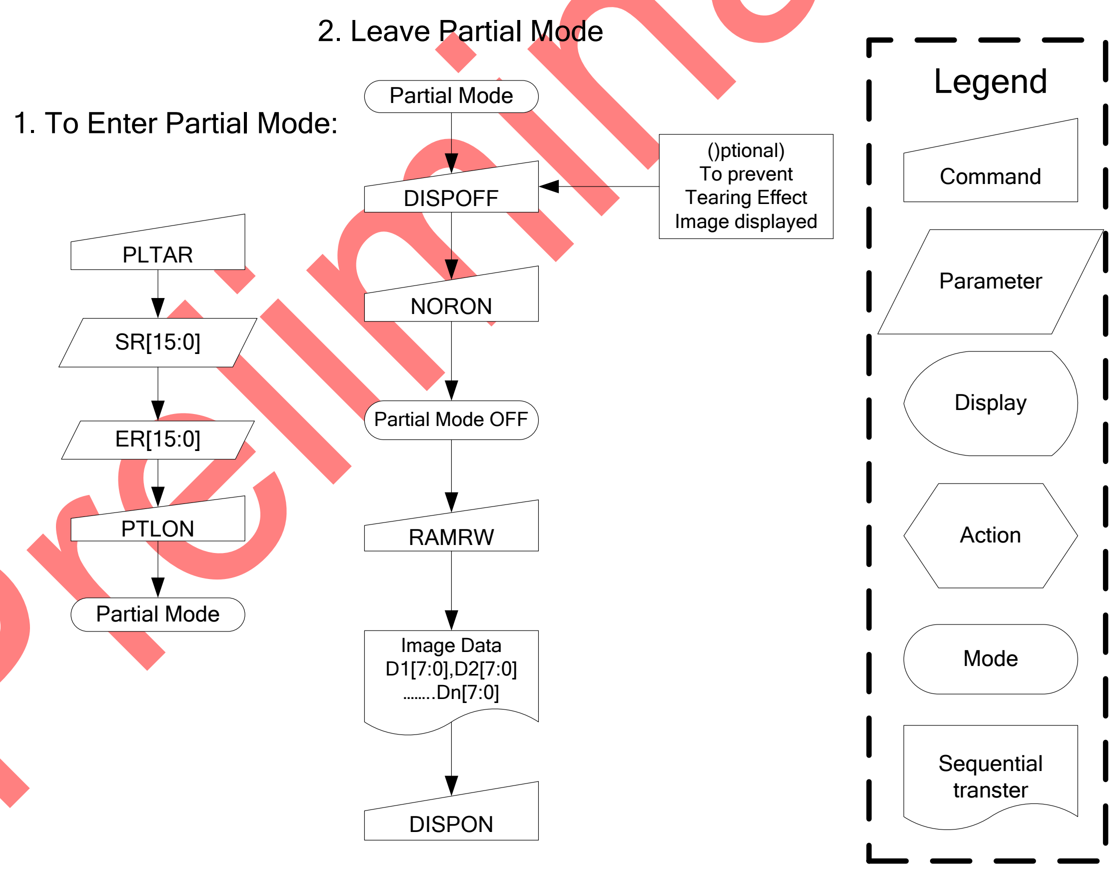
-If End Row = Start Row then the Partial Area will be one row deep.

<table>
<tr><td>Restriction</td><td>Each detail initial value by the display resolution will be updated.</td></tr>
<tr><td>Register availability</td><td>

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

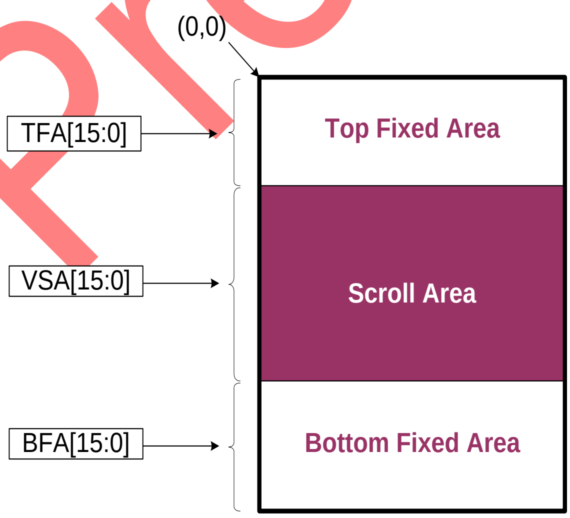
</td></tr>
<tr><td>Default</td><td>

Status	Default Value
Power On Sequence	PSL[15:0]=0000h, PEL=013Fh
S/W Reset	PSL[15:0]=0000h, PEL=013Fh
H/W Reset	PSL[15:0]=0000h, PEL=013Fh

</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

9.1.25 VSCRDEF (33h): Vertical Scrolling Definition

33H	(Vertical Scrolling Definition)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)
1st parameter	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	
2nd parameter	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	
3rd parameter	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	
4th parameter	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
5th parameter	1	↑	1		BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	
6th parameter	1	↑	1		BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	
Description	-This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll -When MADCTL MV=0 -The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). -The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area. -The 4th & 5th parameter BFA [6:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer 													
Restriction	The condition is TFA+VSA+BFA = 320, otherwise Scrolling mode is undefined.												

	In Vertical Scrolling Mode, MADCTL parameter MV should be set to '0' – this only affects the Frame Memory write.
Register availability	see table below
Default	see table below

Register availability:

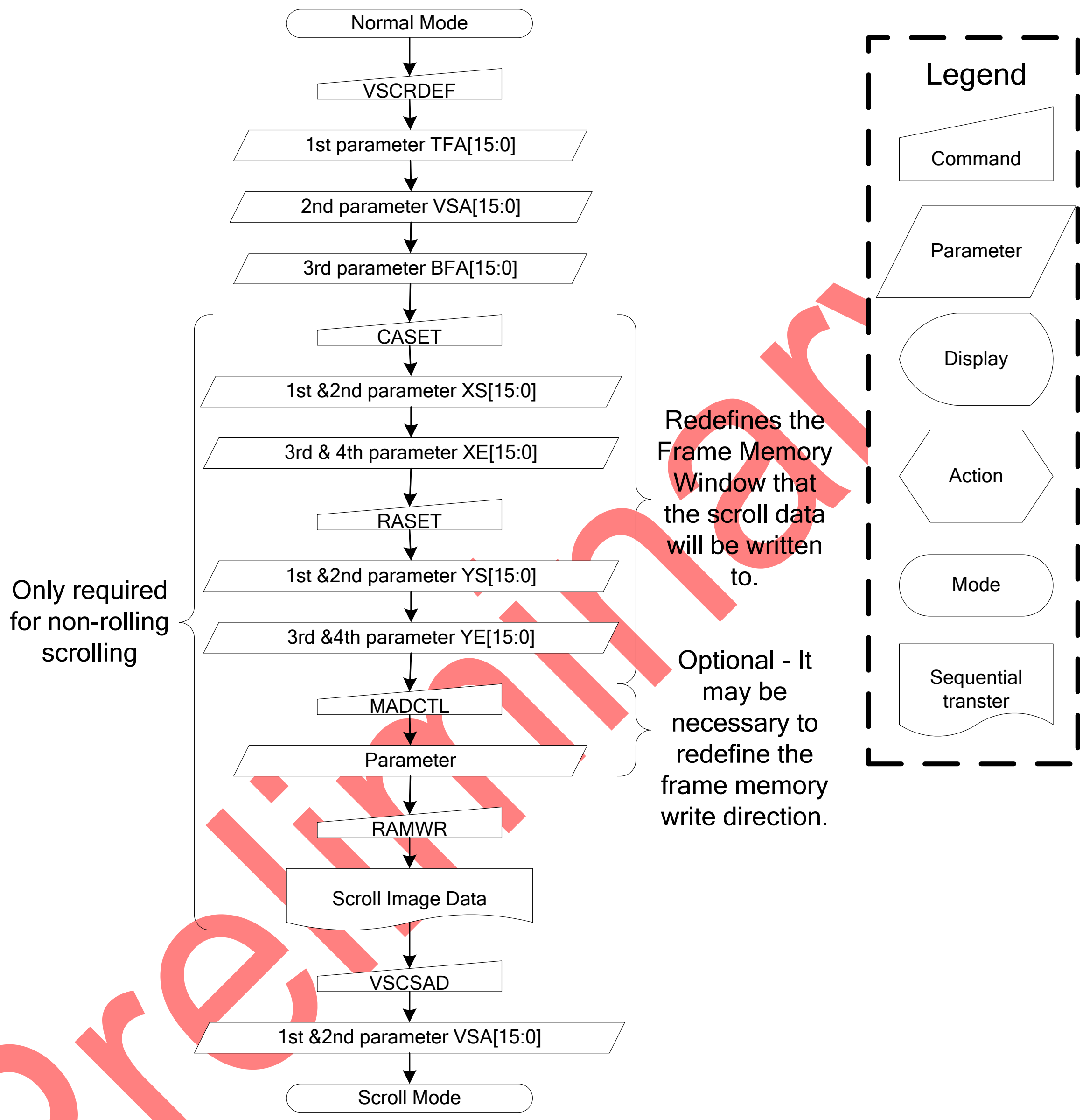
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value		
Power On Sequence	TFA[15:0] = 0000h	VSA[0:15] = 0140h	BFA[15:0] = 0000h
S/W Reset	TFA[15:0] = 0000h	VSA[0:15] = 0140h	BFA[15:0] = 0000h
H/W Reset	TFA[15:0] = 0000h	VSA[0:15] = 0140h	BFA[15:0] = 0000h

Flow Chart

1. TO Enter Vertical Scroll Mode:



9.1.26 TEOFF (34h): Tearing Effect Line OFF

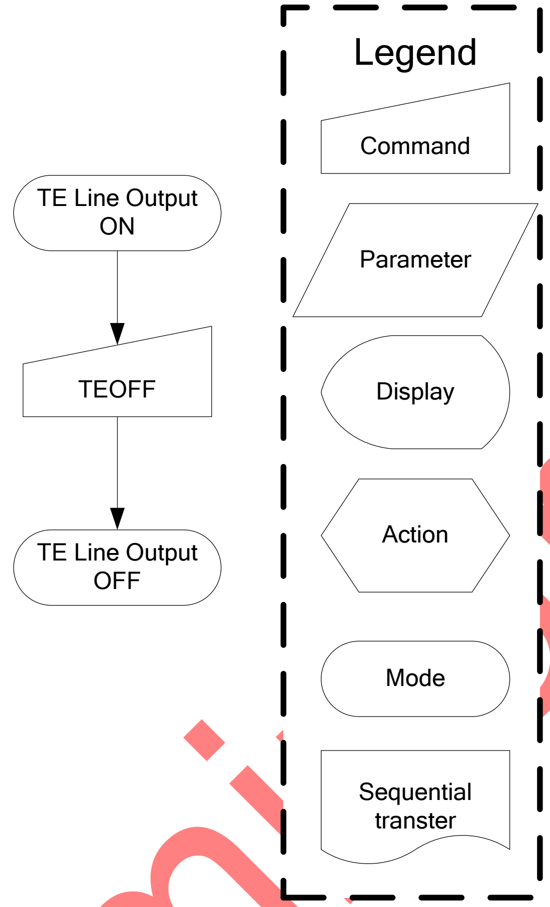
34H	TEOFF (Tearing Effect Line OFF)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
parameter	No Parameter												
Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.												
Restriction	This command has no effect when tearing effect output is already off..												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart	

TE Line Output ON
TEOFF
TE Line Output OFF
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.27 TEON (35h): Tearing Effect Line On

35H	TEON (Tearing Effect Line On)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
parameter	1	↑	1	-	0	0	0	0	0	0	0	TEM	

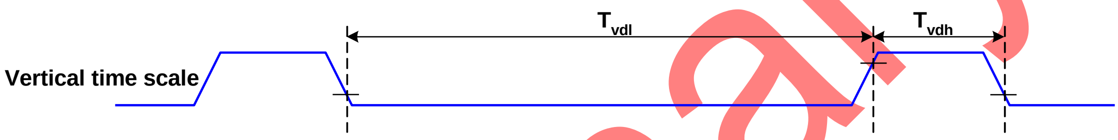
Description

-This command is used to turn ON the Tearing Effect output signal from the TE signal line.

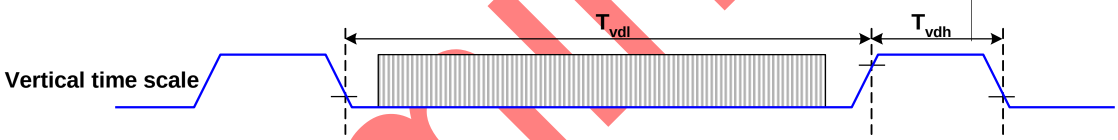
-This output is not affected by changing MADCTL bit ML.

-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line:

-When TEM ='0': The Tearing Effect output line consists of V-Blanking information only



-When TEM ='1': The Tearing Effect output Line consists of both V-Blanking and H-Blanking information



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

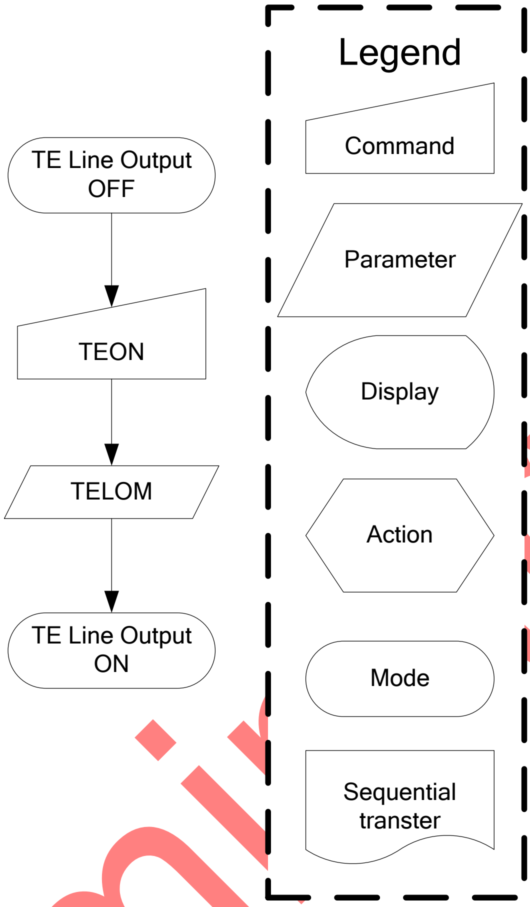
This command has no effect when tearing effect output is already on.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart	TE Line Output OFF TEON TELOM TE Line Output ON Legend Command Parameter Display Action Mode Sequential transter

9.1.28 MADCTL (36h): Memory Data Access Control

36H	MADCTL (Memory Data Access Control)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-	

Description

-This command defines read/ write scanning direction of frame memory.

Bit	NAME	DESCRIPTION
D7	MY	Page Address Order
D6	MX	Column Address Order
D5	MV	Page/Column Order
D4	ML	Line Address Order
D3	RGB	RGB/BGR Order
D2	MH	Display Data Latch Order

-Bit Assignment

Bit D7- Page Address Order

"0" = Top to Bottom (When MADCTL D7="0").

"1" = Bottom to Top (When MADCTL D7="1").

Bit D6- Column Address Order

"0" = Left to Right (When MADCTL D6="0").

"1" = Right to Left (When MADCTL D6="1").

Bit D5- Page/Column Order

"0" = Normal Mode (When MADCTL D5="0").

"1" = Reverse Mode (When MADCTL D5="1")

Note: Bits D7 to D5, alse refer to section 8.12 Address Control

Bit D4- Line Address Order

"0" = LCD Refresh Top to Bottom (When MADCTL D4="0")

"1" = LCD Refresh Bottom to Top (When MADCTL D4="1")

Bit D3- RGB/BGR Order

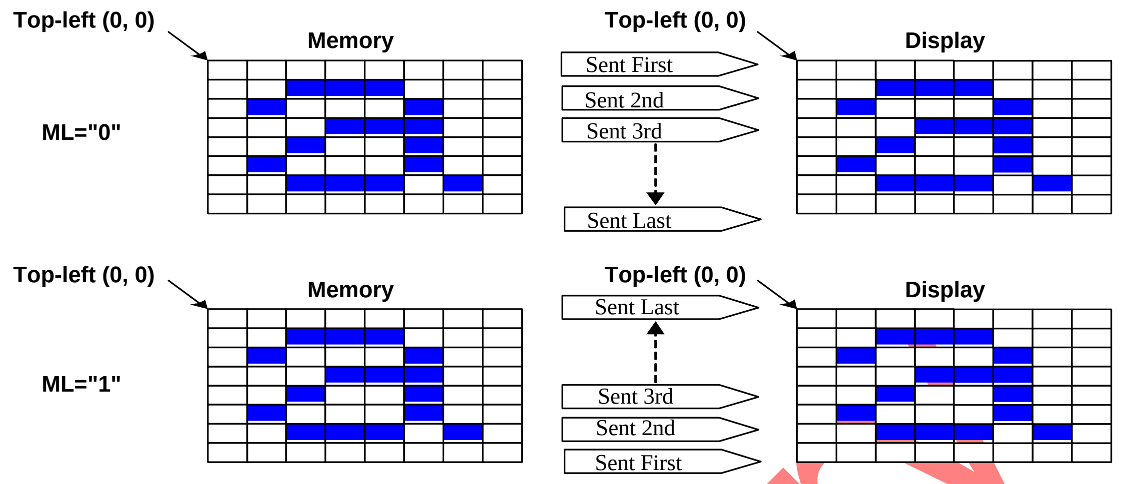
"0" = RGB (When MADCTL D3="0")

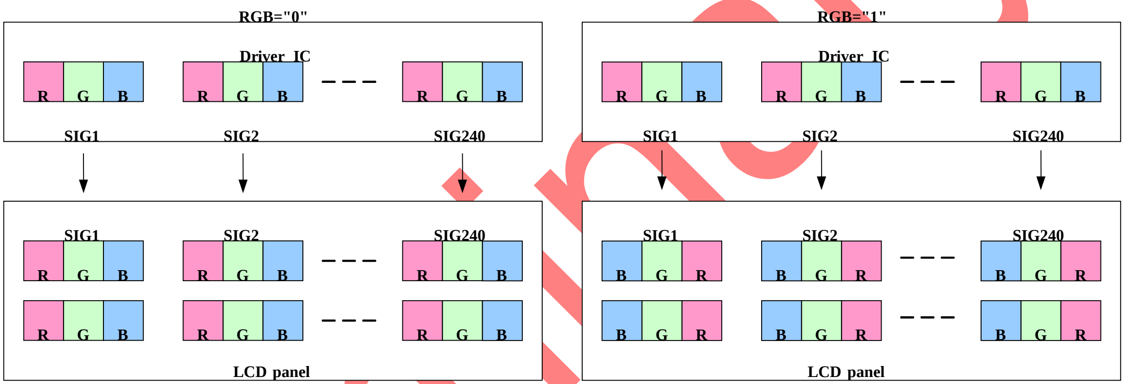
"1" = BGR (When MADCTL D3="1")

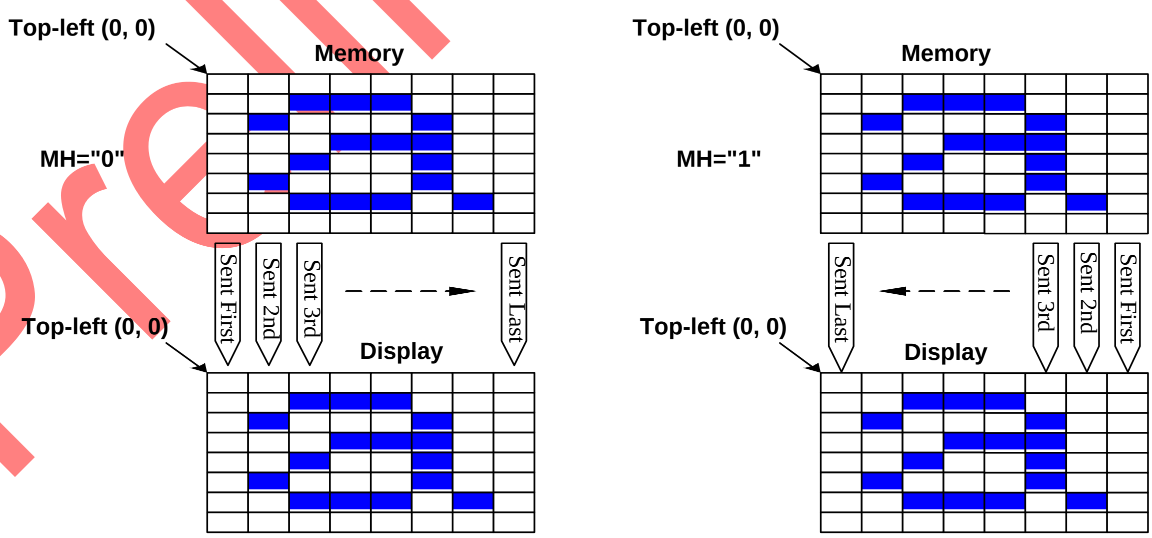
Bit D2- Display Data Latch Data Order

"0" = LCD Refresh Left to Right (When MADCTL D2="0")

"1" = LCD Refresh Right to Left (When MADCTL D2="1")







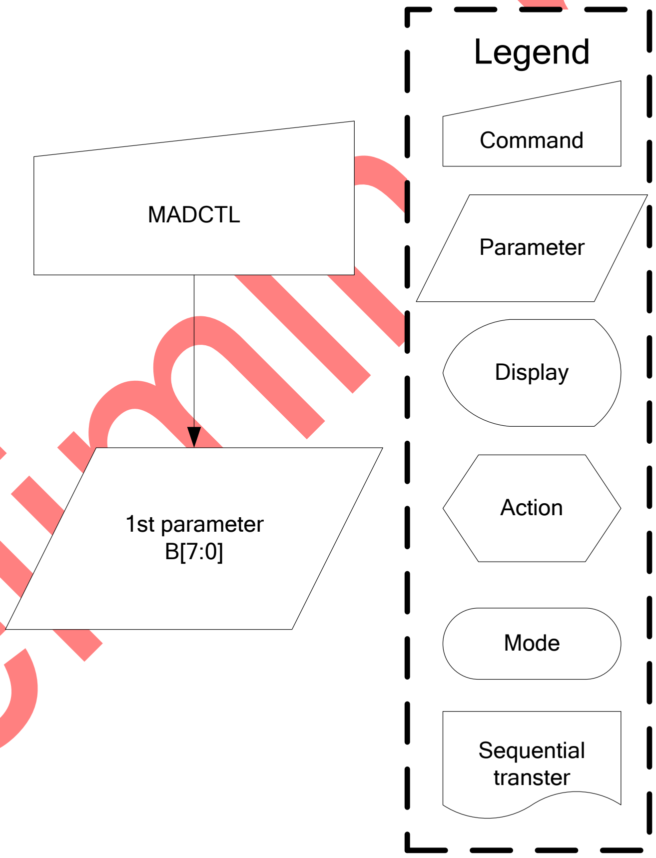
Restriction	
Register availability	Status | Availability

Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	No change
H/W Reset	0000h

Flow Chart



9.1.29 VSCSAD (37h): Vertical Scroll Start Address of RAM

37H	VSCSAD (Vertical Scroll Start Address of RAM)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
1ST parameter	1	↑	1	-	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8	
2ND parameter	1	↑	1	-	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	

Description

-This command is used together with Vertical Scrolling Definition (33h).

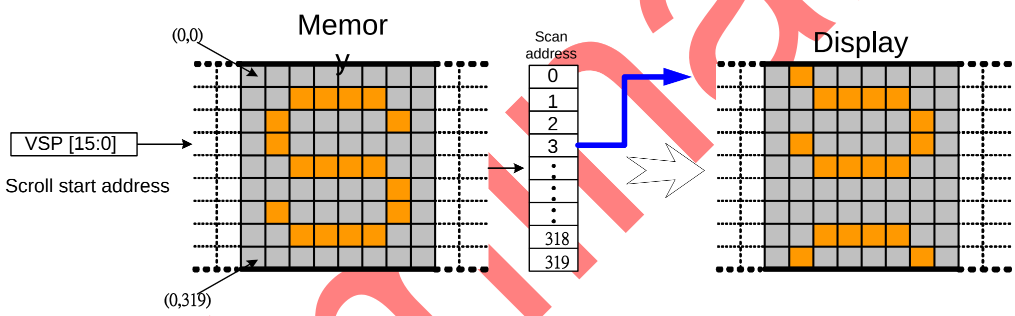
-These two commands describe the scrolling area and the scrolling mode.

-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

When ML=0

Example:

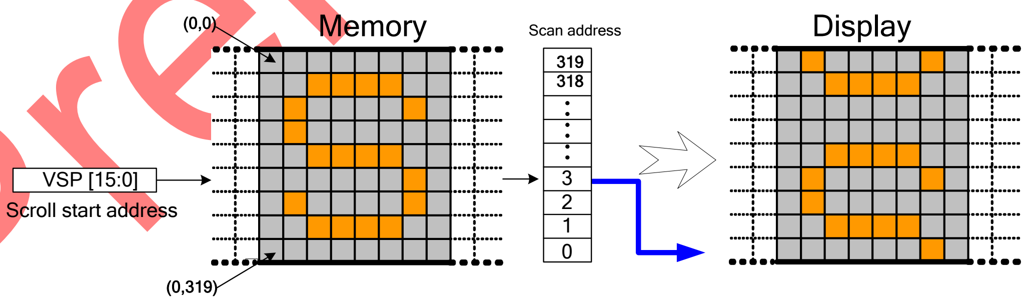
When Top Fixed Area = Bottom Fixed Area = 00, vertical Scrolling Area = 320 and VSP = ‘3’



When ML=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, vertical Scrolling Area = 320 and VSP = ‘3’



NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

VSP refers to the Frame Memory line Pointer

Restriction	Since the value of the vertical scrolling start address is absolute (with reference to the frame memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)- otherwise undesirable image will be displayed on the panel)
Register availability	

		Status / Availability table below

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	See Vertical Scrolling Definition (33h) description

9.1.30 IDMOFF (38h): Idle Mode Off

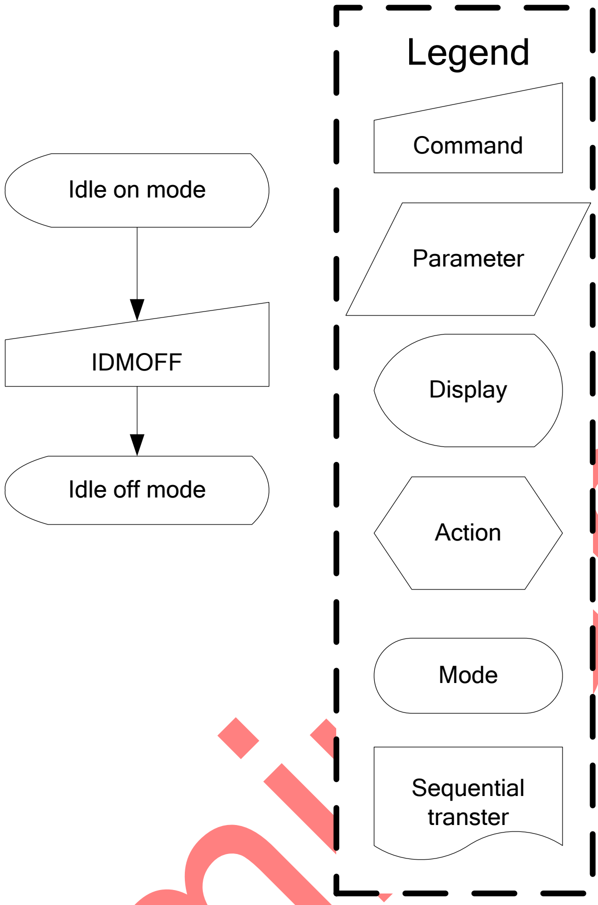
38H	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
parameter	No Parameter												
Description	-This command is used to recover from Idle mode on. -In the idle off mode, 1. LCD can display 4096, 65k or 262k colors. 2. Normal frame frequency is applied.												
Restriction	This command has no effect when module is already in idle off mode												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode off
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Flow Chart	

Idle on mode
IDMOFF
Idle off mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.31 IDMON (39h): Idle mode on

39H	IDMON (Idle Mode On)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
parameter	No Parameter												

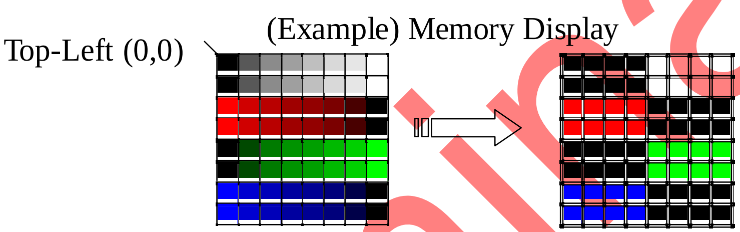
Description

-This command is used to enter into Idle mode on.

-There will be no abnormal visible effect on the display mode change transition.

-In the idle on mode,

1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from IDMON by Idle Mode Off (38h) command

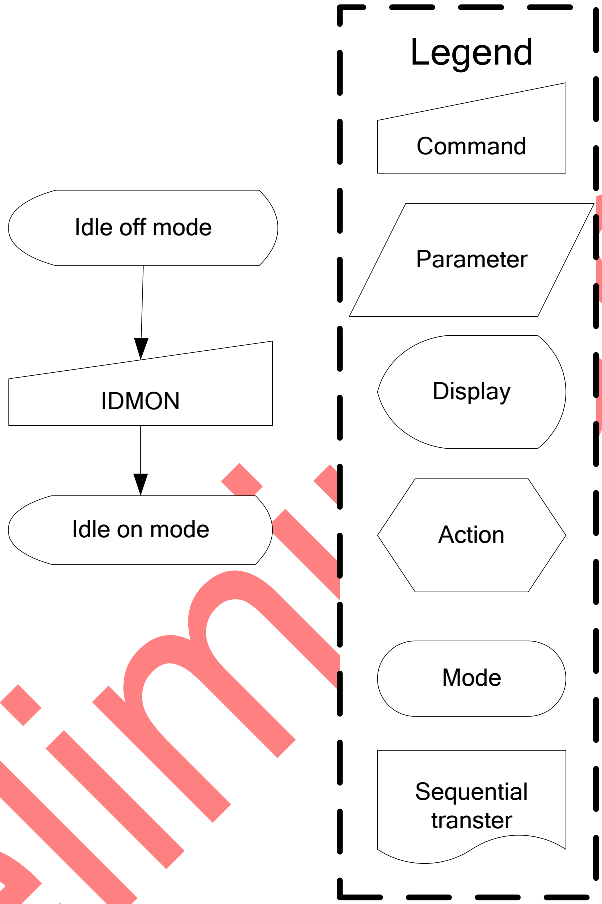


Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0
Black	0xxxxx	0xxxxx	0xxxxx
Blue	0xxxxx	0xxxxx	1xxxxx
Red	1xxxxx	0xxxxx	0xxxxx
Magenta	1xxxxx	0xxxxx	1xxxxx
Green	0xxxxx	1xxxxx	0xxxxx
Cyan	0xxxxx	1xxxxx	1xxxxx
Yellow	1xxxxx	1xxxxx	0xxxxx
White	1xxxxx	1xxxxx	1xxxxx

Restriction: This command has no effect when module is already in idle off mode

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Idle mode off</td></tr>
<tr><td>S/W Reset</td><td>Idle mode off</td></tr>
<tr><td>H/W Reset</td><td>Idle mode off</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

9.1.32 COLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (Interface Pixel Format)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
1st Parameter	1	↑	1	-	0	D6	D5	D4	0	D2	D1	D0	

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:

1st parameter:

Bit	Description	
D7	-	Set to '0'
D6	RGB interface color format	'101' = 65K of RGB interface '110' = 262K of RGB interface
D5		
D4		
D3	-	Set to '0'
D2	Control interface color format	'011' = 12bit/pixel '101' = 16bit/pixel '110' = 18bit/pixel '111' = 16M truncated
D1		
D0		

Note1: In 12-bit/Pixel, 16-bit/Pixel or 18-bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.

Note2: The Command 3Ah should be set at 55h when writing 16-bit/pixel data into frame memory, but 3Ah should be re-set to 66h when reading pixel data from frame memory.

Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	18bit/pixel
S/W Reset	No change
H/W Reset	18bit/pixel

Flow Chart

See Vertical Scrolling Definition (33h) description

9.1.33 WRMEMC (3Ch): Write Memory Continue

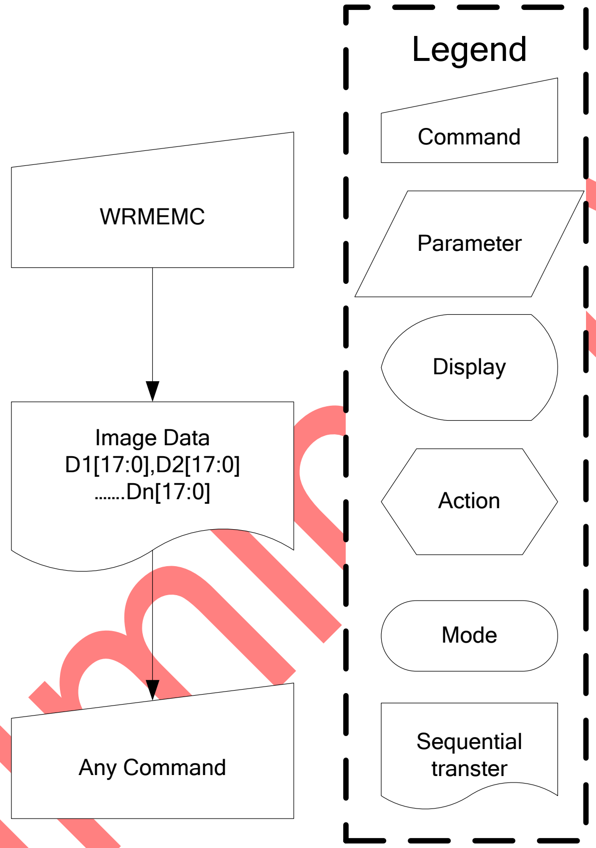
3CH	WRMEMC (Write Memory Continue)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRMEMC	0	↑	1	-	0	0	1	1	1	1	0	0	(3Ch)
1^{ST} parameter	1	↑	1	D1[8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
:	1	↑	1	Dx[8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
N^{th} parameter	1	↑	1	Dn[8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	
Description	-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write memory continue or memory write command. -If MV=0: Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored. If MV=1: Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are written to the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored.												
Restriction	A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.												
Register availability	(see table below)												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

<table>
<tr><td>Default</td><td>

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

</td></tr>
<tr><td>Flow Chart</td><td>



</td></tr>
</table>

9.1.34 RDMEMC (3Eh): Read Memory Continue

3EH	RDMEMC (Read Memory Continue)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDMEMC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)
1ST parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	D1[8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
⋮	1	1	↑	Dx[8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
Nth parameter	1	1	↑	Dn[8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	

Description

-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous read memory continue or memory read command.

-If MV=0:

Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are read from the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command.

If MV=1:

Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are read from the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command.

Restriction

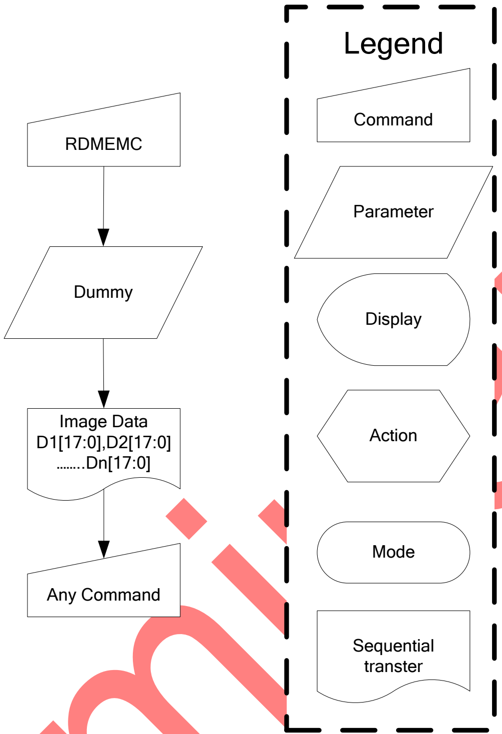
Regardless of the color mode set in interface pixel format, the pixel format returned by read memory continue is always 18-bit so there is no restriction on the length of data

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared

<table>
<tr><td></td><td><table><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td>
</td></tr>
</table>

9.1.35 STE (44h): Set Tear Scanline

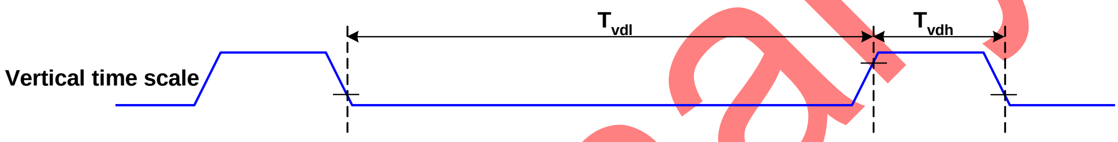
44H	STE (Set Tear ScanLine)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
STE	0	↑	1	-	0	1	0	0	0	1	0	0	(44h)
1st parameter	1	↑	1	-	N15	N14	N13	N12	N11	N10	N9	N8	
2nd parameter	1	↑	1	-	N7	N6	N5	N4	N3	N2	N1	N0	

Description

-This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MV.

-The tearing effect line on has one parameter that describes the tearing effect output line mode.

-The tearing effect output line consist of V-blanking information only.



Note that set tear scanline with N=0 is equivalent to tearing effect line on with TEM=0.

The tearing effect output line shall be active low when the display module is in sleep mode

Restriction

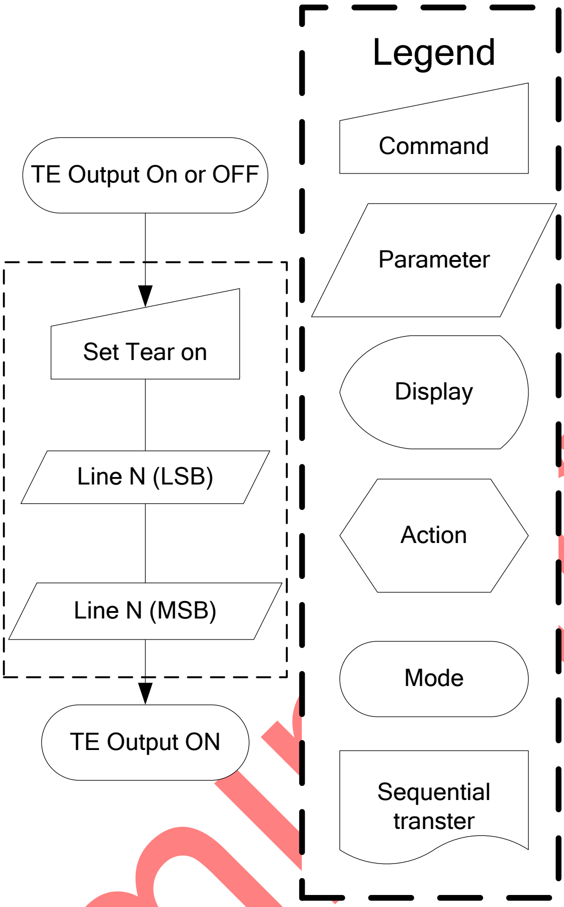
This command takes affect on the frame following the current frame. Therefore, if the tear effect (TE) output is already on, the TE output shall continue to operate as programmed by the previous tearing effect line on or set tear scanline command until the end of the frame

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	 TE Output On or OFF Set Tear on Line N (LSB) Line N (MSB) TE Output ON Legend Command Parameter Display Action Mode Sequential transter

9.1.36 GSCAN (45h): Get Scanline

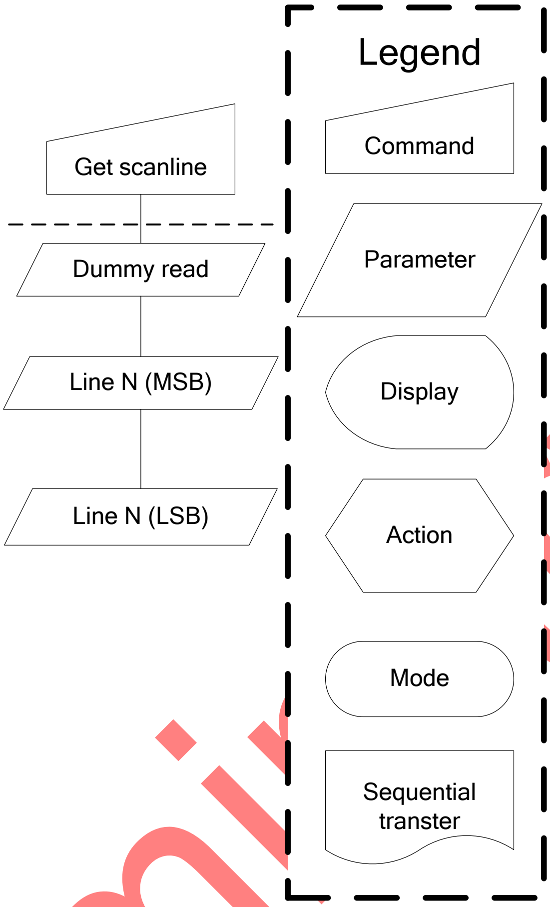
45H	GSCAN (Get ScanLine)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GSCAN	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	N15	N14	N13	N12	N11	N10	N9	N8	
3rd parameter	1	1	↑	-	N7	N6	N5	N4	N3	N2	N1	N0	
Description	-The display module returns the current scanline ,N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. -When in sleep in mode, the value returned by get scanline is undefined.												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	Get scanline Dummy read Line N (MSB) Line N (LSB) Legend Command Parameter Display Action Mode Sequential transter

9.1.37 WRDISBV (51h): Write Display Brightness

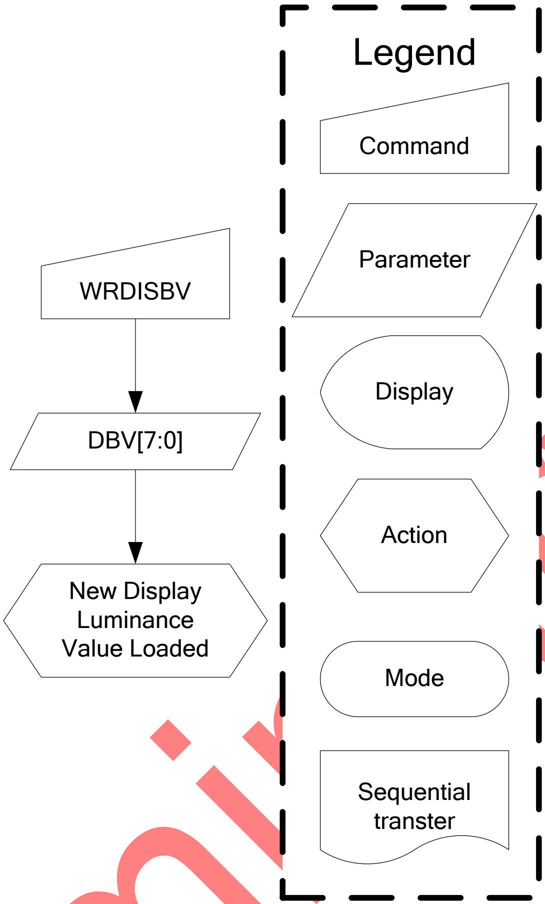
51H	WRDISBV (Write Display Brightness)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)
Parameter	1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	
Description	-This command is used to adjust the brightness value of the display. -It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. -In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	WRDISBV DBV[7:0] New Display Luminance Value Loaded Legend Command Parameter Display Action Mode Sequential transter

9.1.38 RDDISBV (52h): Read Display Brightness Value

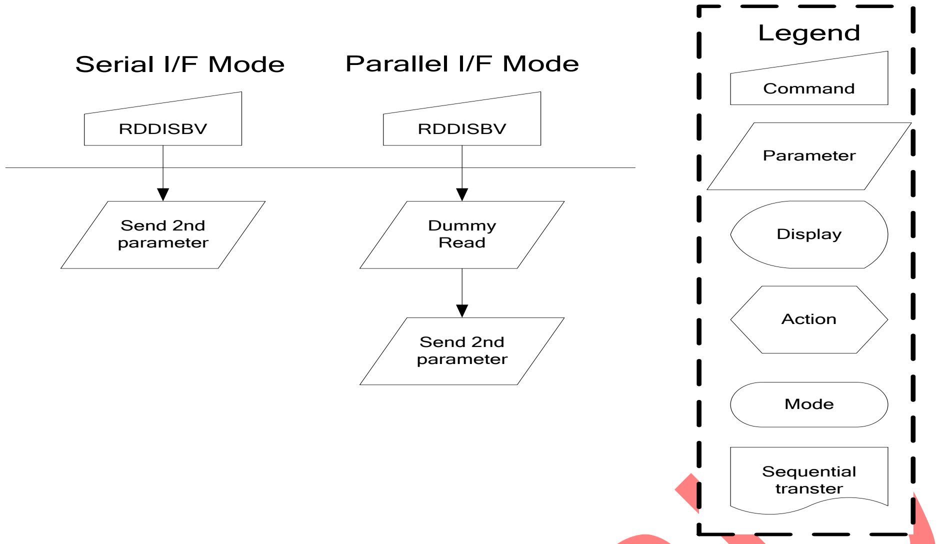
52H	RDDISBV (Read Display Brightness Value)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	
Description	-This command returns the brightness value of the display. -It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. -In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. -DBV[7:0] is reset when display is in sleep in mode. -DBV[7:0] is '0' when bit BCTRL of write CTRL display command (53h) is '0' -DBV[7:0] IS manual set brightness specified with write CTRL display command (53h) when bit BCTRL is '1'												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	 Serial I/F Mode Parallel I/F Mode RDDISBV Send 2nd parameter RDDISBV Dummy Read Send 2nd parameter Legend Command Parameter Display Action Mode Sequential transter

9.1.39 WRCTRLD (53h): Write CTRL Display

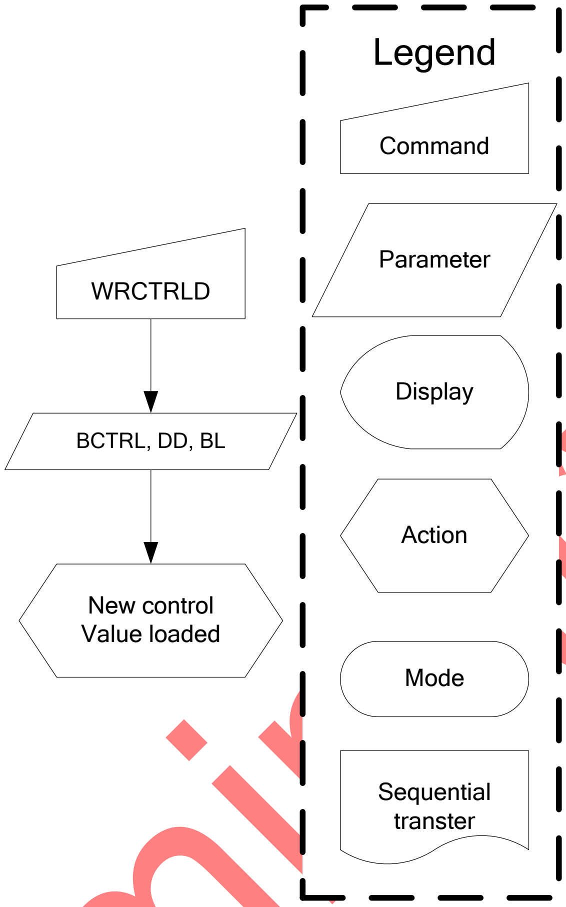
53H	WRCTRLD (Write CTRL Display)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)
Parameter	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0	
Description	-This command is used to control display brightness. -BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness register are 00h, DBV[7:0]) 1 = On (Brightness register are active, according to the other parameters.) -DD: Display Dimming (Only for manual brightness setting) DD = 0: Display Dimming is off. DD = 1: Display Dimming is on. -BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On -Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1. -When BL bit changed from 'on' to 'off', backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.												
Restriction													

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	WRCTRLD BCTRL, DD, BL New control Value loaded Legend Command Parameter Display Action Mode Sequential transter

9.1.40 RDCTRLD (54h): Read CTRL Value Display

54H	RDCTRLD (Read CTRL value Display)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0	

Description

-This command returns ambient light and brightness control values.

-BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

0 = Off

1 = On

-DD: Display Dimming (Only for manual brightness setting)

DD = 0

DD = 1

-BL: Backlight Control On/Off

0 = Off

1 = On

Restriction

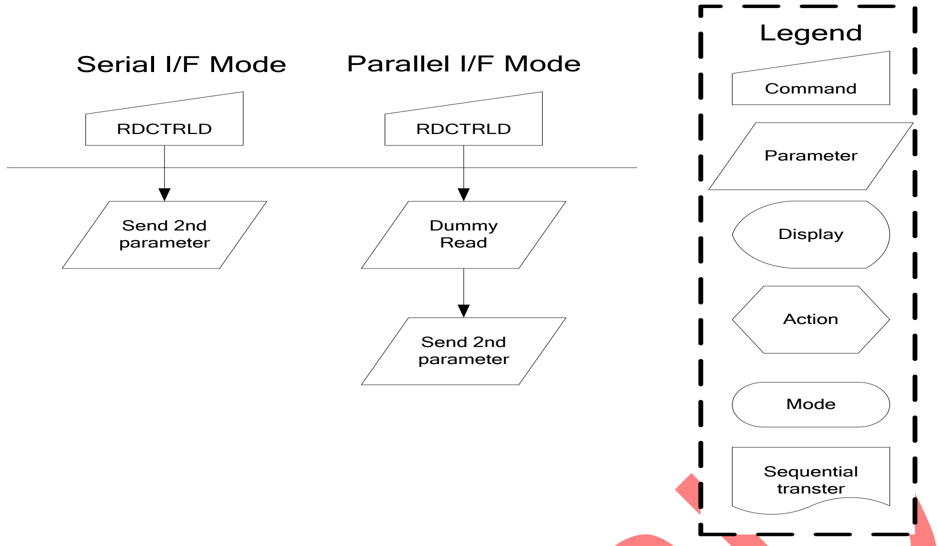
-

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	 Serial I/F Mode Parallel I/F Mode RDCTRLD RDCTRLD Send 2nd parameter Dummy Read Send 2nd parameter Legend Command Parameter Display Action Mode Sequential transter

9.1.41 WRCACE (55h): Write Content Adaptive Brightness Control and Color Enhancement

55H	WRCACE (Write Content Adaptive Brightness Control and Color Enhancement)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCACE	0	↑	1	-	0	1	0	1	0	1	0	1	(55h)
Parameter	1	↑	1	-	CECTRL	0	CE1	CE0	0	0	C1	C0	

Description

-This command is used to set parameters for image content based adaptive brightness control functionality and Color Enhancement function.

-There is possible to used 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function
0	0	Off
0	1	User Interface Mode
1	0	Still Picture
1	1	Moving Image

-CECTRL: Color Enhancement Control Bit:

CECTRL=0: Color Enhancement Off.

CECTRL=1: Color Enhancement On.

-There are three color enhancement levels can be set.

CE1	CE0	Color enhancement level
0	0	Low enhancement
0	1	Medium enhancement
1	1	High enhancement

'-': Don't care

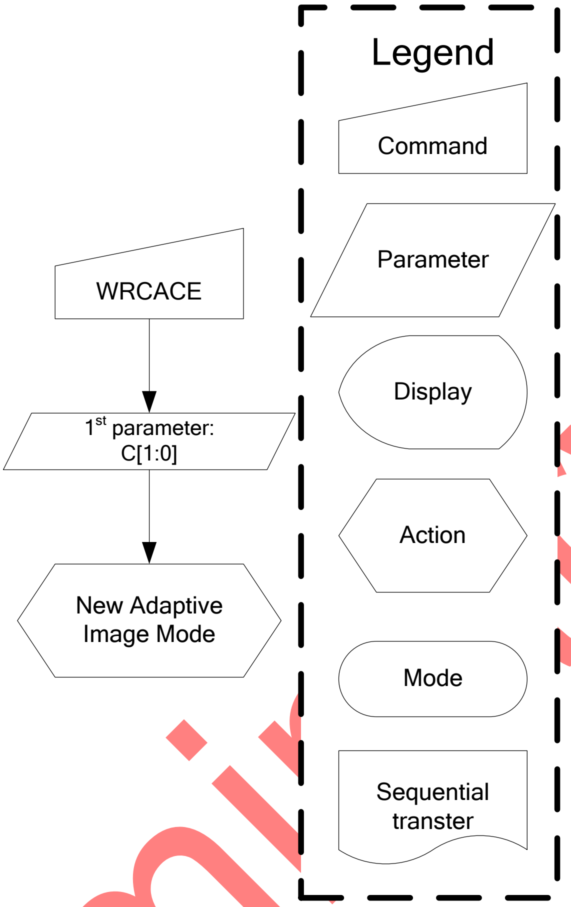
Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	

WRCACE
1st parameter: C[1:0]
New Adaptive Image Mode
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.42 RDCABC (56h): Read Content Adaptive Brightness Control

56H	RDCABC (Read Content Adaptive Brightness Control)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	(56h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	0	0	0	0	0	0	C1	C0	
Description	-This command is used to read the settings for image content based adaptive brightness control functionality. -There is possible to used 4 different modes for content adaptive image functionality, which are defined on a table below. C1 / C0 / Function: 0 0 Off; 0 1 User Interface Mode; 1 0 Still Picture; 1 1 Moving Image '-': Don't care												
Restriction	-												
Register availability	(see table below)												
Default	(see table below)												

Description:

C1	C0	Function
0	0	Off
0	1	User Interface Mode
1	0	Still Picture
1	1	Moving Image

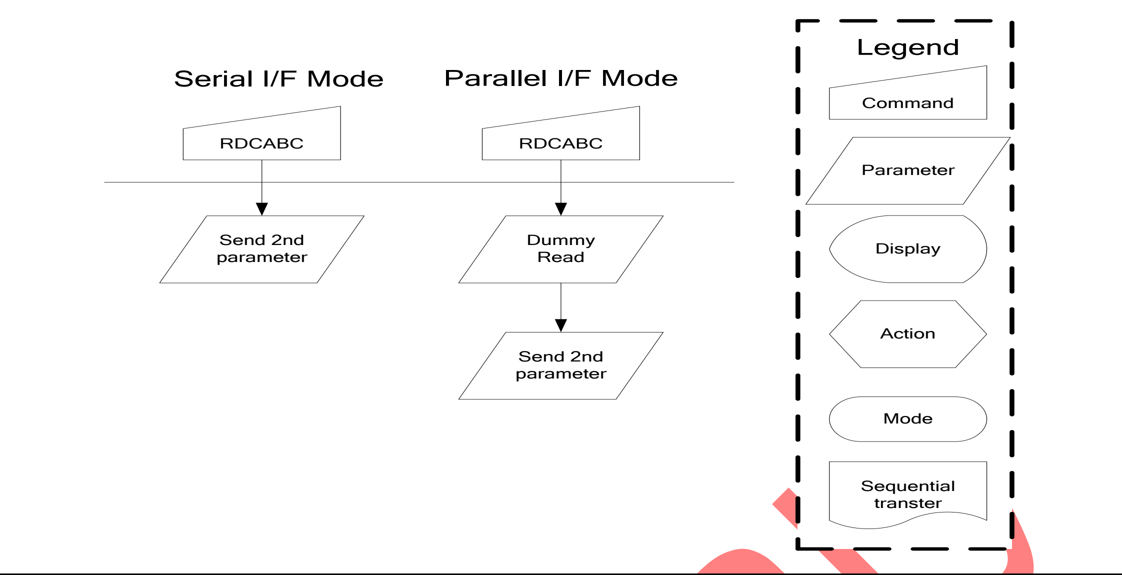
'-': Don't care

Register availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	

Serial I/F Mode
Parallel I/F Mode
RDCABC
Send 2nd parameter
RDCABC
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.43 WRCABCMB (5Eh): Write CABC Minimum Brightness

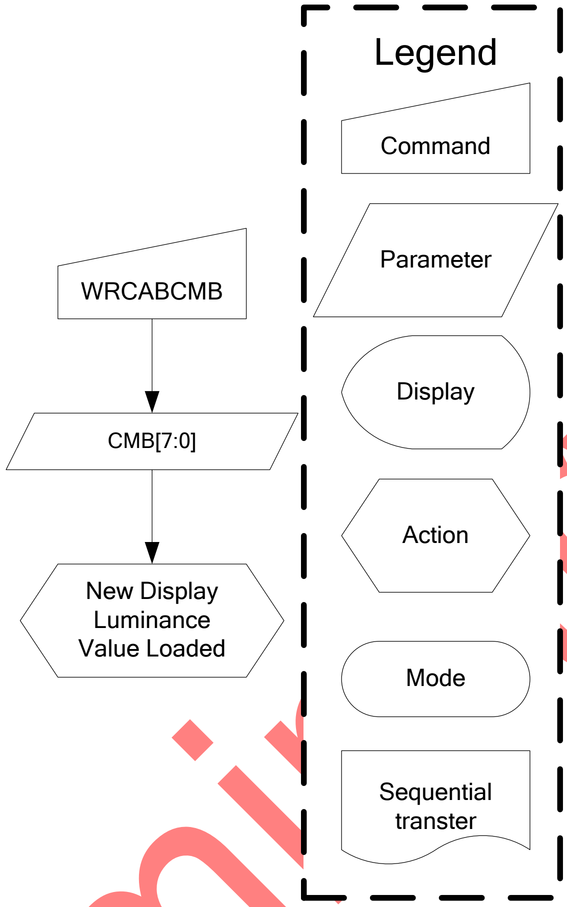
5EH	WRCABCMB (Write CABC Minimum Brightness)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCABCMB	0	↑	1	-	0	1	0	1	1	1	1	0	(5Eh)
Parameter	1	↑	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	
Description	-This command is used to set the minimum brightness value of the display for CABC function. -In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the brightness for CABC. '-': Don't care												
Restriction													
Register availability													
Default													

Register availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	 WRCABCMB CMB[7:0] New Display Luminance Value Loaded Legend Command Parameter Display Action Mode Sequential transter

9.1.44 RDCABCMB (5Fh): Read CABC Minimum Brightness

5FH	RDCABCMB (Read CABC Minimum Brightness)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCABCMB	0	↑	1	-	0	1	0	1	1	1	1	1	(5Fh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	

Description

-This command returns the minimum brightness value of CABC function.

-In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the brightness for CABC.

'-': Don't care

Restriction

-

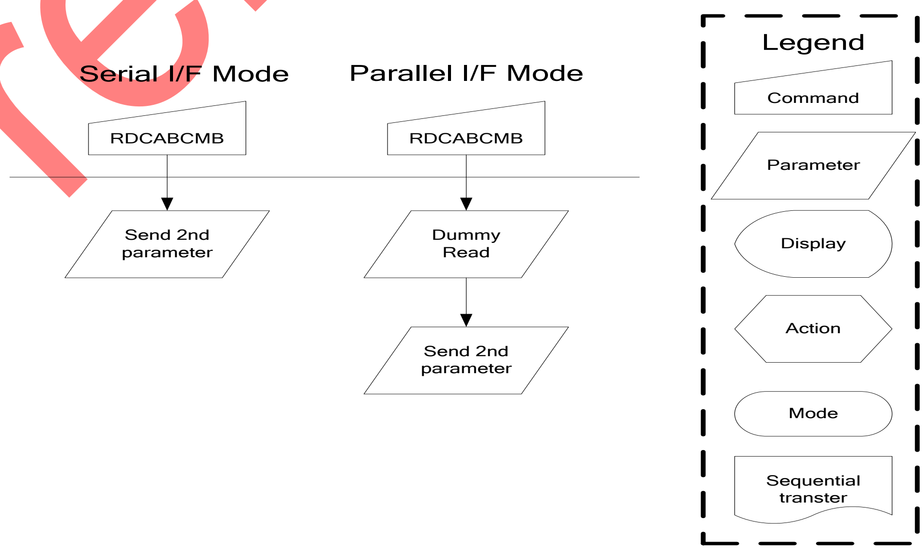
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



9.1.45 RDABCSDR (68h): Read Automatic Brightness Control Self-Diagnostic Result

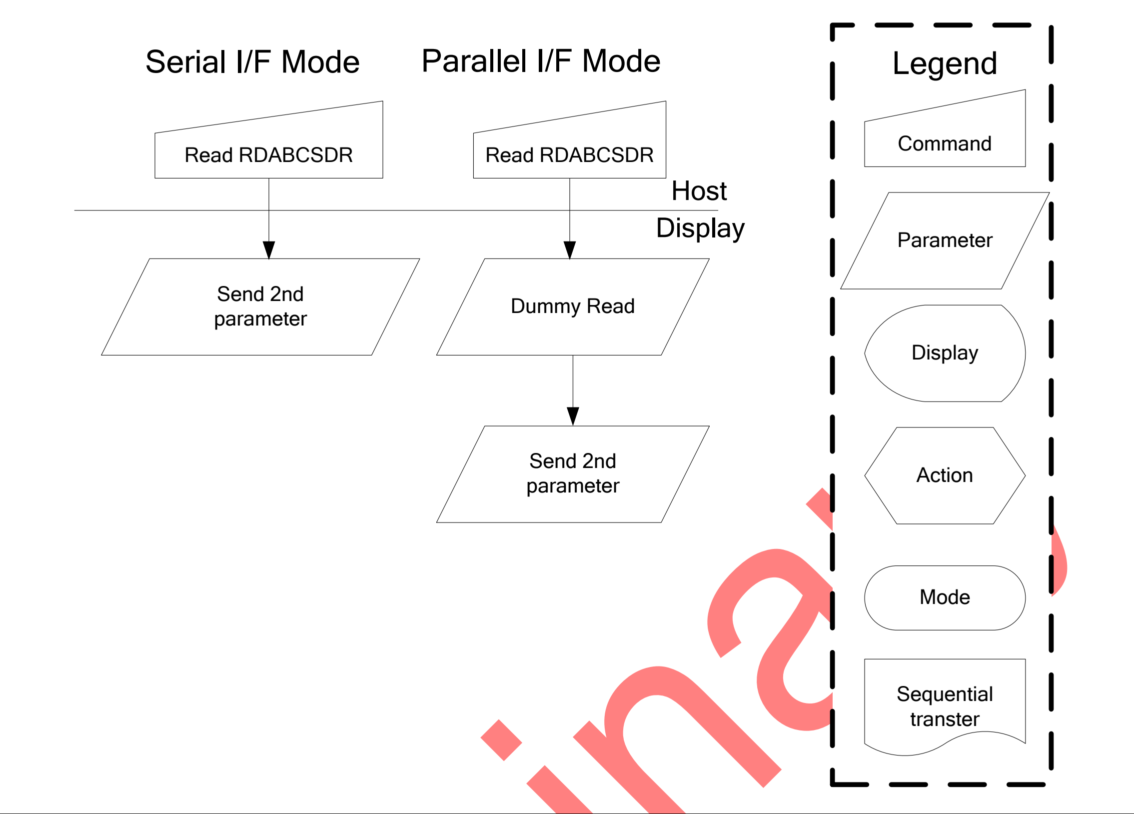
68H	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDABCSDR	0	↑	1	-	0	1	1	0	1	0	0	0	(68h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	0	0	0	0	0	0	-
Description	This command indicates the current status of the display self-diagnostic results for automatic brightness control after sleep out -command as described below: -D7: Register loading detection -D6: Functionality detection "-" Don't care												
Restriction													
Register availability	see table below												
Default	see table below												

Register availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

Serial I/F Mode
Parallel I/F Mode
Read RDABCSDR
Read RDABCSDR
Host
Display
Send 2nd parameter
Dummy Read
Send 2nd parameter
Legend
Command
Parameter
Display
Action
Mode
Sequential transter

9.1.46 RDID1 (DAh): Read ID1

DAH	RDID1 (Read ID1)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(Dah)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
Description	-This read byte identifies the LCD module's manufacturer.												
Restriction	-												

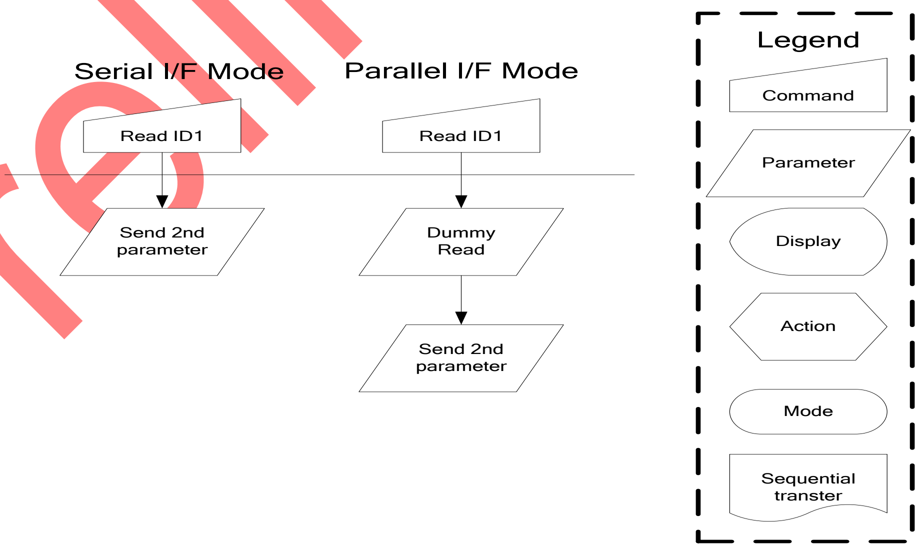
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	85h
S/W Reset	85h
H/W Reset	85h

Flow Chart



9.1.47 RDID2 (DBh): Read ID2

DBH	RDID2 (Read ID2)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	

Description	This read byte is used to track the LCD module/driver IC version. ‘-’: Don’t care.
Restriction	-

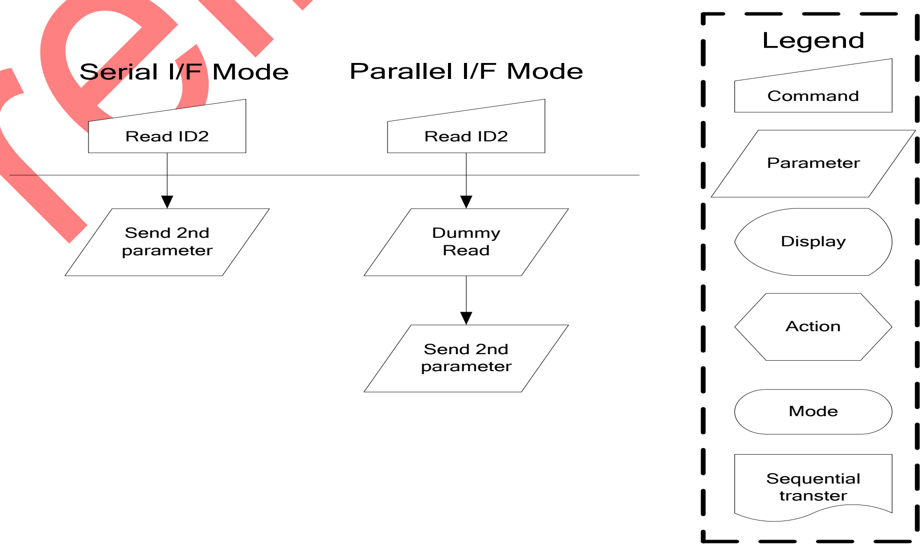
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	85h
S/W Reset	85h
H/W Reset	85h

Flow Chart



9.1.48 RDID3 (DCh): Read ID3

DCH	RDID3 (Read ID3)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
Description	This read byte identifies the LCD module/driver.												
Restriction	-												

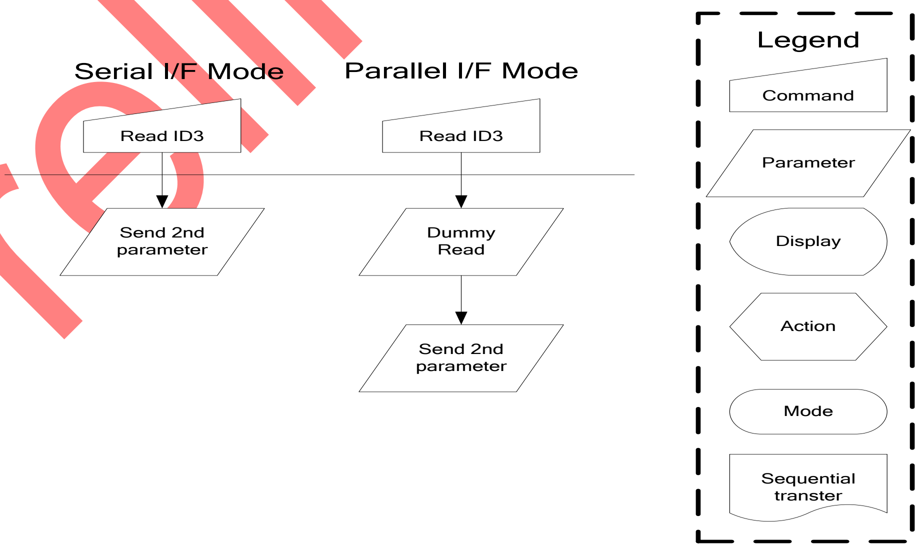
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	52h
S/W Reset	52h
H/W Reset	52h

Flow Chart



9.2 System Function Command Table 2

Instruction	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
RAMCTRL	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)	RAM Control
	1	↑	1	-	0	0	0	RM	0	0	DM1	DM0		
	1	↑	1	-	1	1	EPF1	EPF0	ENDIAN	RIM	MDT1	MDT0		
RGBCTRL	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	RGB Control
	1	↑	1	-	WO	RCM1	RCM0	0	VSPL	HSPL	DPL	EPL		
	1	↑	1	-	0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0		
	1	↑	1	-	0	0	0	HBP4	HBP3	HBP2	HBP1	HBP0		
PORCTRL	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	Porch control
	1	↑	1	-	0	BPA6	BPA5	BPA4	BPA3	BPA2	BPA1	BPA0		
	1	↑	1	-	0	FPA6	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0		
	1	↑	1	-	0	0	0	0	0	0	0	PSEN		
	1	↑	1		BPB3	BPB2	BPB1	BPB0	FPB3	FPB2	FPB1	FPB0		
	1	↑	1		BPC3	BPC2	BPC1	BPC0	FPC3	FPC2	FPC1	FPC0		
FRCTRL1	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	Frame Rate Control 1
	1	↑	1	-	0	0	0	FRSEN	0	0	DIV1	DIV0		
	1	↑	1	-	NLB2	NLB1	NLB0	RTNB4	RTNB3	RTNB2	RTNB1	RTNB0		
	1	↑	1	-	NLC2	NLC1	NLC0	RTNC4	RTNC3	RTNC2	RTNC1	RTNC0		
PARCTRL	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)	Partial mode Control
	1	↑	1	-	NDL	0	0	PTGISC	ISC3	ISC2	ISC1	ISC0		
DSTBMDSEL	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)	Deep Standby Mode Selection
	1	↑	1	-	0	0	0	0	0	0	0	DSTBMD		
GCTRL	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)	Gate control
	1	↑	1	-	0	VGHS2	VGHS1	VGHS0	0	VGLS2	VGLS1	VGLS0		
GTADJ	0	↑	1	-	1	0	1	1	1	0	0	0	(B8h)	Gate on timing adjustment
	1	↑	1	-	0	0	1	0	1	0	1	0		
	1	↑	1	-	0	0	1	0	1	0	1	1		
	1	↑	1	-	0	0	GTA5	GTA4	GTA3	GTA2	GTA1	GTA0		
	1	↑	1	-	GOFR3	GOFR2	GOFR1	GOFR0	GOF3	GOF2	GOF1	GOF0		
DGMEN	0	↑	1	-	1	0	1	1	1	0	1	0	(BAh)	Digital Gamma Enable
	1	↑	1	-	0	0	0	0	0	DGMEN	0	0		
VCOMS	0	↑	1	-	1	0	1	1	1	0	1	1	(BBh)	VCOMS

Instruction	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	1	-	0	0	VCOMS5	VCOMS4	VCOMS3	VCOMS2	VCOMS1	VCOMS0		Setting
LCMCTRL	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)	LCM Control
	1	↑	1	-	0	XMY	XBGR	XINV	XMX	XMH	XMV	XGS		
IDSET	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)	ID Setting
	1	↑	1	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
	1	↑	1	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
VDVVRHEN	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)	VDV and VRH Command Enable
	1	↑	1	-	0	0	0	0	0	0	0	CMDEN		
	1	↑	1	-	1	1	1	1	1	1	1	1		
VRHS	0	↑	1		1	1	0	0	0	0	1	1	(C3h)	VRH Set
	1	↑	1		0	0	VRHS5	VRHS4	VRHS3	VRHS2	VRHS1	VRHS0		
VDVSET	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)	VDV Setting
	1	↑	1	-	0	0	VDVS5	VDVS4	VDVS3	VDVS2	VDVS1	VDVS0		
VCMOFSET	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)	VCOMS Offset Set
	1	↑	1	-	0	0	VCMOFS5	VCMOFS4	VCMOFS3	VCMOFS2	VCMOFS1	VCMOFS0		
FRCTR2	0	↑	1		1	1	0	0	0	1	1	0	(C6h)	FR Control 2
	1	↑	1		NLA2	NLA1	NLA0	RTNA4	RTNA3	RTNA2	RTNA1	RTNA0		
CABCCTRL	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)	CABC Control
	1	↑	1	-	0	0	0	0	LEDONREV	DPOFPWM	PWMFIX	PWMPOL		
REGSEL1	0	↑	1	-	1	1	0	0	1	0	0	0	(C8h)	Register value selection1
	1	↑	1	-	0	0	0	0	1	0	0	0		
REGSEL2	0	↑	1	-	1	1	0	0	1	0	1	0	(CAh)	Register value selection2
	1	↑	1	-	0	0	0	0	1	1	1	1		
PWMFRSEL	0	↑	1	-	1	1	0	0	1	1	0	0	(CCh)	PWM Frequency Selection
	1	↑	1	-	0	0	CS2	CS1	CS0	CLK2	CLK1	CLK0		
PWCTRL1	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)	Power Control 1
	1	↑	1	-	1	0	1	0	0	1	0	0		
	1	↑	1	-	AVDD1	AVDD0	AVCL1	AVCL0	0	0	VDS1	VDS0		
VAPVANEN	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	Enable

Instruction	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	1	-	0	1	0	0	1	1	0	0		VAP/VAN signal output
CMD2EN	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	Command 2 Enable
	1	↑	1	-	0	1	0	1	1	0	1	0	(5Ah)	
	1	↑	1	-	0	1	1	0	1	0	0	1	(69h)	
	1	↑	1	-	0	0	0	0	0	0	1	0	(02h)	
	1	↑	1	-	0	0	0	DSTB	PROMD	0	0	EN		
PVGAMCTRL	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Positive Voltage Gamma Control
	1	↑	1	-	V63P3	V63P2	V63P1	V63P0	V0P3	V0P2	V0P1	V0P0		
	1	↑	1	-	0	0	V1P5	V1P4	V1P3	V1P2	V1P1	V1P0		
	1	↑	1	-	0	0	V2P5	V2P4	V2P3	V2P2	V2P1	V2P0		
	1	↑	1	-	0	0	0	V4P4	V4P3	V4P2	V4P1	V4P0		
	1	↑	1	-	0	0	0	V6P4	V6P3	V6P2	V6P1	V6P0		
	1	↑	1	-	0	0	J0P1	J0P0	V13P3	V13P2	V13P1	V13P0		
	1	↑	1	-	0	V20P6	V20P5	V20P4	V20P3	V20P2	V20P1	V20P0		
	1	↑	1	-	0	V36P2	V36P1	V36P0	0	V27P2	V27P1	V27P0		
	1	↑	1	-	0	V43P6	V43P5	V43P4	V43P3	V43P2	V43P1	V43P0		
	1	↑	1	-	0	0	J1P1	J1P0	V50P3	V50P2	V50P1	V50P0		
	1	↑	1	-	0	0	0	V57P4	V57P3	V57P2	V57P1	V57P0		
	1	↑	1	-	0	0	0	V59P4	V59P3	V59P2	V59P1	V59P0		
	1	↑	1	-	0	0	V61P5	V61P4	V61P3	V61P2	V61P1	V61P0		
	1	↑	1	-	0	0	V62P5	V62P4	V62P3	V62P2	V62P1	V62P0		
NVGAMCTRL	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Negative Voltage Gamma Control
	1	↑	1	-	V63N3	V63N2	V63N1	V63N0	V0N3	V0N2	V0N1	V0N0		
	1	↑	1	-	0	0	V1N5	V1N4	V1N3	V1N2	V1N1	V1N0		
	1	↑	1	-	0	0	V2N5	V2N4	V2N3	V2N2	V2N1	V2N0		
	1	↑	1	-	0	0	0	V4N4	V4N3	V4N2	V4N1	V4N0		
	1	↑	1	-	0	0	0	V6N4	V6N3	V6N2	V6N1	V6N0		
	1	↑	1	-	0	0	J0N1	J0N0	V13N3	V13N2	V13N1	V13N0		

Instruction	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	1		0	V20N6	V20N5	V20N4	V20N3	V20N2	V20N1	V20N0		
	1	↑	1		0	V36N2	V36N1	V36N0	0	V27N2	V27N1	V27N0		
	1	↑	1		0	V43N6	V43N5	V43N4	V43N3	V43N2	V43N1	V43N0		
	1	↑	1		0	0	J1N1	J1N0	V50N3	V50N2	V50N1	V50N0		
	1	↑	1		0	0	0	V57N4	V57N3	V57N2	V57N1	V57N0		
	1	↑	1		0	0	0	V59N4	V59N3	V59N2	V59N1	V59N0		
	1	↑	1		0	0	V61N5	V61N4	V61N3	V61N2	V61N1	V61N0		
	1	↑	1		0	0	V62N5	V62N4	V62N3	V62N2	V62N1	V62N0		
DGMLUTR	0	↑	1	-	1	1	1	0	0	0	1	0	(E2h)	Digital Gamma Look-up Table for Red
	1	↑	1	-	DGM_LUT_R00[7:0]									
	1	↑	1	-	DGM_LUT_R01[7:0]									
	1	↑	1	-	⋮									
	1	↑	1	-	DGM_LUT_R30[7:0]									
	1	↑	1	-	DGM_LUT_R31[7:0]									
	1	↑	1	-	⋮									
	1	↑	1	-	DGM_LUT_R62[7:0]									
	1	↑	1	-	DGM_LUT_R63[7:0]									
DGMLUTB	0	↑	1	-	1	1	1	0	0	0	1	1	(E3h)	Digital Gamma Look-up Table for Blue
	1	↑	1	-	DGM_LUT_B00[7:0]									
	1	↑	1	-	DGM_LUT_B01[7:0]									
	1	↑	1	-	⋮									
	1	↑	1	-	DGM_LUT_B30[7:0]									
	1	↑	1	-	DGM_LUT_B31[7:0]									
	1	↑	1	-	⋮									
	1	↑	1	-	DGM_LUT_B62[7:0]									
	1	↑	1	-	DGM_LUT_B63[7:0]									
GATECTRL	0	↑	1	-	1	1	1	0	0	1	0	0	(E4h)	Gate control
	1	↑	1	-	0	0	NL5	NL4	NL3	NL2	NL1	NL0		
	1	↑	1	-	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0		
	1	↑	1	-	0	0	0	TMG	0	SM	0	GS		

Instruction	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
SPI2EN	0	↑	1	-	1	1	1	0	0	1	1	1	(E7h)	SPI2 enable
	1	↑	1	-	0	0	0	SPI2EN	0	0	0	SPIRD		
PWCTRL2	0	↑	1	-	1	1	1	0	1	0	0	0	(E8h)	Power Control 2
	1	↑	1	-	1	0	SBCLK1	SBCLK0	0	0	STP14CK1	STP14CK0		
EQCTRL	0	↑	1	-	1	1	1	0	1	0	0	1	(E9h)	Equalize Time Control
	1	↑	1	-	0	0	0	SEQ4	SEQ3	SEQ2	SEQ1	SEQ0		
	1	↑	1	-	0	0	0	SPRET4	SPRET3	SPRET2	SPRET1	SPRET0		
	1	↑	1	-	0	0	0	0	GEQ3	GEQ2	GEQ1	GEQ0		
PROMCTRL	0	↑	1	-	1	1	1	0	1	1	0	0	(ECh)	Program Control
	1	↑	1	-	0	0	0	0	0	0	0	1		
PROMEN	0	↑	1	-	1	1	1	1	1	0	1	0	(FAh)	Program Mode Enable
	1	↑	1	-	0	1	0	1	1	0	1	0		
	1	↑	1	-	0	1	1	0	1	0	0	1		
	1	↑	1	-	1	1	1	0	1	1	1	0		
	1	↑	1	-	VPPINTMD	0	0	0	0	PROMEN	0	0		
NVMSET	0	↑	1	-	1	1	1	1	1	1	0	0	(FCh)	NVM Setting
	1	↑	1	-	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0		
	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0		
PROMACT	0	↑	1	-	1	1	1	1	1	1	1	0	(FEh)	Program Action
	1	↑	1	-	0	0	0	1	1	0	0	1		
	1	↑	1	-	1	0	1	0	0	1	0	1		

Note: 1. If host uses high speed mode in MIPI interface, please send one dummy byte before every parameter.

9.2.1 RAMCTRL (B0h): RAM Control

B0H	RAMCTR (RAM Control)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMCTRL	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)
1st Parameter	1	↑	1	-	0	0	0	RM	0	0	DM1	DM0	
2nd Parameter	1	↑	1	-	1	1	EPF1	EPF0	ENDIAN	1	MDT1	MDT0	

Description

RM : ram access selection.

RM="0" : Ram access from MCU interface

RM="1" : Ram access from RGB interface and MIPI interface

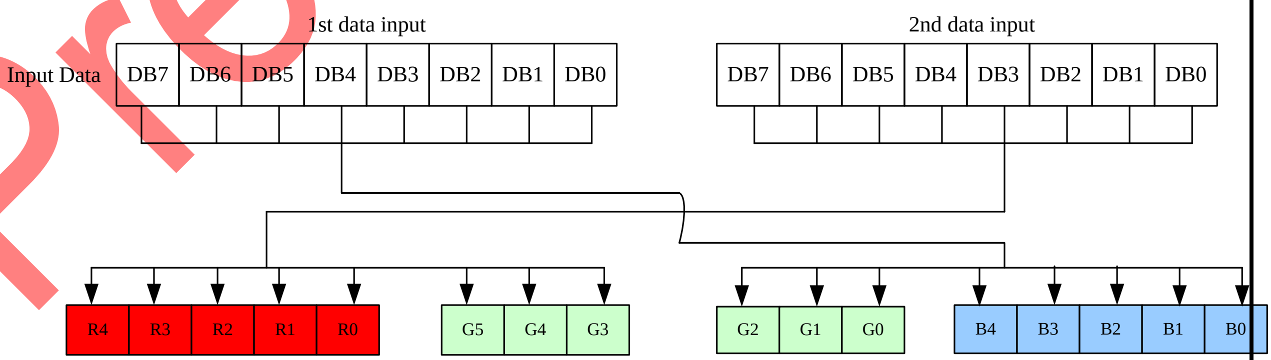
DM[1:0] : Display operation selection.

DM[1:0]	Mode
00h	MCU interface
01h	RGB interface
10h	VSYNC interface
11h	Reserved

ENDIAN :

ENDIAN	Mode
0	Normal (MSB first)
1	Little Endian (LSB first)

Note: Little Endian only can be supported in 65K 8-bit and 9-bit interface.



MDT[1:0] : Method of pixel data transfer.

Please refer to **section 8.8 Data Color Coding**

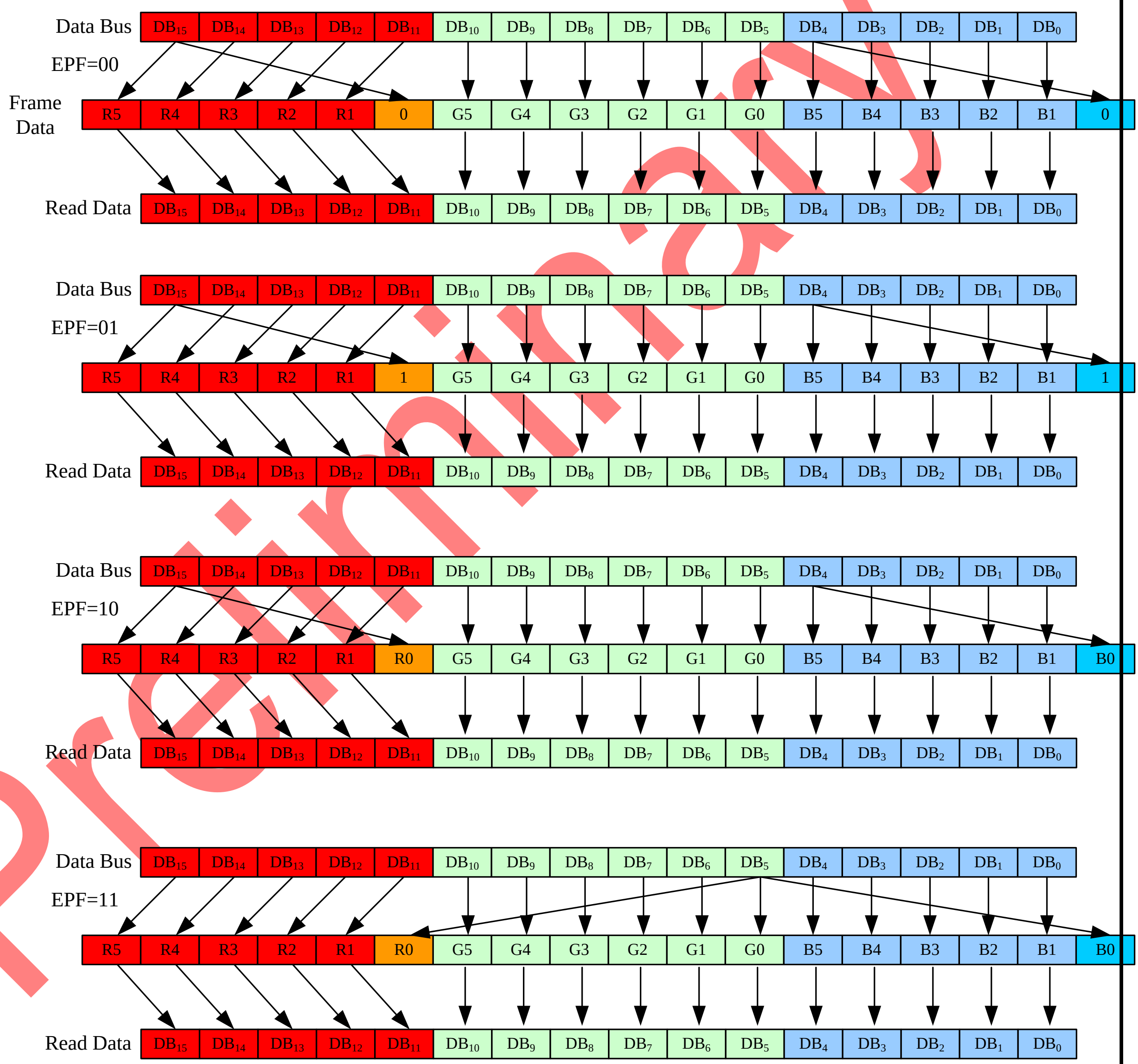
RIM: Specify RGB interface bus width.

RIM=”0”: Reserved

RIM=”1”: 6 bit bus width

EPF[1:0] : Data translate of 65k and 4k to frame data.

65K data formate:



Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes

		Normal Mode On, Idle Mode On, Sleep Out	Yes
		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h/F0h
S/W Reset	00h/F0h
H/W Reset	00h/F0h

9.2.2 RGBCTRL (B1h): RGB Interface Control

B1H	RGBCTRL (RGB Interface Control)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGBCTRL	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st parameter	1	↑	1	-	WO	RCM1	RCM0	0	VSPL	HSPL	DPL	EPL	
2nd parameter	1	↑	1	-	0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	
3rd parameter	1	↑	1	-	0	0	0	HBP4	HBP3	HBP2	HBP1	HBP0	

Description:

WO: Direct RGB mode.

WO	Mode
0	Memory
1	Shift register

RCM[1:0]: RGB I/F enable mode selection.

RCM[1:0]	Mode
00	MCU interface
01	MCU interface
10	RGB DE mode
11	RGB HV mode

VSPL : Sets the signal polarity of the VSYNC pin.
VSPL="0", Low active
VSPL="1", High active

HSPL : Sets the signal polarity of the HSYNC pin.
HSPL="0", Low active
HSPL="1", High active

DPL : Sets the signal polarity of the DOTCLK pin.
DPL = "0" The data is input on the positive edge of DOTCLK
DPL = "1" The data is input on the negative edge of DOTCLK

EPL : Sets the signal polarity of the ENABLE pin.
EPL = "0" The data DB17-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0".
EPL = "1" The data DB17-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1".

VBP[6:0]: RGB interface Vsync back porch setting. Minimum setting is 0x02.

HBP[4:0]: RGB interface Hsync back porch setting. Please refer to the section 8.9.3 for minimum setting.

Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	40h/02h/14h
S/W Reset	40h/02h/14h
H/W Reset	40h/02h/14h

9.2.3 PORCTRL (B2h): Porch Setting

B2H	PORCTRL (Porch Setting)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PORCTRL	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1st parameter	1	↑	1	-	0	BPA6	BPA5	BPA4	BPA3	BPA2	BPA1	BPA0	
2nd parameter	1	↑	1	-	0	FPA6	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0	
3rd parameter	1	↑	1	-	0	0	0	0	0	0	0	PSEN	
4th parameter	1	↑	1	-	BPB3	BPB2	BPB1	BPB0	FPB3	FPB2	FPB1	FPB0	
5th parameter	1	↑	1	-	BPC3	BPC2	BPC1	BPC0	FPC3	FPC2	FPC1	FPC0	

Description

BPA[6:0]: Back porch setting in normal mode. The minimum setting is 0x01.

FPA[6:0]: Front porch setting in normal mode. The minimum setting is 0x01.

PSEN: Enable separate porch control.

PSEN	**Mode**
0	Disable separate porch control
1	Enable separate porch control

BPB[3:0]: Back porch setting in idle mode. The minimum setting is 0x01.

FPB[3:0]: Front porch setting in idle mode. The minimum setting is 0x01.

BPC[3:0]: Back porch setting in partial mode. The minimum setting is 0x01.

FPC[3:0]: Front porch setting in partial mode. The minimum setting is 0x01.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0Ch/0Ch/00h/33h/33h
S/W Reset	0Ch/0Ch/00h/33h/33h
H/W Reset	0Ch/0Ch/00h/33h/33h

9.2.4 FRCTRL1 (B3h): Frame Rate Control 1 (In partial mode/ idle colors)

B3H	FRCTRL1 (Frame rate control 1)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRCTRL1	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)
1st parameter	1	↑	1	-	0	0	0	FRSEN	0	0	DIV1	DIV0	
2nd parameter	1	↑	1	-	NLB2	NLB1	NLB0	RTNB4	RTNB3	RTNB2	RTNB1	RTNB0	
3rd parameter	1	↑	1	-	NLC2	NLC1	NLC0	RTNC4	RTNC3	RTNC2	RTNC1	RTNC0	

Description

FRSEN: Enable separate frame rate control.

When FRSEN=0, Frame rate of idle and partial mode are determined by C6h

When FRSEN=1, Frame rate of idle and partial mode are determined by B3h

FRSEN	Mode
0	Disable separate FR control
1	Enable separate FR control

DIV[1:0]: Frame rate divided control

DIV[1:0]	Mode
00	Divide by 1
01	Divide by 2
10	Divide by 4
11	Divide by 8

NLB[2:0]: Inversion selection in idle mode.

0x00: dot inversion.

0x07: column inversion.

RTNB[4:0]: Frame rate control in idle mode.

RTNB[4:0]	FR in idle mode (Hz)	RTNB[4:0]	FR in idle mode (Hz)
00h	119	10h	58
01h	111	11h	57
02h	105	12h	55
03h	99	13h	53
04h	94	14h	52
05h	90	15h	50
06h	86	16h	49
07h	82	17h	48
08h	78	18h	46
09h	75	19h	45
0Ah	72	1Ah	44

0Bh	69	1Bh	43
0Ch	67	1Ch	42
0Dh	64	1Dh	41
0Eh	62	1Eh	40
0Fh	60	1Fh	39

Note:

1. If FRSEN=1, Frame rate in idle mode=10MHz/(320+(FPB[3:0]+BPB[3:0])*4)*(250+RTNB[4:0]*16).
2. FPB[6:0] and BPB[6:0] are in command B2h
3. In this frame rate table, FPB[3:0]=03h, BPB[3:0]=03h

NLC[2:0]: Inversion setting in partial mode.

0x00: dot inversion.

0x07: column inversion.

RTNC[4:0]: Frame rate control in partial mode. This setting is equal to RTNB.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h/0Fh/0Fh
S/W Reset	00h/0Fh/0Fh
H/W Reset	00h/0Fh/0Fh

9.2.5 PARCTRL (B5h): Partial mode Control

B5H	PARCTRL (Partial mode Control)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PARCTRL	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)
Parameter	1	↑	1	-	NDL	0	0	PTGISC	ISC3	ISC2	ISC1	ISC0	

Description

NDL: Source output level selection in non-display area in partial mode.

"0": V63

"1": V0

PTGISC: Non-display area scan mode.

"0": Normal mode.

"1": Interval scan mode.

ISC[3:0]: Non-display area Scan frequency selection in interval scan mode

ISC[3:0]	Scan frequency
00h	Every frame
01h	1/3 frame
02h	1/5 frame
03h	1/7 frame
04h	1/9 frame
05h	1/11 frame
06h	1/13 frame
07h	1/15 frame
08h	1/17 frame
09h	1/19 frame
0Ah	1/21 frame
0Bh	1/23 frame
0Ch	1/25 frame
0Dh	1/27 frame
0Eh	1/29 frame
0Fh	1/31 frame

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes

<table>
<tr><td></td><td>
<table>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

9.2.6 DSTBMDSEL (B6h): Deep Standby Mode Selection

B6H	DSTBMDSEL (Deep Standby Mode Selection)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DSTBMDSEL	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)
Parameter	1	↑	1	-	0	0	0	0	0	0	0	DSTBMD	
Description	**DSTBMD:** "0": Normal mode "1": Power saving mode												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

9.2.7 GCTRL (B7h): Gate Control

B7H	GCTRL (Gate Control)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GCTRL	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)
Parameter	1	↑	1	-	0	VGHS2	VGHS1	VGHS0	0	VGLS2	VGLS1	VGLS0	

Description

VGHS[2:0]: VGH Setting.

VGHS[2:0]	VGH (V)
00h	12.2
01h	12.54
02h	12.89
03h	13.26
04h	13.65
05h	14.06
06h	14.5
07h	14.97

VGLS[2:0]: VGL Setting.

VGLS[2:0]	VGL (V)
00h	-7.16
01h	-7.67
02h	-8.23
03h	-8.87
04h	-9.6
05h	-10.43
06h	-11.38
07h	-12.5

Register Availability

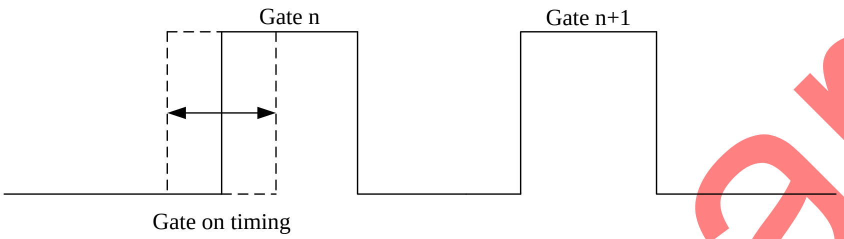
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	35h
	S/W Reset	35h
	H/W Reset	35h

9.2.8 GTADJ (B8h): Gate On Timing Adjustment

B8H	GTADJ(Gate On Timing Adjustment)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GTADJ	0	↑	1	-	1	0	1	1	1	0	0	0	(B8h)
1st Parameter	1	↑	1	-	0	0	1	0	1	0	1	0	2Ah
2nd Parameter	1	↑	1	-	0	0	1	0	1	0	1	1	2Bh
3rd Parameter	1	↑	1	-	0	0	GTA5	GTA4	GTA3	GTA2	GTA1	GTA0	
4th Parameter	1	↑	1	-	GOFR3	GOFR2	GOFR1	GOFR0	GOF3	GOF2	GOF1	GOF0	

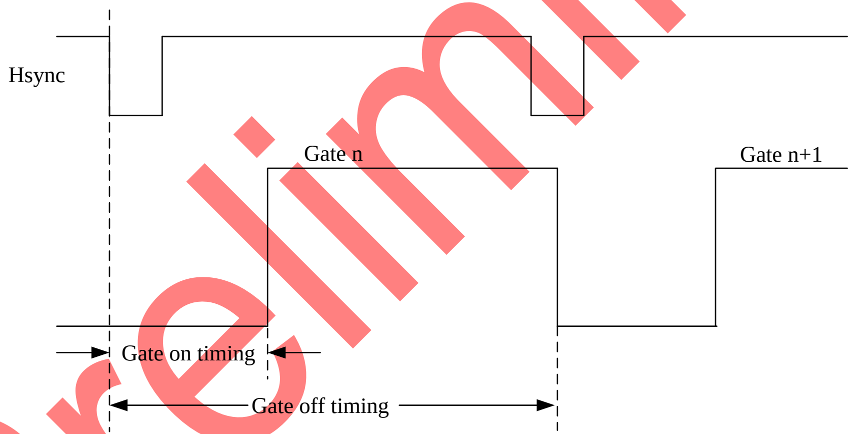
Description



GTA[5:0]: Gate on timing adjustment.

Gate on timing=300ns+GTA[5:0]*400ns

In RGB interface:



In 6bit RGB interface:

Gate on timing=6*3dotclk+GTA[5:0]*4*3dotclk

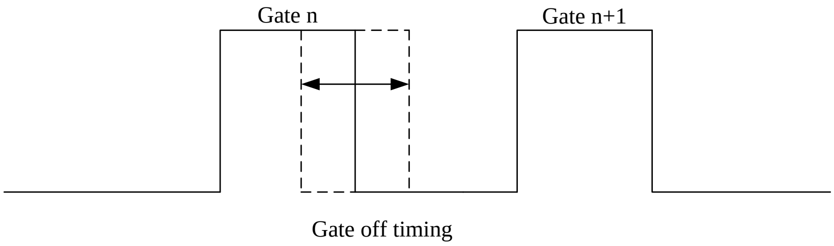
GOFR[3:0]: Gate off timing adjustment only for RGB interface

In 6bit RGB interface:

Gate off timing=512*3dotclk-16dotclk*3*GOFR[3:0]

Note:

In rgb interface, if the setting of gate off timing is more than the number of dotclk in one line, the gate off timing is determined by hsync.

<table>
<tr>
<td></td>
<td>


GOF[3:0]: Gate off timing adjustment
Gate off timing=-GOF[3:0]*400ns
</td>
</tr>
<tr>
<td>Register Availability</td>
<td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
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<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td>
</tr>
<tr>
<td>Default</td>
<td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>2Ah/2Bh/22h/F5h</td></tr>
<tr><td>S/W Reset</td><td>2Ah/2Bh/22h/F5h</td></tr>
<tr><td>H/W Reset</td><td>2Ah/2Bh/22h/F5h</td></tr>
</table>
</td>
</tr>
</table>

9.2.9 DGMEN (BAh): Digital Gamma Enable

BAH	DGMEN (Digital Gamma Enable)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGMEN	0	↑	1	-	1	0	1	1	1	0	1	0	(BAh)
Parameter	1	↑	1	-	0	0	0	0	0	DGMEN	0	0	
Description	**DGMEN:** "0": disable digital gamma. "1": enable digital gamma.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

9.2.10 VCOMS (BBh): VCOMS Setting

BBH	VCOMS (VCOMS Setting)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCOMS	0	↑	1	-	1	0	1	1	1	0	1	1	(BBh)
Parameter	1	↑	1	-	0	0	VCOMS5	VCOMS4	VCOMS3	VCOMS2	VCOMS1	VCOMS0	

Description

VCOMS[5:0]:

VCOMS[5:0]	VCOMS (V)	VCOMS[5:0]	VCOMS (V)
00h	0.1	20h	0.9
01h	0.125	21h	0.925
02h	0.15	22h	0.95
03h	0.175	23h	0.975
04h	0.2	24h	1.0
05h	0.225	25h	1.025
06h	0.25	26h	1.05
07h	0.275	27h	1.075
08h	0.3	28h	1.1
09h	0.325	29h	1.125
0Ah	0.35	2Ah	1.15
0Bh	0.375	2Bh	1.175
0Ch	0.4	2Ch	1.2
0Dh	0.425	2Dh	1.225
0Eh	0.45	2Eh	1.25
0Fh	0.475	2Fh	1.275
10h	0.5	30h	1.3
11h	0.525	31h	1.325
12h	0.55	32h	1.35
13h	0.575	33h	1.375
14h	0.6	34h	1.4
15h	0.625	35h	1.425
16h	0.65	36h	1.45
17h	0.675	37h	1.475
18h	0.7	38h	1.5
19h	0.725	39h	1.525
1Ah	0.75	3Ah	1.55
1Bh	0.775	3Bh	1.575
1Ch	0.8	3Ch	1.6
1Dh	0.825	3Dh	1.625

	1Eh	0.85	3Eh	1.65
	1Fh	0.875	3Fh	1.675

Note:

1. VCOMS is used for feed through voltage compensation.
2. Setting limitation: VCOMS+VCOMS offset+VDV=0.1V~1.675V.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	20h
S/W Reset	20h
H/W Reset	20h

9.2.11 LCMCTRL (C0h): LCM Control

C0H	LCMCTRL (LCM Control)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
LCMCTRL	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)
1st parameter	1	↑	1	-	0	XMY	XBGR	XINV	XMX	XMH	XMV	XGS	

Description

XMY: XOR MY setting in command 36h.

XBGR: XOR RGB setting in command 36h.

XREV: XOR inverse setting in command 21h

XMH: this bit can reverse source output order and only support for RGB interface without RAM mode

XMV: XOR MV setting in command 36h

XMX: XOR MX setting in command 36h.

XGS: XOR GS setting in command E4h.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	2Ch
S/W Reset	2Ch
H/W Reset	2Ch

9.2.12 IDSET (C1h): ID Code Setting

C1H	IDSET (ID Code Setting)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDSET	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
Parameter 1st	1	↑	1	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
Parameter 2nd	1	↑	1	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
Parameter 3rd	1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
Description	**ID1[7:0]:** ID1 Setting. **ID2[7:0]:** ID2 Setting. **ID3[7:0]:** ID3 Setting.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	85h/85h/52h
S/W Reset	85h/85h/52h
H/W Reset	85h/85h/52h

9.2.13 VDVVRHEN (C2h): VDV and VRH Command Enable

C2H	VDVVRHEN (VDV and VRH Command Enable)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VDVVRHEN	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)
1st Parameter	1	↑	1	-	0	0	0	0	0	0	0	CMDEN	
2nd Parameter	1	↑	1	-	1	1	1	1	1	1	1	1	
Description	**CMDEN:** VDV and VRH command write enable. CMDEN=”0”: VDV and VRH register value comes from NVM. CMDEN=”1”, VDV and VRH register value comes from command write.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h/FFh
S/W Reset	01h/FFh
H/W Reset	01h/FFh

9.2.14 VRHS (C3h): VRH Set

C3H	VRHS (VRH Set)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VRHS	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)
1st Parameter	1	↑	1	-	0	0	VRHS5	VRHS4	VRHS3	VRHS2	VRHS1	VRHS0	

Description

VRHS[5:0]: VRH Set.

VRHS[5:0]	VAP(GVDD) (V)	VRHS[5:0]	VAP(GVDD) (V)
00h	3.55+(vcom+vcom offset+vdv)	15h	4.6+(vcom+vcom offset+vdv)
01h	3.6+(vcom+vcom offset+vdv)	16h	4.65+(vcom+vcom offset+vdv)
02h	3.65+(vcom+vcom offset+vdv)	17h	4.7+(vcom+vcom offset+vdv)
03h	3.7+(vcom+vcom offset+vdv)	18h	4.75+(vcom+vcom offset+vdv)
04h	3.75+(vcom+vcom offset+vdv)	19h	4.8+(vcom+vcom offset+vdv)
05h	3.8+(vcom+vcom offset+vdv)	1Ah	4.85+(vcom+vcom offset+vdv)
06h	3.85+(vcom+vcom offset+vdv)	1Bh	4.9+(vcom+vcom offset+vdv)
07h	3.9+(vcom+vcom offset+vdv)	1Ch	4.95+(vcom+vcom offset+vdv)
08h	3.95+(vcom+vcom offset+vdv)	1Dh	5+(vcom+vcom offset+vdv)
09h	4+(vcom+vcom offset+vdv)	1Eh	5.05+(vcom+vcom offset+vdv)
0Ah	4.05+(vcom+vcom offset+vdv)	1Fh	5.1+(vcom+vcom offset+vdv)
0Bh	4.1+(vcom+vcom offset+vdv)	20h	5.15+(vcom+vcom offset+vdv)
0Ch	4.15+(vcom+vcom offset+vdv)	21h	5.2+(vcom+vcom offset+vdv)
0Dh	4.2+(vcom+vcom offset+vdv)	22h	5.25+(vcom+vcom offset+vdv)
0Eh	4.25+(vcom+vcom offset+vdv)	23h	5.3+(vcom+vcom offset+vdv)
0Fh	4.3+(vcom+vcom offset+vdv)	24h	5.35+(vcom+vcom offset+vdv)
10h	4.35+(vcom+vcom offset+vdv)	25h	5.4+(vcom+vcom offset+vdv)
11h	4.4+(vcom+vcom offset+vdv)	26h	5.45+(vcom+vcom offset+vdv)
12h	4.45+(vcom+vcom offset+vdv)	27h	5.5+(vcom+vcom offset+vdv)
13h	4.5+(vcom+vcom offset+vdv)	28h~3Fh	Reserved
14h	4.55+(vcom+vcom offset+vdv)	--	--

VRHS[5:0]	VAN(GVCL) (V)	VRHS[5:0]	VAN(GVCL) (V)
00h	-3.55+(vcom+vcom offset-vdv)	15h	-4.6+(vcom+vcom offset-vdv)
01h	-3.6+(vcom+vcom offset-vdv)	16h	-4.65+(vcom+vcom offset-vdv)
02h	-3.65+(vcom+vcom offset-vdv)	17h	-4.7+(vcom+vcom offset-vdv)
03h	-3.7+(vcom+vcom offset-vdv)	18h	-4.75+(vcom+vcom offset-vdv)
04h	-3.75+(vcom+vcom offset-vdv)	19h	-4.8+(vcom+vcom offset-vdv)
05h	-3.8+(vcom+vcom offset-vdv)	1Ah	-4.85+(vcom+vcom offset-vdv)
06h	-3.85+(vcom+vcom offset-vdv)	1Bh	-4.9+(vcom+vcom offset-vdv)

07h	-3.9+(vcom+vcom offset-vdv)	1Ch	-4.95+(vcom+vcom offset-vdv)
08h	-3.95+(vcom+vcom offset-vdv)	1Dh	-5+(vcom+vcom offset-vdv)
09h	-4+(vcom+vcom offset-vdv)	1Eh	-5.05+(vcom+vcom offset-vdv)
0Ah	-4.05+(vcom+vcom offset-vdv)	1Fh	-5.1+(vcom+vcom offset-vdv)
0Bh	-4.1+(vcom+vcom offset-vdv)	20h	-5.15+(vcom+vcom offset-vdv)
0Ch	-4.15+(vcom+vcom offset-vdv)	21h	-5.2+(vcom+vcom offset-vdv)
0Dh	-4.2+(vcom+vcom offset-vdv)	22h	-5.25+(vcom+vcom offset-vdv)
0Eh	-4.25+(vcom+vcom offset-vdv)	23h	-5.3+(vcom+vcom offset-vdv)
0Fh	-4.3+(vcom+vcom offset-vdv)	24h	-5.35+(vcom+vcom offset-vdv)
10h	-4.35+(vcom+vcom offset-vdv)	25h	-5.4+(vcom+vcom offset-vdv)
11h	-4.4+(vcom+vcom offset-vdv)	26h	-5.45+(vcom+vcom offset-vdv)
12h	-4.45+(vcom+vcom offset-vdv)	27h	-5.5+(vcom+vcom offset-vdv)
13h	-4.5+(vcom+vcom offset-vdv)	28h~3Fh	Reserved
14h	-4.55+(vcom+vcom offset-vdv)	--	--

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0Bh
S/W Reset	0Bh
H/W Reset	0Bh

9.2.15 VDVS (C4h): VDV Set

C4H	VDVS (VDV Set)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VDVS	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)
1st Parameter	1	↑	1	-	0	0	VDVS5	VDVS4	VDVS3	VDVS2	VDVS1	VDVS0	

Description

VDVS[5:0]: VDV Set.

VDVS[5:0]	VDV (V)	VDVS[5:0]	VDV (V)
00h	-0.8	20h	0
01h	-0.775	21h	0.025
02h	-0.75	22h	0.05
03h	-0.725	23h	0.075
04h	-0.7	24h	0.1
05h	-0.675	25h	0.125
06h	-0.65	26h	0.15
07h	-0.625	27h	0.175
08h	-0.6	28h	0.2
09h	-0.575	29h	0.225
0Ah	-0.55	2Ah	0.25
0Bh	-0.525	2Bh	0.275
0Ch	-0.5	2Ch	0.3
0Dh	-0.475	2Dh	0.325
0Eh	-0.45	2Eh	0.35
0Fh	-0.425	2Fh	0.375
10h	-0.4	30h	0.4
11h	-0.375	31h	0.425
12h	-0.35	32h	0.45
13h	-0.325	33h	0.475
14h	-0.3	34h	0.5
15h	-0.275	35h	0.525
16h	-0.25	36h	0.55
17h	-0.225	37h	0.575
18h	-0.2	38h	0.6
19h	-0.175	39h	0.625
1Ah	-0.15	3Ah	0.65
1Bh	-0.125	3Bh	0.675
1Ch	-0.1	3Ch	0.7
1Dh	-0.075	3Dh	0.725

<table>
<tr><td></td><td>

1Eh	-0.05	3Eh	0.75
1Fh	-0.025	3Fh	0.775

Note:
Setting limitation: VCOMS+VCOMS offset+VDV=0.1V~1.675V</td></tr>
<tr><td>Register Availability</td><td>

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

</td></tr>
<tr><td>Default</td><td>

Status	Default Value
Power On Sequence	20h
S/W Reset	20h
H/W Reset	20h

</td></tr>
</table>

9.2.16 VCMOFSET (C5h): VCOMS Offset Set

C5H	VCMOFSET (VCOMS Offset Set)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCMOFSET	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1st Parameter	1	↑	1	-	0	0	VCMOFS5	VCMOFS4	VCMOFS3	VCMOFS2	VCMOFS1	VCMOFS0	

Description

VCOMS offset setting:

VCMOFS[5:0]	VCOMS OFFSET (V)	VCMOFS[5:0]	VCOMS OFFSET(V)
00h	-0.8	20h	0
01h	-0.775	21h	0.025
02h	-0.75	22h	0.05
03h	-0.725	23h	0.075
04h	-0.7	24h	0.1
05h	-0.675	25h	0.125
06h	-0.65	26h	0.15
07h	-0.625	27h	0.175
08h	-0.6	28h	0.2
09h	-0.575	29h	0.225
0Ah	-0.55	2Ah	0.25
0Bh	-0.525	2Bh	0.275
0Ch	-0.5	2Ch	0.3
0Dh	-0.475	2Dh	0.325
0Eh	-0.45	2Eh	0.35
0Fh	-0.425	2Fh	0.375
10h	-0.4	30h	0.4
11h	-0.375	31h	0.425
12h	-0.35	32h	0.45
13h	-0.325	33h	0.475
14h	-0.3	34h	0.5
15h	-0.275	35h	0.525
16h	-0.25	36h	0.55
17h	-0.225	37h	0.575
18h	-0.2	38h	0.6
19h	-0.175	39h	0.625
1Ah	-0.15	3Ah	0.65
1Bh	-0.125	3Bh	0.675
1Ch	-0.1	3Ch	0.7
1Dh	-0.075	3Dh	0.725

	1Eh	-0.05	3Eh	0.75
	1Fh	-0.025	3Fh	0.775
	Note: Setting limitation: VCOMS+VCOMS offset+VDV=0.1V~1.675V			

	Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

	Status	Default Value
Default	Power On Sequence	20h
	S/W Reset	20h
	H/W Reset	20h

9.2.17 FRCTRL2 (C6h): Frame Rate Control in Normal Mode

C6H	FRCTRL2 (Frame Rate Control in Normal Mode)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRCTRL2	0	↑	1	-	1	1	0	0	0	1	1	0	(C6h)
1st Parameter	1	↑	1	-	NLA2	NLA1	NLA0	RTNA4	RTNA3	RTNA2	RTNA1	RTNA0	

Description

NLA[2 :0] : Inversion selection in normal mode.

0x00 : dot inversion.

0x07: column inversion.

RTNA[4:0]:

RTNA[4:0]	FR in normal mode (Hz)	RTNA[4:0]	FR in normal mode (Hz)
00h	119	10h	58
01h	111	11h	57
02h	105	12h	55
03h	99	13h	53
04h	94	14h	52
05h	90	15h	50
06h	86	16h	49
07h	82	17h	48
08h	78	18h	46
09h	75	19h	45
0Ah	72	1Ah	44
0Bh	69	1Bh	43
0Ch	67	1Ch	42
0Dh	64	1Dh	41
0Eh	62	1Eh	40
0Fh	60	1Fh	39

Note:

1. Frame rate=10MHz/(320+FPA[6:0]+BPA[6:0])*(250+RTNA[4:0]*16).
2. FPA[6:0] and BPA[6:0] are in command B2h
3. In this frame rate table, FPA[6:0]=0Ch, BPA[6:0]=0Ch
4. The deviation of frame rate is +/- 5%.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

		Sleep In	Yes
Default			

Status	Default Value
Power On Sequence	0Fh
S/W Reset	0Fh
H/W Reset	0Fh

9.2.18 CABCCTRL (C7h): CABC Control

C7H	CABCCTRL (CABC Control)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CABCCTRL	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)
1st Parameter	1	↑	1	-	0	0	0	0	LEDONREV	DPOFPWM	PWMFIX	PWMPOL	

Description:

LEDONREV: Reverse the status of LED_ON:

"0": keep the status of LED_ON.

"1": reverse the status of LED_ON.

DPOFPWM: initial state control of LEDPWM.

"0": The initial state of LEDPWM is low.

"1": The initial state of LEDPWM is high.

PWMFIX: LEDPWM fix control.

"0": LEDPWM control by CABC.

"1": fix LEDPWM in "ON" status.

PWMPOL: LEDPWM polarity control.

"0": polarity high.

"1": polarity low.

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default:

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

9.2.19 REGSEL1 (C8h): Register Value Selection 1

C8H	REGSEL1 (Register Value Selection 1)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
REGSEL1	0	↑	1	-	1	1	0	0	1	0	0	0	(C8h)
Parameter	1	↑	1	-	0	0	0	0	1	0	0	0	
Description	Reserved for testing												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

9.2.20 REGSEL2 (CAh): Register Value Selection 2

CAH	REGSEL2 (Register Value Selection 2)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
REGSEL2	0	↑	1	-	1	1	0	0	1	0	1	0	(CAh)
Parameter	1	↑	1	-	0	0	0	0	1	1	1	1	
Description	Reserved for testing												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0Fh
S/W Reset	0Fh
H/W Reset	0Fh

9.2.21 PWMFRSEL (CCh): PWM Frequency Selection

CCH	PWMFRSEL (PWM Frequency Selection)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWMFRSEL	0	↑	1	-	1	1	0	0	1	1	0	0	(CCh)
1st Parameter	1	↑	1	-	0	0	CS2	CS1	CS0	CLK2	CLK1	CLK0	

Description

CS[2:0]/CLK[2:0]:

CLK[2:0] \ CS[2:0]	00h	01h	02h	03h	04h	05h
00h	39.2	78.7	158.7	322.6	666.7	1428.6
01h	19.6	39.4	79.4	161.3	333.3	714.3
02h	9.8	19.7	39.7	80.6	166.7	357.1
03h	4.9	9.8	19.8	40.3	83.3	178.6
04h	2.45	4.9	9.9	20.2	41.7	89.3
05h	1.23	2.5	5	10.1	20.8	44.6
06h	0.61	1.23	2.48	5	10.4	22.3
07h	0.31	0.62	1.24	2.5	5.2	11.2

Unit: kHz

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	02h
S/W Reset	02h
H/W Reset	02h

9.2.22 PWCTRL1 (D0h): Power Control 1

D0H	PWCTRL (Power Control)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTRL	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)
1st Parameter	1	↑	1	-	1	0	1	0	0	1	0	0	
2nd Parameter	1	↑	1	-	AVDD1	AVDD0	AVCL1	AVCL0	0	0	VDS1	VDS0	

Description:

AVDD[1:0]:

AVDD[1:0]	AVDD (V)
00h	6.4
01h	6.6
02h	6.8
03h	Reserved

AVCL[1:0]:

AVCL[1:0]	AVCL (V)
00h	-4.4
01h	-4.6
02h	-4.8
03h	-5.0

VDS[1:0]:

VDS[1:0]	VDDS (V)
00h	2.19
01h	2.3
02h	2.4
03h	2.51

VDDS: Power of source OP

Register Availability:

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>A4h/81h</td></tr><tr><td>S/W Reset</td><td>A4h/81h</td></tr><tr><td>H/W Reset</td><td>A4h/81h</td></tr></table>

9.2.23 VAPVANEN (D2h): Enable VAP/VAN signal output

D2H	VAPVANEN (Enable VAP/VAN signal output)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VAPVANEN	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)
1st Parameter	1	↑	1	-	0	1	0	0	0	0	0	0	(40h)
2nd Parameter	1	↑	1	-	0	0	1	1	0	0	0	0	(30h)
Description	Enable VAP/VAN signal output												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

9.2.24 CMD2EN (DFh): Command 2 Enable

DFH	CMD2EN (Command 2 Enable)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CMD2EN	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)
1st Parameter	1	↑	1	-	0	1	0	1	1	0	1	0	(5Ah)
2nd Parameter	1	↑	1	-	0	1	1	0	1	0	0	1	(69h)
3rd Parameter	1	↑	1	-	0	0	0	0	0	0	1	0	(02h)
4th Parameter	1	↑	1	-	DSTB	0	0	0	PRGMD	0	0	EN	

Description

EN:

"0": Commands in Command table 2 cannot be executed when EXTC level is "Low".

"1": Commands in command table 2 can be executed when EXTC level is "Low".

PRGMD:

"0": For external VPP mode

"1": For internal VPP mode

DSTB:

"0": No function.

"1": Trigger IC enter the deep standby mode when DSTBMD=1.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	5Ah/69h/02h/00h
S/W Reset	5Ah/69h/02h/00h
H/W Reset	5Ah/69h/02h/00h

9.2.25 PVGAMCTRL (E0h): Positive Voltage Gamma Control

E0H	PVGAMCTRL (Positive Voltage Gamma Control)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PVGAMCTRL	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1st Parameter	1	↑	1	-	V63P3	V63P2	V63P1	V63P0	V0P3	V0P2	V0P1	V0P0	
2nd Parameter	1	↑	1	-	0	0	V1P5	V1P4	V1P3	V1P2	V1P1	V1P0	
3rd Parameter	1	↑	1	-	0	0	V2P5	V2P4	V2P3	V2P2	V2P1	V2P0	
4th Parameter	1	↑	1	-	0	0	0	V4P4	V4P3	V4P2	V4P1	V4P0	
5th Parameter	1	↑	1	-	0	0	0	V6P4	V6P3	V6P2	V6P1	V6P0	
6th Parameter	1	↑	1	-	0	0	J0P1	J0P0	V13P3	V13P2	V13P1	V13P0	
7th Parameter	1	↑	1	-	0	V20P6	V20P5	V20P4	V20P3	V20P2	V20P1	V20P0	
8th Parameter	1	↑	1	-	0	V36P2	V36P1	V36P0	0	V27P2	V27P1	V27P0	
9th Parameter	1	↑	1	-	0	V43P6	V43P5	V43P4	V43P3	V43P2	V43P1	V43P0	
10th Parameter	1	↑	1	-	0	0	J1P1	J1P0	V50P3	V50P2	V50P1	V50P0	
11th Parameter	1	↑	1	-	0	0	0	V57P4	V57P3	V57P2	V57P1	V57P0	
12th Parameter	1	↑	1	-	0	0	0	V59P4	V59P3	V59P2	V59P1	V59P0	
13th Parameter	1	↑	1	-	0	0	V61P5	V61P4	V61P3	V61P2	V61P1	V61P0	
14th Parameter	1	↑	1	-	0	0	V62P5	V62P4	V62P3	V62P2	V62P1	V62P0	

Description

Please refer to 8.19.

Default value:

	Value(hex)
VP0[3:0]	0
VP1[5:0]	0
VP2[5:0]	2
VP4[4:0]	7
VP6[4:0]	B
VP13[3:0]	A
VP20[6:0]	31
VP27[2:0]	4
VP36[2:0]	5
VP43[6:0]	40
VP50[3:0]	9
VP57[4:0]	12
VP59[4:0]	12
VP61[5:0]	12
VP62[5:0]	17
VP63[3:0]	D

	JP0[1:0]	1
	JP1[1:0]	2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to description
S/W Reset	Refer to description
H/W Reset	Refer to description

9.2.26 NVGAMCTRL (E1h): Negative Voltage Gamma Control

E1H	NVGAMCTRL (Negative Voltage Gamma Control)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVGAMCTRL	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)
1st Parameter	1	↑	1	-	V63N3	V63N2	V63N1	V63N0	V0N3	V0N2	V0N1	V0N0	
2nd Parameter	1	↑	1	-	0	0	V1N5	V1N4	V1N3	V1N2	V1N1	V1N0	
3rd Parameter	1	↑	1	-	0	0	V2N5	V2N4	V2N3	V2N2	V2N1	V2N0	
4th Parameter	1	↑	1	-	0	0	0	V4N4	V4N3	V4N2	V4N1	V4N0	
5th Parameter	1	↑	1	-	0	0	0	V6N4	V6N3	V6N2	V6N1	V6N0	
6th Parameter	1	↑	1	-	0	0	J0N1	J0N0	V13N3	V13N2	V13N1	V13N0	
7th Parameter	1	↑	1	-	0	V20N6	V20N5	V20N4	V20N3	V20N2	V20N1	V20N0	
8th Parameter	1	↑	1	-	0	V36N2	V36N1	V36N0	0	V27N2	V27N1	V27N0	
9th Parameter	1	↑	1	-	0	V43N6	V43N5	V43N4	V43N3	V43N2	V43N1	V43N0	
10th Parameter	1	↑	1	-	0	0	J1N1	J1N0	V50N3	V50N2	V50N1	V50N0	
11th Parameter	1	↑	1	-	0	0	0	V57N4	V57N3	V57N2	V57N1	V57N0	
12th Parameter	1	↑	1	-	0	0	0	V59N4	V59N3	V59N2	V59N1	V59N0	
13th Parameter	1	↑	1	-	0	0	V61N5	V61N4	V61N3	V61N2	V61N1	V61N0	
14th Parameter	1	↑	1	-	0	0	V62N5	V62N4	V62N3	V62N2	V62N1	V62N0	

Description

Please refer to 8.19.

Default value:

	Value(hex)
VN0[3:0]	0
VN1[5:0]	0
VN2[5:0]	2
VN4[4:0]	7
VN6[4:0]	5
VN13[3:0]	5
VN20[6:0]	2D
VN27[2:0]	4
VN36[2:0]	4
VN43[6:0]	44
VN50[3:0]	C
VN57[4:0]	18
VN59[4:0]	16
VN61[5:0]	1C
VN62[5:0]	1D
VN63[3:0]	D

	JN0[1:0]	2
	JN1[1:0]	1

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to description
S/W Reset	Refer to description
H/W Reset	Refer to description

9.2.27 DGMLUTR (E2h): Digital Gamma Look-up Table for Red

E2H	DGMLUTR (Digital Gamma Look-up Table for Red)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGMLUTR	0	↑	1	-	1	1	1	0	0	0	1	0	(E2h)
1st Parameter	1	↑	1	-	DGM_LUT_R00[7:0]								
2nd Parameter	1	↑	1	-	DGM_LUT_R01[7:0]								
⋮	1	↑	1	-	⋮								
31th Parameter	1	↑	1	-	DGM_LUT_R30[7:0]								
32th Parameter	1	↑	1	-	DGM_LUT_R31[7:0]								
⋮	1	↑	1	-	⋮								
63th Parameter	1	↑	1	-	DGM_LUT_R62[7:0]								
64th Parameter	1	↑	1	-	DGM_LUT_R63[7:0]								

Description

Please refer to 8.20.

Default value:

	Value(hex)
DGM_LUT_R00[7:0]	00h
DGM_LUT_R01[7:0]	04h
⋮	⋮
DGM_LUT_R30[7:0]	78h
DGM_LUT_R31[7:0]	7Ch
⋮	⋮
DGM_LUT_R62[7:0]	F8h
DGM_LUT_R63[7:0]	FCh

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to description
S/W Reset	Refer to description

		H/W Reset	Refer to description

9.2.28 DGMLUTB (E3h): Digital Gamma Look-up Table for Blue

E3H	DGMLUTB (Digital Gamma Look-up Table for Blue)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGMLUTB	0	↑	1	-	1	1	1	0	0	0	1	1	(E3h)
1st Parameter	1	↑	1	-	DGM_LUT_B00[7:0]								
2nd Parameter	1	↑	1	-	DGM_LUT_B01[7:0]								
:	1	↑	1	-	:								
31th Parameter	1	↑	1	-	DGM_LUT_B30[7:0]								
32th Parameter	1	↑	1	-	DGM_LUT_B31[7:0]								
:	1	↑	1	-	:								
63th Parameter	1	↑	1	-	DGM_LUT_B62[7:0]								
64th Parameter	1	↑	1	-	DGM_LUT_B63[7:0]								

Description

Please refer to 8.20.

Default value:

	Value(hex)
DGM_LUT_B00[7:0]	00h
DGM_LUT_B01[7:0]	04h
:	:
DGM_LUT_B30[7:0]	78h
DGM_LUT_B31[7:0]	7Ch
:	:
DGM_LUT_B62[7:0]	F8h
DGM_LUT_B63[7:0]	FCh

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Refer to description
S/W Reset	Refer to description

		H/W Reset	Refer to description

9.2.29 GATECTRL (E4h): Gate Control

E4H	GATECTRL (Gate Control)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GATECTRL	0	↑	1	-	1	1	1	0	0	1	0	0	(E4h)
1st Parameter	1	↑	1	-	0	0	NL5	NL4	NL3	NL2	NL1	NL0	
2nd Parameter	1	↑	1	-	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	
3rd Parameter	1	↑	1	-	0	0	0	TMG	0	SM	0	GS	

Description

NL[5:0]: Set the number of gate line.

NL[5:0]	The number of gate line
0x00	8 gate line
0x01	16 gate line
0x02	24 gate line
⋮	⋮
0x27	320 gate line

SCN[5:0]: set the first scan line

SCN[5:0]	The first scan line
0x00	Gate 0
0x01	Gate 8
⋮	⋮
0x27	Gate 312

TMG: Gate scan mirror mode selection

"TMG=0": when GS=1, gate scan will local mirror (mirror by gate line setting).

"TMG=1": when GS=1, gate scan will full mirror (mirror by 320 gate lines).

SM: Gate interlace mode selection

SM="0": Gate scan using interlace mode.

SM="1": Gate scan using non-interlace mode.

GS: Gate scan direction

GS="0": Gate scan direction is 0→319

GS="1": Gate scan direction is 319→0

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>27h/00h/10h</td></tr><tr><td>S/W Reset</td><td>27h/00h/10h</td></tr><tr><td>H/W Reset</td><td>27h/00h/10h</td></tr></table>

9.2.30 SPI2EN (E7h): SPI2 Enable

E7H	SPI2EN (SPI2 Enable)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SPI2EN	0	↑	1	-	1	1	1	0	0	1	1	1	(E7h)
Parameter	1	↑	1	-	0	0	0	SPI2EN	0	0	0	SPIRD	
Description	**SPI2EN:** 2 data lane enable control. "0": disable 2 data lane mode. "1": enable 2 data lane mode **SPIRD:** SPI read enable for command table 2 "0": commands in command table 2 cannot be read in serial interface "1": commands in command table 2 can be read in serial interface. Note: It needs one dummy clock if commands in command table 2 need to be read in serial interface.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

9.2.31 PWCTRL2 (E8h): Power Control 2

E8H	PWCTRL2 (Power Control 2)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTRL2	0	↑	1	-	1	1	1	0	1	0	0	0	(E8h)
Parameter	1	↑	1	-	1	0	SBCLK1	SBCLK0	0	0	STP14CK1	STP14CK0	

Description

SBCLK[1:0]: Source booster clock selection

SBCLK[1:0]	
00h	SBCLK DIV 2
01h	SBCLK DIV 3
02h	SBCLK DIV 4
03h	SBCLK DIV 6

STP14CK[1:0]:STP14(AVDD/AVCL) booster clock selection

STP14CK[1:0]	
00h	BCLK DIV 2
01h	BCLK DIV 3
02h	BCLK DIV 4
03h	BCLK DIV 6

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	93h
S/W Reset	93h
H/W Reset	93h

9.2.32 EQCTRL (E9h): Equalize time control

E9H	EQCTRL (Equalize time Control)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EQCTRL	0	↑	1	-	1	1	1	0	1	0	0	1	(E9h)
1st Parameter	1	↑	1	-	0	0	0	SEQ4	SEQ3	SEQ2	SEQ1	SEQ0	
2nd Parameter	1	↑	1	-	0	0	0	SPRET4	SPRET3	SPRET2	SPRET1	SPRET0	
3rd Parameter	1	↑	1	-	0	0	0	0	GEQ3	GEQ2	GEQ1	GEQ0	

Description

SEQ[4:0]:Source Equalize Time

Source equalize time: SEQ[4:0]*400ns, SEQ[4:0]=0x01~0x1f

In 6bit RGB interface:

Source equalize time: SEQ[4:0]*4*3*1period of dotclk, SEQ[4:0]=0x01~0x1f

SPRET[4:0]: Source Pre-drive Time

Source pre-drive time: SPRET[4:0]*400ns, SPRET[4:0]=0x01~0x1f

In 6bit RGB interface:

Source equalize time: SPRET[4:0]*4*3*1period of dotclk, SPRET[4:0]=0x01~0x1f

GEQ[3:0]: Gate Equalize Time

Gate equalize time: GEQ[3:0]*400ns, GEQ[3:0]=0x00~0x0f

In 6bit RGB interface:

Gate equalize time: GEQ[3:0]*4*3*1period of dotclk, GEQ[3:0]=0x00~0x0f

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	11h/11h/08h
S/W Reset	11h/11h/08h
H/W Reset	11h/11h/08h

9.2.33 PROMCTRL (ECh): Program Mode Control

ECH	PROMCTRL (Program Mode Control)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PROMCTRL	0	↑	1	-	1	1	1	0	1	1	0	0	(ECh)
Parameter	1	↑	1	-	0	0	0	0	0	0	0	1	
Description	When program mode enable, this command need be set.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

9.2.34 PROMEN (FAh): Program Mode Enable

FAH	PROMEN (Program Mode Enable)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PROMEN	0	↑	1	-	1	1	1	1	1	0	1	0	(Fah)
1st Parameter	1	↑	1	-	0	1	0	1	1	0	1	0	(5Ah)
2nd Parameter	1	↑	1	-	0	1	1	0	1	0	0	1	(69h)
3rd Parameter	1	↑	1	-	1	1	1	0	1	1	1	0	(EEh)
4th Parameter	1	↑	1	-	VPPINTMD	0	0	0	0	PROMEN	0	0	

Description

PROMEN:

“0”: Program mode disable

“1”: Program mode enable

VPPINTMD:

“0”: Internal VPP mode disable

“1”: Internal VPP mode enable

Note: Host has to delay 40msec after VPPINTMD=1

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

9.2.35 NVMSET (FCh): NVM Setting

FCH	NVMSET (NVM Setting)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVMSET	0	↑	1	-	1	1	1	1	1	1	0	0	(FCh)
1st Parameter	1	↑	1	-	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	
2nd Parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0	
Description	**ADD[7:0]:** NVM address setting **D[7:0]:** Data setting of NVM address												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h/00h
S/W Reset	00h/00h
H/W Reset	00h/00h

9.2.36 PROMACT (FEh): Program action

FEH	PROMACT (Program action)											
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PROMACT	0	↑	1	-	1	1	1	1	1	1	1	0	(FEh)
1st Parameter	1	↑	1	-	0	0	1	0	1	0	0	1	(29h)
2nd Parameter	1	↑	1	-	1	0	1	0	0	1	0	1	(A5h)
Description	When program mode enable, this command need be set.												

Register Availability

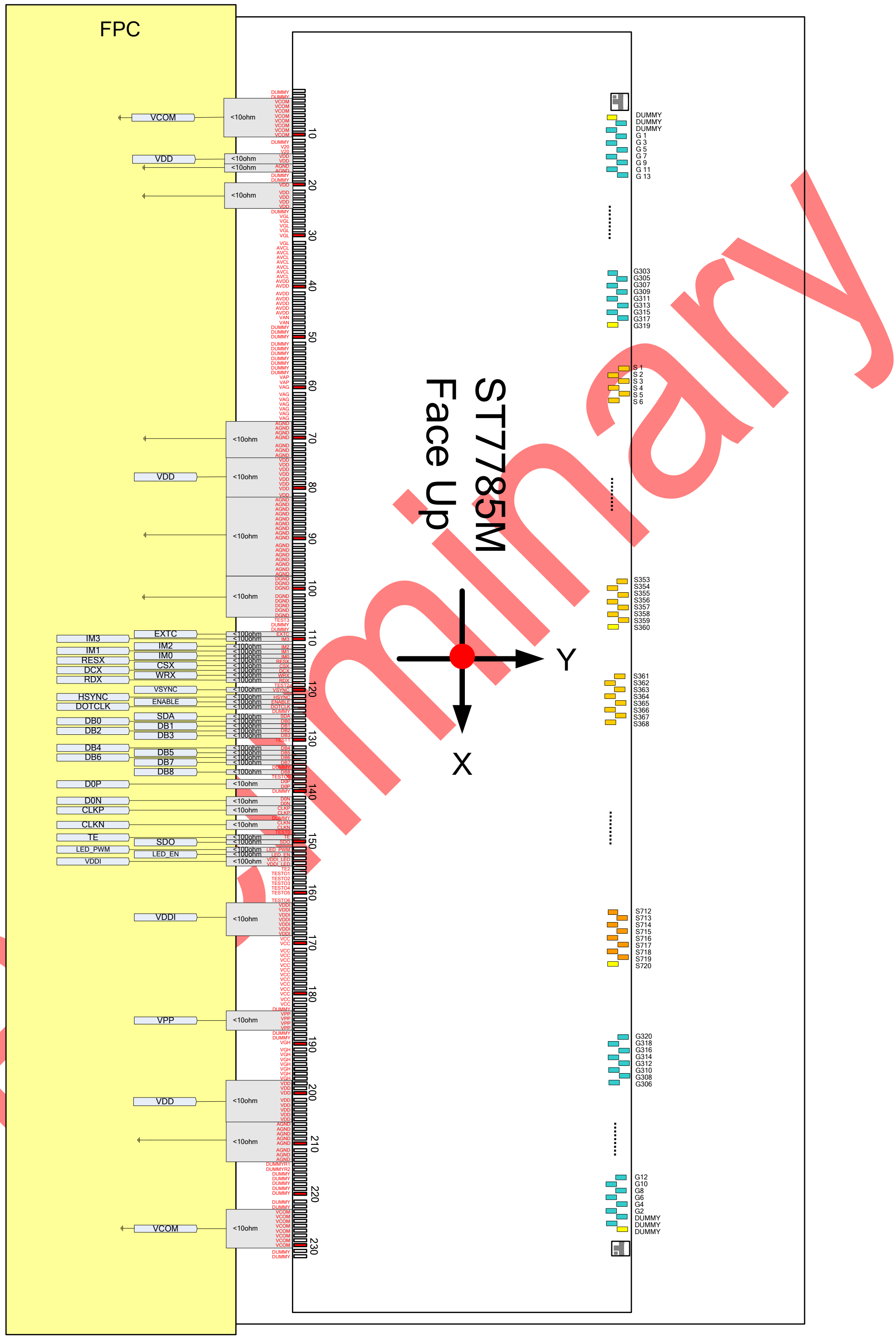
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h/00h
S/W Reset	00h/00h
H/W Reset	00h/00h

10 APPLICATION

10.1 Configuration of Power Supply Circuit



10.2 Voltage Generation

The following is the ST7785M analog voltage pattern diagram:

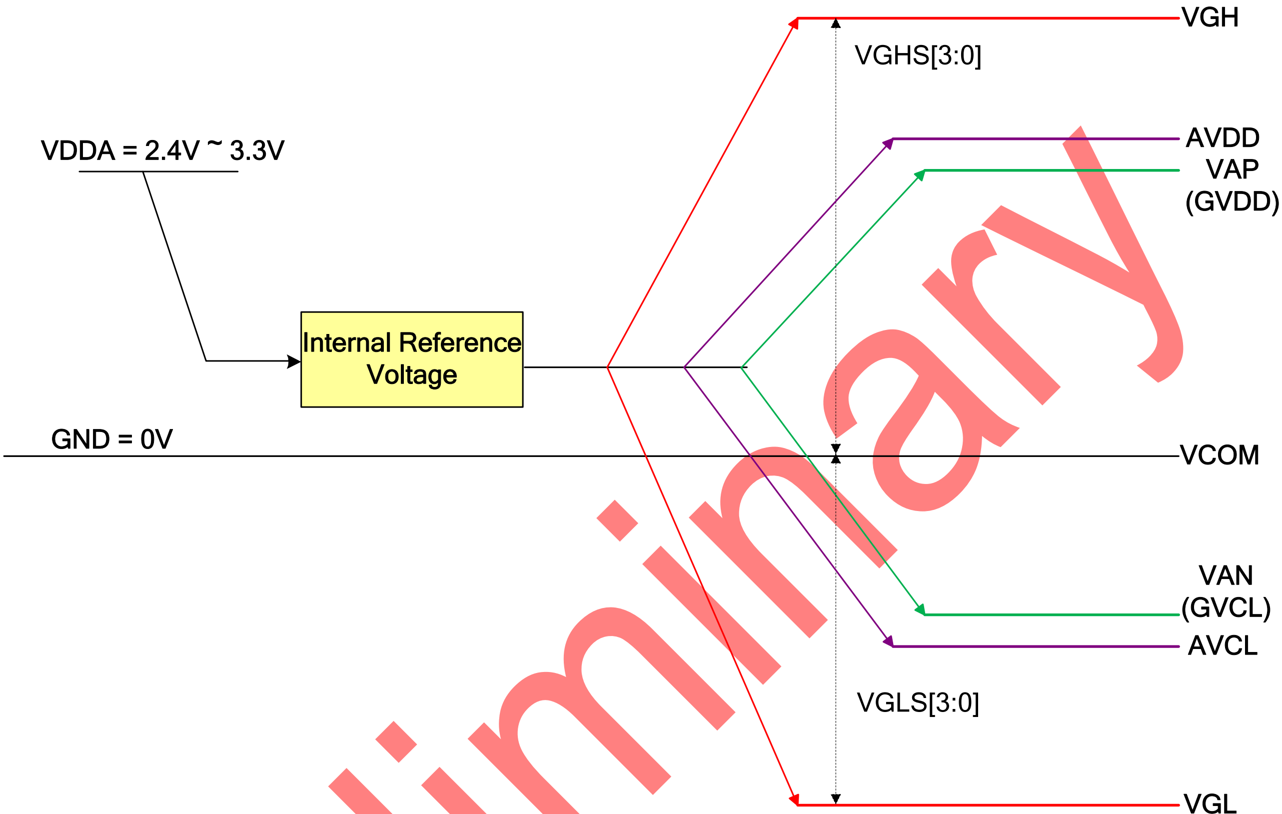


Figure 105 Power Booster Level

10.3 Relationship about source voltage

The relationship about source voltage is shown as below:

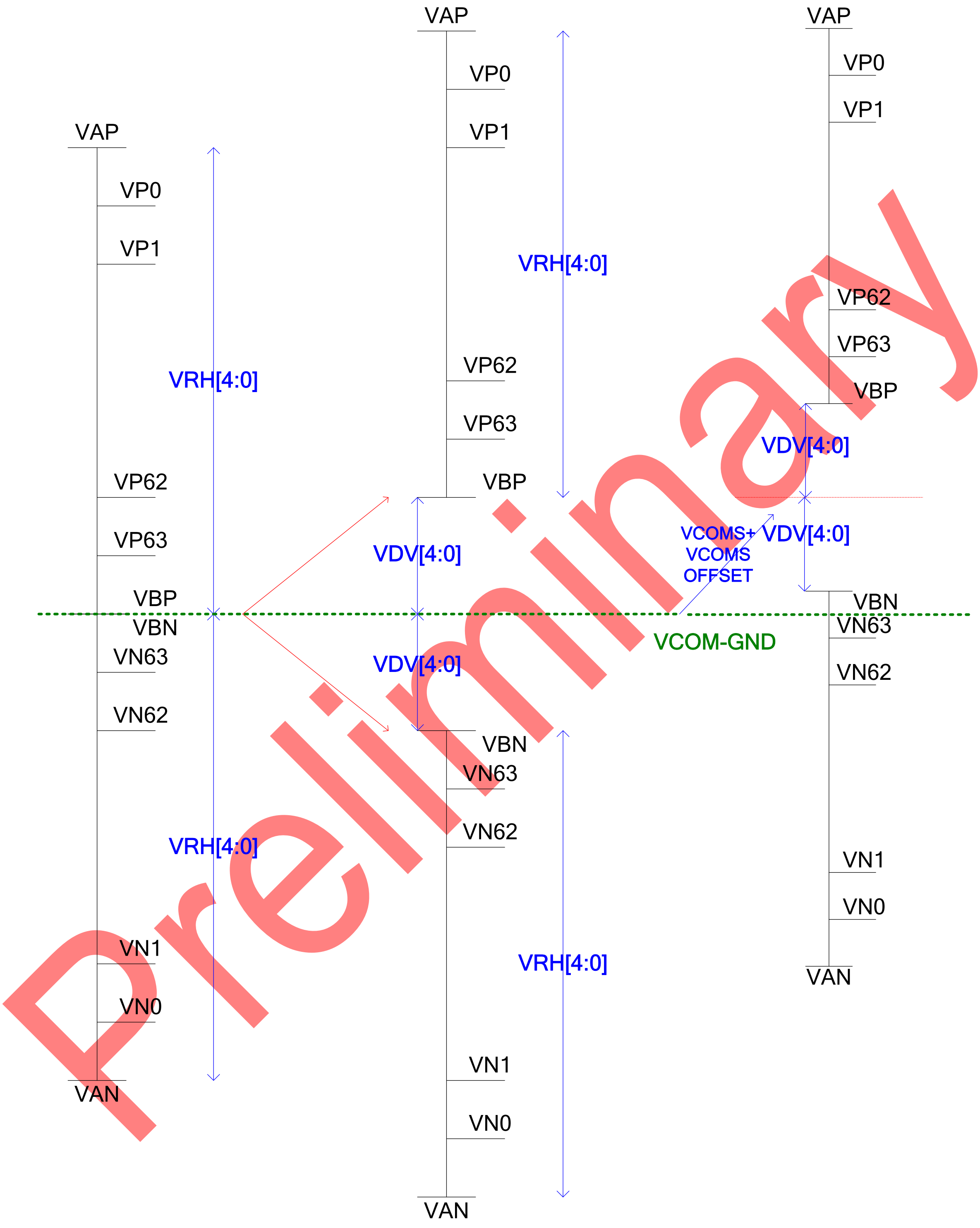


Figure 106 Relationship about source voltage

Note: if VDV=0V, VBP=VBN=VCOM+VCOM OFFSET.

10.4 Applied Voltage to the TFT panel

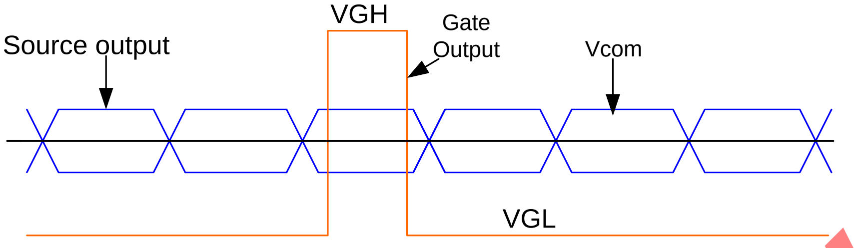


Figure 107 Voltage Output to TFT LCD Panel

11 REVISION HISTORY

Version	Date	Description
V0.0	2020/01	First issue