ST7796U

320RGB x 480 dot 16.7M Color with Frame Memory Single-Chip TFT Controller/Driver

Datasheet

Version V1.0

2020/02

Sitronix Technology Corporation

LIST OF CONTENT

1 GENERAL DESCRIPTION

The ST7796U is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 960 source lines and 480 gate lines driving circuits. The ST7796U is capable of connecting directly to an external microprocessor, and accepts 8-bit/9-bit/16-bit/18-bit parallel interface, SPI, and the ST7796U also provides MIPI interface. Display data can be stored in the on-chip display data RAM of 320x480x18 bits. It can perform display data RAM read-/write-operation with no external clock to minimize power consumption. In addition, because of the integrated power supply circuit necessary to drive liquid crystal; it is possible to make a display system with fewest components.

2 FEATURES

- Single chip TFT-LCD Controller/Driver with On-chip Frame Memory
- Display Resolution: 320*RGB (H) *480(V)
- Frame Memory Size: 320 x 480 x 18-bit = 2,764,800 bits
- LCD Driver Output Circuits
  - Source Outputs: 320 RGB Channels
  - Gate Outputs: 480 Channels
  - Common Electrode Output
- Display Colors (Color Mode)
  - Full Color: 16M, RGB=(888) max., Idle Mode Off
  - Color Reduce: 8-color, RGB=(111), Idle Mode On
- Programmable Pixel Color Format (Color Depth) for Various Display Data Input Format
  - 16-bit/pixel: RGB=(565) 65K color
  - 18-bit/pixel: RGB=(666) 262K color
  - 24-bit/pixel: RGB=(888) 16M color
- Interface
  - Parallel 8080-series MCU Interface (8-bit, 9-bit, 16-bit, and 18-bit)
  - 16/18 RGB Interface (VSYNCX, HSYNCX, DOTCLK, ENABLE, DB[17:0])
  - Serial Peripheral Interface (SPI Interface)
  - MIPI
- Display Features
  - Partial Display Function
  - 8-color Display Function
  - Vertical Scroll Function
- Support LC Type Option
  - MVA LC Type
  - Transflective LC Type
  - Transmissive LC Type
- On Chip Build-In Circuits
  - DC/DC Converter
  - Non-Volatile (NV) Memory to Store Initial Register Setting and Factory Default Value (Module ID, Module Version, etc)
  - Internal Oscillator for Display Clock Generation
  - Timing Controller
- Build-In NV Memory for LCD Initial Register Setting
  - 8-bit for ID1
  - 8-bit for ID2

- 8-bit for ID3
- 6-bit for flicker adjustment

● Driving Algorithm

- Dot Inversion
- Column Inversion

● Wide Supply Voltage Range

- I/O Voltage (VDDI to DGND): 1.65V ~ 3.3V (VDDI≦VDD)
- Voltage for Digital Circuit (VDD to DGND): 2.5V ~ 3.3V
- Voltage for Analog Circuit (VDDA to AGND): 2.5V ~ 3.3V

● On-Chip Power System

- VCOM Level: AGND

● Optimized layout for COG Assembly

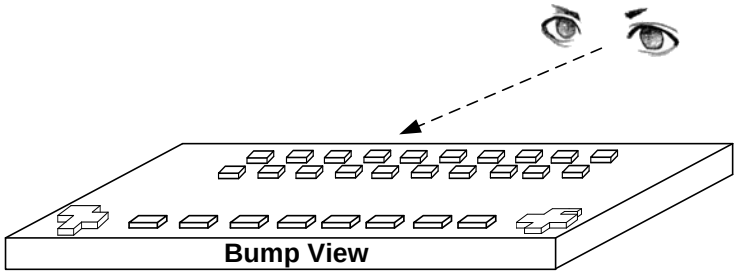
● Operate temperature range: −30ºC to +85 ºC

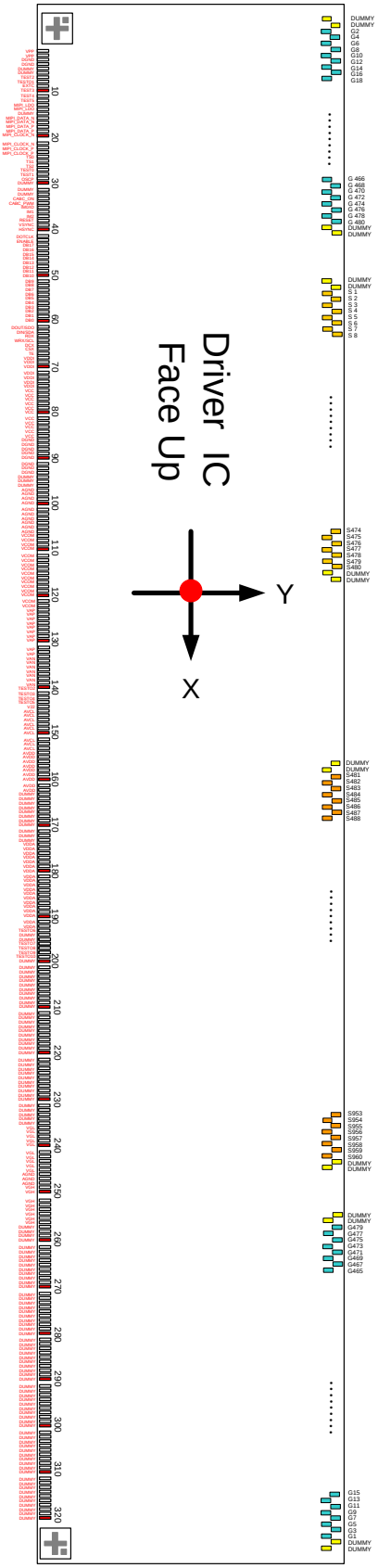
● Lower Power Consumption

3 PAD ARRANGEMENT

3.1.. Output Bump Dimension

Au bump height	9μm
Au bump size	15μmx80μm Gate : G1~G480 Source : S1~S960
	50μmx66μm (Pad1 to Pad320)

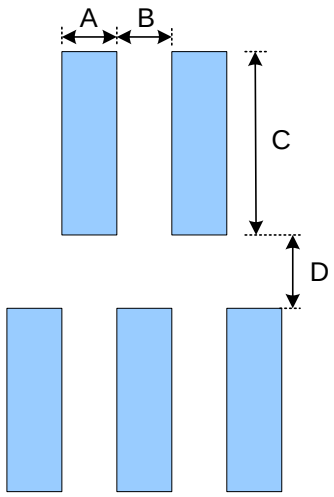




3.2.. Bump Dimension

● **Output Pads**

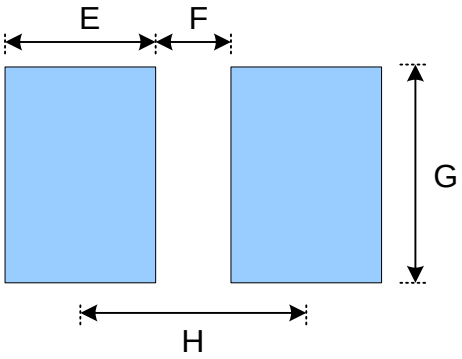
Pad No.



Symbol	Item	Size
A	Bump Width	15 um
B	Bump Gap 1 (Horizontal)	15 um
C	Bump Height	80um
D	Bump Gap 2 (Vertical)	25um

● **Input Pads**

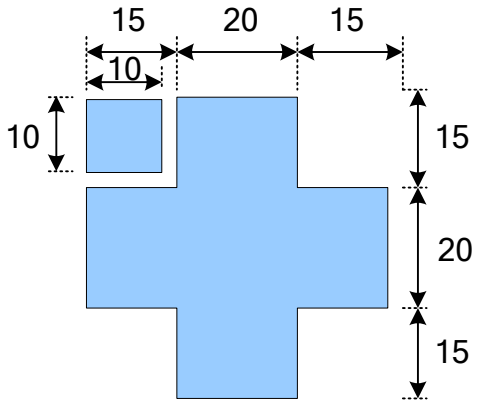
Pad No.1~320



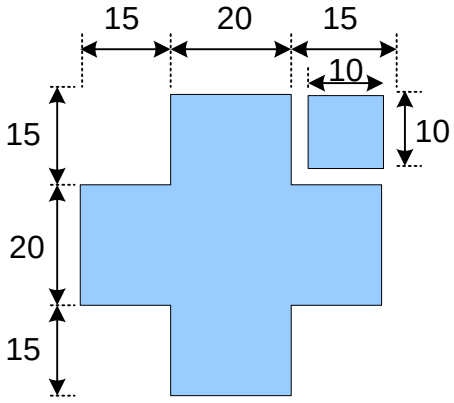
Symbol	Item	Size
E	Bump Width	50 um
F	Bump Gap	20 um
G	Bump Height	66um
H	Bump Pitch	70 um

3.3.. Alignment Mark Dimension

- **Alignment Mark Left: L(X,Y)=(-11300, -277)**



- **Alignment Mark Right: R(X,Y)= (11300, -277)**



3.4.. Chip Information

Chip size	22682um x 636um
Chip thickness	250um
Pad Location	Pad center
Coordinate Origin	Chip center

4 PAD CENTER COORDINATES (AFTER HEAT CORRECTION)

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	VPP	-11165	-279	34	CABC_PWN	-8855	-279
2	VPP	-11095	-279	35	IM0/ID	-8785	-279
3	DGND	-11025	-279	36	IM1	-8715	-279
4	DGND	-10955	-279	37	IM2	-8645	-279
5	DUMMY	-10885	-279	38	RESET	-8575	-279
6	DUMMY	-10815	-279	39	VSYNC	-8505	-279
7	TEST2	-10745	-279	40	HSYNC	-8435	-279
8	TESTO1	-10675	-279	41	DOTCLK	-8365	-279
9	EXTC	-10605	-279	42	ENABLE	-8295	-279
10	TEST3	-10535	-279	43	DB17	-8225	-279
11	TEST4	-10465	-279	44	DB16	-8155	-279
12	TEST5	-10395	-279	45	DB15	-8085	-279
13	MIPI_LDO	-10325	-279	46	DB14	-8015	-279
14	MIPI_LDO	-10255	-279	47	DB13	-7945	-279
15	DUMMY	-10185	-279	48	DB12	-7875	-279
16	MIPI_DATA_N	-10115	-279	49	DB11	-7805	-279
17	MIPI_DATA_N	-10045	-279	50	DB10	-7735	-279
18	MIPI_DATA_P	-9975	-279	51	DB9	-7665	-279
19	MIPI_DATA_P	-9905	-279	52	DB8	-7595	-279
20	MIPI_CLOCK_N	-9835	-279	53	DB7	-7525	-279
21	MIPI_CLOCK_N	-9765	-279	54	DB6	-7455	-279
22	MIPI_CLOCK_P	-9695	-279	55	DB5	-7385	-279
23	MIPI_CLOCK_P	-9625	-279	56	DB4	-7315	-279
24	TS0	-9555	-279	57	DB3	-7245	-279
25	TS1	-9485	-279	58	DB2	-7175	-279
26	TS2	-9415	-279	59	DB1	-7105	-279
27	TEST0	-9345	-279	60	DB0	-7035	-279
28	TEST1	-9275	-279	61	DOUT	-6965	-279
29	OSCP	-9205	-279	62	DIN/SDA	-6895	-279
30	DUMMY	-9135	-279	63	RDX	-6825	-279
31	DUMMY	-9065	-279	64	WRX/SCL	-6755	-279
32	DUMMY	-8995	-279	65	DCX	-6685	-279
33	CABC_ON	-8925	-279	66	CSX	-6615	-279

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
67	TE	-6545	-279	101	AGND	-4165	-279
68	VDDI	-6475	-279	102	AGND	-4095	-279
69	VDDI	-6405	-279	103	AGND	-4025	-279
70	VDDI	-6335	-279	104	AGND	-3955	-279
71	VDDI	-6265	-279	105	AGND	-3885	-279
72	VDDI	-6195	-279	106	AGND	-3815	-279
73	VDDI	-6125	-279	107	VCOM	-3745	-279
74	VDDI	-6055	-279	108	VCOM	-3675	-279
75	VCC	-5985	-279	109	VCOM	-3605	-279
76	VCC	-5915	-279	110	VCOM	-3535	-279
77	VCC	-5845	-279	111	VCOM	-3465	-279
78	VCC	-5775	-279	112	VCOM	-3395	-279
79	VCC	-5705	-279	113	VCOM	-3325	-279
80	VCC	-5635	-279	114	VCOM	-3255	-279
81	VCC	-5565	-279	115	VCOM	-3185	-279
82	VCC	-5495	-279	116	VCOM	-3115	-279
83	VCC	-5425	-279	117	VCOM	-3045	-279
84	VCC	-5355	-279	118	VCOM	-2975	-279
85	VCC	-5285	-279	119	VCOM	-2905	-279
86	DGND	-5215	-279	120	VCOM	-2835	-279
87	DGND	-5145	-279	121	VCOM	-2765	-279
88	DGND	-5075	-279	122	VCOM	-2695	-279
89	DGND	-5005	-279	123	VAP	-2625	-279
90	DGND	-4935	-279	124	VAP	-2555	-279
91	DGND	-4865	-279	125	VAP	-2485	-279
92	DGND	-4795	-279	126	VAP	-2415	-279
93	DGND	-4725	-279	127	VAP	-2345	-279
94	DUMMY	-4655	-279	128	VAP	-2275	-279
95	DUMMY	-4585	-279	129	VAP	-2205	-279
96	DUMMY	-4515	-279	130	VAP	-2135	-279
97	AGND	-4445	-279	131	VAP	-2065	-279
98	AGND	-4375	-279	132	VAP	-1995	-279
99	AGND	-4305	-279	133	VAN	-1925	-279
100	AGND	-4235	-279	134	VAN	-1855	-279

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
135	VAN	-1785	-279	169	DUMMY	595	-279
136	VAN	-1715	-279	170	DUMMY	665	-279
137	VAN	-1645	-279	171	DUMMY	735	-279
138	VAN	-1575	-279	172	DUMMY	805	-279
139	VAN	-1505	-279	173	DUMMY	875	-279
140	TESTO2	-1435	-279	174	VDDA	945	-279
141	TESTO3	-1365	-279	175	VDDA	1015	-279
142	TESTO4	-1295	-279	176	VDDA	1085	-279
143	TESTO5	-1225	-279	177	VDDA	1155	-279
144	V22	-1155	-279	178	VDDA	1225	-279
145	AVCL	-1085	-279	179	VDDA	1295	-279
146	AVCL	-1015	-279	180	VDDA	1365	-279
147	AVCL	-945	-279	181	VDDA	1435	-279
148	AVCL	-875	-279	182	VDDA	1505	-279
149	AVCL	-805	-279	183	VDDA	1575	-279
150	AVCL	-735	-279	184	VDDA	1645	-279
151	AVCL	-665	-279	185	VDDA	1715	-279
152	AVCL	-595	-279	186	VDDA	1785	-279
153	AVCL	-525	-279	187	VDDA	1855	-279
154	AVDD	-455	-279	188	VDDA	1925	-279
155	AVDD	-385	-279	189	VDDA	1995	-279
156	AVDD	-315	-279	190	VDDA	2065	-279
157	AVDD	-245	-279	191	VDDA	2135	-279
158	AVDD	-175	-279	192	VDDA	2205	-279
159	AVDD	-105	-279	193	TESTO6	2275	-279
160	AVDD	-35	-279	194	DUMMY	2345	-279
161	AVDD	35	-279	195	DUMMY	2415	-279
162	AVDD	105	-279	196	TESTO7	2485	-279
163	DUMMY	175	-279	197	TESTO8	2555	-279
164	DUMMY	245	-279	198	TESTO9	2625	-279
165	DUMMY	315	-279	199	TESTO10	2695	-279
166	DUMMY	385	-279	200	DUMMY	2765	-279
167	DUMMY	455	-279	201	DUMMY	2835	-279
168	DUMMY	525	-279	202	DUMMY	2905	-279

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
203	DUMMY	2975	-279	237	VGL	5355	-279
204	DUMMY	3045	-279	238	VGL	5425	-279
205	DUMMY	3115	-279	239	VGL	5495	-279
206	DUMMY	3185	-279	240	VGL	5565	-279
207	DUMMY	3255	-279	241	VGL	5635	-279
208	DUMMY	3325	-279	242	VGL	5705	-279
209	DUMMY	3395	-279	243	VGL	5775	-279
210	DUMMY	3465	-279	244	VGL	5845	-279
211	DUMMY	3535	-279	245	VGL	5915	-279
212	DUMMY	3605	-279	246	AGND	5985	-279
213	DUMMY	3675	-279	247	AGND	6055	-279
214	DUMMY	3745	-279	248	AGND	6125	-279
215	DUMMY	3815	-279	249	VGH	6195	-279
216	DUMMY	3885	-279	250	VGH	6265	-279
217	DUMMY	3955	-279	251	VGH	6335	-279
218	DUMMY	4025	-279	252	VGH	6405	-279
219	DUMMY	4095	-279	253	VGH	6475	-279
220	DUMMY	4165	-279	254	VGH	6545	-279
221	DUMMY	4235	-279	255	VGH	6615	-279
222	DUMMY	4305	-279	256	VGH	6685	-279
223	DUMMY	4375	-279	257	DUMMY	6755	-279
224	DUMMY	4445	-279	258	DUMMY	6825	-279
225	DUMMY	4515	-279	259	DUMMY	6895	-279
226	DUMMY	4585	-279	260	DUMMY	6965	-279
227	DUMMY	4655	-279	261	DUMMY	7035	-279
228	DUMMY	4725	-279	262	DUMMY	7105	-279
229	DUMMY	4795	-279	263	DUMMY	7175	-279
230	DUMMY	4865	-279	264	DUMMY	7245	-279
231	DUMMY	4935	-279	265	DUMMY	7315	-279
232	DUMMY	5005	-279	266	DUMMY	7385	-279
233	DUMMY	5075	-279	267	DUMMY	7455	-279
234	DUMMY	5145	-279	268	DUMMY	7525	-279
235	DUMMY	5215	-279	269	DUMMY	7595	-279
236	VGL	5285	-279	270	DUMMY	7665	-279

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
271	DUMMY	7735	-279	305	DUMMY	10115	-279
272	DUMMY	7805	-279	306	DUMMY	10185	-279
273	DUMMY	7875	-279	307	DUMMY	10255	-279
274	DUMMY	7945	-279	308	DUMMY	10325	-279
275	DUMMY	8015	-279	309	DUMMY	10395	-279
276	DUMMY	8085	-279	310	DUMMY	10465	-279
277	DUMMY	8155	-279	311	DUMMY	10535	-279
278	DUMMY	8225	-279	312	DUMMY	10605	-279
279	DUMMY	8295	-279	313	DUMMY	10675	-279
280	DUMMY	8365	-279	314	DUMMY	10745	-279
281	DUMMY	8435	-279	315	DUMMY	10815	-279
282	DUMMY	8505	-279	316	DUMMY	10885	-279
283	DUMMY	8575	-279	317	DUMMY	10955	-279
284	DUMMY	8645	-279	318	DUMMY	11025	-279
285	DUMMY	8715	-279	319	DUMMY	11095	-279
286	DUMMY	8785	-279	320	DUMMY	11165	-279
287	DUMMY	8855	-279	321	ALIGN_R	11300	-277
288	DUMMY	8925	-279	322	DUMMY	11205	167
289	DUMMY	8995	-279	323	DUMMY	11190	272
290	DUMMY	9065	-279	324	G1	11175	167
291	DUMMY	9135	-279	325	G3	11160	272
292	DUMMY	9205	-279	326	G5	11145	167
293	DUMMY	9275	-279	327	G7	11130	272
294	DUMMY	9345	-279	328	G9	11115	167
295	DUMMY	9415	-279	329	G11	11100	272
296	DUMMY	9485	-279	330	G13	11085	167
297	DUMMY	9555	-279	331	G15	11070	272
298	DUMMY	9625	-279	332	G17	11055	167
299	DUMMY	9695	-279	333	G19	11040	272
300	DUMMY	9765	-279	334	G21	11025	167
301	DUMMY	9835	-279	335	G23	11010	272
302	DUMMY	9905	-279	336	G25	10995	167
303	DUMMY	9975	-279	337	G27	10980	272
304	DUMMY	10045	-279	338	G29	10965	167

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
339	G31	10950	272	373	G99	10440	272
340	G33	10935	167	374	G101	10425	167
341	G35	10920	272	375	G103	10410	272
342	G37	10905	167	376	G105	10395	167
343	G39	10890	272	377	G107	10380	272
344	G41	10875	167	378	G109	10365	167
345	G43	10860	272	379	G111	10350	272
346	G45	10845	167	380	G113	10335	167
347	G47	10830	272	381	G115	10320	272
348	G49	10815	167	382	G117	10305	167
349	G51	10800	272	383	G119	10290	272
350	G53	10785	167	384	G121	10275	167
351	G55	10770	272	385	G123	10260	272
352	G57	10755	167	386	G125	10245	167
353	G59	10740	272	387	G127	10230	272
354	G61	10725	167	388	G129	10215	167
355	G63	10710	272	389	G131	10200	272
356	G65	10695	167	390	G133	10185	167
357	G67	10680	272	391	G135	10170	272
358	G69	10665	167	392	G137	10155	167
359	G71	10650	272	393	G139	10140	272
360	G73	10635	167	394	G141	10125	167
361	G75	10620	272	395	G143	10110	272
362	G77	10605	167	396	G145	10095	167
363	G79	10590	272	397	G147	10080	272
364	G81	10575	167	398	G149	10065	167
365	G83	10560	272	399	G151	10050	272
366	G85	10545	167	400	G153	10035	167
367	G87	10530	272	401	G155	10020	272
368	G89	10515	167	402	G157	10005	167
369	G91	10500	272	403	G159	9990	272
370	G93	10485	167	404	G161	9975	167
371	G95	10470	272	405	G163	9960	272
372	G97	10455	167	406	G165	9945	167

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
407	G167	9930	272	441	G235	9420	272
408	G169	9915	167	442	G237	9405	167
409	G171	9900	272	443	G239	9390	272
410	G173	9885	167	444	G241	9375	167
411	G175	9870	272	445	G243	9360	272
412	G177	9855	167	446	G245	9345	167
413	G179	9840	272	447	G247	9330	272
414	G181	9825	167	448	G249	9315	167
415	G183	9810	272	449	G251	9300	272
416	G185	9795	167	450	G253	9285	167
417	G187	9780	272	451	G255	9270	272
418	G189	9765	167	452	G257	9255	167
419	G191	9750	272	453	G259	9240	272
420	G193	9735	167	454	G261	9225	167
421	G195	9720	272	455	G263	9210	272
422	G197	9705	167	456	G265	9195	167
423	G199	9690	272	457	G267	9180	272
424	G201	9675	167	458	G269	9165	167
425	G203	9660	272	459	G271	9150	272
426	G205	9645	167	460	G273	9135	167
427	G207	9630	272	461	G275	9120	272
428	G209	9615	167	462	G277	9105	167
429	G211	9600	272	463	G279	9090	272
430	G213	9585	167	464	G281	9075	167
431	G215	9570	272	465	G283	9060	272
432	G217	9555	167	466	G285	9045	167
433	G219	9540	272	467	G287	9030	272
434	G221	9525	167	468	G289	9015	167
435	G223	9510	272	469	G291	9000	272
436	G225	9495	167	470	G293	8985	167
437	G227	9480	272	471	G295	8970	272
438	G229	9465	167	472	G297	8955	167
439	G231	9450	272	473	G299	8940	272
440	G233	9435	167	474	G301	8925	167

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
475	G303	8910	272	509	G371	8400	272
476	G305	8895	167	510	G373	8385	167
477	G307	8880	272	511	G375	8370	272
478	G309	8865	167	512	G377	8355	167
479	G311	8850	272	513	G379	8340	272
480	G313	8835	167	514	G381	8325	167
481	G315	8820	272	515	G383	8310	272
482	G317	8805	167	516	G385	8295	167
483	G319	8790	272	517	G387	8280	272
484	G321	8775	167	518	G389	8265	167
485	G323	8760	272	519	G391	8250	272
486	G325	8745	167	520	G393	8235	167
487	G327	8730	272	521	G395	8220	272
488	G329	8715	167	522	G397	8205	167
489	G331	8700	272	523	G399	8190	272
490	G333	8685	167	524	G401	8175	167
491	G335	8670	272	525	G403	8160	272
492	G337	8655	167	526	G405	8145	167
493	G339	8640	272	527	G407	8130	272
494	G341	8625	167	528	G409	8115	167
495	G343	8610	272	529	G411	8100	272
496	G345	8595	167	530	G413	8085	167
497	G347	8580	272	531	G415	8070	272
498	G349	8565	167	532	G417	8055	167
499	G351	8550	272	533	G419	8040	272
500	G353	8535	167	534	G421	8025	167
501	G355	8520	272	535	G423	8010	272
502	G357	8505	167	536	G425	7995	167
503	G359	8490	272	537	G427	7980	272
504	G361	8475	167	538	G429	7965	167
505	G363	8460	272	539	G431	7950	272
506	G365	8445	167	540	G433	7935	167
507	G367	8430	272	541	G435	7920	272
508	G369	8415	167	542	G437	7905	167

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
543	G439	7890	272	577	S951	7230	272
544	G441	7875	167	578	S950	7215	167
545	G443	7860	272	579	S949	7200	272
546	G445	7845	167	580	S948	7185	167
547	G447	7830	272	581	S947	7170	272
548	G449	7815	167	582	S946	7155	167
549	G451	7800	272	583	S945	7140	272
550	G453	7785	167	584	S944	7125	167
551	G455	7770	272	585	S943	7110	272
552	G457	7755	167	586	S942	7095	167
553	G459	7740	272	587	S941	7080	272
554	G461	7725	167	588	S940	7065	167
555	G463	7710	272	589	S939	7050	272
556	G465	7695	167	590	S938	7035	167
557	G467	7680	272	591	S937	7020	272
558	G469	7665	167	592	S936	7005	167
559	G471	7650	272	593	S935	6990	272
560	G473	7635	167	594	S934	6975	167
561	G475	7620	272	595	S933	6960	272
562	G477	7605	167	596	S932	6945	167
563	G479	7590	272	597	S931	6930	272
564	DUMMY	7575	167	598	S930	6915	167
565	DUMMY	7560	272	599	S929	6900	272
566	DUMMY	7395	167	600	S928	6885	167
567	DUMMY	7380	272	601	S927	6870	272
568	S960	7365	167	602	S926	6855	167
569	S959	7350	272	603	S925	6840	272
570	S958	7335	167	604	S924	6825	167
571	S957	7320	272	605	S923	6810	272
572	S956	7305	167	606	S922	6795	167
573	S955	7290	272	607	S921	6780	272
574	S954	7275	167	608	S920	6765	167
575	S953	7260	272	609	S919	6750	272
576	S952	7245	167	610	S918	6735	167

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
611	S917	6720	272	645	S883	6210	272
612	S916	6705	167	646	S882	6195	167
613	S915	6690	272	647	S881	6180	272
614	S914	6675	167	648	S880	6165	167
615	S913	6660	272	649	S879	6150	272
616	S912	6645	167	650	S878	6135	167
617	S911	6630	272	651	S877	6120	272
618	S910	6615	167	652	S876	6105	167
619	S909	6600	272	653	S875	6090	272
620	S908	6585	167	654	S874	6075	167
621	S907	6570	272	655	S873	6060	272
622	S906	6555	167	656	S872	6045	167
623	S905	6540	272	657	S871	6030	272
624	S904	6525	167	658	S870	6015	167
625	S903	6510	272	659	S869	6000	272
626	S902	6495	167	660	S868	5985	167
627	S901	6480	272	661	S867	5970	272
628	S900	6465	167	662	S866	5955	167
629	S899	6450	272	663	S865	5940	272
630	S898	6435	167	664	S864	5925	167
631	S897	6420	272	665	S863	5910	272
632	S896	6405	167	666	S862	5895	167
633	S895	6390	272	667	S861	5880	272
634	S894	6375	167	668	S860	5865	167
635	S893	6360	272	669	S859	5850	272
636	S892	6345	167	670	S858	5835	167
637	S891	6330	272	671	S857	5820	272
638	S890	6315	167	672	S856	5805	167
639	S889	6300	272	673	S855	5790	272
640	S888	6285	167	674	S854	5775	167
641	S887	6270	272	675	S853	5760	272
642	S886	6255	167	676	S852	5745	167
643	S885	6240	272	677	S851	5730	272
644	S884	6225	167	678	S850	5715	167

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
679	S849	5700	272	713	S815	5190	272
680	S848	5685	167	714	S814	5175	167
681	S847	5670	272	715	S813	5160	272
682	S846	5655	167	716	S812	5145	167
683	S845	5640	272	717	S811	5130	272
684	S844	5625	167	718	S810	5115	167
685	S843	5610	272	719	S809	5100	272
686	S842	5595	167	720	S808	5085	167
687	S841	5580	272	721	S807	5070	272
688	S840	5565	167	722	S806	5055	167
689	S839	5550	272	723	S805	5040	272
690	S838	5535	167	724	S804	5025	167
691	S837	5520	272	725	S803	5010	272
692	S836	5505	167	726	S802	4995	167
693	S835	5490	272	727	S801	4980	272
694	S834	5475	167	728	S800	4965	167
695	S833	5460	272	729	S799	4950	272
696	S832	5445	167	730	S798	4935	167
697	S831	5430	272	731	S797	4920	272
698	S830	5415	167	732	S796	4905	167
699	S829	5400	272	733	S795	4890	272
700	S828	5385	167	734	S794	4875	167
701	S827	5370	272	735	S793	4860	272
702	S826	5355	167	736	S792	4845	167
703	S825	5340	272	737	S791	4830	272
704	S824	5325	167	738	S790	4815	167
705	S823	5310	272	739	S789	4800	272
706	S822	5295	167	740	S788	4785	167
707	S821	5280	272	741	S787	4770	272
708	S820	5265	167	742	S786	4755	167
709	S819	5250	272	743	S785	4740	272
710	S818	5235	167	744	S784	4725	167
711	S817	5220	272	745	S783	4710	272
712	S816	5205	167	746	S782	4695	167

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
747	S781	4680	272	781	S747	4170	272
748	S780	4665	167	782	S746	4155	167
749	S779	4650	272	783	S745	4140	272
750	S778	4635	167	784	S744	4125	167
751	S777	4620	272	785	S743	4110	272
752	S776	4605	167	786	S742	4095	167
753	S775	4590	272	787	S741	4080	272
754	S774	4575	167	788	S740	4065	167
755	S773	4560	272	789	S739	4050	272
756	S772	4545	167	790	S738	4035	167
757	S771	4530	272	791	S737	4020	272
758	S770	4515	167	792	S736	4005	167
759	S769	4500	272	793	S735	3990	272
760	S768	4485	167	794	S734	3975	167
761	S767	4470	272	795	S733	3960	272
762	S766	4455	167	796	S732	3945	167
763	S765	4440	272	797	S731	3930	272
764	S764	4425	167	798	S730	3915	167
765	S763	4410	272	799	S729	3900	272
766	S762	4395	167	800	S728	3885	167
767	S761	4380	272	801	S727	3870	272
768	S760	4365	167	802	S726	3855	167
769	S759	4350	272	803	S725	3840	272
770	S758	4335	167	804	S724	3825	167
771	S757	4320	272	805	S723	3810	272
772	S756	4305	167	806	S722	3795	167
773	S755	4290	272	807	S721	3780	272
774	S754	4275	167	808	S720	3765	167
775	S753	4260	272	809	S719	3750	272
776	S752	4245	167	810	S718	3735	167
777	S751	4230	272	811	S717	3720	272
778	S750	4215	167	812	S716	3705	167
779	S749	4200	272	813	S715	3690	272
780	S748	4185	167	814	S714	3675	167

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
815	S713	3660	272	849	S679	3150	272
816	S712	3645	167	850	S678	3135	167
817	S711	3630	272	851	S677	3120	272
818	S710	3615	167	852	S676	3105	167
819	S709	3600	272	853	S675	3090	272
820	S708	3585	167	854	S674	3075	167
821	S707	3570	272	855	S673	3060	272
822	S706	3555	167	856	S672	3045	167
823	S705	3540	272	857	S671	3030	272
824	S704	3525	167	858	S670	3015	167
825	S703	3510	272	859	S669	3000	272
826	S702	3495	167	860	S668	2985	167
827	S701	3480	272	861	S667	2970	272
828	S700	3465	167	862	S666	2955	167
829	S699	3450	272	863	S665	2940	272
830	S698	3435	167	864	S664	2925	167
831	S697	3420	272	865	S663	2910	272
832	S696	3405	167	866	S662	2895	167
833	S695	3390	272	867	S661	2880	272
834	S694	3375	167	868	S660	2865	167
835	S693	3360	272	869	S659	2850	272
836	S692	3345	167	870	S658	2835	167
837	S691	3330	272	871	S657	2820	272
838	S690	3315	167	872	S656	2805	167
839	S689	3300	272	873	S655	2790	272
840	S688	3285	167	874	S654	2775	167
841	S687	3270	272	875	S653	2760	272
842	S686	3255	167	876	S652	2745	167
843	S685	3240	272	877	S651	2730	272
844	S684	3225	167	878	S650	2715	167
845	S683	3210	272	879	S649	2700	272
846	S682	3195	167	880	S648	2685	167
847	S681	3180	272	881	S647	2670	272
848	S680	3165	167	882	S646	2655	167

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
883	S645	2640	272	917	S611	2130	272
884	S644	2625	167	918	S610	2115	167
885	S643	2610	272	919	S609	2100	272
886	S642	2595	167	920	S608	2085	167
887	S641	2580	272	921	S607	2070	272
888	S640	2565	167	922	S606	2055	167
889	S639	2550	272	923	S605	2040	272
890	S638	2535	167	924	S604	2025	167
891	S637	2520	272	925	S603	2010	272
892	S636	2505	167	926	S602	1995	167
893	S635	2490	272	927	S601	1980	272
894	S634	2475	167	928	S600	1965	167
895	S633	2460	272	929	S599	1950	272
896	S632	2445	167	930	S598	1935	167
897	S631	2430	272	931	S597	1920	272
898	S630	2415	167	932	S596	1905	167
899	S629	2400	272	933	S595	1890	272
900	S628	2385	167	934	S594	1875	167
901	S627	2370	272	935	S593	1860	272
902	S626	2355	167	936	S592	1845	167
903	S625	2340	272	937	S591	1830	272
904	S624	2325	167	938	S590	1815	167
905	S623	2310	272	939	S589	1800	272
906	S622	2295	167	940	S588	1785	167
907	S621	2280	272	941	S587	1770	272
908	S620	2265	167	942	S586	1755	167
909	S619	2250	272	943	S585	1740	272
910	S618	2235	167	944	S584	1725	167
911	S617	2220	272	945	S583	1710	272
912	S616	2205	167	946	S582	1695	167
913	S615	2190	272	947	S581	1680	272
914	S614	2175	167	948	S580	1665	167
915	S613	2160	272	949	S579	1650	272
916	S612	2145	167	950	S578	1635	167

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
951	S577	1620	272	985	S543	1110	272
952	S576	1605	167	986	S542	1095	167
953	S575	1590	272	987	S541	1080	272
954	S574	1575	167	988	S540	1065	167
955	S573	1560	272	989	S539	1050	272
956	S572	1545	167	990	S538	1035	167
957	S571	1530	272	991	S537	1020	272
958	S570	1515	167	992	S536	1005	167
959	S569	1500	272	993	S535	990	272
960	S568	1485	167	994	S534	975	167
961	S567	1470	272	995	S533	960	272
962	S566	1455	167	996	S532	945	167
963	S565	1440	272	997	S531	930	272
964	S564	1425	167	998	S530	915	167
965	S563	1410	272	999	S529	900	272
966	S562	1395	167	1000	S528	885	167
967	S561	1380	272	1001	S527	870	272
968	S560	1365	167	1002	S526	855	167
969	S559	1350	272	1003	S525	840	272
970	S558	1335	167	1004	S524	825	167
971	S557	1320	272	1005	S523	810	272
972	S556	1305	167	1006	S522	795	167
973	S555	1290	272	1007	S521	780	272
974	S554	1275	167	1008	S520	765	167
975	S553	1260	272	1009	S519	750	272
976	S552	1245	167	1010	S518	735	167
977	S551	1230	272	1011	S517	720	272
978	S550	1215	167	1012	S516	705	167
979	S549	1200	272	1013	S515	690	272
980	S548	1185	167	1014	S514	675	167
981	S547	1170	272	1015	S513	660	272
982	S546	1155	167	1016	S512	645	167
983	S545	1140	272	1017	S511	630	272
984	S544	1125	167	1018	S510	615	167

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1019	S509	600	272	1053	S479	-195	167
1020	S508	585	167	1054	S478	-210	272
1021	S507	570	272	1055	S477	-225	167
1022	S506	555	167	1056	S476	-240	272
1023	S505	540	272	1057	S475	-255	167
1024	S504	525	167	1058	S474	-270	272
1025	S503	510	272	1059	S473	-285	167
1026	S502	495	167	1060	S472	-300	272
1027	S501	480	272	1061	S471	-315	167
1028	S500	465	167	1062	S470	-330	272
1029	S499	450	272	1063	S469	-345	167
1030	S498	435	167	1064	S468	-360	272
1031	S497	420	272	1065	S467	-375	167
1032	S496	405	167	1066	S466	-390	272
1033	S495	390	272	1067	S465	-405	167
1034	S494	375	167	1068	S464	-420	272
1035	S493	360	272	1069	S463	-435	167
1036	S492	345	167	1070	S462	-450	272
1037	S491	330	272	1071	S461	-465	167
1038	S490	315	167	1072	S460	-480	272
1039	S489	300	272	1073	S459	-495	167
1040	S488	285	167	1074	S458	-510	272
1041	S487	270	272	1075	S457	-525	167
1042	S486	255	167	1076	S456	-540	272
1043	S485	240	272	1077	S455	-555	167
1044	S484	225	167	1078	S454	-570	272
1045	S483	210	272	1079	S453	-585	167
1046	S482	195	167	1080	S452	-600	272
1047	S481	180	272	1081	S451	-615	167
1048	DUMMY	165	167	1082	S450	-630	272
1049	DUMMY	150	272	1083	S449	-645	167
1050	DUMMY	-150	272	1084	S448	-660	272
1051	DUMMY	-165	167	1085	S447	-675	167
1052	S480	-180	272	1086	S446	-690	272

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1087	S445	-705	167	1121	S411	-1215	167
1088	S444	-720	272	1122	S410	-1230	272
1089	S443	-735	167	1123	S409	-1245	167
1090	S442	-750	272	1124	S408	-1260	272
1091	S441	-765	167	1125	S407	-1275	167
1092	S440	-780	272	1126	S406	-1290	272
1093	S439	-795	167	1127	S405	-1305	167
1094	S438	-810	272	1128	S404	-1320	272
1095	S437	-825	167	1129	S403	-1335	167
1096	S436	-840	272	1130	S402	-1350	272
1097	S435	-855	167	1131	S401	-1365	167
1098	S434	-870	272	1132	S400	-1380	272
1099	S433	-885	167	1133	S399	-1395	167
1100	S432	-900	272	1134	S398	-1410	272
1101	S431	-915	167	1135	S397	-1425	167
1102	S430	-930	272	1136	S396	-1440	272
1103	S429	-945	167	1137	S395	-1455	167
1104	S428	-960	272	1138	S394	-1470	272
1105	S427	-975	167	1139	S393	-1485	167
1106	S426	-990	272	1140	S392	-1500	272
1107	S425	-1005	167	1141	S391	-1515	167
1108	S424	-1020	272	1142	S390	-1530	272
1109	S423	-1035	167	1143	S389	-1545	167
1110	S422	-1050	272	1144	S388	-1560	272
1111	S421	-1065	167	1145	S387	-1575	167
1112	S420	-1080	272	1146	S386	-1590	272
1113	S419	-1095	167	1147	S385	-1605	167
1114	S418	-1110	272	1148	S384	-1620	272
1115	S417	-1125	167	1149	S383	-1635	167
1116	S416	-1140	272	1150	S382	-1650	272
1117	S415	-1155	167	1151	S381	-1665	167
1118	S414	-1170	272	1152	S380	-1680	272
1119	S413	-1185	167	1153	S379	-1695	167
1120	S412	-1200	272	1154	S378	-1710	272

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1155	S377	-1725	167	1189	S343	-2235	167
1156	S376	-1740	272	1190	S342	-2250	272
1157	S375	-1755	167	1191	S341	-2265	167
1158	S374	-1770	272	1192	S340	-2280	272
1159	S373	-1785	167	1193	S339	-2295	167
1160	S372	-1800	272	1194	S338	-2310	272
1161	S371	-1815	167	1195	S337	-2325	167
1162	S370	-1830	272	1196	S336	-2340	272
1163	S369	-1845	167	1197	S335	-2355	167
1164	S368	-1860	272	1198	S334	-2370	272
1165	S367	-1875	167	1199	S333	-2385	167
1166	S366	-1890	272	1200	S332	-2400	272
1167	S365	-1905	167	1201	S331	-2415	167
1168	S364	-1920	272	1202	S330	-2430	272
1169	S363	-1935	167	1203	S329	-2445	167
1170	S362	-1950	272	1204	S328	-2460	272
1171	S361	-1965	167	1205	S327	-2475	167
1172	S360	-1980	272	1206	S326	-2490	272
1173	S359	-1995	167	1207	S325	-2505	167
1174	S358	-2010	272	1208	S324	-2520	272
1175	S357	-2025	167	1209	S323	-2535	167
1176	S356	-2040	272	1210	S322	-2550	272
1177	S355	-2055	167	1211	S321	-2565	167
1178	S354	-2070	272	1212	S320	-2580	272
1179	S353	-2085	167	1213	S319	-2595	167
1180	S352	-2100	272	1214	S318	-2610	272
1181	S351	-2115	167	1215	S317	-2625	167
1182	S350	-2130	272	1216	S316	-2640	272
1183	S349	-2145	167	1217	S315	-2655	167
1184	S348	-2160	272	1218	S314	-2670	272
1185	S347	-2175	167	1219	S313	-2685	167
1186	S346	-2190	272	1220	S312	-2700	272
1187	S345	-2205	167	1221	S311	-2715	167
1188	S344	-2220	272	1222	S310	-2730	272

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1223	S309	-2745	167	1257	S275	-3255	167
1224	S308	-2760	272	1258	S274	-3270	272
1225	S307	-2775	167	1259	S273	-3285	167
1226	S306	-2790	272	1260	S272	-3300	272
1227	S305	-2805	167	1261	S271	-3315	167
1228	S304	-2820	272	1262	S270	-3330	272
1229	S303	-2835	167	1263	S269	-3345	167
1230	S302	-2850	272	1264	S268	-3360	272
1231	S301	-2865	167	1265	S267	-3375	167
1232	S300	-2880	272	1266	S266	-3390	272
1233	S299	-2895	167	1267	S265	-3405	167
1234	S298	-2910	272	1268	S264	-3420	272
1235	S297	-2925	167	1269	S263	-3435	167
1236	S296	-2940	272	1270	S262	-3450	272
1237	S295	-2955	167	1271	S261	-3465	167
1238	S294	-2970	272	1272	S260	-3480	272
1239	S293	-2985	167	1273	S259	-3495	167
1240	S292	-3000	272	1274	S258	-3510	272
1241	S291	-3015	167	1275	S257	-3525	167
1242	S290	-3030	272	1276	S256	-3540	272
1243	S289	-3045	167	1277	S255	-3555	167
1244	S288	-3060	272	1278	S254	-3570	272
1245	S287	-3075	167	1279	S253	-3585	167
1246	S286	-3090	272	1280	S252	-3600	272
1247	S285	-3105	167	1281	S251	-3615	167
1248	S284	-3120	272	1282	S250	-3630	272
1249	S283	-3135	167	1283	S249	-3645	167
1250	S282	-3150	272	1284	S248	-3660	272
1251	S281	-3165	167	1285	S247	-3675	167
1252	S280	-3180	272	1286	S246	-3690	272
1253	S279	-3195	167	1287	S245	-3705	167
1254	S278	-3210	272	1288	S244	-3720	272
1255	S277	-3225	167	1289	S243	-3735	167
1256	S276	-3240	272	1290	S242	-3750	272

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1291	S241	-3765	167	1325	S207	-4275	167
1292	S240	-3780	272	1326	S206	-4290	272
1293	S239	-3795	167	1327	S205	-4305	167
1294	S238	-3810	272	1328	S204	-4320	272
1295	S237	-3825	167	1329	S203	-4335	167
1296	S236	-3840	272	1330	S202	-4350	272
1297	S235	-3855	167	1331	S201	-4365	167
1298	S234	-3870	272	1332	S200	-4380	272
1299	S233	-3885	167	1333	S199	-4395	167
1300	S232	-3900	272	1334	S198	-4410	272
1301	S231	-3915	167	1335	S197	-4425	167
1302	S230	-3930	272	1336	S196	-4440	272
1303	S229	-3945	167	1337	S195	-4455	167
1304	S228	-3960	272	1338	S194	-4470	272
1305	S227	-3975	167	1339	S193	-4485	167
1306	S226	-3990	272	1340	S192	-4500	272
1307	S225	-4005	167	1341	S191	-4515	167
1308	S224	-4020	272	1342	S190	-4530	272
1309	S223	-4035	167	1343	S189	-4545	167
1310	S222	-4050	272	1344	S188	-4560	272
1311	S221	-4065	167	1345	S187	-4575	167
1312	S220	-4080	272	1346	S186	-4590	272
1313	S219	-4095	167	1347	S185	-4605	167
1314	S218	-4110	272	1348	S184	-4620	272
1315	S217	-4125	167	1349	S183	-4635	167
1316	S216	-4140	272	1350	S182	-4650	272
1317	S215	-4155	167	1351	S181	-4665	167
1318	S214	-4170	272	1352	S180	-4680	272
1319	S213	-4185	167	1353	S179	-4695	167
1320	S212	-4200	272	1354	S178	-4710	272
1321	S211	-4215	167	1355	S177	-4725	167
1322	S210	-4230	272	1356	S176	-4740	272
1323	S209	-4245	167	1357	S175	-4755	167
1324	S208	-4260	272	1358	S174	-4770	272

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1359	S173	-4785	167	1393	S139	-5295	167
1360	S172	-4800	272	1394	S138	-5310	272
1361	S171	-4815	167	1395	S137	-5325	167
1362	S170	-4830	272	1396	S136	-5340	272
1363	S169	-4845	167	1397	S135	-5355	167
1364	S168	-4860	272	1398	S134	-5370	272
1365	S167	-4875	167	1399	S133	-5385	167
1366	S166	-4890	272	1400	S132	-5400	272
1367	S165	-4905	167	1401	S131	-5415	167
1368	S164	-4920	272	1402	S130	-5430	272
1369	S163	-4935	167	1403	S129	-5445	167
1370	S162	-4950	272	1404	S128	-5460	272
1371	S161	-4965	167	1405	S127	-5475	167
1372	S160	-4980	272	1406	S126	-5490	272
1373	S159	-4995	167	1407	S125	-5505	167
1374	S158	-5010	272	1408	S124	-5520	272
1375	S157	-5025	167	1409	S123	-5535	167
1376	S156	-5040	272	1410	S122	-5550	272
1377	S155	-5055	167	1411	S121	-5565	167
1378	S154	-5070	272	1412	S120	-5580	272
1379	S153	-5085	167	1413	S119	-5595	167
1380	S152	-5100	272	1414	S118	-5610	272
1381	S151	-5115	167	1415	S117	-5625	167
1382	S150	-5130	272	1416	S116	-5640	272
1383	S149	-5145	167	1417	S115	-5655	167
1384	S148	-5160	272	1418	S114	-5670	272
1385	S147	-5175	167	1419	S113	-5685	167
1386	S146	-5190	272	1420	S112	-5700	272
1387	S145	-5205	167	1421	S111	-5715	167
1388	S144	-5220	272	1422	S110	-5730	272
1389	S143	-5235	167	1423	S109	-5745	167
1390	S142	-5250	272	1424	S108	-5760	272
1391	S141	-5265	167				
1392	S140	-5280	272				

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1425	S107	-5775	167	1459	S73	-6285	167
1426	S106	-5790	272	1460	S72	-6300	272
1427	S105	-5805	167	1461	S71	-6315	167
1428	S104	-5820	272	1462	S70	-6330	272
1429	S103	-5835	167	1463	S69	-6345	167
1430	S102	-5850	272	1464	S68	-6360	272
1431	S101	-5865	167	1465	S67	-6375	167
1432	S100	-5880	272	1466	S66	-6390	272
1433	S99	-5895	167	1467	S65	-6405	167
1434	S98	-5910	272	1468	S64	-6420	272
1435	S97	-5925	167	1469	S63	-6435	167
1436	S96	-5940	272	1470	S62	-6450	272
1437	S95	-5955	167	1471	S61	-6465	167
1438	S94	-5970	272	1472	S60	-6480	272
1439	S93	-5985	167	1473	S59	-6495	167
1440	S92	-6000	272	1474	S58	-6510	272
1441	S91	-6015	167	1475	S57	-6525	167
1442	S90	-6030	272	1476	S56	-6540	272
1443	S89	-6045	167	1477	S55	-6555	167
1444	S88	-6060	272	1478	S54	-6570	272
1445	S87	-6075	167	1479	S53	-6585	167
1446	S86	-6090	272	1480	S52	-6600	272
1447	S85	-6105	167	1481	S51	-6615	167
1448	S84	-6120	272	1482	S50	-6630	272
1449	S83	-6135	167	1483	S49	-6645	167
1450	S82	-6150	272	1484	S48	-6660	272
1451	S81	-6165	167	1485	S47	-6675	167
1452	S80	-6180	272	1486	S46	-6690	272
1453	S79	-6195	167	1487	S45	-6705	167
1454	S78	-6210	272	1488	S44	-6720	272
1455	S77	-6225	167	1489	S43	-6735	167
1456	S76	-6240	272	1490	S42	-6750	272
1457	S75	-6255	167	1491	S41	-6765	167
1458	S74	-6270	272	1492	S40	-6780	272

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1493	S39	-6795	167	1527	S5	-7305	167
1494	S38	-6810	272	1528	S4	-7320	272
1495	S37	-6825	167	1529	S3	-7335	167
1496	S36	-6840	272	1530	S2	-7350	272
1497	S35	-6855	167	1531	S1	-7365	167
1498	S34	-6870	272	1532	DUMMY	-7380	272
1499	S33	-6885	167	1533	DUMMY	-7395	167
1500	S32	-6900	272	1534	DUMMY	-7560	272
1501	S31	-6915	167	1535	DUMMY	-7575	167
1502	S30	-6930	272	1536	G480	-7590	272
1503	S29	-6945	167	1537	G478	-7605	167
1504	S28	-6960	272	1538	G476	-7620	272
1505	S27	-6975	167	1539	G474	-7635	167
1506	S26	-6990	272	1540	G472	-7650	272
1507	S25	-7005	167	1541	G470	-7665	167
1508	S24	-7020	272	1542	G468	-7680	272
1509	S23	-7035	167	1543	G466	-7695	167
1510	S22	-7050	272	1544	G464	-7710	272
1511	S21	-7065	167	1545	G462	-7725	167
1512	S20	-7080	272	1546	G460	-7740	272
1513	S19	-7095	167	1547	G458	-7755	167
1514	S18	-7110	272	1548	G456	-7770	272
1515	S17	-7125	167	1549	G454	-7785	167
1516	S16	-7140	272	1550	G452	-7800	272
1517	S15	-7155	167	1551	G450	-7815	167
1518	S14	-7170	272	1552	G448	-7830	272
1519	S13	-7185	167	1553	G446	-7845	167
1520	S12	-7200	272	1554	G444	-7860	272
1521	S11	-7215	167	1555	G442	-7875	167
1522	S10	-7230	272	1556	G440	-7890	272
1523	S9	-7245	167	1557	G438	-7905	167
1524	S8	-7260	272	1558	G436	-7920	272
1525	S7	-7275	167	1559	G434	-7935	167
1526	S6	-7290	272	1560	G432	-7950	272

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1561	G430	-7965	167	1595	G362	-8475	167
1562	G428	-7980	272	1596	G360	-8490	272
1563	G426	-7995	167	1597	G358	-8505	167
1564	G424	-8010	272	1598	G356	-8520	272
1565	G422	-8025	167	1599	G354	-8535	167
1566	G420	-8040	272	1600	G352	-8550	272
1567	G418	-8055	167	1601	G350	-8565	167
1568	G416	-8070	272	1602	G348	-8580	272
1569	G414	-8085	167	1603	G346	-8595	167
1570	G412	-8100	272	1604	G344	-8610	272
1571	G410	-8115	167	1605	G342	-8625	167
1572	G408	-8130	272	1606	G340	-8640	272
1573	G406	-8145	167	1607	G338	-8655	167
1574	G404	-8160	272	1608	G336	-8670	272
1575	G402	-8175	167	1609	G334	-8685	167
1576	G400	-8190	272	1610	G332	-8700	272
1577	G398	-8205	167	1611	G330	-8715	167
1578	G396	-8220	272	1612	G328	-8730	272
1579	G394	-8235	167	1613	G326	-8745	167
1580	G392	-8250	272	1614	G324	-8760	272
1581	G390	-8265	167	1615	G322	-8775	167
1582	G388	-8280	272	1616	G320	-8790	272
1583	G386	-8295	167	1617	G318	-8805	167
1584	G384	-8310	272	1618	G316	-8820	272
1585	G382	-8325	167	1619	G314	-8835	167
1586	G380	-8340	272	1620	G312	-8850	272
1587	G378	-8355	167	1621	G310	-8865	167
1588	G376	-8370	272	1622	G308	-8880	272
1589	G374	-8385	167	1623	G306	-8895	167
1590	G372	-8400	272	1624	G304	-8910	272
1591	G370	-8415	167	1625	G302	-8925	167
1592	G368	-8430	272	1626	G300	-8940	272
1593	G366	-8445	167	1627	G298	-8955	167
1594	G364	-8460	272	1628	G296	-8970	272

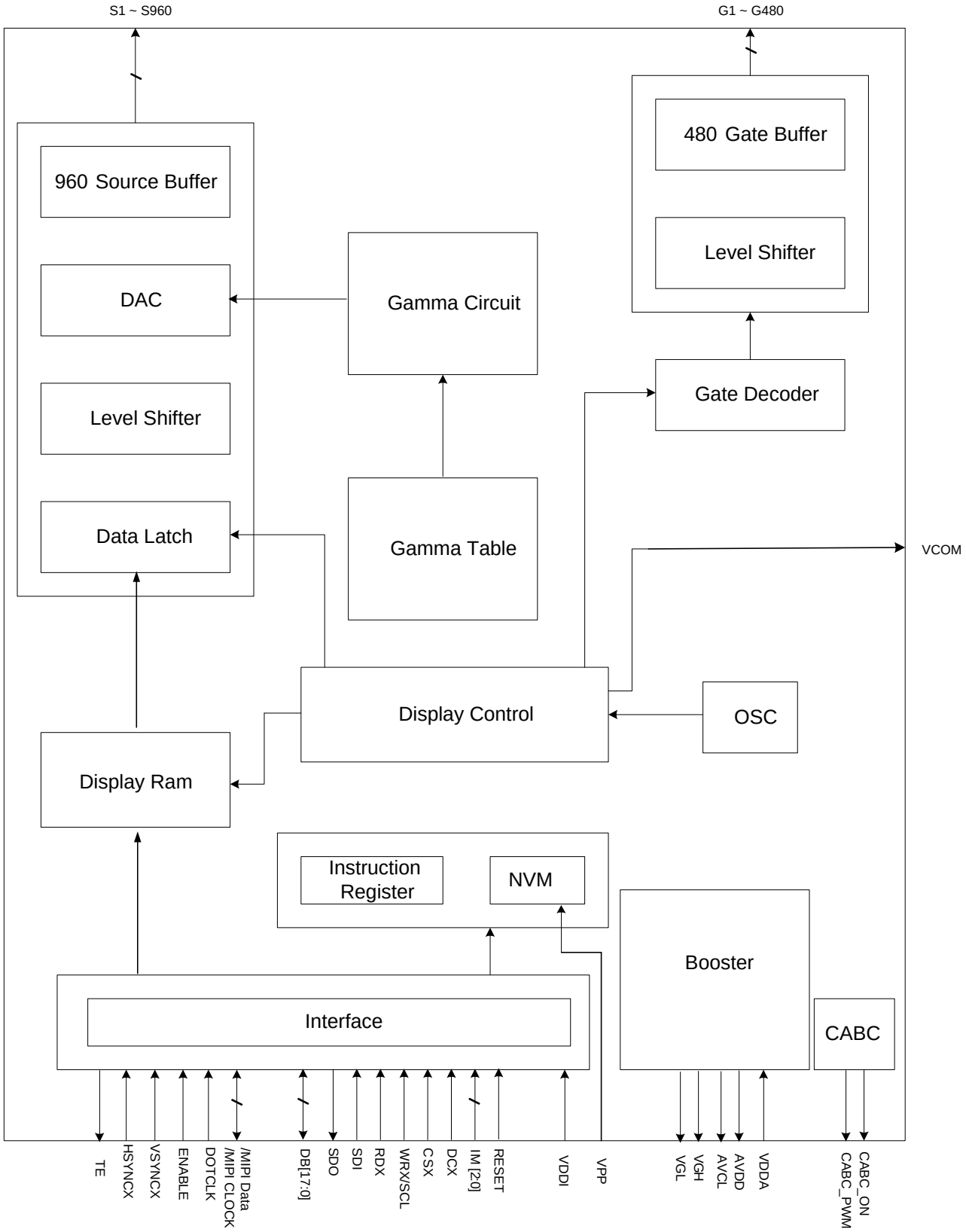
PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1629	G294	-8985	167	1663	G226	-9495	167
1630	G292	-9000	272	1664	G224	-9510	272
1631	G290	-9015	167	1665	G222	-9525	167
1632	G288	-9030	272	1666	G220	-9540	272
1633	G286	-9045	167	1667	G218	-9555	167
1634	G284	-9060	272	1668	G216	-9570	272
1635	G282	-9075	167	1669	G214	-9585	167
1636	G280	-9090	272	1670	G212	-9600	272
1637	G278	-9105	167	1671	G210	-9615	167
1638	G276	-9120	272	1672	G208	-9630	272
1639	G274	-9135	167	1673	G206	-9645	167
1640	G272	-9150	272	1674	G204	-9660	272
1641	G270	-9165	167	1675	G202	-9675	167
1642	G268	-9180	272	1676	G200	-9690	272
1643	G266	-9195	167	1677	G198	-9705	167
1644	G264	-9210	272	1678	G196	-9720	272
1645	G262	-9225	167	1679	G194	-9735	167
1646	G260	-9240	272	1680	G192	-9750	272
1647	G258	-9255	167	1681	G190	-9765	167
1648	G256	-9270	272	1682	G188	-9780	272
1649	G254	-9285	167	1683	G186	-9795	167
1650	G252	-9300	272	1684	G184	-9810	272
1651	G250	-9315	167	1685	G182	-9825	167
1652	G248	-9330	272	1686	G180	-9840	272
1653	G246	-9345	167	1687	G178	-9855	167
1654	G244	-9360	272	1688	G176	-9870	272
1655	G242	-9375	167	1689	G174	-9885	167
1656	G240	-9390	272	1690	G172	-9900	272
1657	G238	-9405	167	1691	G170	-9915	167
1658	G236	-9420	272	1692	G168	-9930	272
1659	G234	-9435	167	1693	G166	-9945	167
1660	G232	-9450	272	1694	G164	-9960	272
1661	G230	-9465	167	1695	G162	-9975	167
1662	G228	-9480	272	1696	G160	-9990	272

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1697	G158	-10005	167	1731	G90	-10515	167
1698	G156	-10020	272	1732	G88	-10530	272
1699	G154	-10035	167	1733	G86	-10545	167
1700	G152	-10050	272	1734	G84	-10560	272
1701	G150	-10065	167	1735	G82	-10575	167
1702	G148	-10080	272	1736	G80	-10590	272
1703	G146	-10095	167	1737	G78	-10605	167
1704	G144	-10110	272	1738	G76	-10620	272
1705	G142	-10125	167	1739	G74	-10635	167
1706	G140	-10140	272	1740	G72	-10650	272
1707	G138	-10155	167	1741	G70	-10665	167
1708	G136	-10170	272	1742	G68	-10680	272
1709	G134	-10185	167	1743	G66	-10695	167
1710	G132	-10200	272	1744	G64	-10710	272
1711	G130	-10215	167	1745	G62	-10725	167
1712	G128	-10230	272	1746	G60	-10740	272
1713	G126	-10245	167	1747	G58	-10755	167
1714	G124	-10260	272	1748	G56	-10770	272
1715	G122	-10275	167	1749	G54	-10785	167
1716	G120	-10290	272	1750	G52	-10800	272
1717	G118	-10305	167	1751	G50	-10815	167
1718	G116	-10320	272	1752	G48	-10830	272
1719	G114	-10335	167	1753	G46	-10845	167
1720	G112	-10350	272	1754	G44	-10860	272
1721	G110	-10365	167	1755	G42	-10875	167
1722	G108	-10380	272	1756	G40	-10890	272
1723	G106	-10395	167	1757	G38	-10905	167
1724	G104	-10410	272	1758	G36	-10920	272
1725	G102	-10425	167	1759	G34	-10935	167
1726	G100	-10440	272	1760	G32	-10950	272
1727	G98	-10455	167	1761	G30	-10965	167
1728	G96	-10470	272	1762	G28	-10980	272
1729	G94	-10485	167	1763	G26	-10995	167
1730	G92	-10500	272	1764	G24	-11010	272

PAD No.	PIN Name	X	Y
1765	G22	-11025	167
1766	G20	-11040	272
1767	G18	-11055	167
1768	G16	-11070	272
1769	G14	-11085	167
1770	G12	-11100	272
1771	G10	-11115	167
1772	G8	-11130	272
1773	G6	-11145	167
1774	G4	-11160	272
1775	G2	-11175	167
1776	DUMMY	-11190	272
1777	DUMMY	-11205	167
1778	ALIGN_L	-11300	-277

Unit: μm

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1.. Power Supply Pins

Name	I/O	Description	Connect Pin
VDDI	I	- Power supply for I/O system. - VDDI must be lower than or equal to VDD.	VDDI
VDDA	I	- Power supply for analog and booster circuits. Input voltage level should be the same as VDD.	VDDA
AGND	I	- System ground for analog system and booster circuit.	GND
DGND	I	- System ground for I/O system and digital system.	GND
VPP	I	- Power supply for internal NVM. - Writing NVM needs external power supply voltage with 7.5V. - The current of Ivpp must be more than 10mA. - Leaves these pins open if not used.	-

6.2.. Interface Logic Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect Pin</th></tr>
<tr><td>IM2, IM1,IM0</td><td>I</td><td>-The MCU interface mode select.
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8080 18-bit Interface</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>8080 9-bit Interface</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8080 16-bit Interface</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8080 8-bit Interface</td><td>DB[7:0],</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserve</td><td>--</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3SPI</td><td>SDA, SDO</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MIPI</td><td>MIPI_DATA
MIPI_CLOCK</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4Line SPI</td><td>SDA, SDO</td></tr>
</table></td><td>GND / VDDI</td></tr>
<tr><td>RESET</td><td>I</td><td>- This signal will reset the device and it must be applied to properly initialize the chip.
- Signal is active low.</td><td>MCU</td></tr>
<tr><td>CSX</td><td>I</td><td>- Chip selection pin. Low-active.
- If not used, please fix this pin at VDDI or DGND level.</td><td>MCU</td></tr>
<tr><td>DCX</td><td>I</td><td>-Display data/command selection (RS) pin in MCU interface.
DCX=’1’: display data or parameter.
DCX=’0’: register index / command.
- If not used, please fix this pin at VDDI or DGND level.</td><td>MCU / GND</td></tr>
<tr><td>RDX</td><td>I</td><td>- Read enable in 8080 MCU parallel interface. Low-active.
- If not used, please fix this pin at VDDI or DGND level.</td><td>MCU / GND</td></tr>
<tr><td>WRX/SCL</td><td>I</td><td>- Write enable in MCU parallel interface.
- In SPI mode, this pin is used as SCL.
- If not used, please fix this pin at VDDI or DGND level.</td><td>MCU</td></tr>
<tr><td>VSYNC</td><td>I</td><td>-Vertical synchronizing input signal for RGB interface operation.
-If not used, please fix to the VDDI or DGND.</td><td>MCU</td></tr>
<tr><td>HSYNC</td><td>I</td><td>-Horizontal synchronizing input signal for RGB interface operation.
- If not used, please fix to VDDI or DGND.</td><td>MCU</td></tr>
<tr><td>ENABLE</td><td>I</td><td>-Data enable signal for RGB interface operation.
-If not used, please fix this pin at VDDI or DGND.</td><td>MCU</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>-Dot clock signal for RGB interface operation.
-If not used, please fix this pin at VDDI or DGND.</td><td>MCU</td></tr>
</table>

Name	I/O	Description	Connect Pin
SDA	I/O	- SPI interface input/output pin. - The data is latched on the rising edge of the SCL signal. - If not used, please fix this pin at VDDI or DGND level.	MCU
SDO	O	- SPI interface output pin. - The data is outputted on the falling edge of the SCL signal. - If not used, please fix this pin at floating.	MCU
MIPI_CLK_P	I	-Positive polarity of low voltage differential clock signal -Leave the pin to open when not in use.	MIPI
MIPI_CLK_N	I	-Negative polarity of low voltage differential clock signal -Leave the pin to open when not in use.	MIPI
MIPI_DATA_P	I/O	-Positive polarity of low voltage differential data signal -Leave the pin to open when not in use.	MIPI
MIPI_DATA_N	I/O	-Negative polarity of low voltage differential data signal -Leave the pin to open when not in use.	MIPI
DB[17:0]	I/O	- In MCU 8080 parallel interface, DB[17:0] are used as data bus. 8-bit I/F: DB[7:0] is used. 9-bit I/F: DB[8:0] is used. 16-bit I/F: DB[15:0] is used. 18-bit I/F: DB[17:0] is used. - In RGB interface, DB[17:0] are used as data bus. 16-bit RGB I/F: DB[15:0] are used. 18-bit RGB I/F: DB[17:0] are used. - If not used, please fix this pin at VDDI or DGND level.	MCU / DGND /VDDI
TE	O	- Tearing effect output. - If not used, leave this pin open	MCU
EXTC	I	-When programming NVM, this pin should connect to high level. -During normal operation, please open this pin.	DGND/VDDI

Note1. "1" = VDDI level, "0" = DGND level.

Note2. When in parallel mode, unused data pins must be connected to "1" or "0".

Note3. When CSX="1", there is no influence to the parallel and serial interface.

6.3.. Driver Output Pins

Name	I/O	Description	Connect pin
S1 to S960	O	Source output voltage signals applied to liquid crystal.	LCD
G1 to G480	O	-Gate driver output pins. VGH: Selecting Gate Lines Level. VGL: Non-selecting Gate Lines Level.	LCD
AVDD	O	- Power output pin for monitoring analogy circuit. - Leave open when not in use.	-
AVCL	O	- Power output pin for monitoring analogy circuit. - Leave open when not in use.	-
VAP(GVDD)	O	- Used for monitoring - Leave open.	
VAN(GVCL)	O	- Used for monitoring - Leave open.	
V22	O	- Used for monitoring - Leave open.	
VGH	O	- Power output pin for gate driver - Leave open when not in use.	-
VGL	O	- Power output (Negative) pin for gate driver - Leave open when not in use.	-
VCC	O	- Monitoring pin of internal digital reference voltage. - Leave open when not in use.	-
VCOM	O	- A power supply for the TFT-LCD common electrode.	Common Electrode
CABC_PWM	O	-Output pad for PWM output signal to driving LED. -If not used, keep it open.	-
CABC_ON	O	-Output pad for enabling LED. -If not used, keep it open.	-

6.4.. Test and Other Pins

Name	I/O	Description	Connect pin
Dummy	-	- These pins are dummy - ***Leave the pin open.***	-
OSCP		- This pin is for testing. ***- Leave the pin open.***	
TS[0:2]		- Test pins, these pins are internal weak pull low. ***- Leave the pin open.***	
TEST[0:5]		- This pin is for testing ***- Leave the pin open.***	
TESTO1~10		- This pin is for testing output. ***- Leave the pin open.***	

7 DRIVER ELECTRICAL CHARACTERISTICS

7.1.. Absolute Operation Range

Item	Symbol	Range	Unit
Supply Voltage (Analog)	VDDA	- 0.3 ~ +4.6	V
Supply Voltage (I/O)	VDDI	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VCC	-0.3 ~ +2	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	0.5 ~ VDDI + 0.5	V
Logic Output Voltage Range	VO	0.5 ~ VDDI + 0.5	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

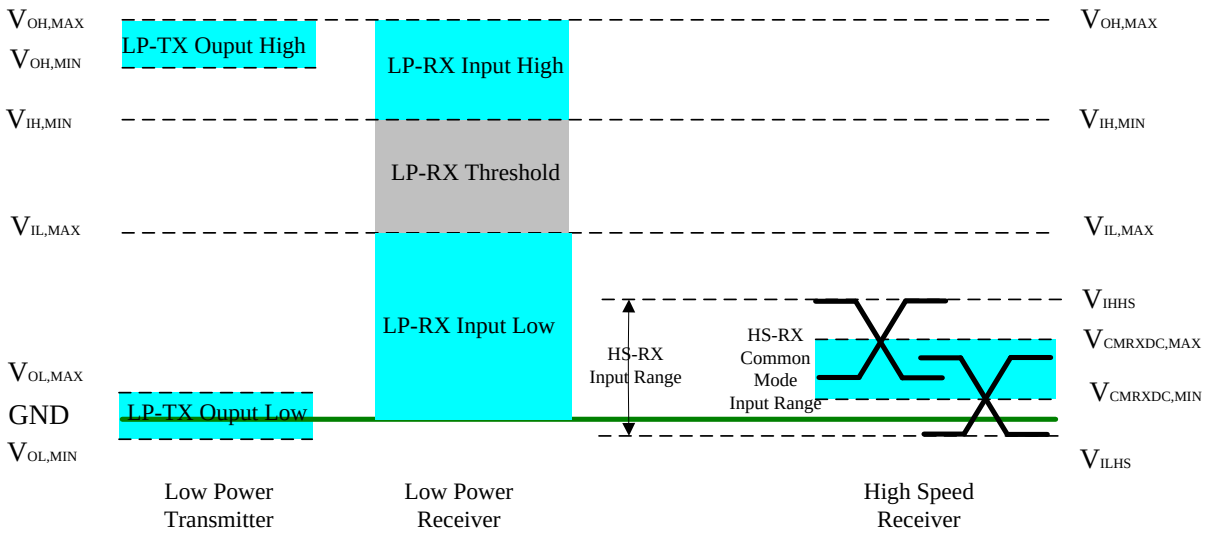
Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2.. DC Characteristics

7.2.1 DC characteristics for MIPI DSI

● MIPI Signaling Voltage Levels



● MIPI DC characteristics

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	V_{LPH}	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Logic 0 input threshold	V_{IL}	0	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	1350	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V

7.2.2 DC Characteristics for Panel Driving

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD / VDDA	Operating voltage	2.5	2.75	3.3	V	
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	
Gate Driver High Voltage	VGH		12.54		15.46	V	
Gate Driver Low Voltage	VGL		-12.5		-7.15	V	
Gate Driver Supply Voltage		| VGH-VGL |			27.96	V	
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	Note 1
Differential Input High Threshold Voltage	VIT+			0	50	mV	MIPI_CLK, MIPI_DATA
Differential Input Low Threshold Voltage	VIT-		-50	0		mV	
Single-ended Receiver Input Operation Voltage Range	VIR		0.5		1.2	V	
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI			1	uA	Note 1
Logic-Low Input Current	IIL	VIN = VSS	-1			uA	Note 1
Input Leakage Current	ILI	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM Voltage							
VCOM Voltage	VCOM			VSS		V	
Source Driver							
Gamma Reference Voltage(Positive)	VAP		4.45		6.4	V	
Gamma Reference Voltage(Negative)	VAN		-4.6		-2.65		
Source Output Settling Time	Tr	Below with 99% precision			20	us	Note 2

Output Offset Voltage	VOFFSET				35	mV	Note 3

Basic DC Characteristics

Notes:

1. TA= -30 to 85℃.

2. Source channel loading= 2KΩ+12pF/channel, Gate channel loading=5KΩ+40pF/channel.

3. The max. value is between measured point of source output and gamma setting value.

7.3.. Power Consumption

Ta=25℃, Frame rate = 60Hz, Registers setting are IC default setting.

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
Normal Mode	Note 1	0.005	12	0.01	16
Stand by Mode	Note 1	0.005	0.025	0.01	0.050

Power Consumption

Notes:

1. All pixels black.

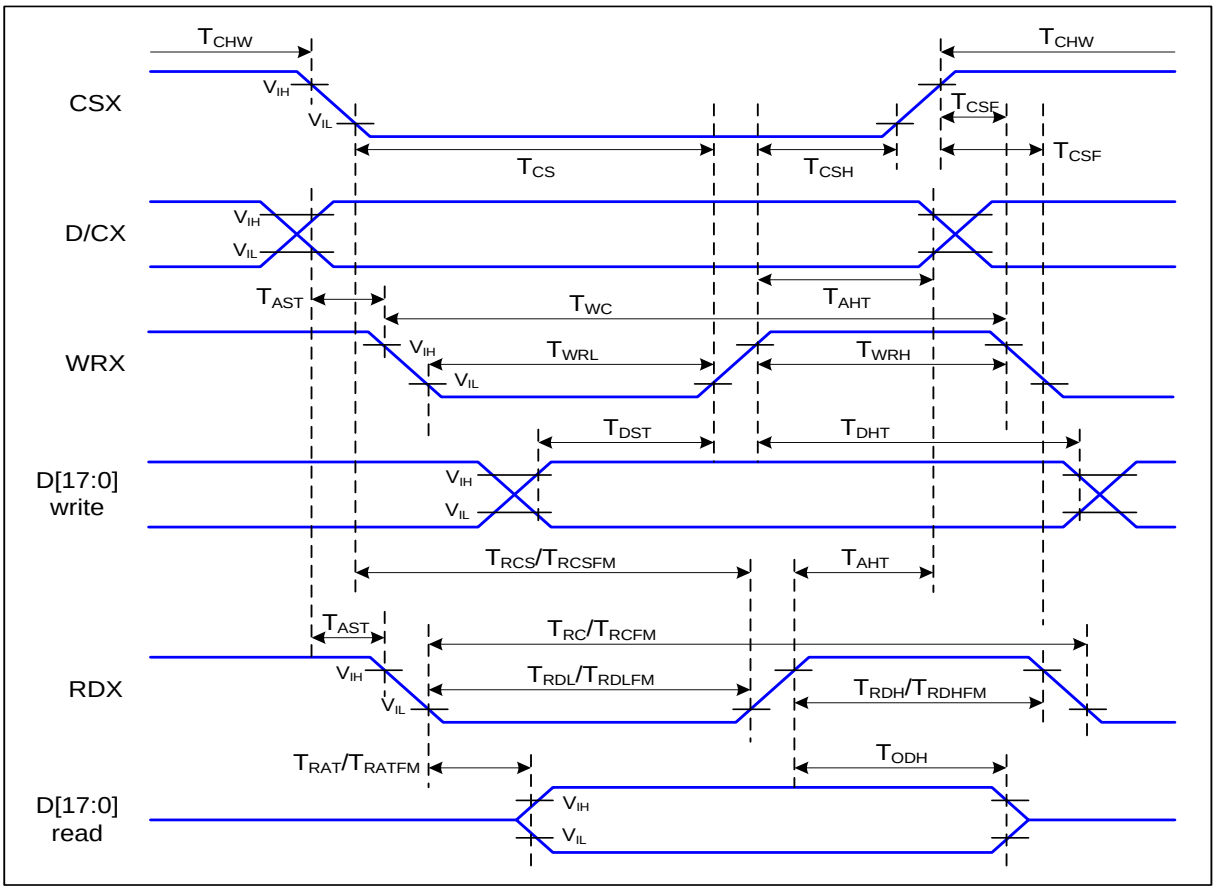
2. All pixels white.

3. The Current Consumption is DC characteristics of ST7796U.

4. Typical: VDDI=1.8V, VDDA=2.8V; Maximum: VDDI=3.3V, VDDA=3.3V

7.4.. AC Characteristics

7.4.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



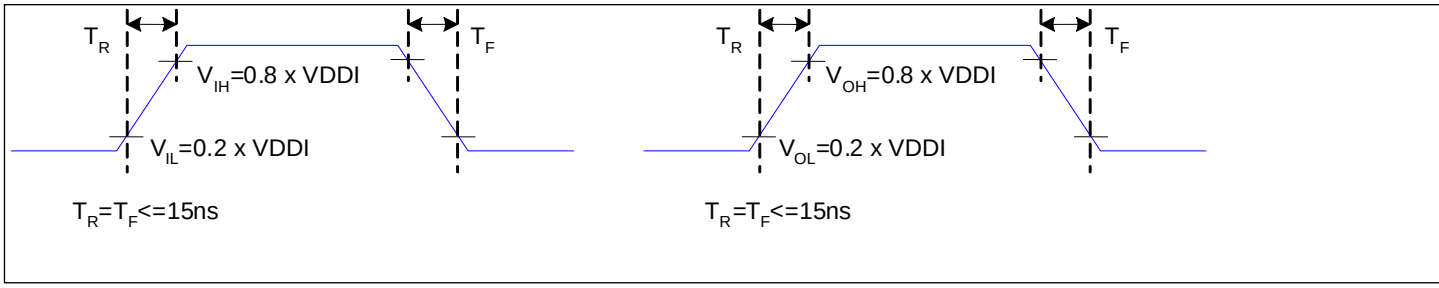
Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select “H” pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse “H” duration	15		ns	

	T_{WRL}	Control pulse “L” duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	20	80	ns	

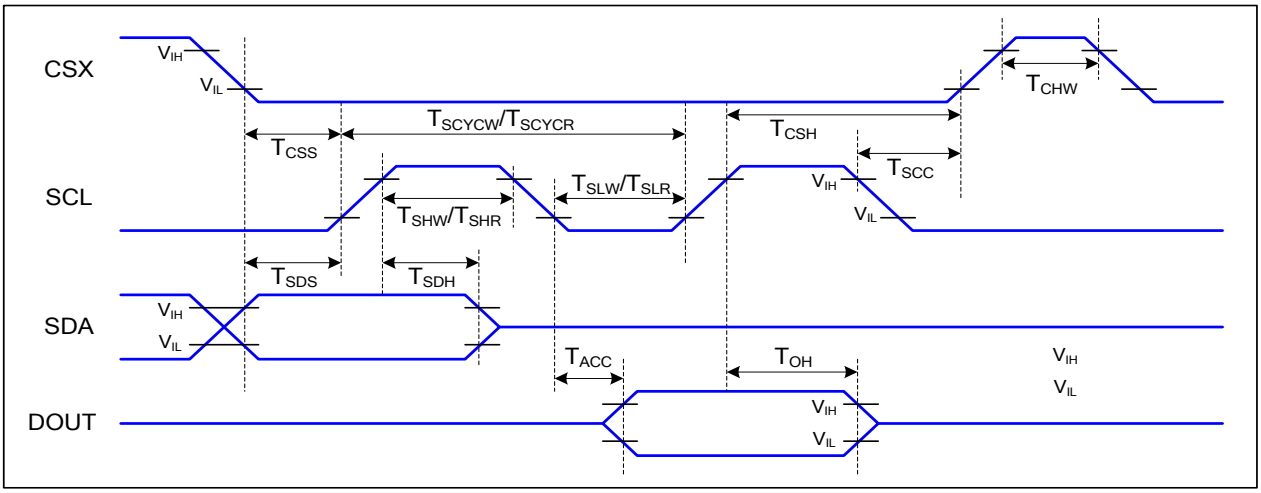
8080 Parallel Interface Characteristics



Rising and Falling Timing for I/O Signal

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

7.4.2 3-SPI Serial Data Transfer Interface Characteristics:



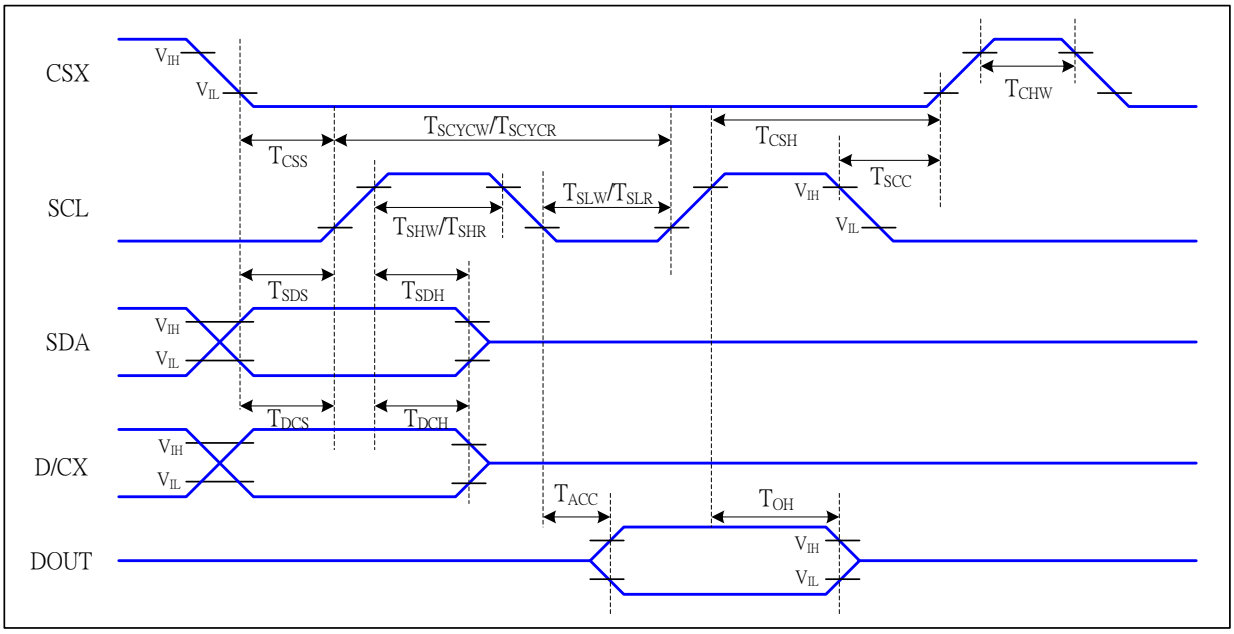
3-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-SPI Interface Characteristics

7.4.3 4-SPI Serial Data Transfer Interface Characteristics:

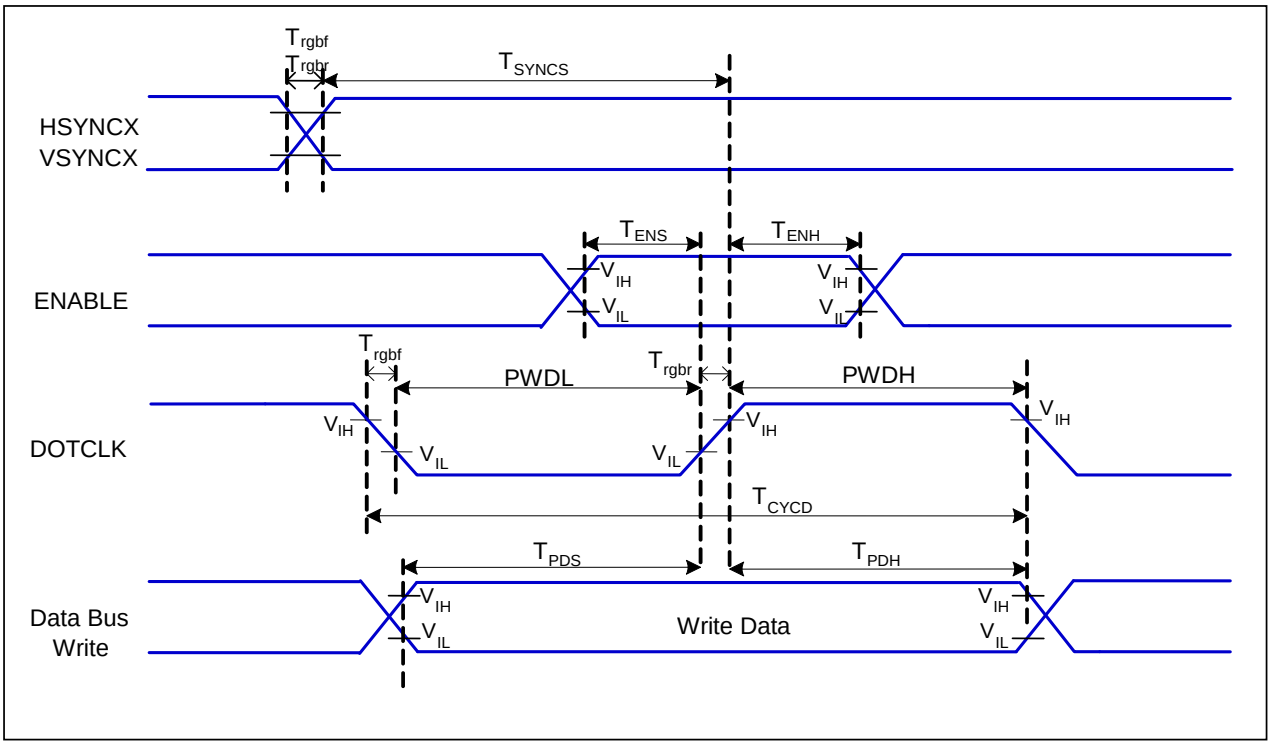


4-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

7.4.4 RGB Interface Characteristics:



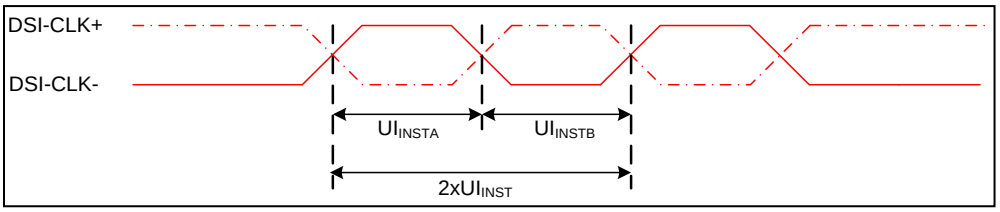
VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	30	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	30	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	66	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

RGB Interface Timing Characteristics

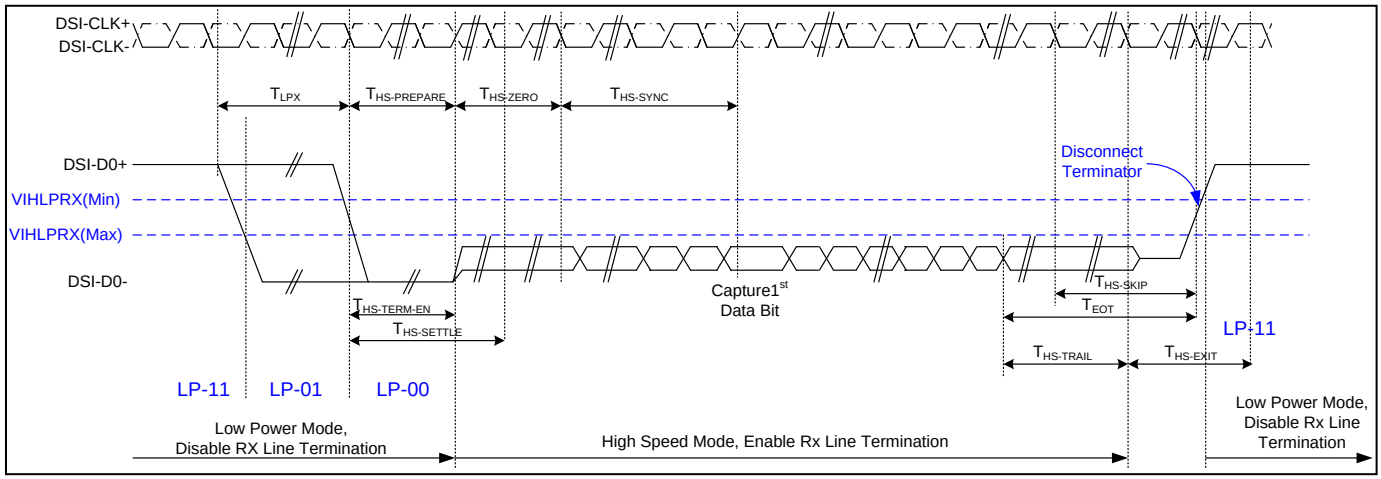
7.4.5 MIPI Interface Characteristics

High Speed Mode – Clock Channel Timing



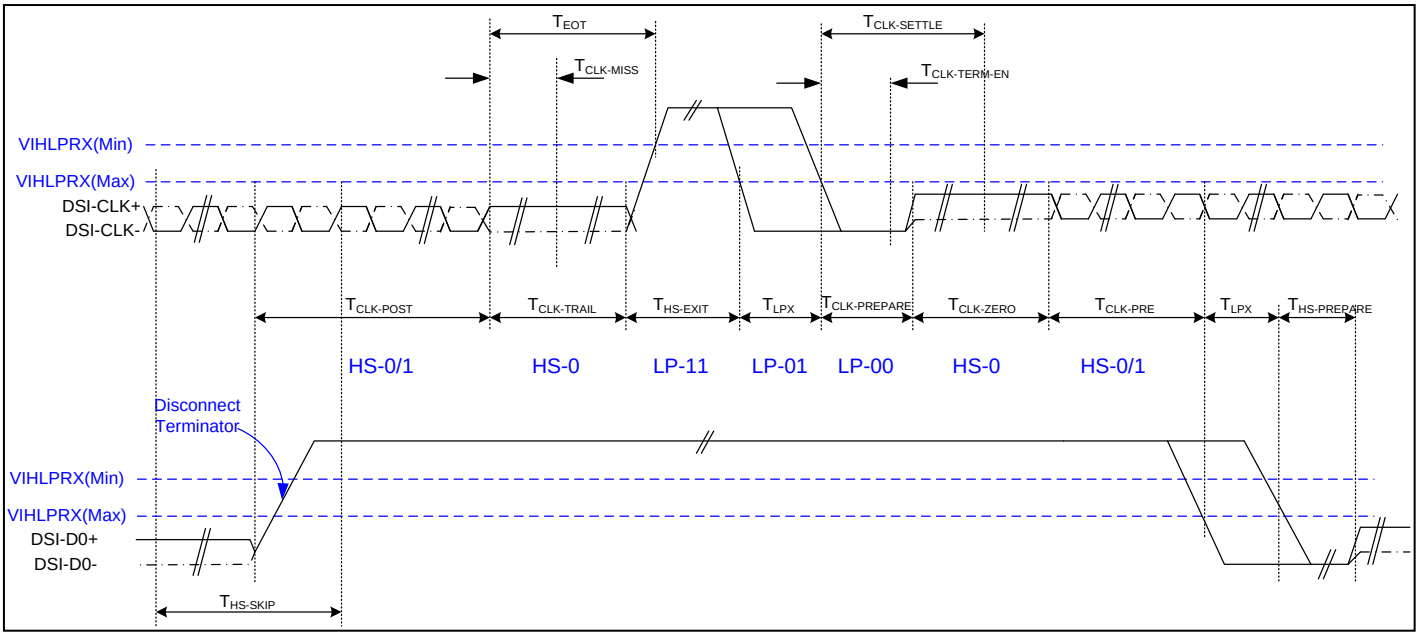
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-DATA_P/N	2xUI INST	Double UI instantaneous	4	25	ns	
DSI-DATA_P/N	UI INSTA ,UI INSTB	UI instantaneous Half	2	12.5	ns	

High-Speed Data Transmission



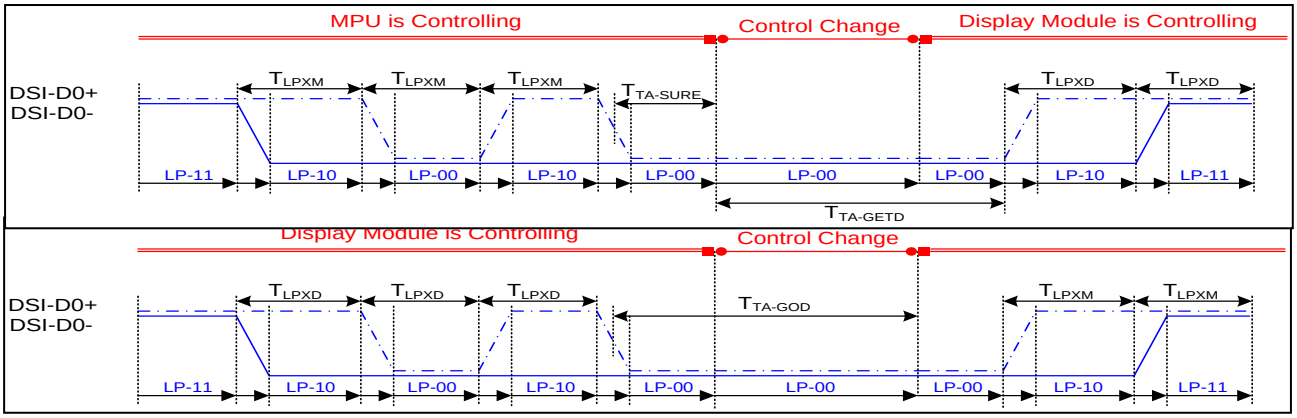
Parameter	Symbol	MIN	TYP	MAX	Unit
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable data receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode



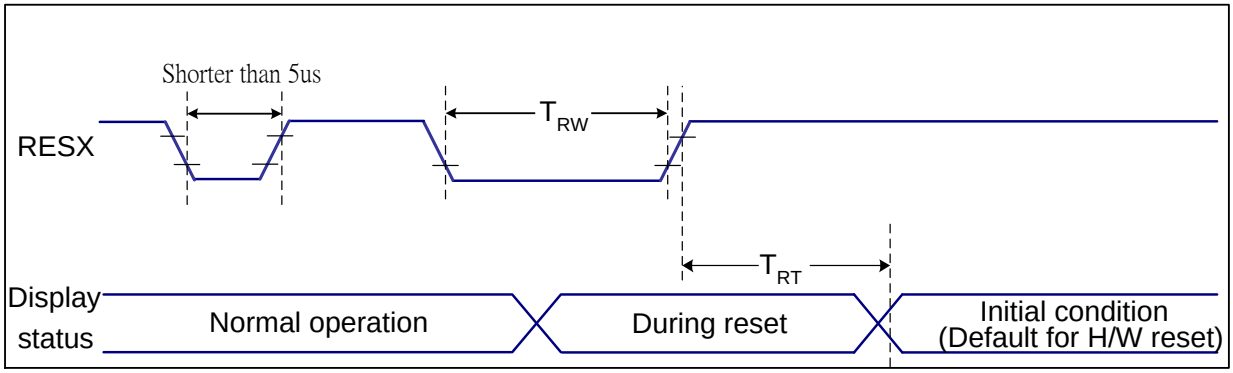
Parameter	Symbol	MIN	TYP	MAX	Unit
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI			ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$			60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38		95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60			ns

Bus Turnaround Procedure



Parameter	Symbol	MIN	TYP	MAX	Unit
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	47.5	50	52.5	ns
Ratio of T_{LPX} (MASTER)/ T_{LPX} (SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		2 T_{LPX}	ns
Time to drive LP-00 by new TX	T_{TA-GET}		5 T_{LPX}		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		4 T_{LPX}		ns

7.4.6 Reset Timing



Reset Timing

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 1 Reset Timing

Notes:

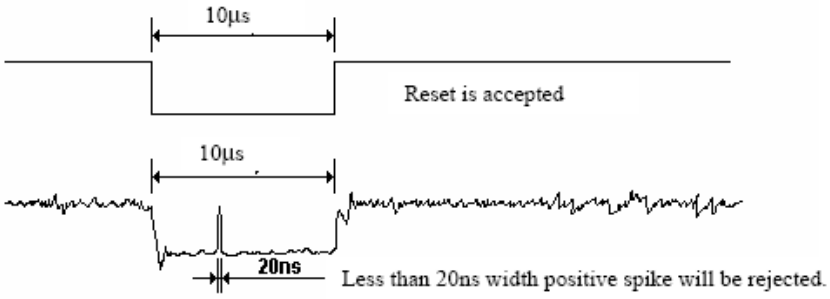
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8 INTERFACE

8.1.. MPU Interface Type Selection

For communicating with MCU, ST7796U supports 8-/9-/16-/18-bit 8080-series interface, SPI, MIPI. Selection of these interfaces are set by IM[2:0] pins as shown below.

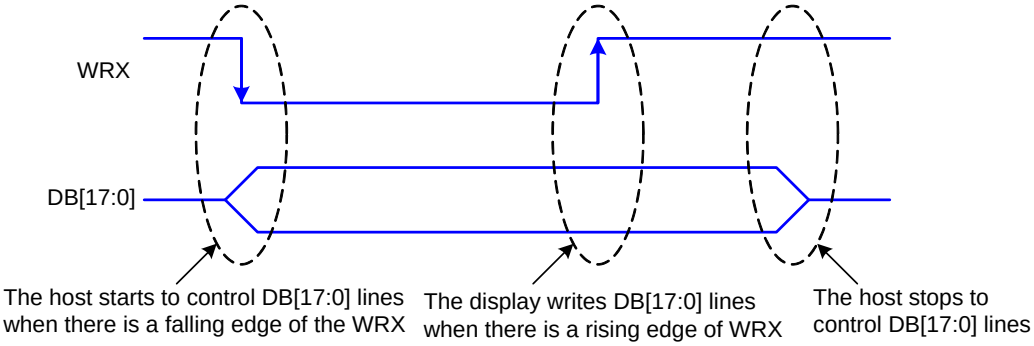
IM2	IM1	IM0	Interface	Read Back Data Bus Selection
0	0	0	8080-series MCU 18-bit	DB[17:0]
0	0	1	8080-series MCU 9-bit	DB[8:0]
0	1	0	8080-series MCU 16-bit	DB[15:0]
0	1	1	8080-series MCU 8-bit	DB[7:0]
1	0	0	Reserve	--
1	0	1	Serial Peripheral Interface(3-Line SPI)	SDA, SDO
1	1	0	MIPI	MIPI_DATA_P/N, MIPI_CLOCK_P/N
1	1	1	Serial Peripheral Interface(4-Line SPI)	SDA, SDO

Interface Type Selection

8.2.. 8080-Series MCU Interface

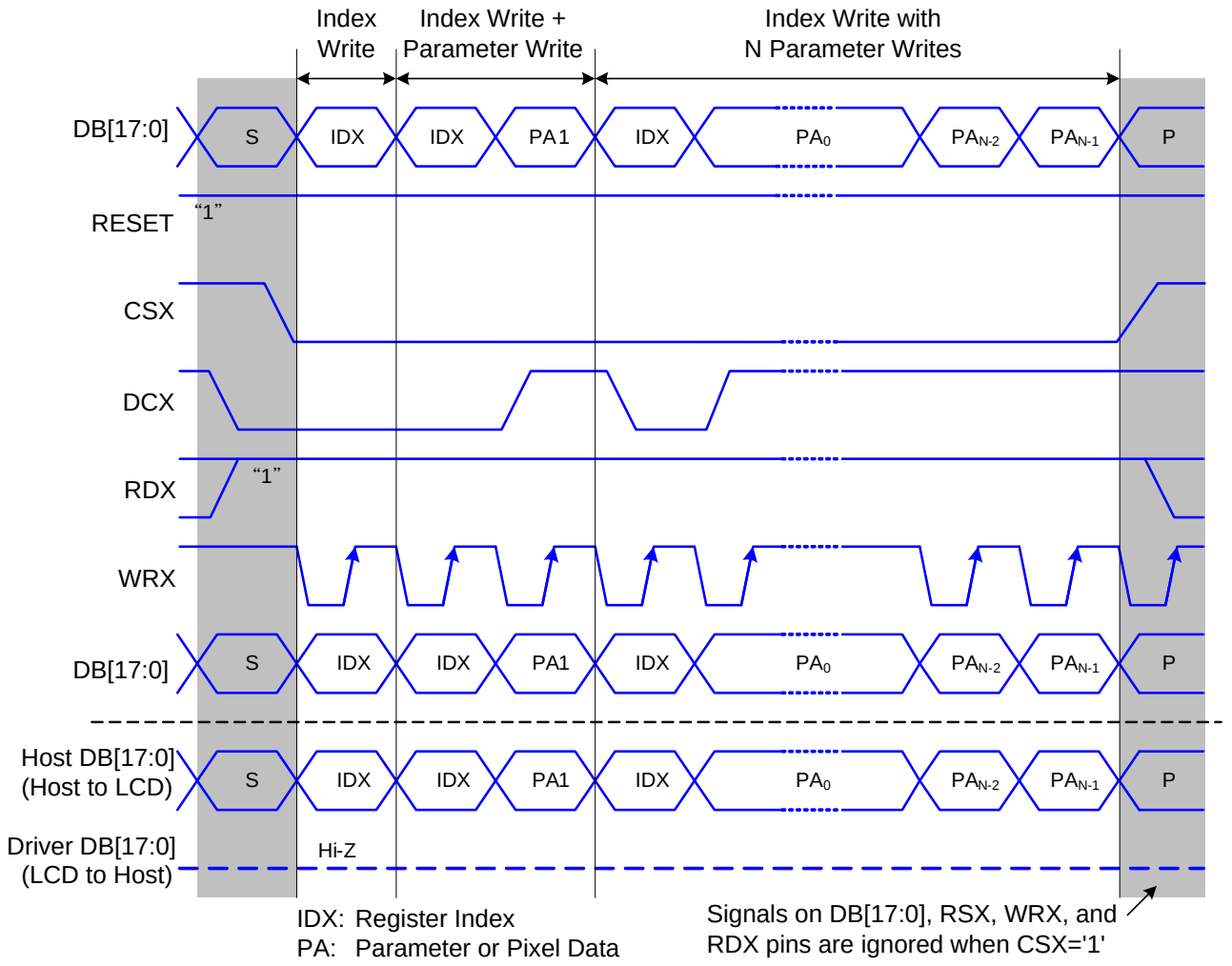
8.2.1 8080-Series MCU Write Cycle Sequence

The write cycle means that the host writes information (register index / parameter) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (DCX, RDX, WRX) and data signals (DB[17:0]). DCX is a control signal, which tells if the data is an index or a parameter. The data signals represent index number if the signal is low (DCX=’0’) and vice versa the data signals represent parameter (DCX=’1’).



Note: WRX is an synchronized signal (It can be stopped).

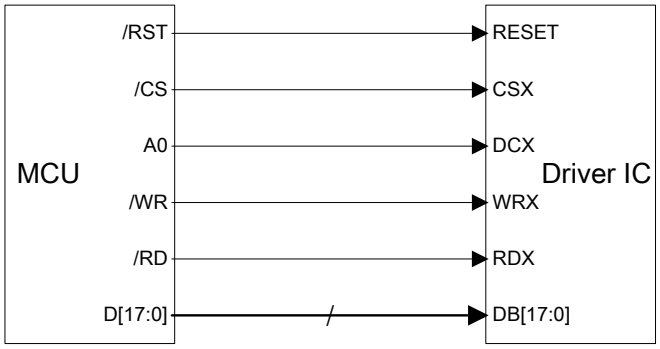
8080-Series WRX Protocol



8080-Series Parallel Bus Protocol, Write to Register or Display RAM

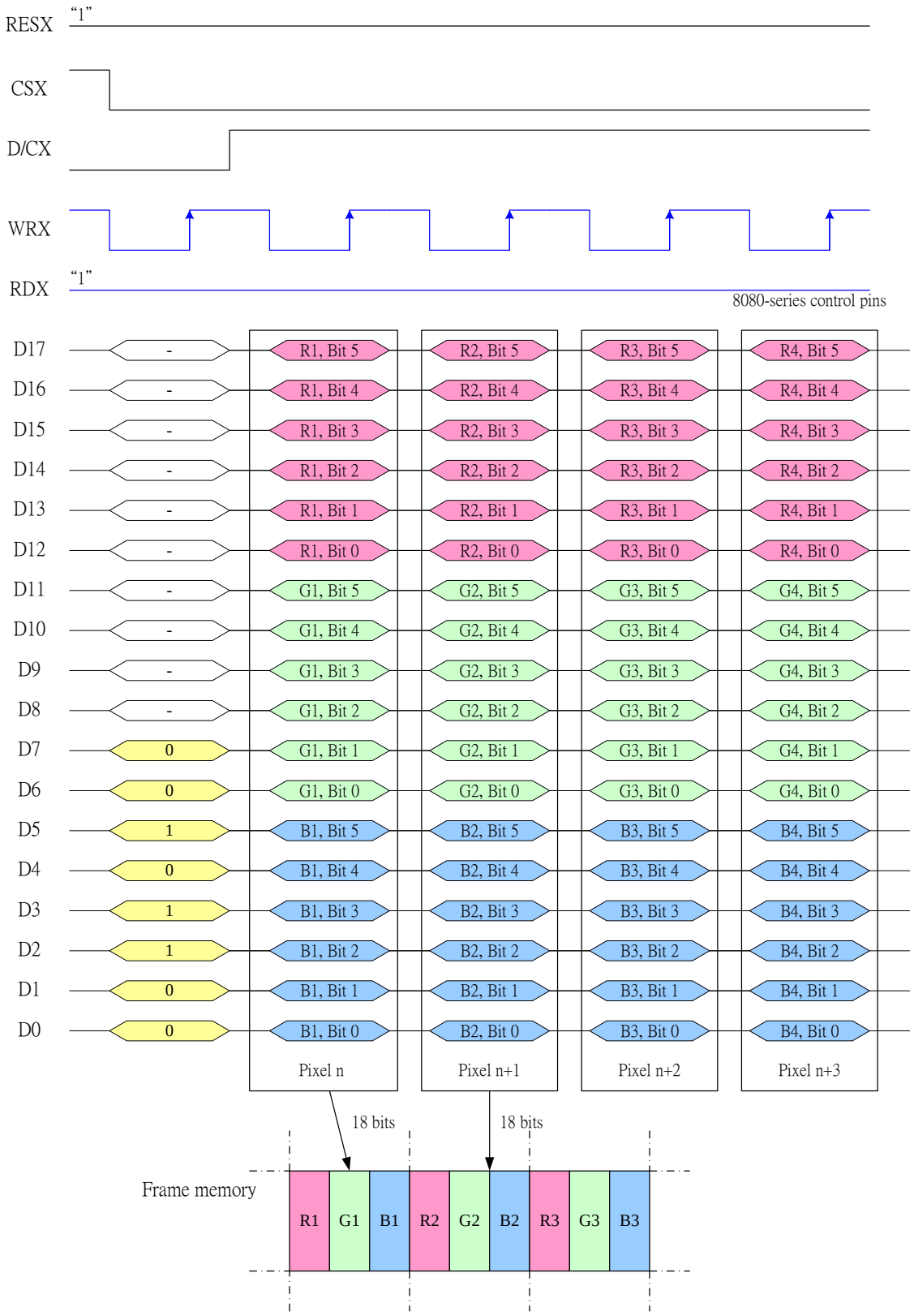
8.2.2 18-bit 8080-Series Interface Write Format

The 18-bit 8080-series interface is selected by setting the IM [2:0] ="000".



18-bit 8080-Series Interface Connection

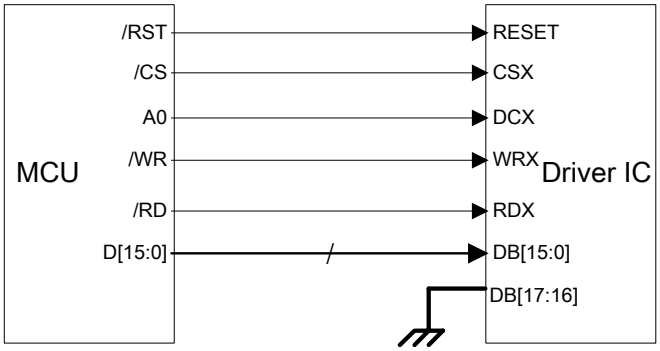
This mode accepts only 262k colors format in display. In this interface, index, parameter, and pixel-data should be written according to the following figures.



18-bit 8080-Series Interface Data Format (Index/Parameter/Pixel Data Write)

8.2.3 16-bit 8080-Series Interface Write Format

The 16-bit 8080-series interface is selected by setting IM[2:0]=”010”.

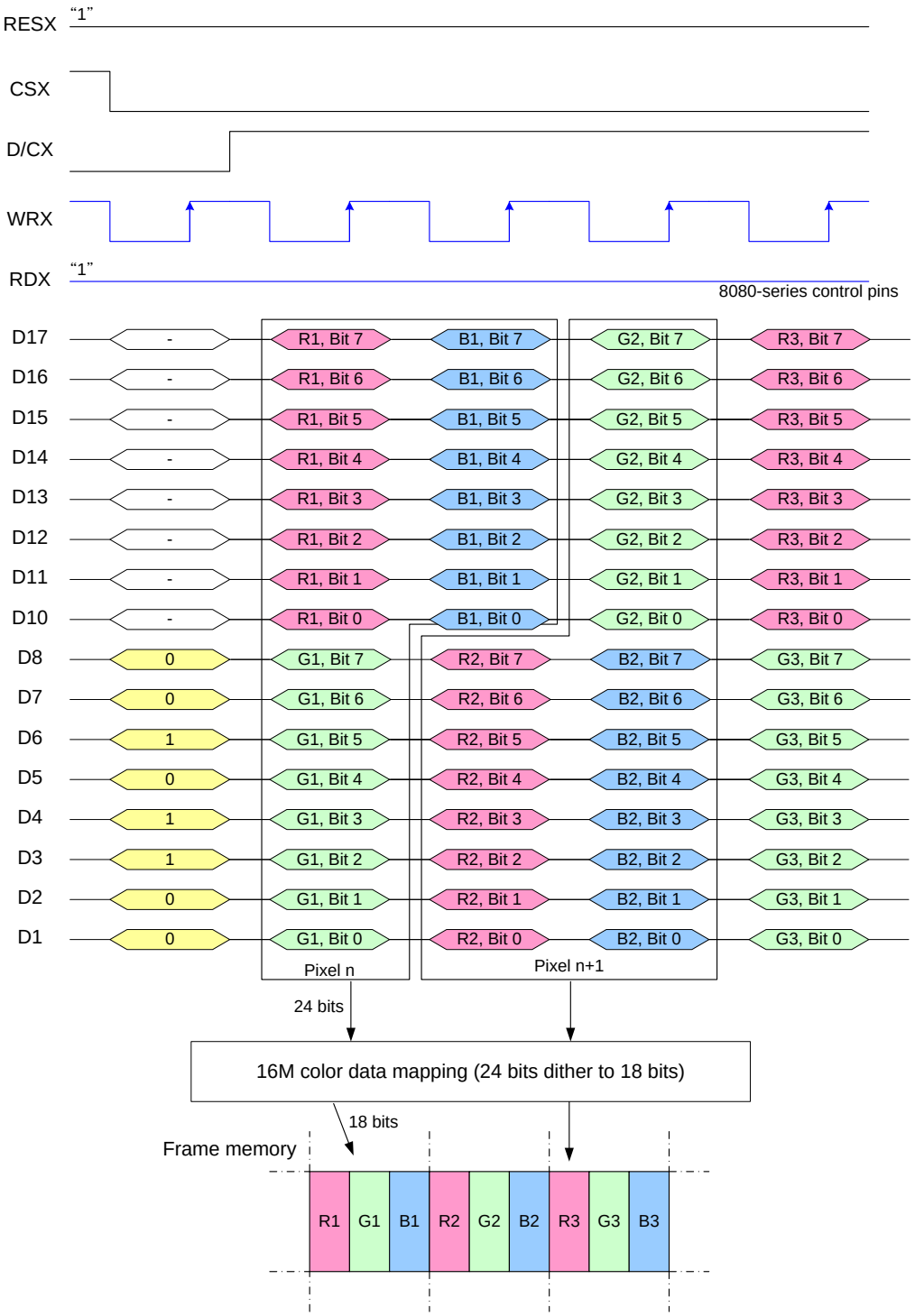


16-bit 8080-Series Interface Connection

ST7796U accepts 262k-color or 65k-color format in this mode. When the 262k-color format is used, two transfers for each pixel are required.

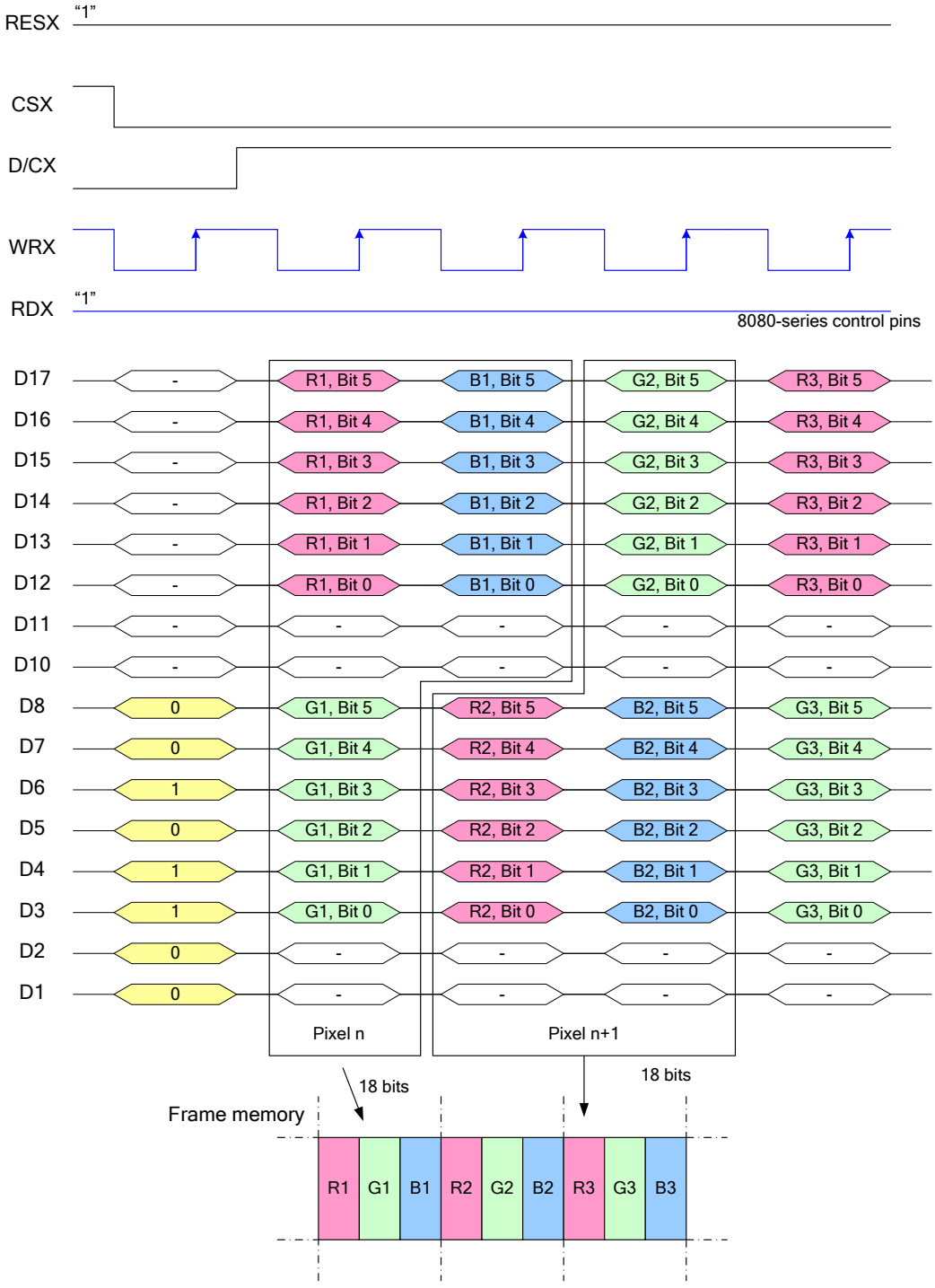
16-bit data bus for 24-bit/pixel (RGB-8-8-8-bit input), 16M-Colors, 3Ah=”07h”)

There are 2 pixels (6 sub-pixels) per 3 bytes



16-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h")

There are 2 pixels (6 sub-pixels) per 3 bytes

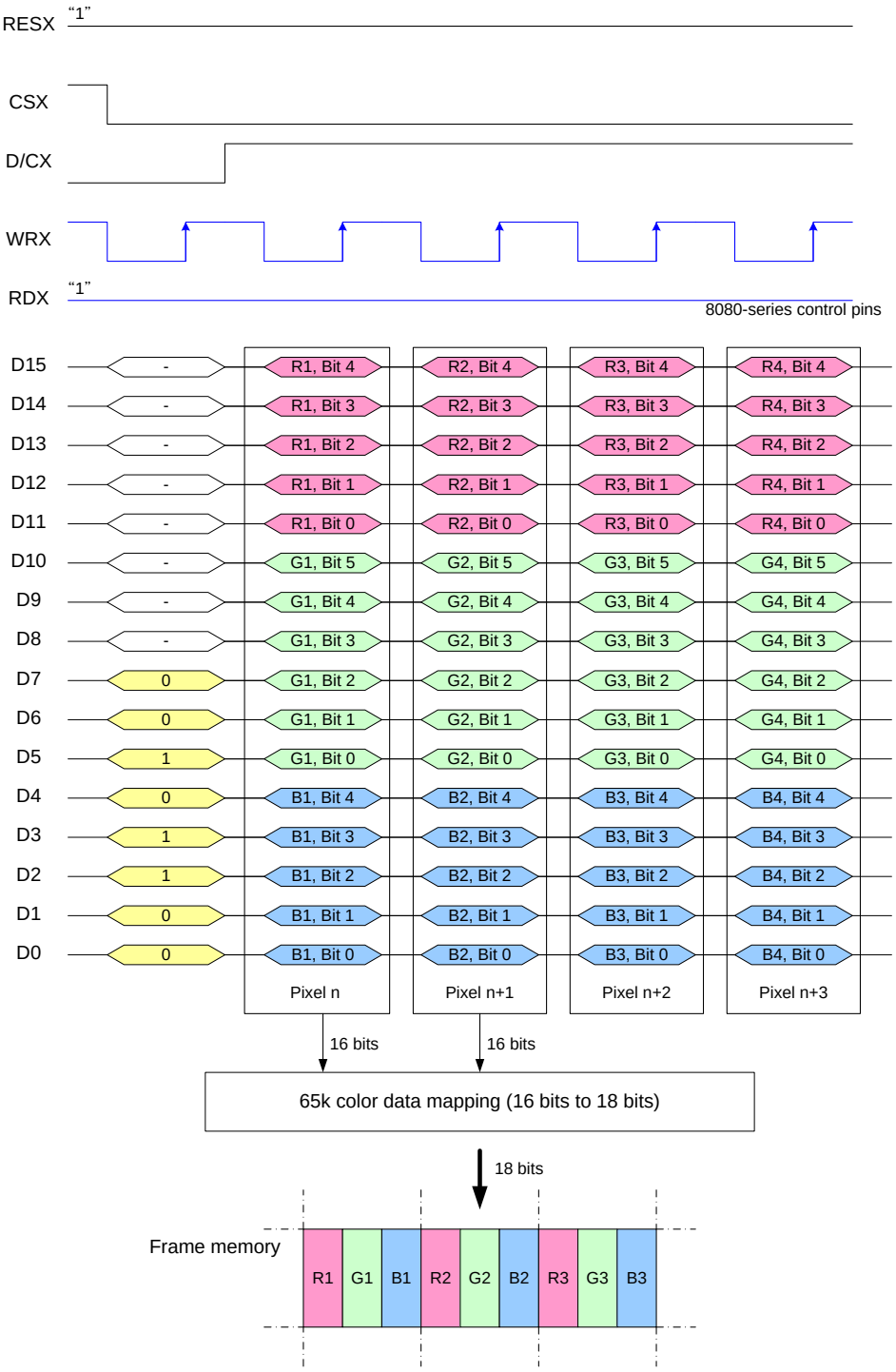


Note 1: The data order is as follows, MSB=D17, LSB=D1 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

16-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input) 65K-Color, 3Ah="05h)



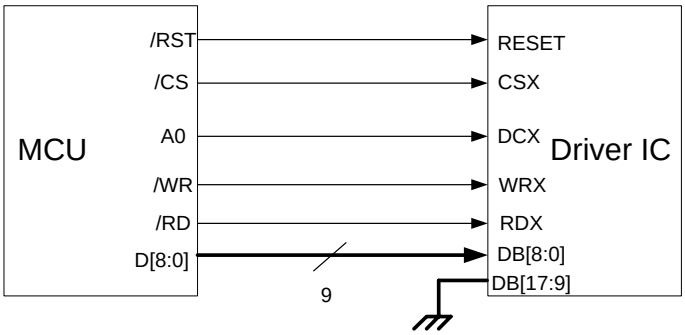
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

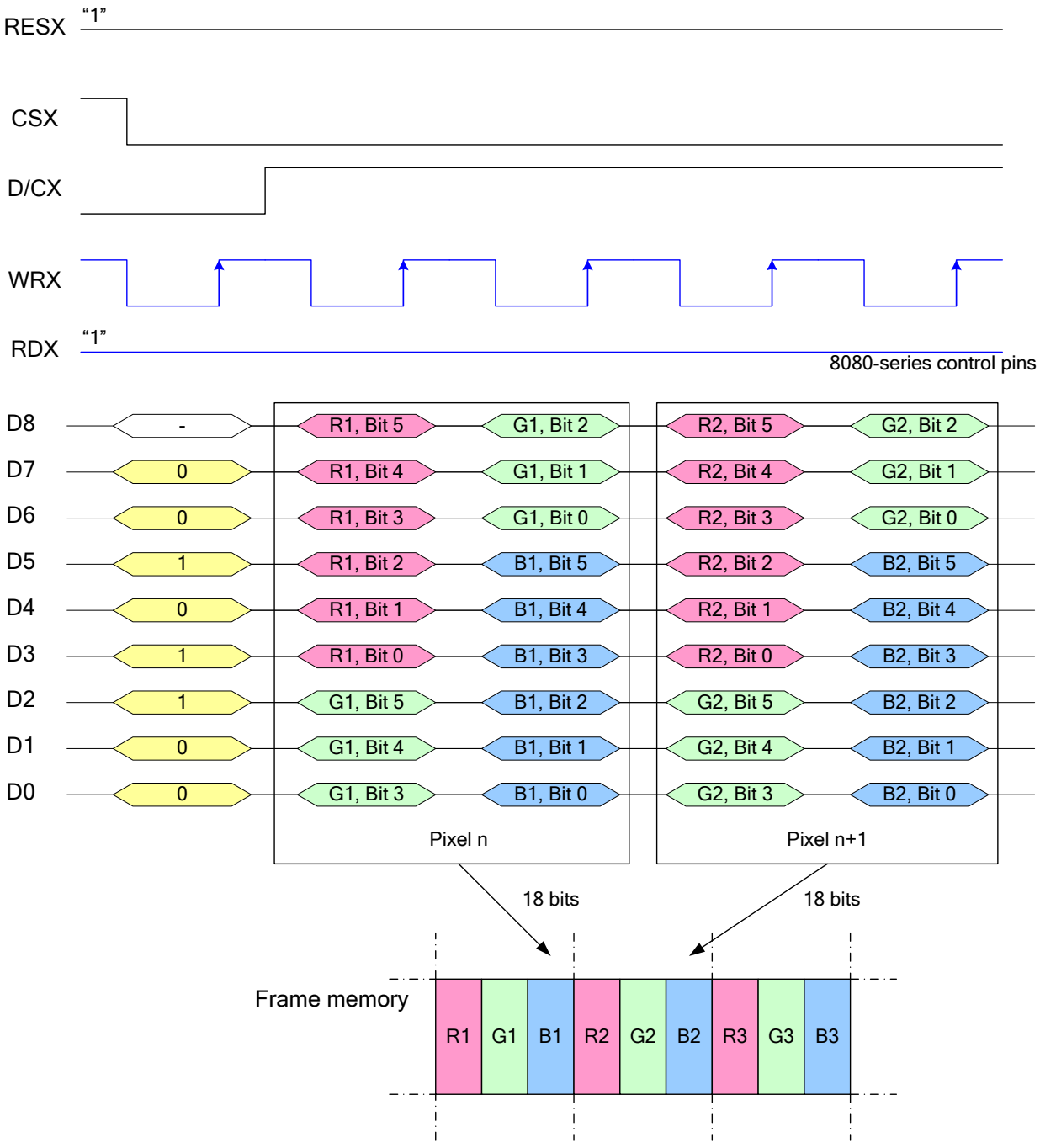
8.2.4 9-bit 8080-Series Interface Write Format

The 9-bit 8080-series interface is selected by setting the IM [2:0] = “011” and the DB [17:9] pins are used to transfer data. The display data is divided into upper part and lower part (9-bit for each part), and the upper part is transferred first. The unused DB [8:0] pins must be tied to either VDDI or DGND.



9-bit 8080-Series Interface Connection

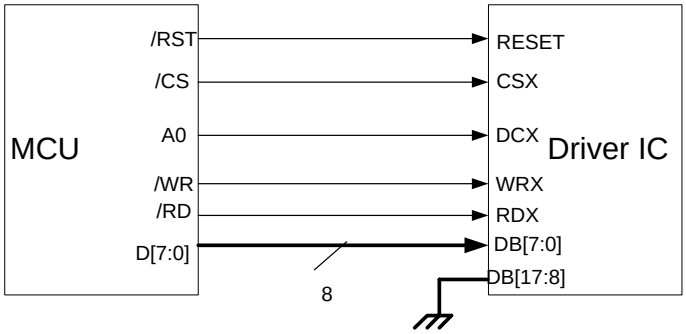
9-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3Ah="06h"



9-bit 8080-Series Interface Data Format (Index/Parameter/Pixel Data Write)

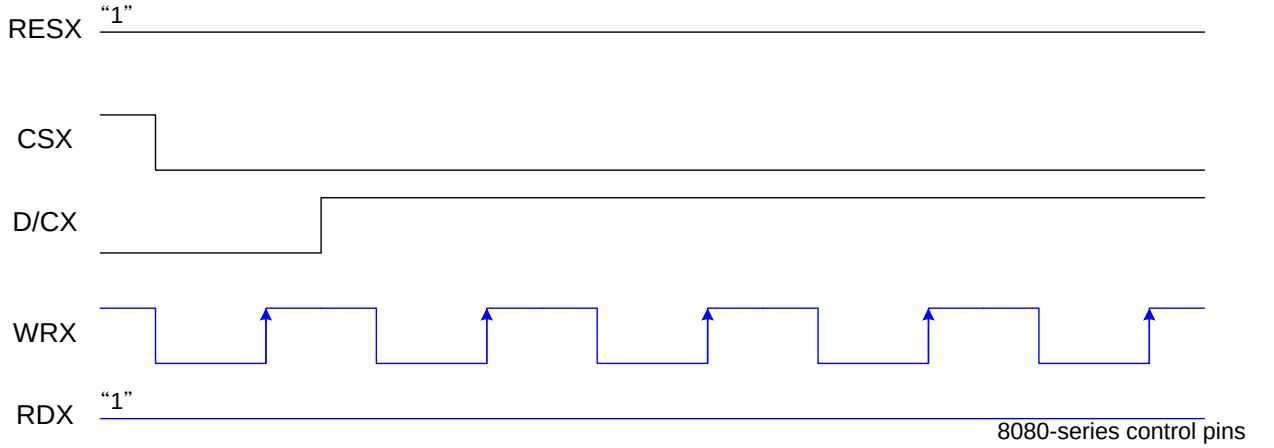
8.2.5 8-bit 8080-Series Interface Write Format

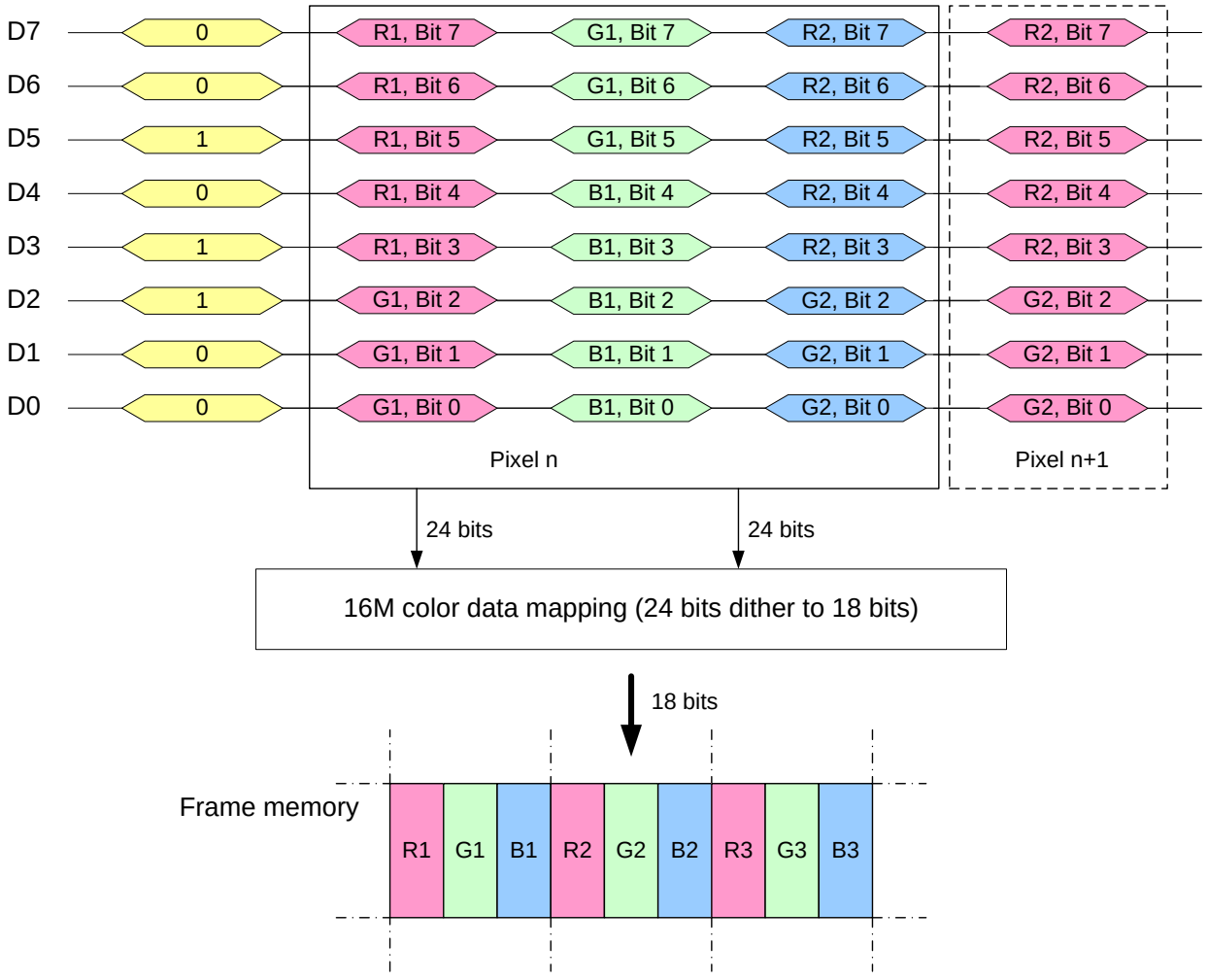
The 8080 8-bit interface is selected by setting the IM [2:0] as “011” and the DB [7:0] pins are used to transfer data. The mode accepts 262k-color or 65k-color format. The display data is divided into upper byte and lower byte, and the upper byte is transferred first. The written data is expanded into 18-bit internally (see the figure below) and then written into DRAM. The unused DB [17:8] pins must be tied to either VDDI or DGND.



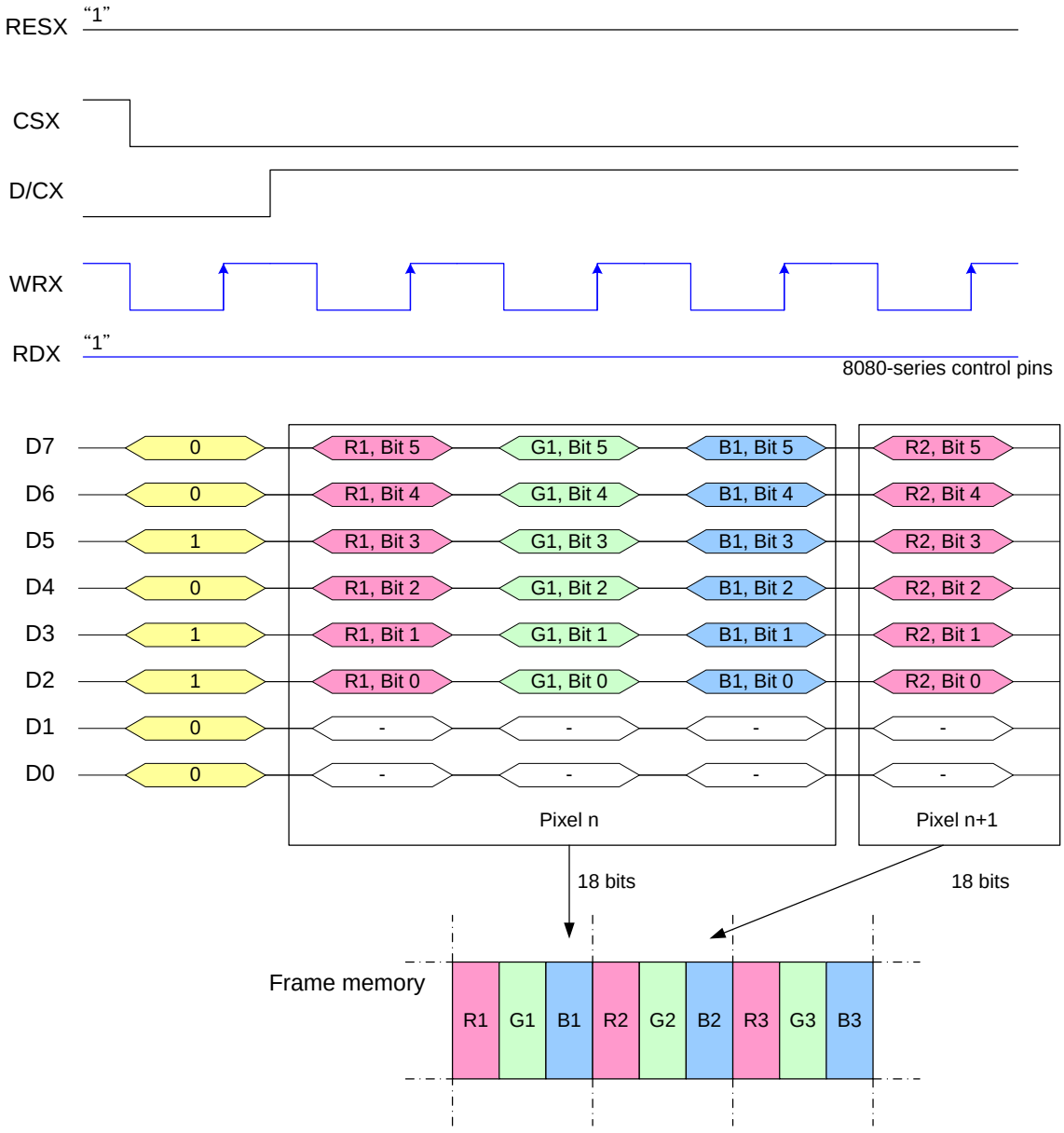
8-bit 8080-Series Interface Connection

8-bit data bus for 24-bit/pixel (RGB 8-8-8-bit input), 16M-Colors, 3Ah="07h"



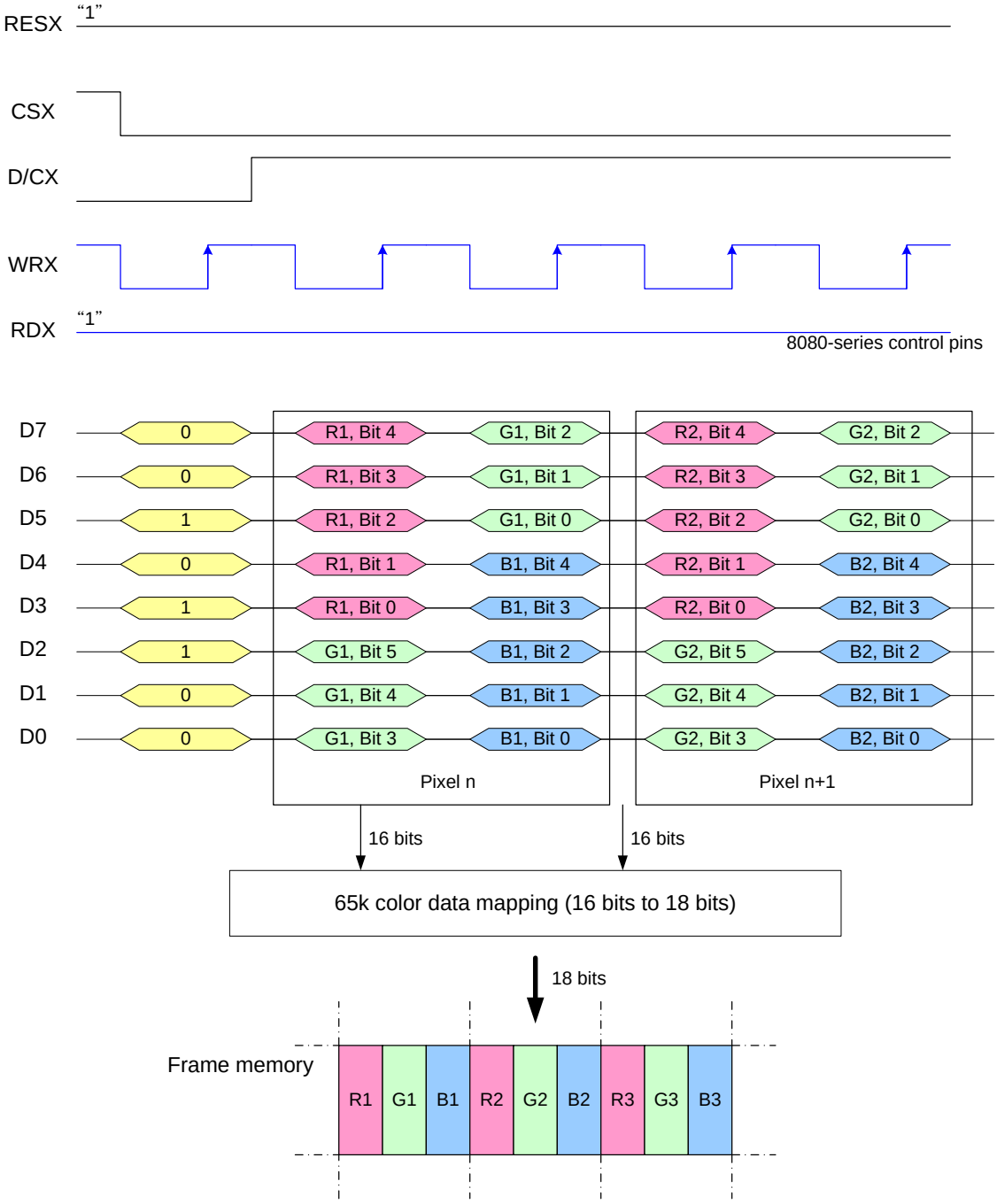


8-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3Ah="06h"



8-bit 8080-Series Interface Data Format (Index/Parameter/Pixel Data Write)

8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="05h"



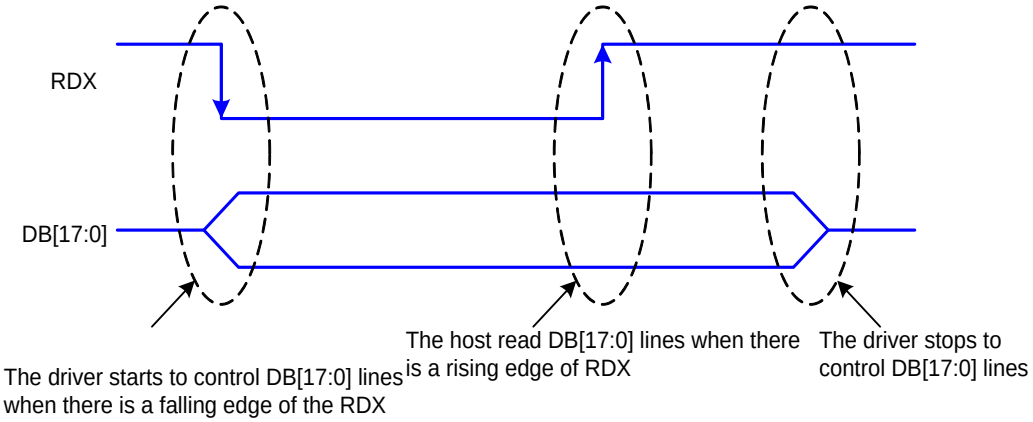
Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer transmit 1 pixel data with the 16-bit color depth information.

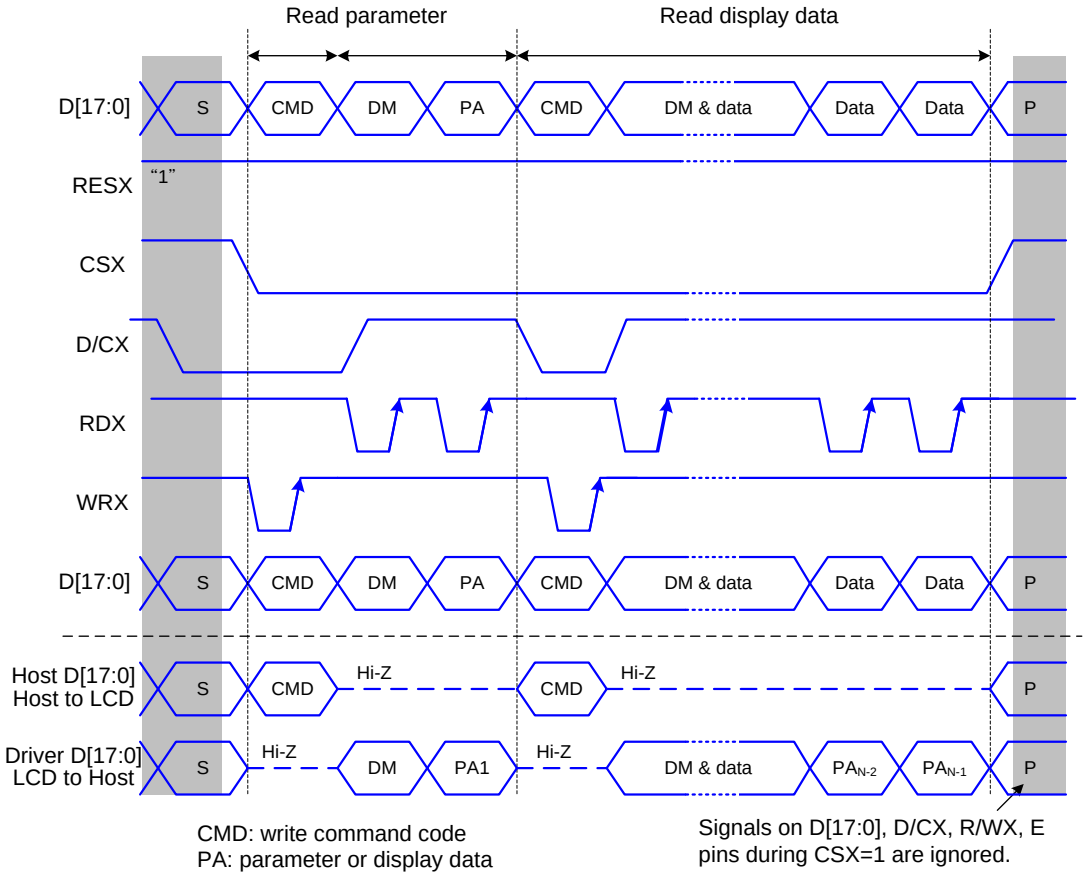
Note 3: '-' = Don't care – Can be set to '0' or '1

8.2.6 8080-series MCU Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The driver sends data (DB [17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

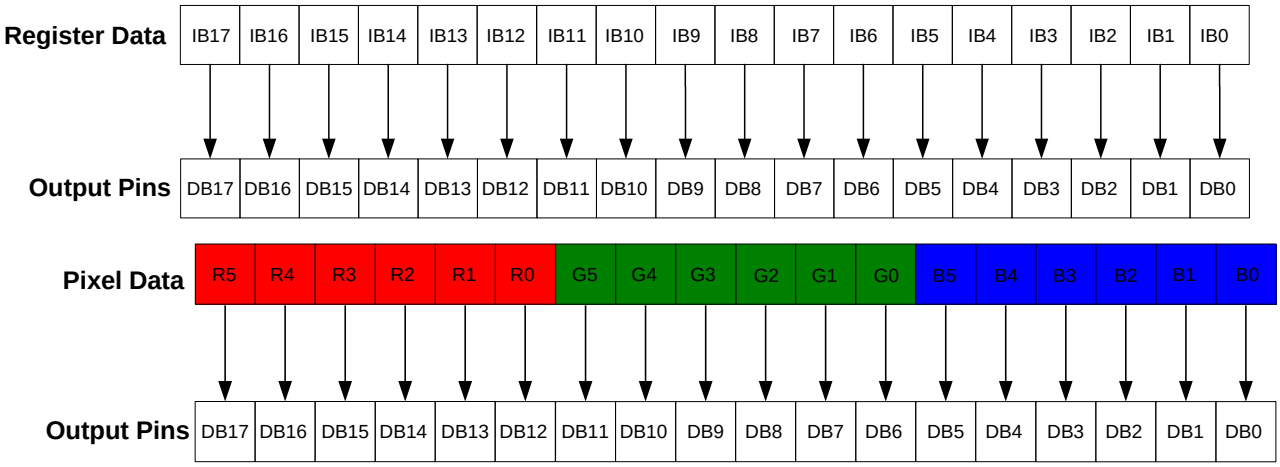


8080-Series RDX Protocol



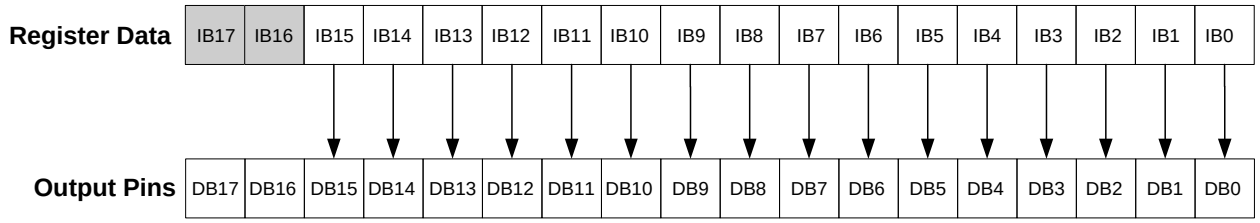
8080-Series Parallel Bus Protocol, Read from Register or Display RAM

8.2.7 18-bit 8080-Series Interface Read Format



18-bit 8080-Series Interface Data Format (Register/Pixel Data Read)

8.2.8 16-bit 8080-Series Interface Read Format



16-bit data bus for 18-bit/pixel, 262K-Colors, 3Ah="06h"

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	BUS width
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Dummy Read
R5	R4	R3	R2	R1	R0	X	X	G5	G4	G3	G2	G1	G0	X	X	3 Transfer 2 Pixel
B5	B4	B3	B2	B1	B0	X	X	R5	R4	R3	R2	R1	R0	X	X	
G5	G4	G3	G2	G1	G0	X	X	B5	B4	B3	B2	B1	B0	X	X	

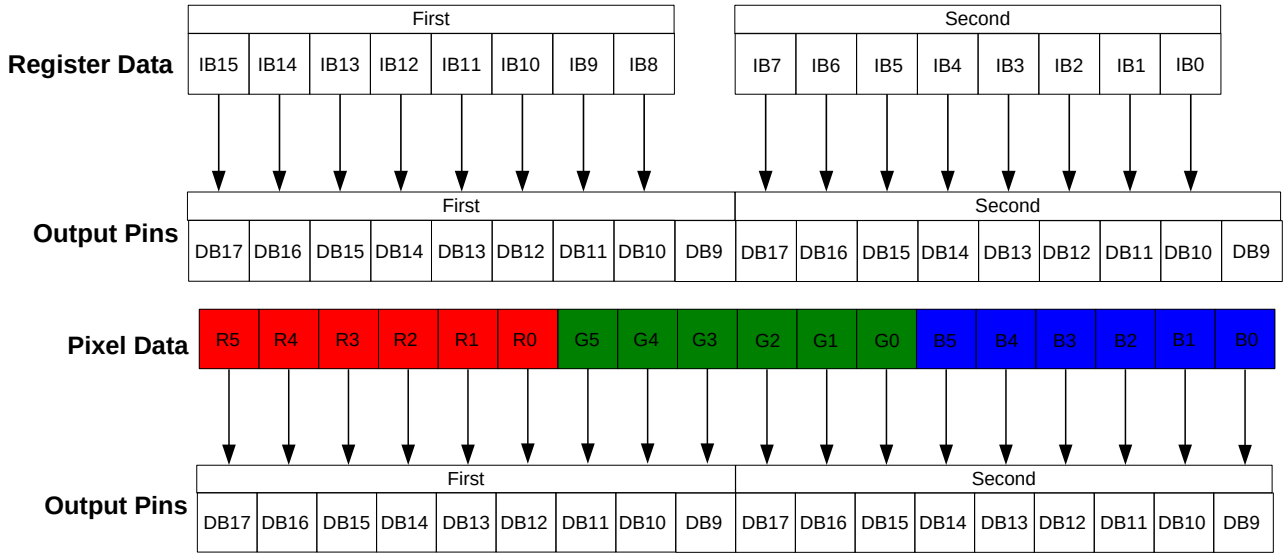
16-bit 8080-Series Interface Data Format 262K (Register/Pixel Data Read)

16-bit data bus for 16-bit/pixel, 65K-Colors, 3Ah="05h"

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	BUS width
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Dummy Read
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1 Transfer 1 Pixel

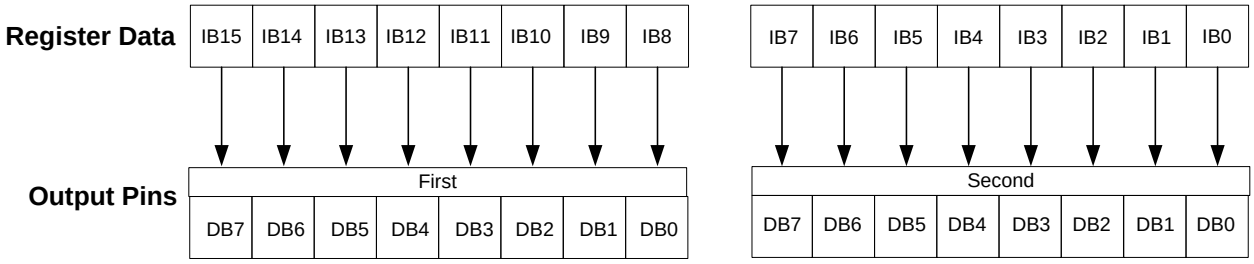
16-bit 8080-Series Interface Data Format 65K (Register/Pixel Data Read)

8.2.9 9-bit 8080-Series Interface Read Format



9-bit 8080-Series Interface Data Format (Register/Pixel Data Read)

8.2.10 8-bit 8080-Series Interface Read Format



8-bit data bus for 18-bit/pixel, 262K-Colors, 3Ah=”06h”

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	BUS width
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Dummy Read
X	X	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	X	X	3 Transfer 1 Pixel
X	X	X	X	X	X	X	X	G5	G4	G3	G2	G1	G0	X	X	
X	X	X	X	X	X	X	X	B5	B4	B3	B2	B1	B0	X	X	

8-bit 8080-Series Interface Data Format (Register/Pixel Data Read)

8-bit data bus for 16-bit/pixel, 65K-Colors, 3Ah=”05h”

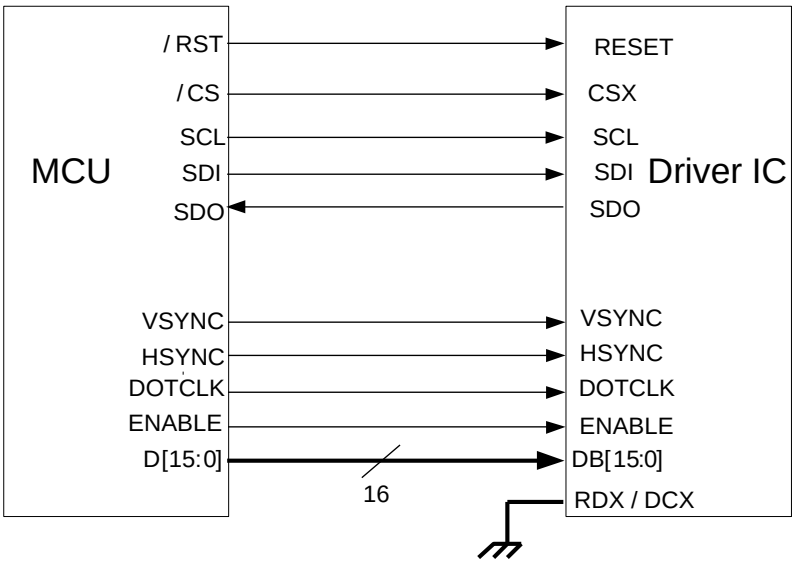
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	BUS width
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Dummy Read
X	X	X	X	X	X	X	X	R4	R3	R2	R1	R0	G5	G4	G3	2 Transfer 1 Pixel
X	X	X	X	X	X	X	X	G2	G1	G0	B4	B3	B2	B1	B0	

8.3.. RGB Interface

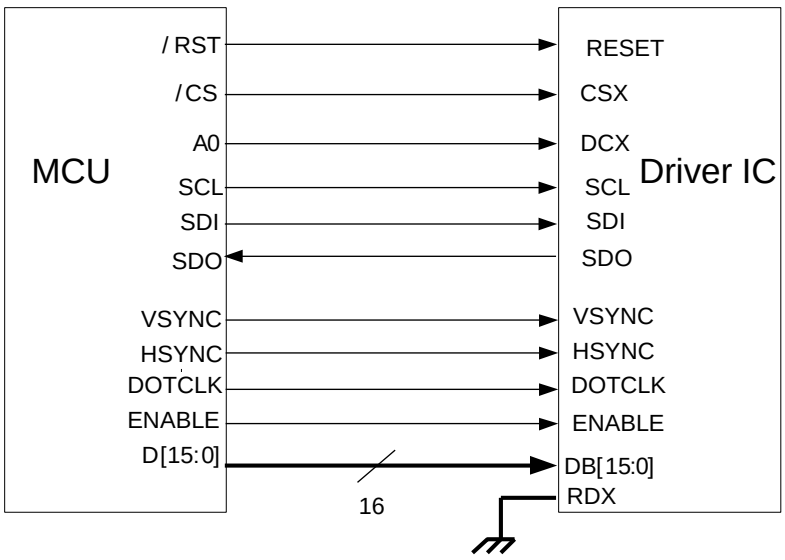
8.3.1 RGB Color Format

ST7796U supports two kinds of RGB interface, DE mode and HV mode, and 16bit/18bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[17:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[17:0] pins can be used. When using RGB interface, only serial interface can be selected. The connection is showed as below.

1. Set 16bit 65K pixel format. (3A = 55h)

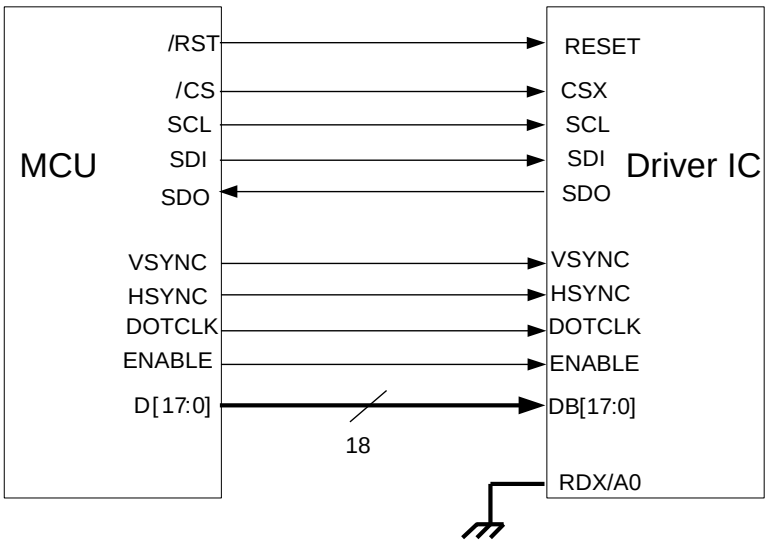


3SPI and RGB Interface Connection

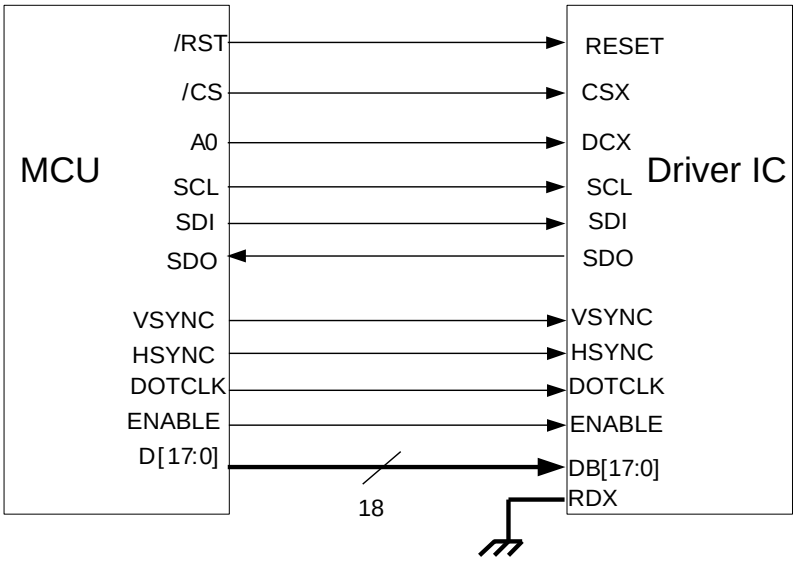


4SPI and RGB Interface Connection

2. Set 18bit 262K pixel format. (3A = 66h)

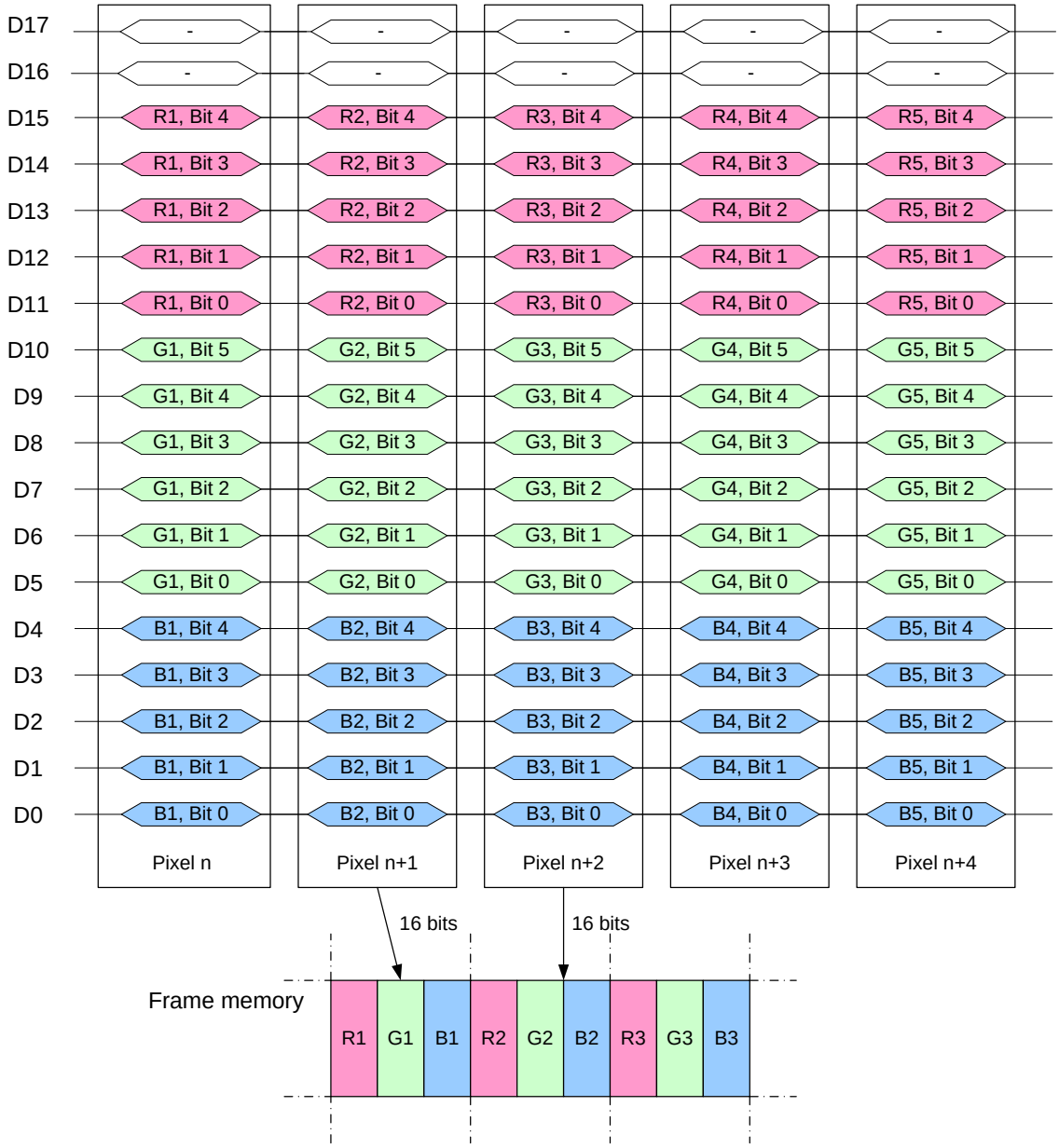


3SPI and RGB Interface Connection

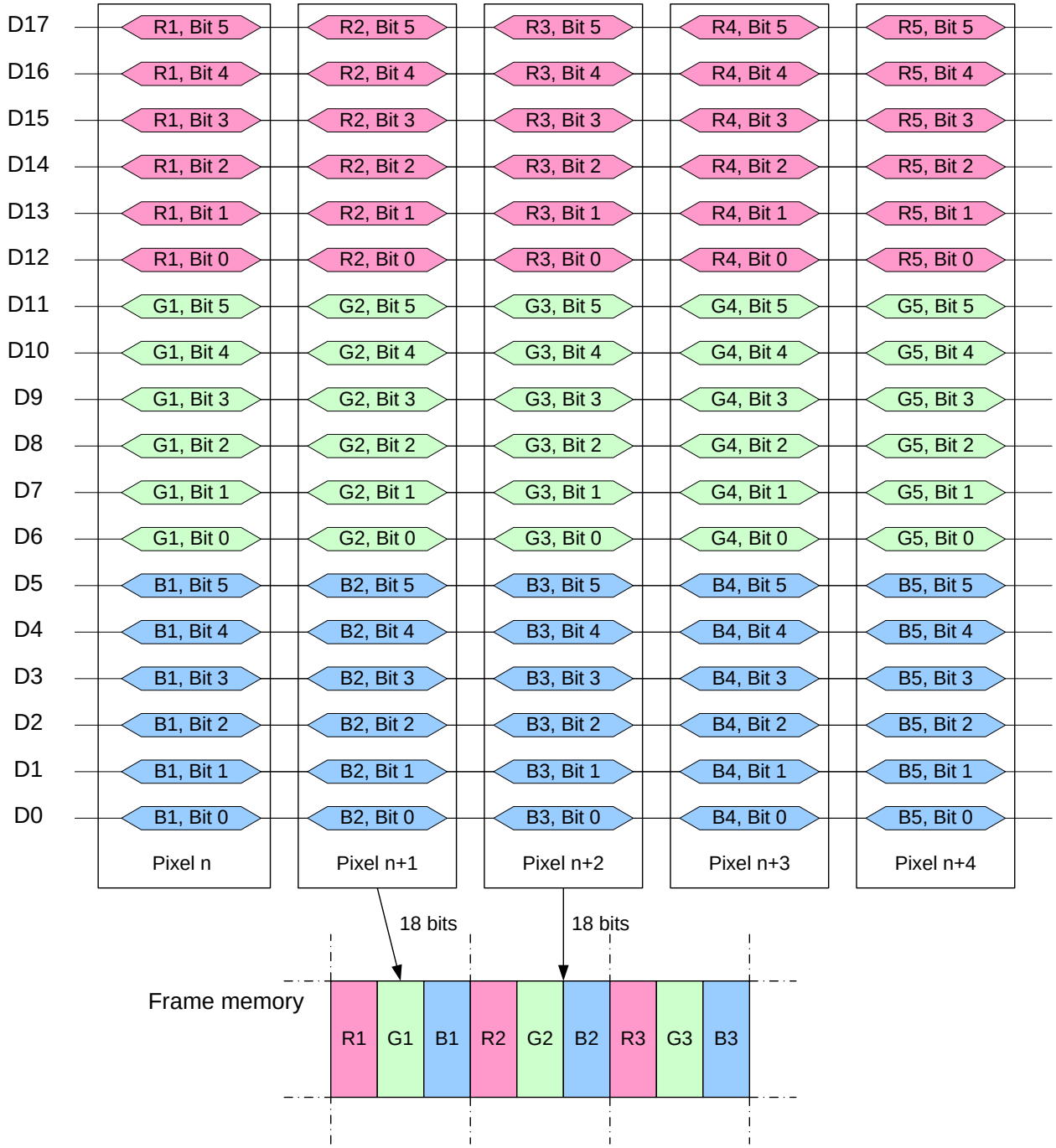


4SPI and RGB Interface Connection

Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors

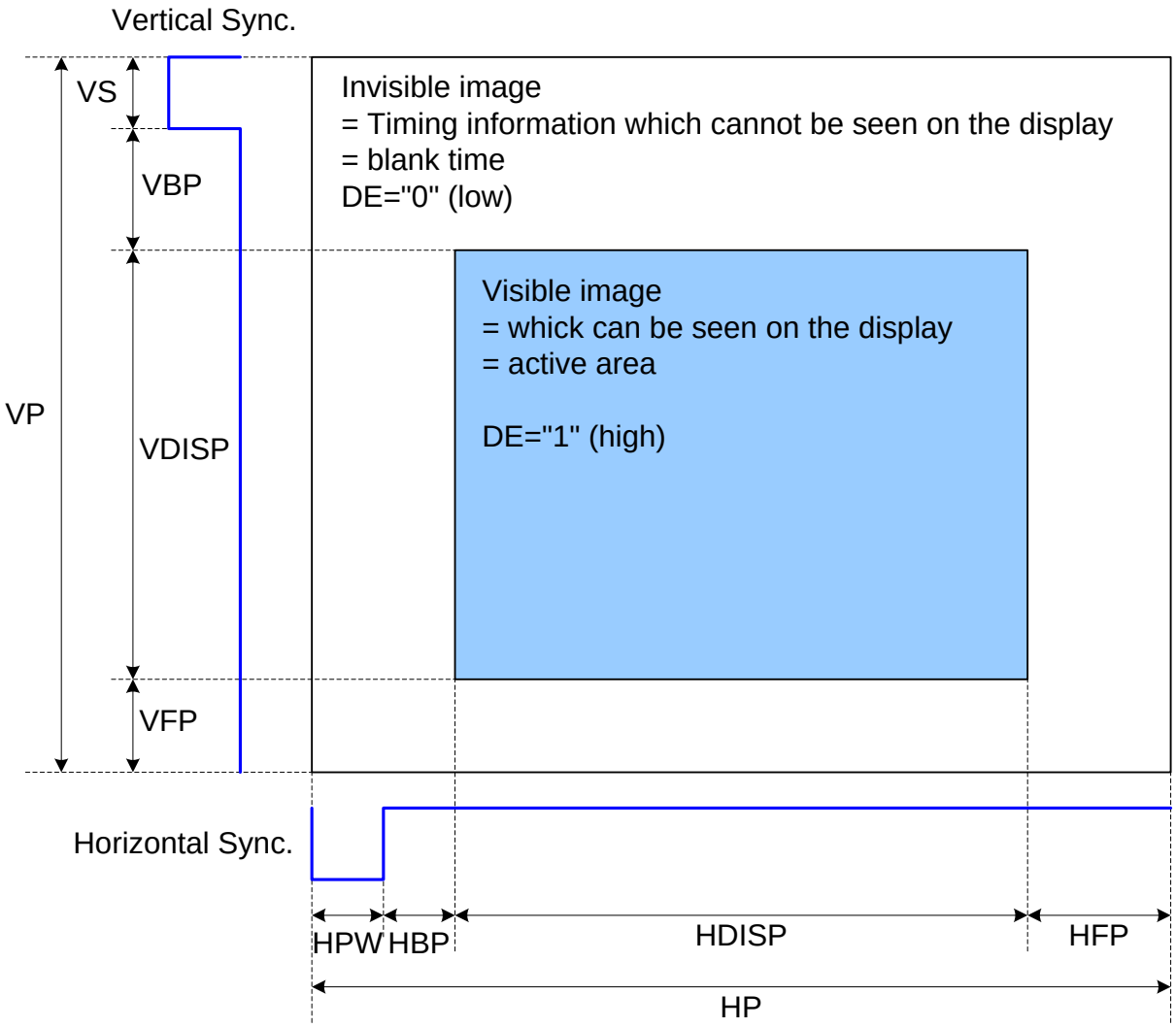


Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors



8.3.2 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.



DRAM Access Area by RGB Interface

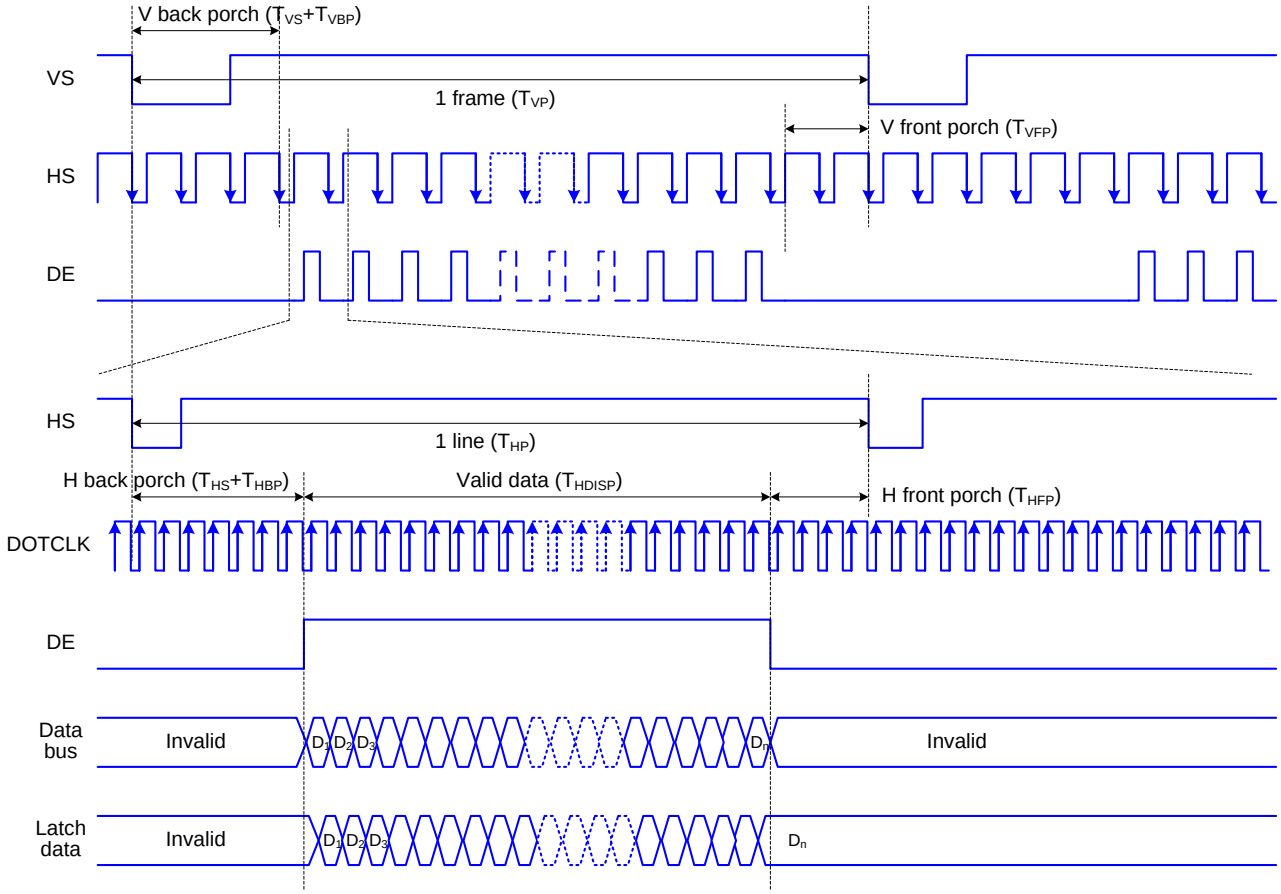
Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	40	50	256	Clock
Horizontal Sync. Back Porch	hbp	40	50		Clock
Horizontal Sync. Front Porch	hfp	10	38	-	Clock
Vertical Sync. Width	vs	2	4	-	Line
Vertical Sync. Back Porch	vbp	2	4		Line
Vertical Sync. Front Porch	vfp	2	8	-	Line

Note:

8.3.3 RGB Interface Timing

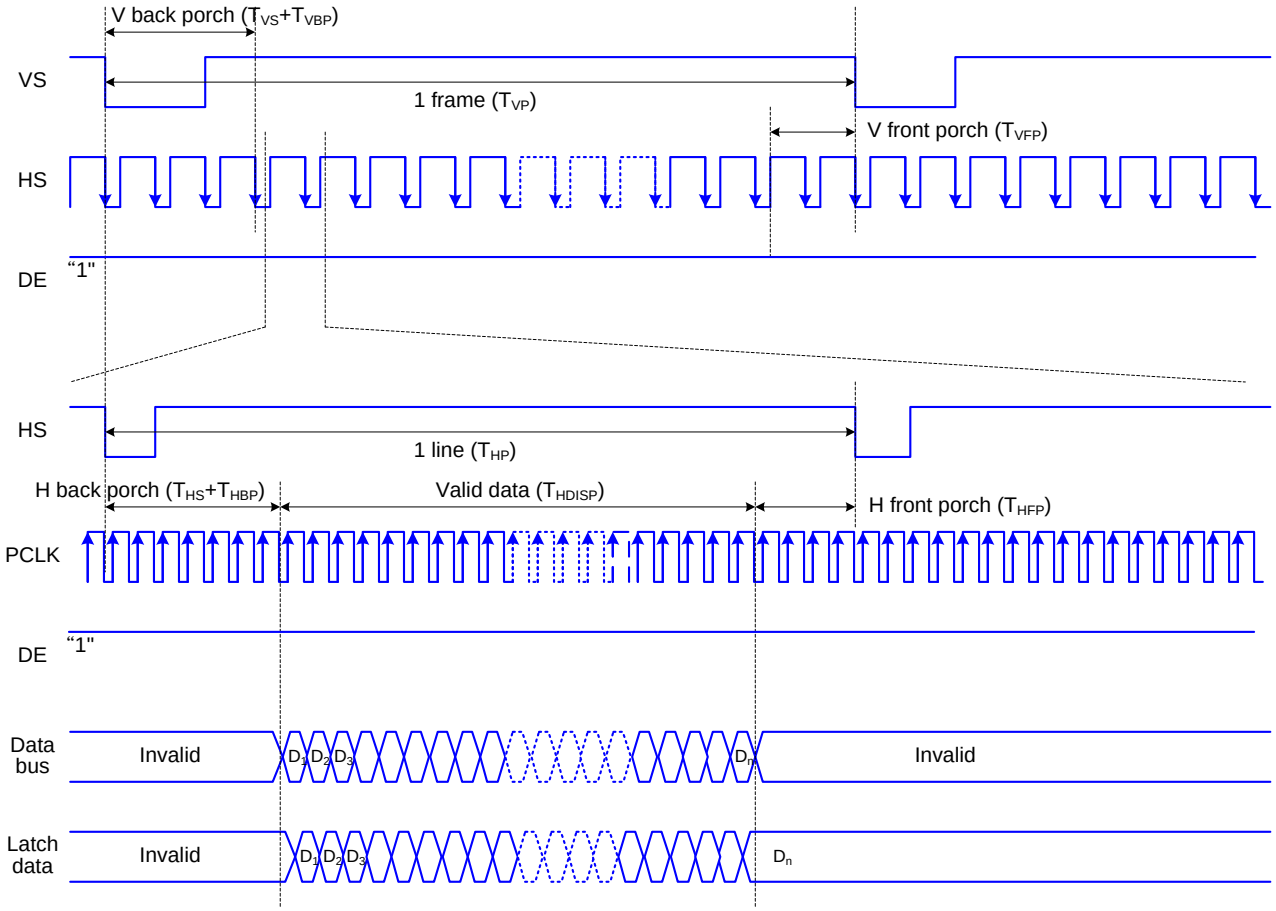
The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.



Timing chart of RGB interface HV mode

The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period. In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

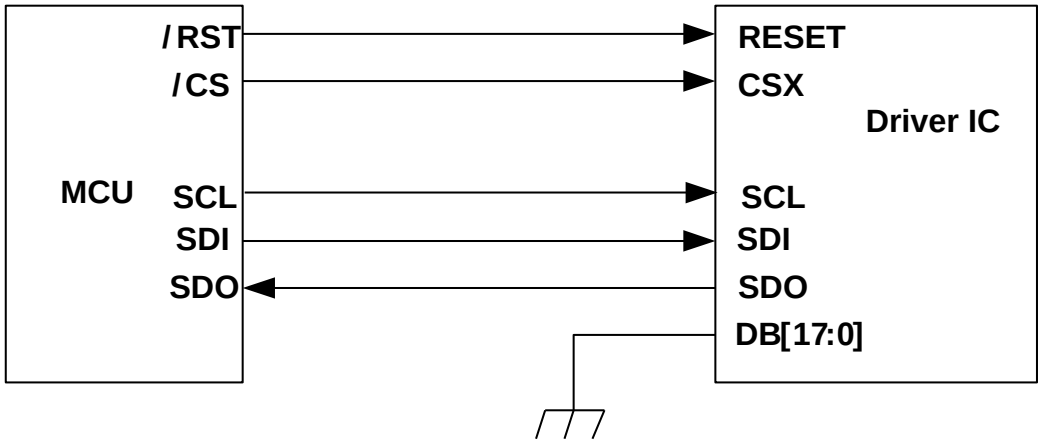
In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

In RGB interface mode, a RAM address is set in the address counter every frame on the falling edge of VSYNC.

8.4.. Serial Peripheral Interface (SPI)

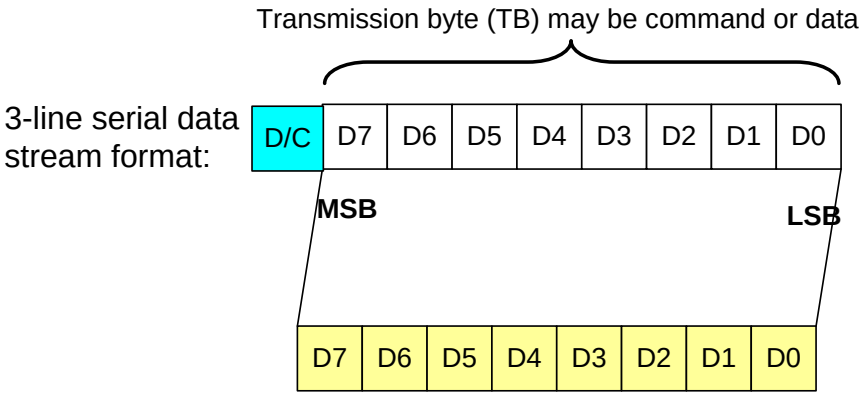
8.4.1 3-Line Interface

The Serial Peripheral Interface (SPI) is selected by setting the IM[2:0] pins as “101” level. The chip select pin (CSX), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to GND



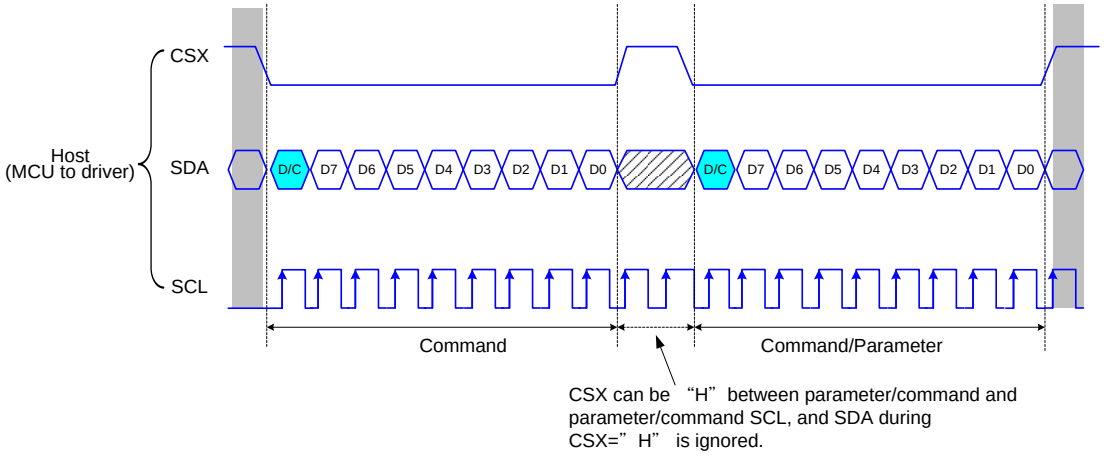
8.4.1.1 Write Sequence.

In the write mode of 3-line serial interface contains a D/CX (data/command) select bit and a transmission byte. If the D/C bit is “0”, the transmission byte is interpreted as a command byte. If the D/C bit is “1”, the transmission byte is display data, or stored in the command register as parameter data.



8 Bit Data Trasmission Byte

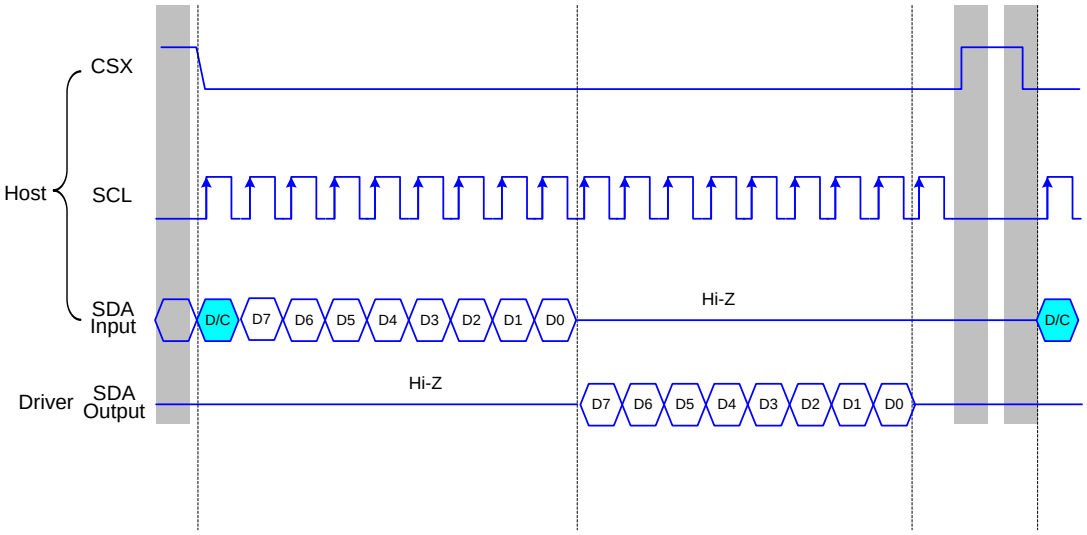
The instruction of ST7796U can be sent in any order, and the MSB is transmitted first. The 3-line serial interface is initialized when the CSX keeps high level. In this state, the SCL clock pulse and SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.



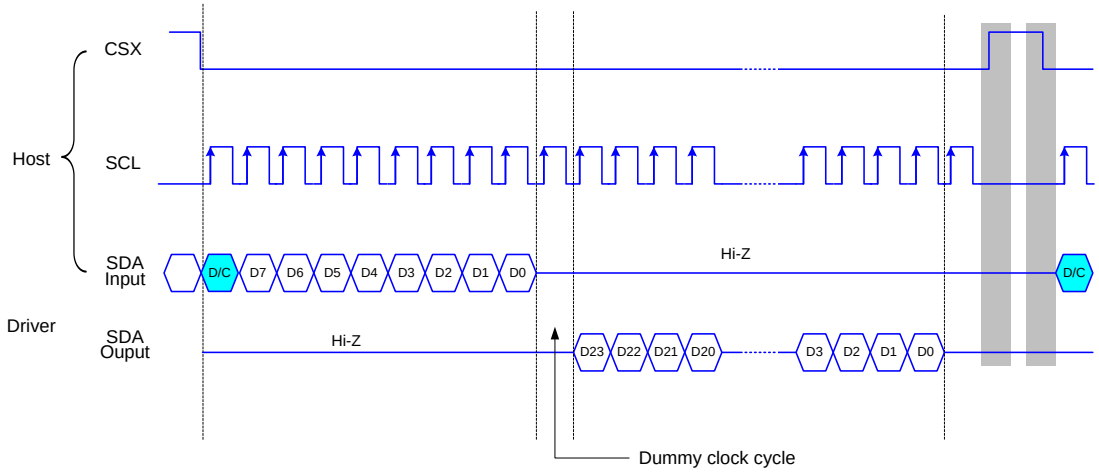
8.4.1.2 Read Sequence

In the read mode of the interface, the host reads the register value from the ST7796U. The host sends out a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The ST7796U samples the SDA (input data) at the rising edges of the SCL (serial clock), and shifts to SDO (output data) at the falling edges of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according to the command code.

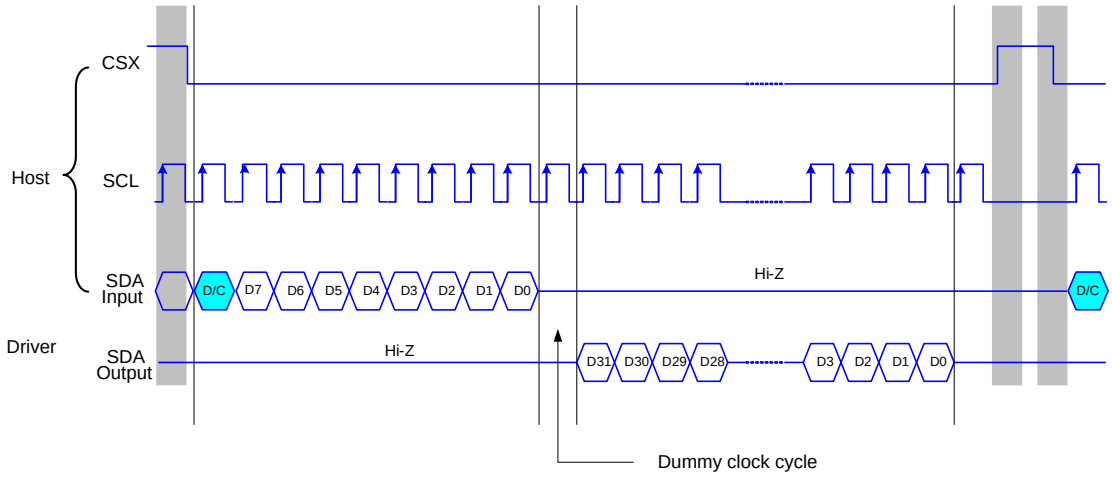
3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read)



3-line serial protocol (for RDDST command: 32-bit read)



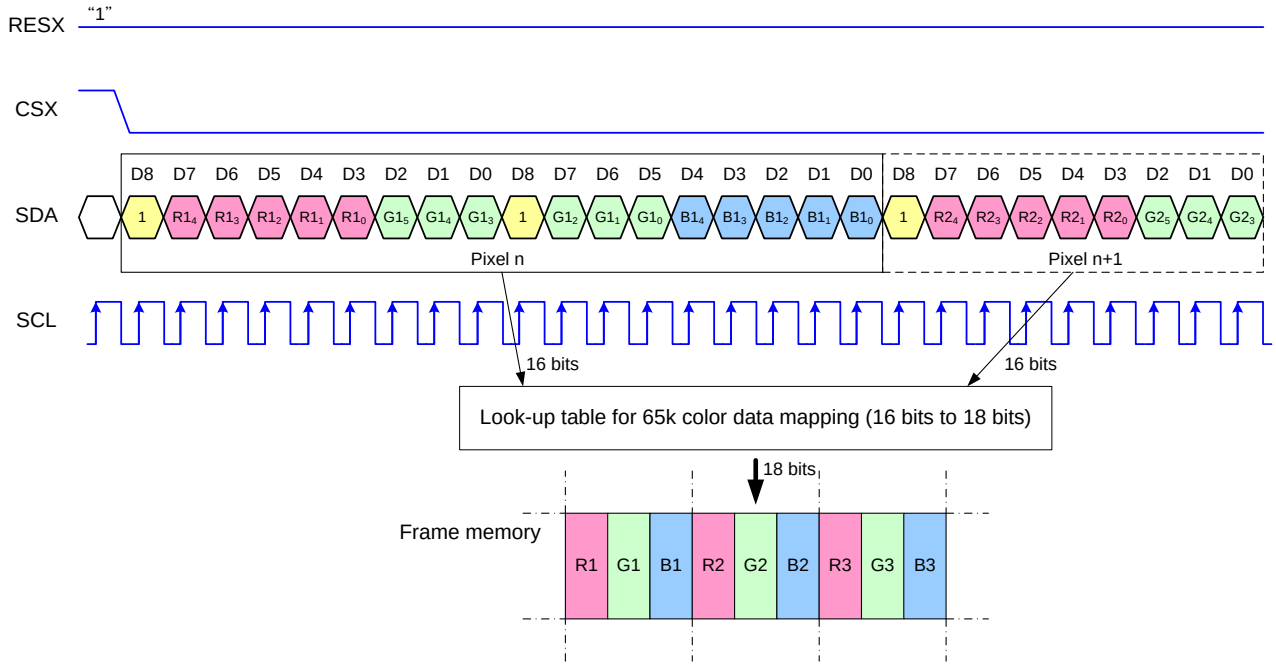
8.4.1.3 3-SPI Color format

Different display data formats are available for three colors depth supported by the LCM listed below.

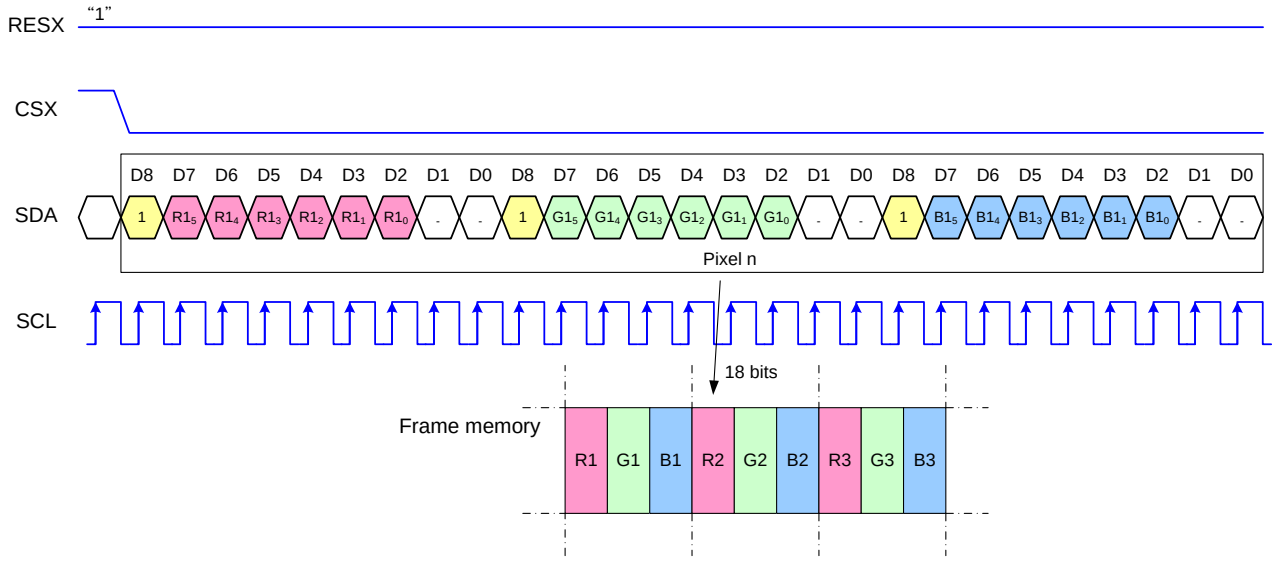
65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="05h"



Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h"

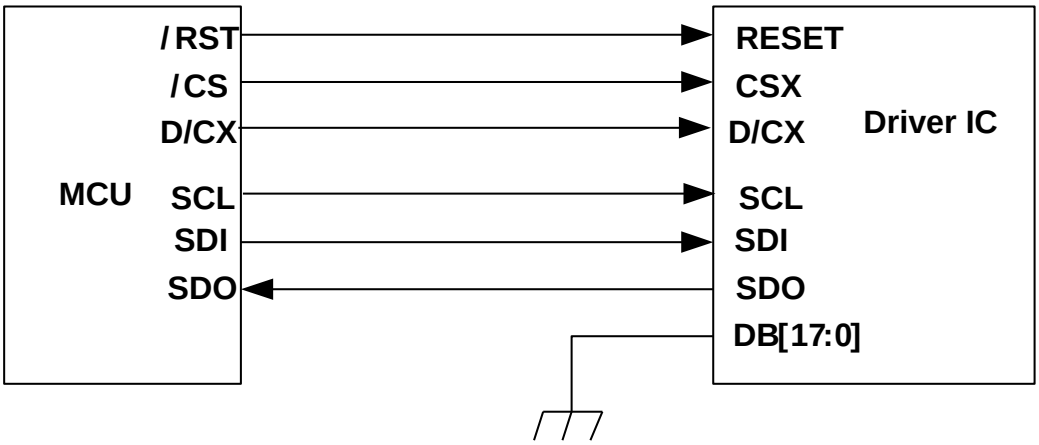


The SPI interface operation enables from the falling edge of CSX and ends of data transfer on the rising

edge of CSX. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ST7796U.

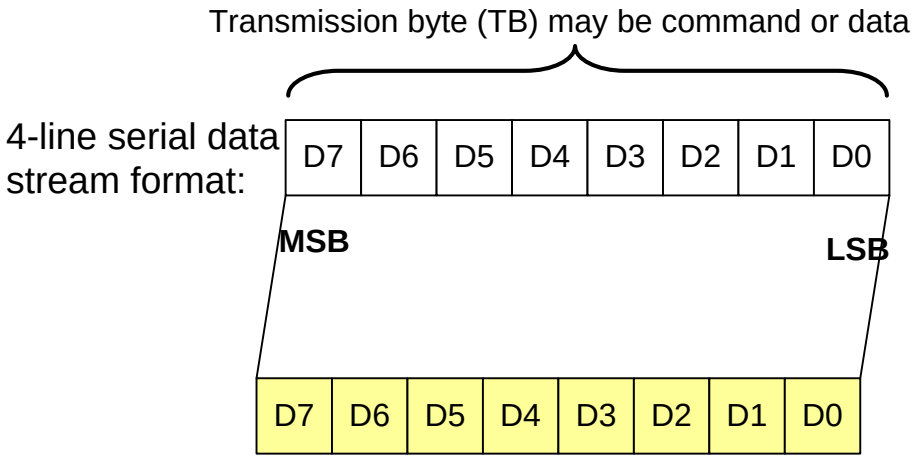
8.4.2 4-Line Interface

The Serial Peripheral Interface (SPI) is selected by setting the IM[2:0] pins as “111” level. The chip select pin (CSX), the serial transfer clock pin (SCL), the display data/command selection (DCX), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to GND



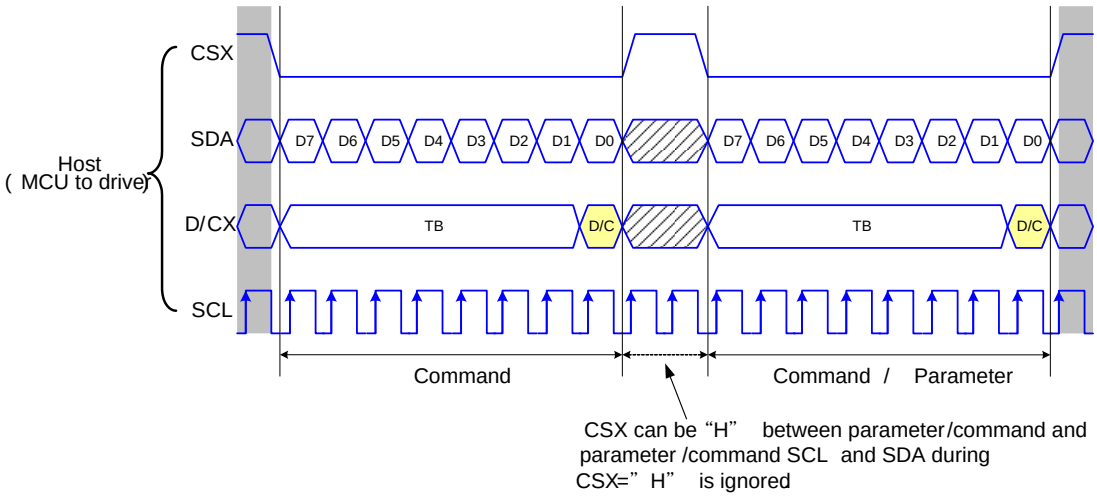
8.4.2.1 Write Sequence

The write mode of the interface means the host writes commands and data to ST7796U. The 4-lines serial data packet contains a data/command and a transmission byte. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.



8 Bit Data Trasmission Byte

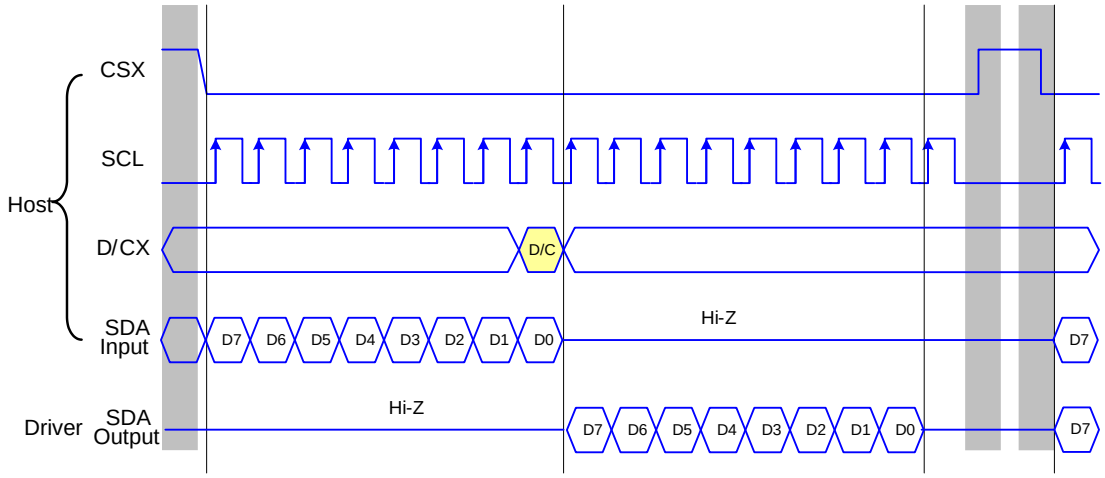
The host drives the CSX pin to low and the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle long. The 4-line serial interface writes sequence described in the Figure as below.



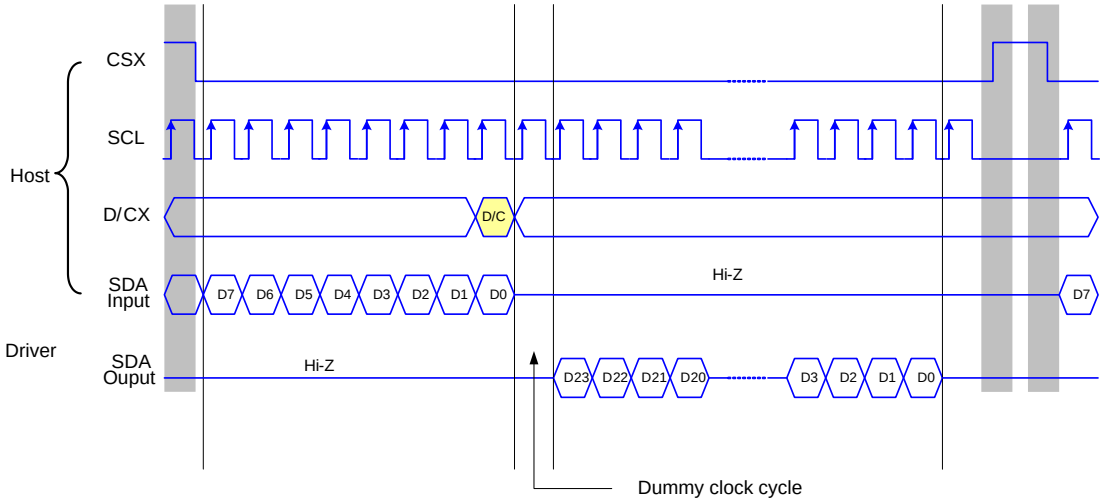
8.4.2.2 Read Sequence

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

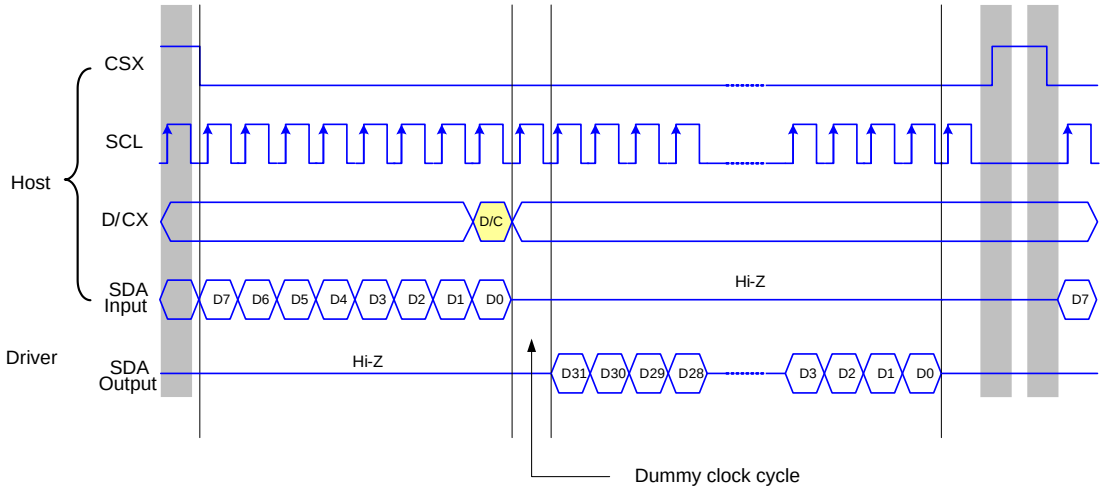
4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



4-line serial protocol (for RDDID command: 24-bit read)



4-line serial protocol (for RDDST command: 32-bit read)



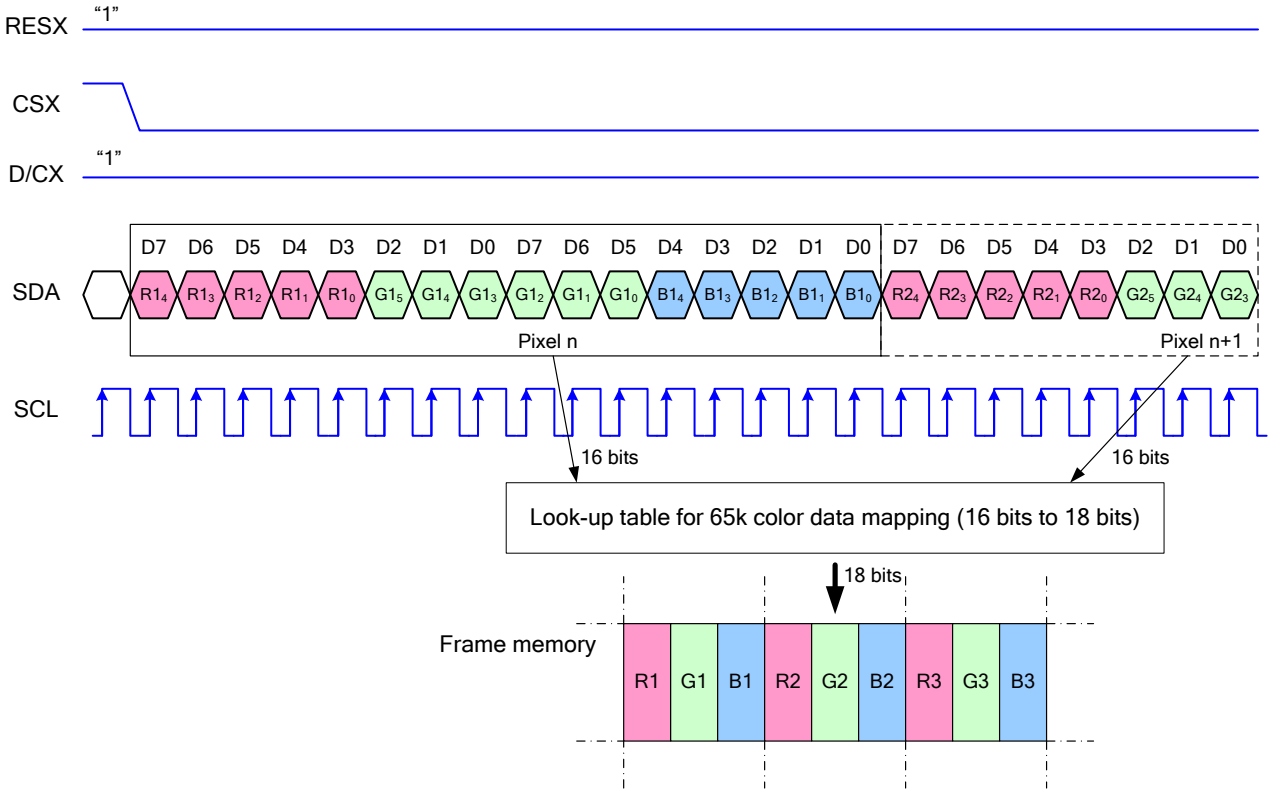
8.4.2.3 4-SPI Color format

Different display data formats are available for three colors depth supported by the LCM listed below.

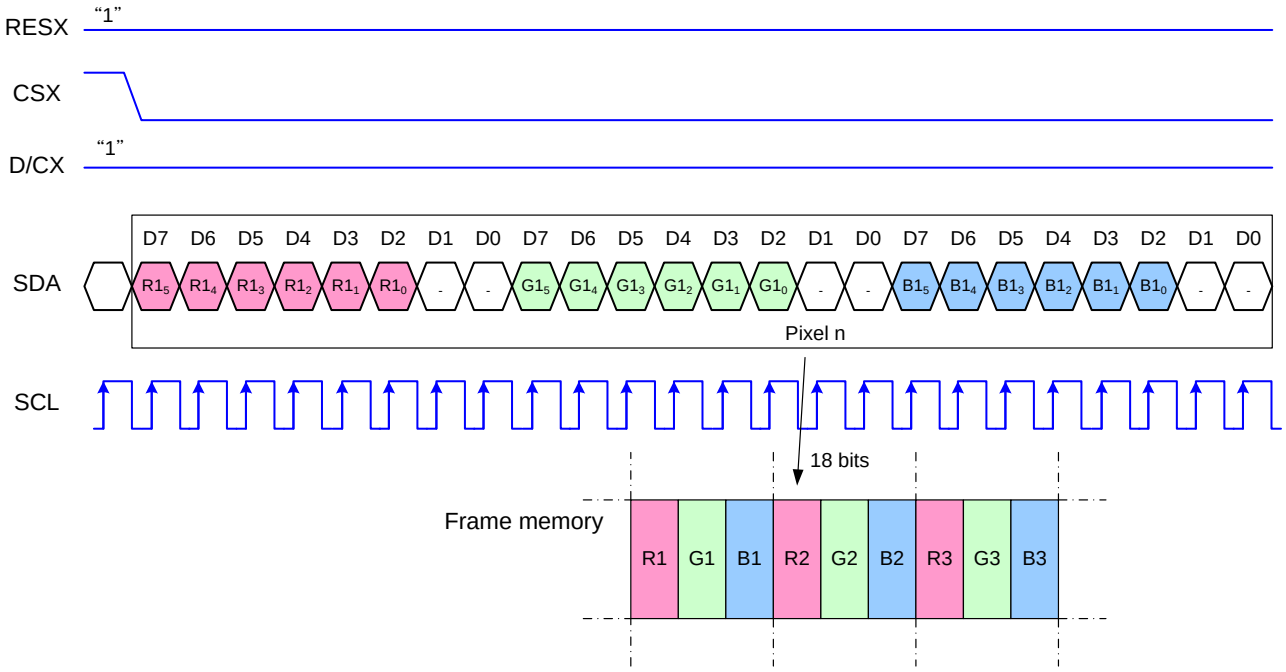
65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

Write data for 16-bit/pixel (RGB-5-6-5-bit input), 65K-Colors, 3Ah="05h"



Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h"



8.5.. Mobile Industry Processor Interface (MIPI)

8.5.1 Display Serial Interface (DSI)

8.5.1.1 GENERAL DESCRIPTION

The communication can be separated 2 different levels between the MCU and the display module:

1. Low level communication what is done on the interface level
2. High level communication what is done on the packet level

8.5.1.2 Interface Level Communication

The display module uses data and clock lane differential pairs for DSI (DSI-1M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocols in each mode when there wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	CLOCK_P	CLOCK_N
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark – 0
LP-10	High (LP)	Low (LP)	Not Defined	LP – Request	Mark – 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes:

(1) Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

(2 If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

8.5.1.3 DSI-CLOCK Lanes

DSI-CLOCK_P/N lanes can be driven into three different power modes:

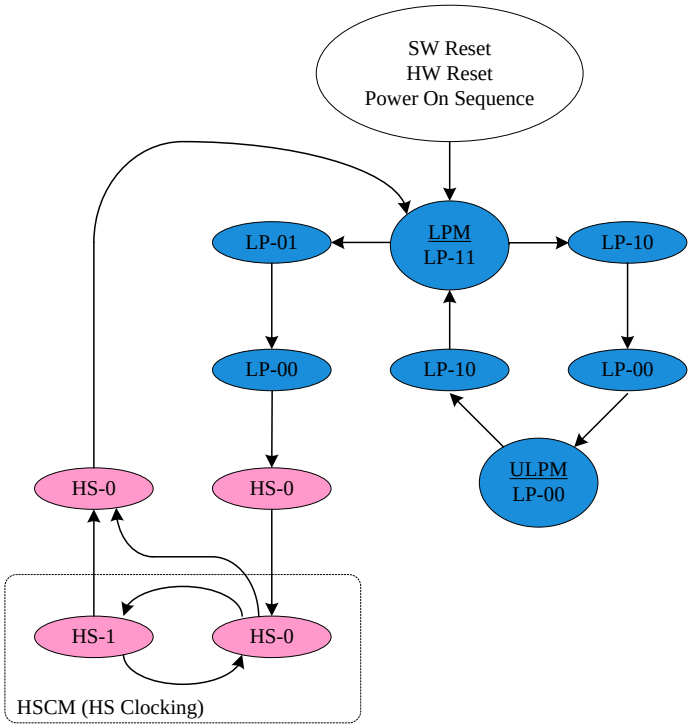
- Low Power Mode (LPM)
- Ultra Low Power Mode (ULPM)

- High Speed Clock Mode (HSCM)

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM). These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

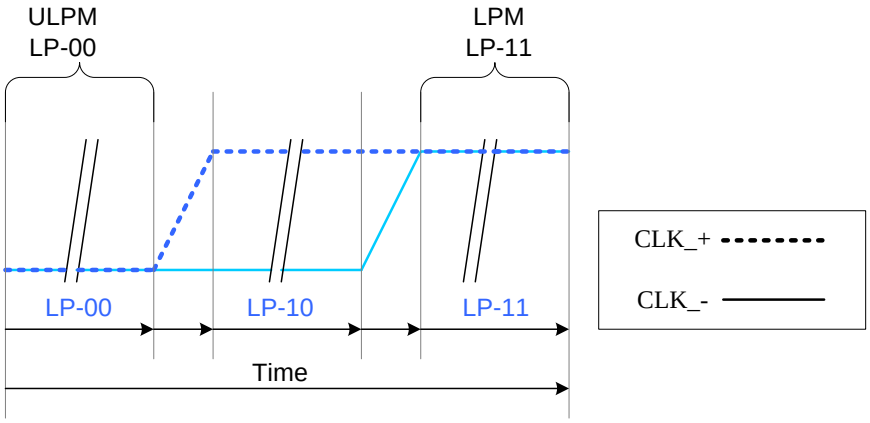


Flow chart of the different clock lanes

1. Low Power Mode (LPM)

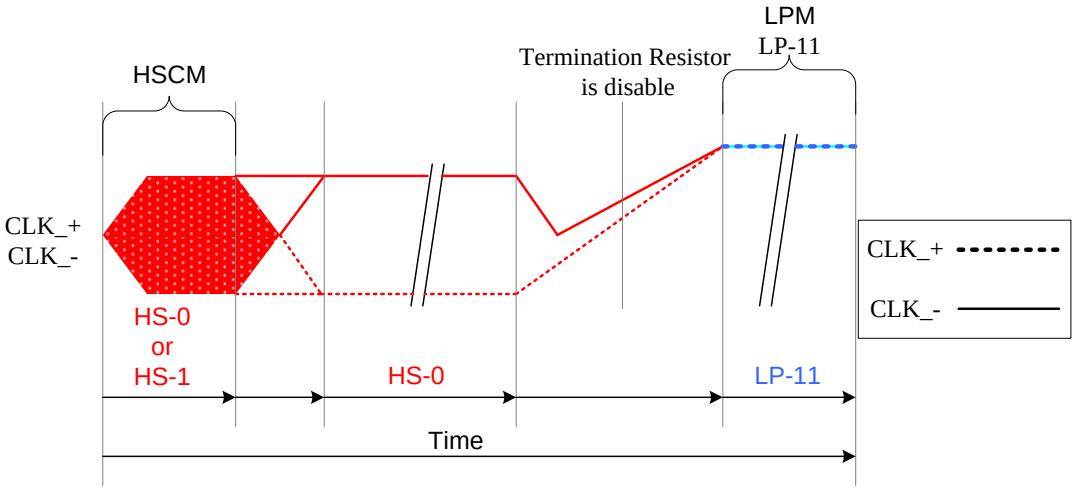
DSI-CLOCK_P/N lanes can be driven to the Low Power Mode (LPM), when DSI-CLOCK lanes are entering LP-11 State Code, in three different ways:

- After SW Reset, HW Reset or Power On Sequence =>LP-11 After DSI-CLOCK_P/N lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10
- LP-11 (LPM). This sequence is illustrated below.



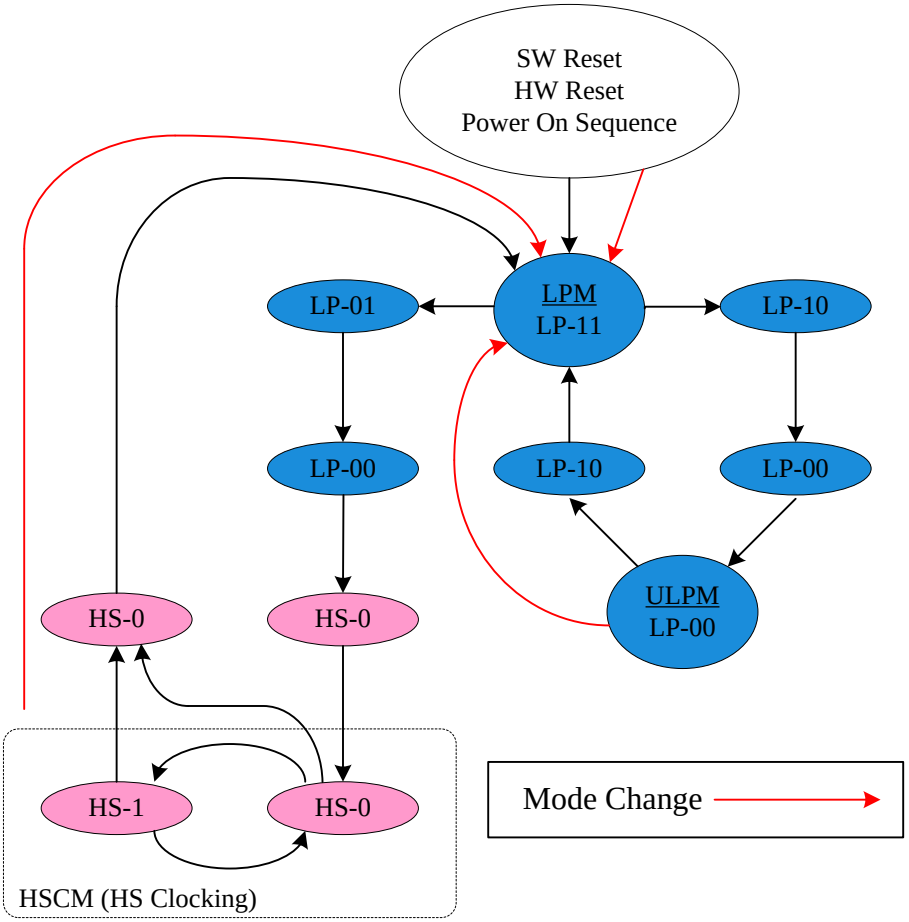
From ULPM to LPM

◆ After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0=>LP-11 (LPM). This sequence is illustrated below.



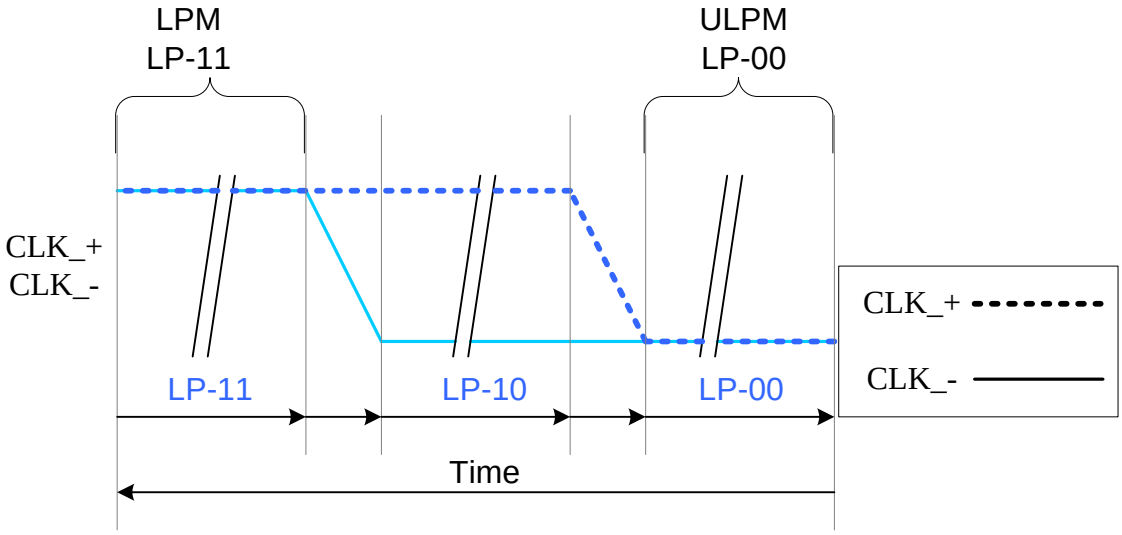
From High Speed Clock Mode (HSCM) to LPM

All three mode changes are illustrated a flow chart below.



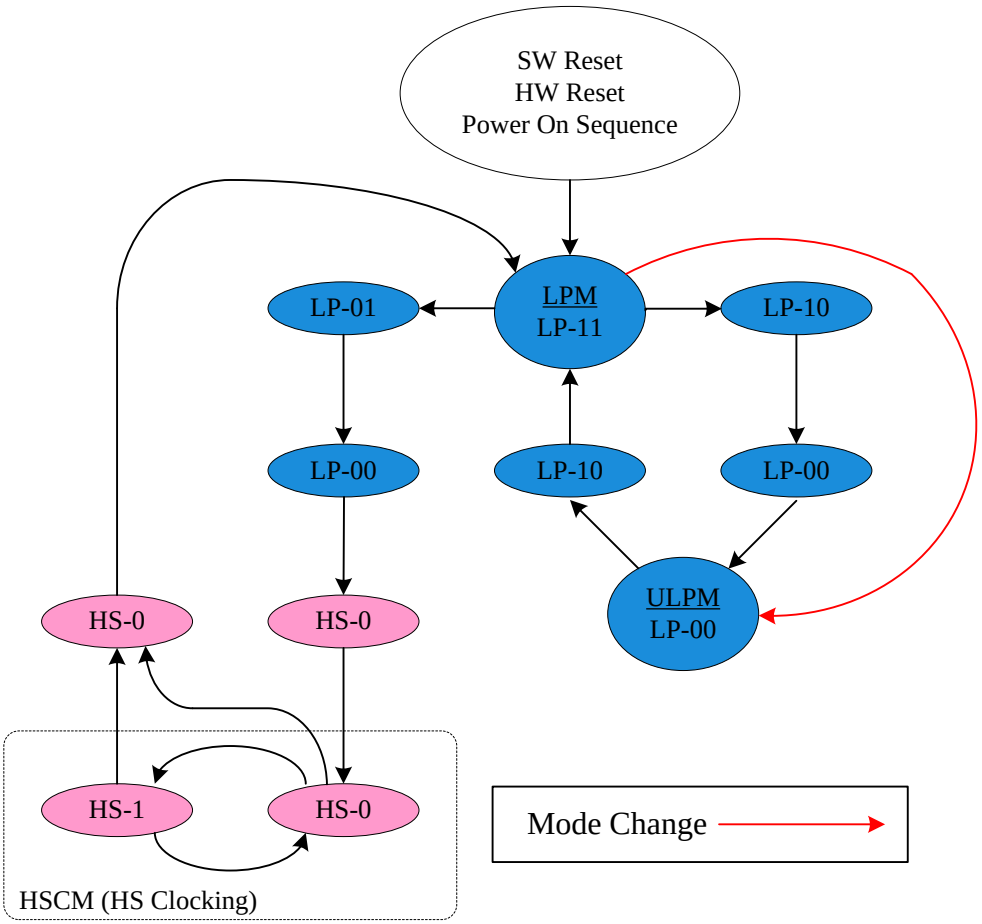
All Three Mode Changes to LPM on the Flow Chart

2. Ultra Low Power Mode (ULPM)



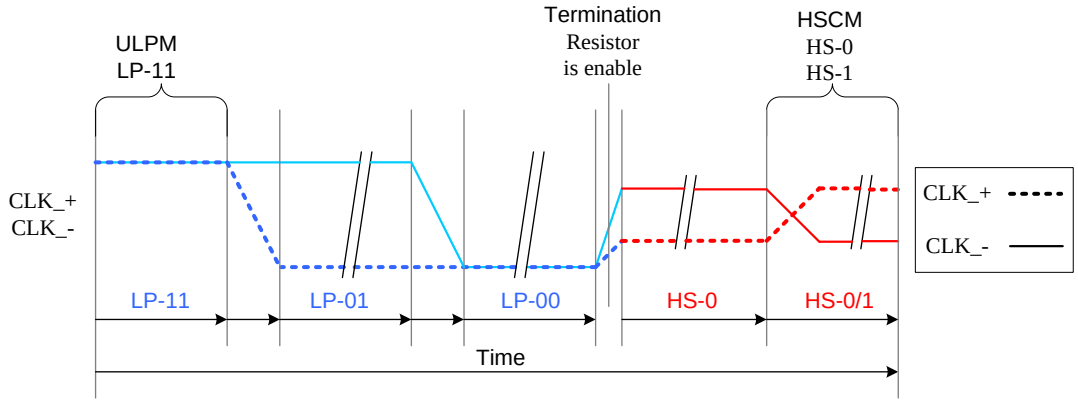
From LPM to ULPM

The mode change is also illustrated below.



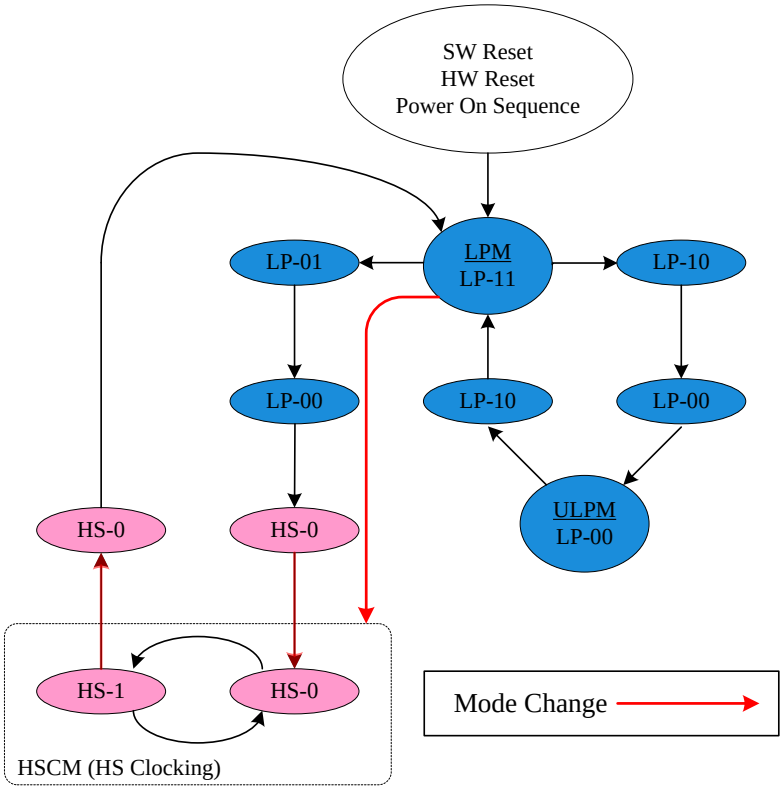
Mode Change from LPM to ULPM on the Flow Chart

3. High Speed Clock Mode (HSCM)



From LPM to HSCM

The mode change is also illustrated below.

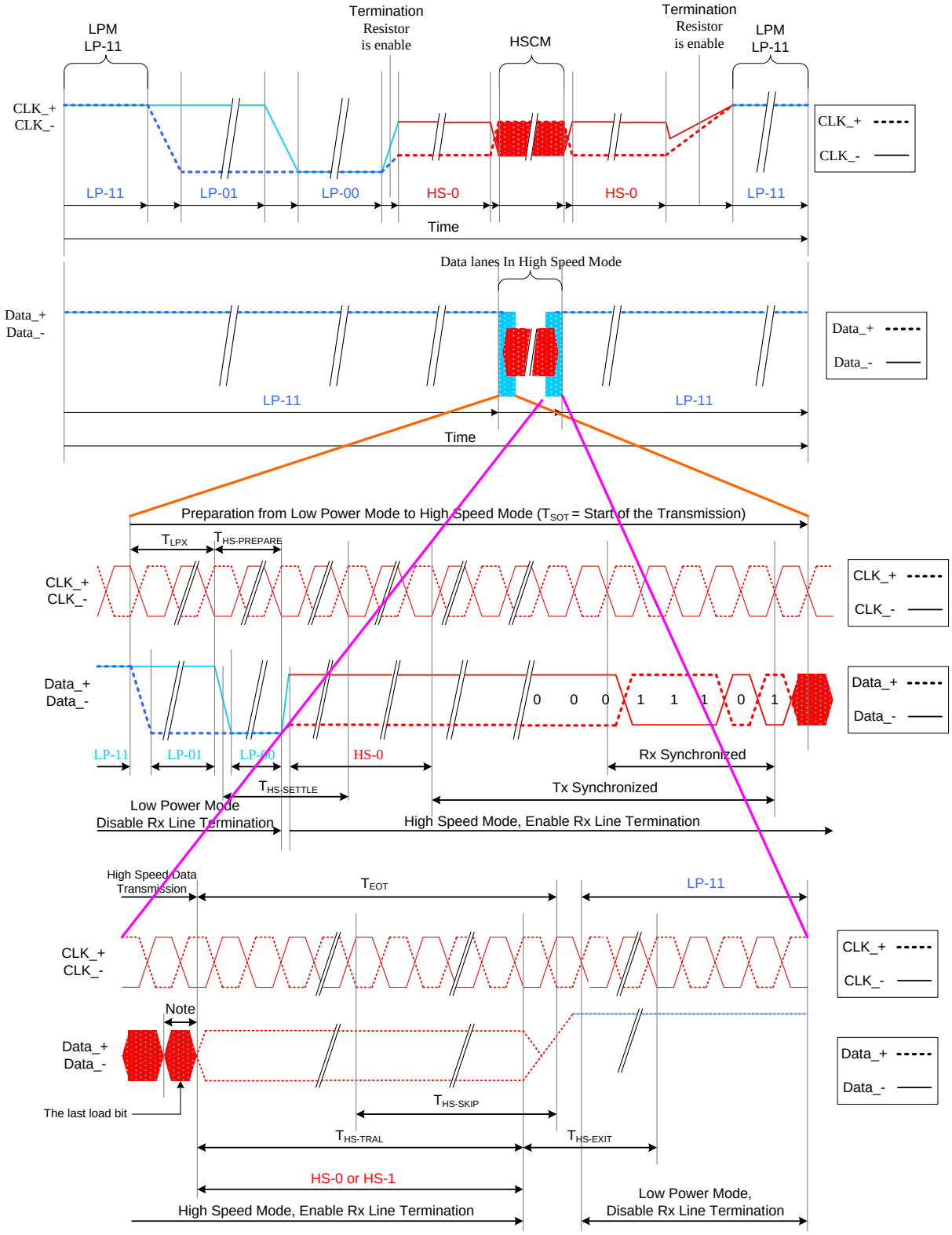


Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLOCK_P/N) is started before high speed data is sent via DSI-DATA_P/N lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0



High Speed Clock Burst

Note:

If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0

8.5.1.4 DSI-DATA Lanes

DSI-DATA_P/N Data Lanes can be driven in different modes which are:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP-11(Mark-1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z, Note

1. **Escape Mode**

Data lanes (DSI-DATA_P/N) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

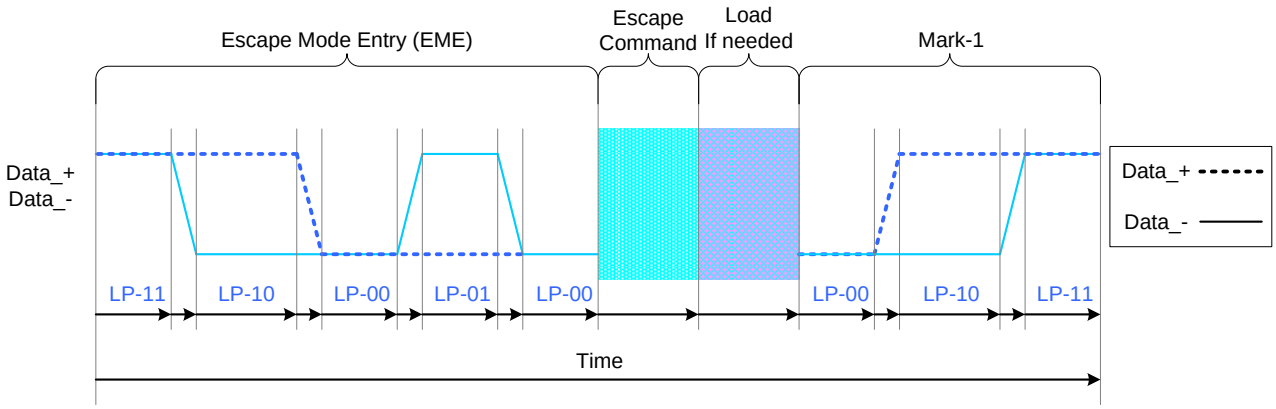
These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is reset the display module
- Indicate “Tearing Effect”, which is used for a TE line event from the display module to the MCU
- Indicate (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:



General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different Escape Commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (RX_D0P/N) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module an event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Escape commands are defined on the next table.

Escape command	Command Type Mode / Trigger	Entry command Pattern (First Last Bit Transmitted)
Low-Power Data	Mode	1110 0001 b
Ultra-Low Power Mode	Mode	0001 1110 b
Undefined-1, Note	Mode	1001 1111 b
Undefined-2, Note	Mode	1101 1110 b
Remote Application Reset	Trigger	0110 0010 b
Tearing Effect	Trigger	0101 1101 b
Acknowledge	Trigger	0010 0001 b
Uknown-5, Note	Trigger	1010 0000 b

Note: This Escape command support has not been implemented on the display module.

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

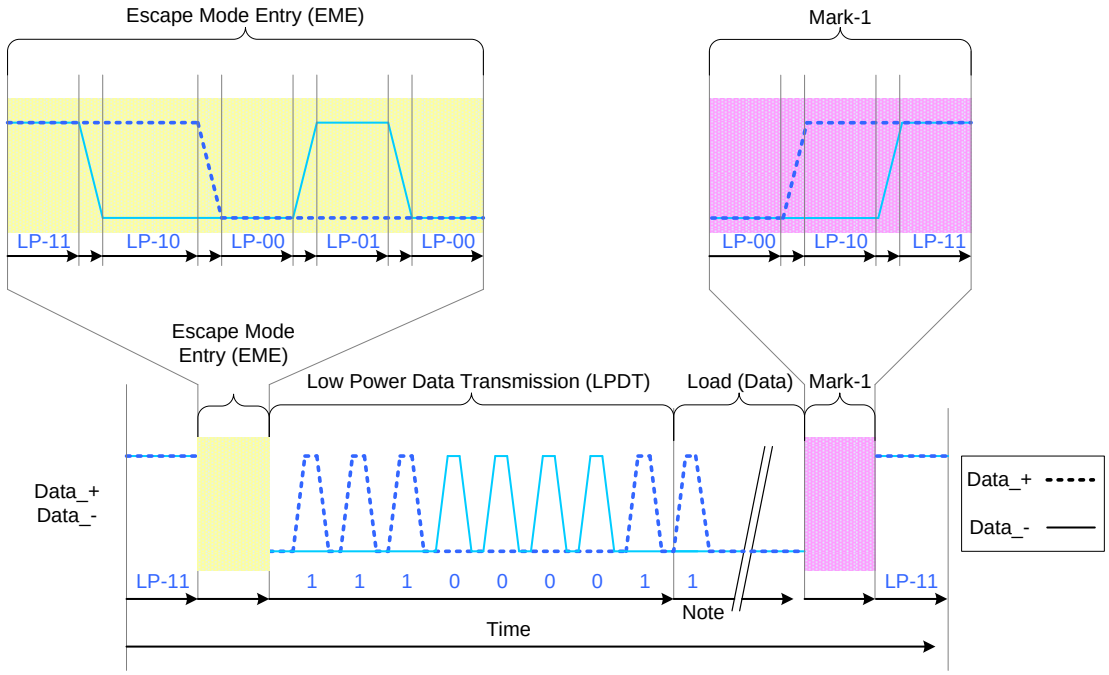
The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):

  One or more bytes (8 bit)

  Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

The Low-Power Data Transmission (LPDT) is as below,



Note : Load (Data) is presenting that the first bit is logical "1" in this Exsample

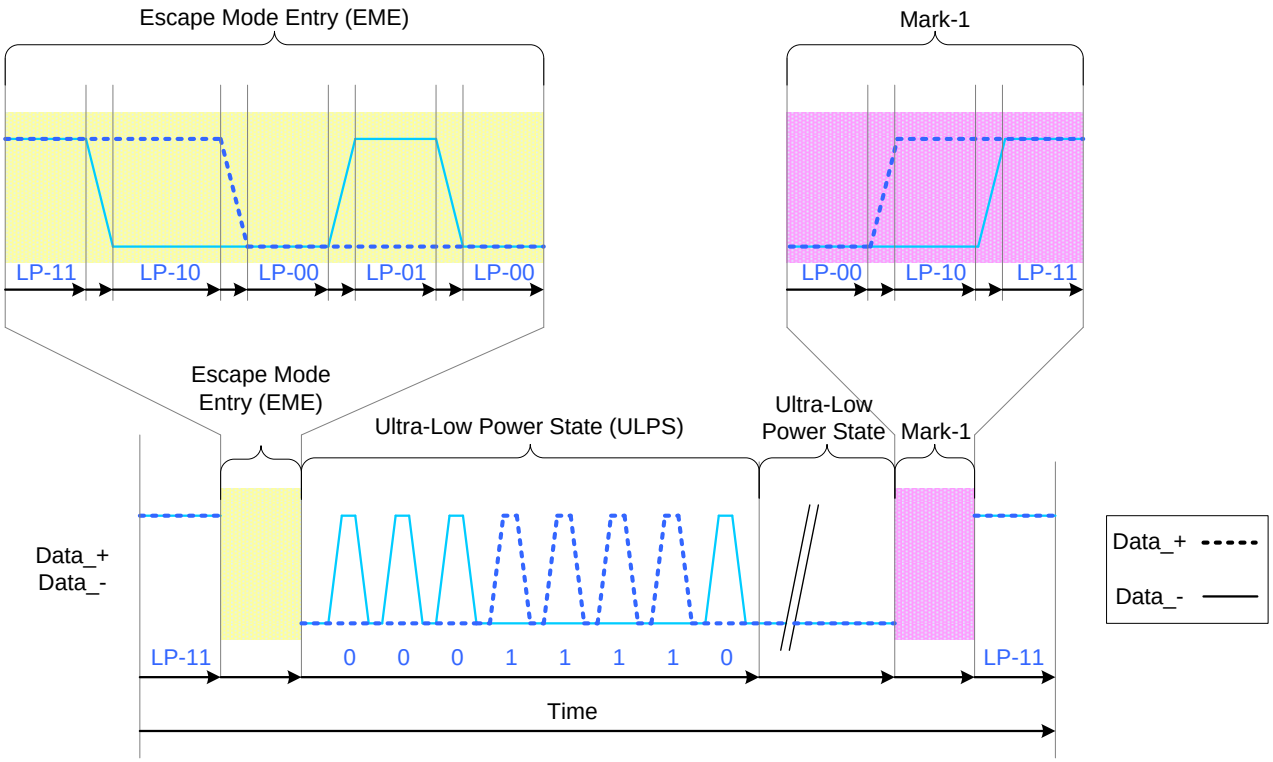
Low-Power Data Transmission (LPDT)

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode. The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Ultra-Low Power State (ULPS)

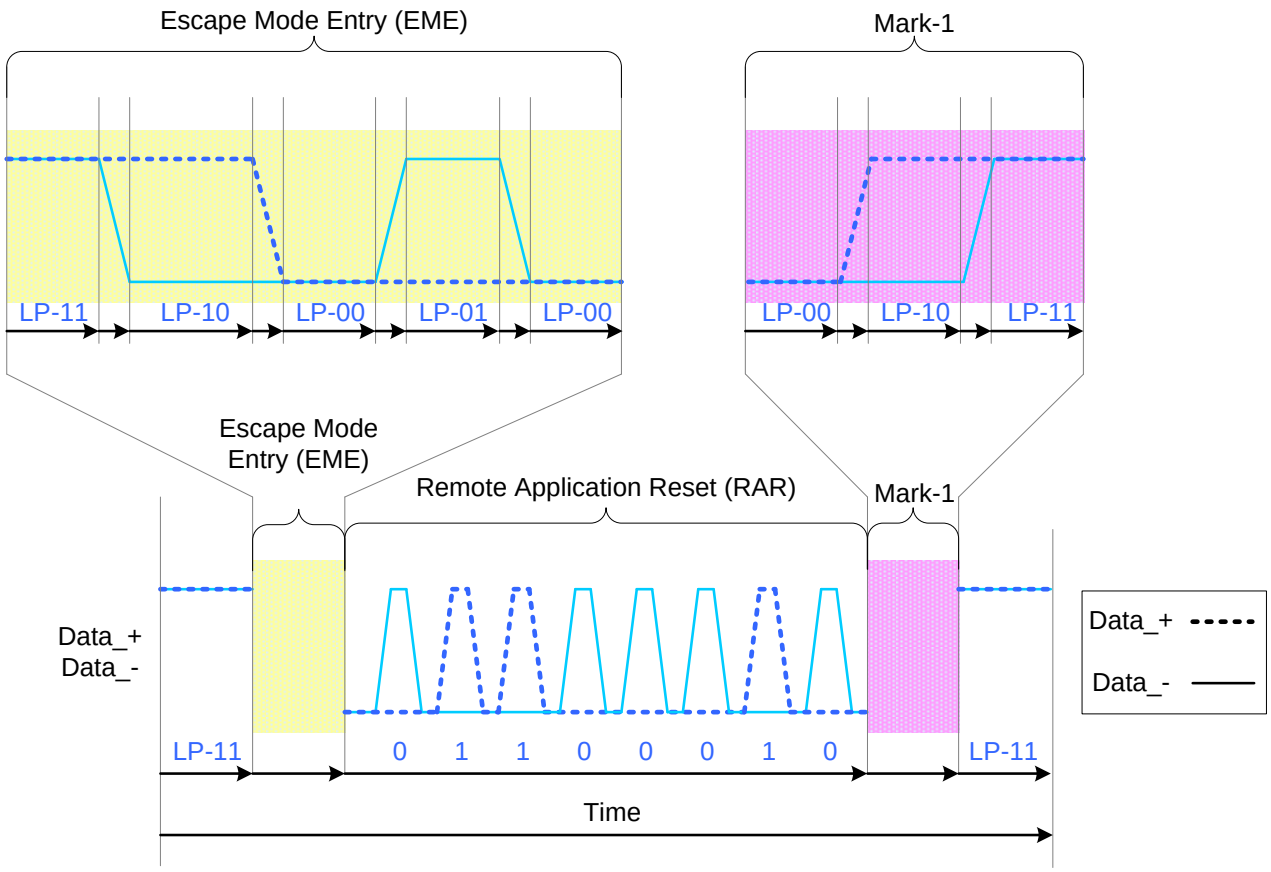
Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Remote Application Reset (RAR)

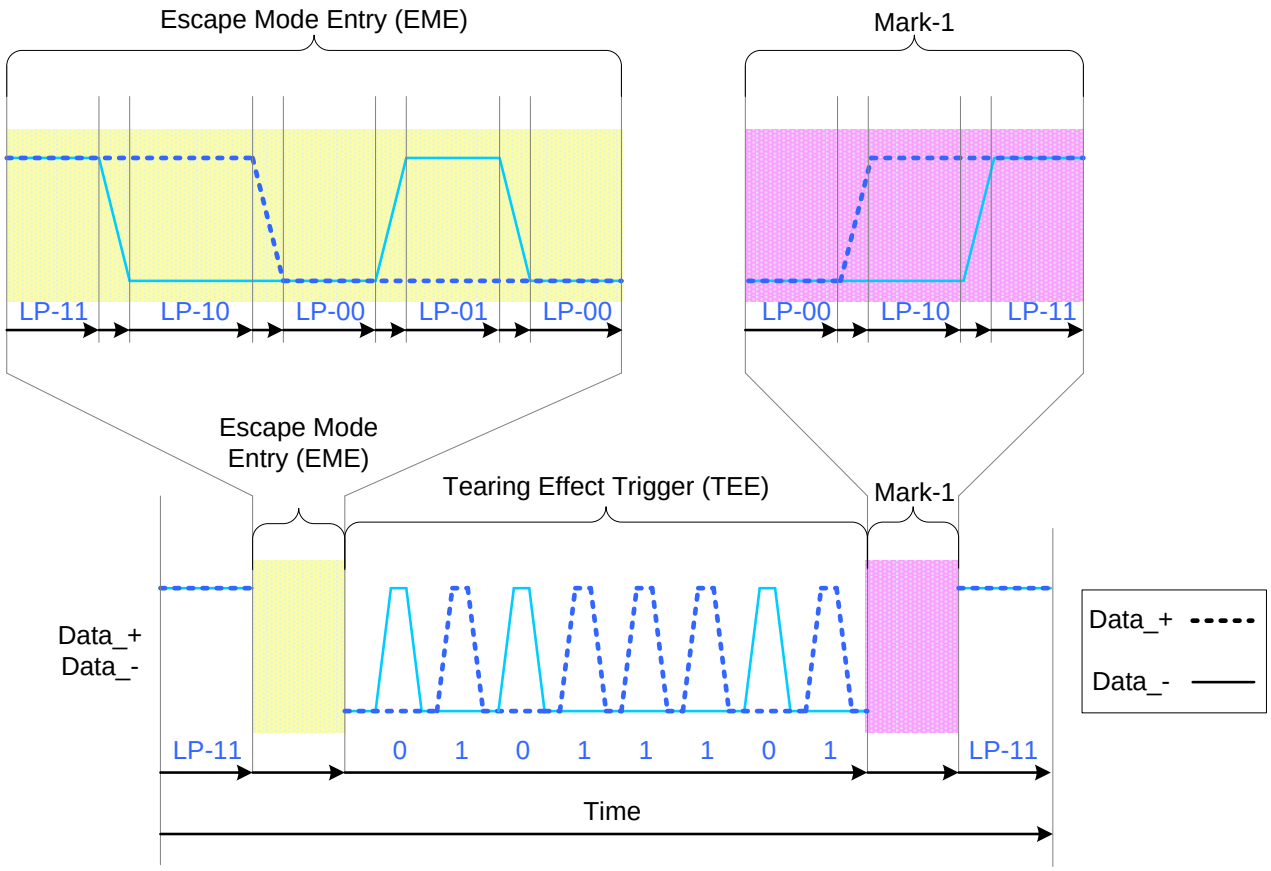
Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been appened on the display module by Tearing Effect (TEE).

The display module is sending the Tearing Effect (TEE) what is a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Tearing Effect (TEE)

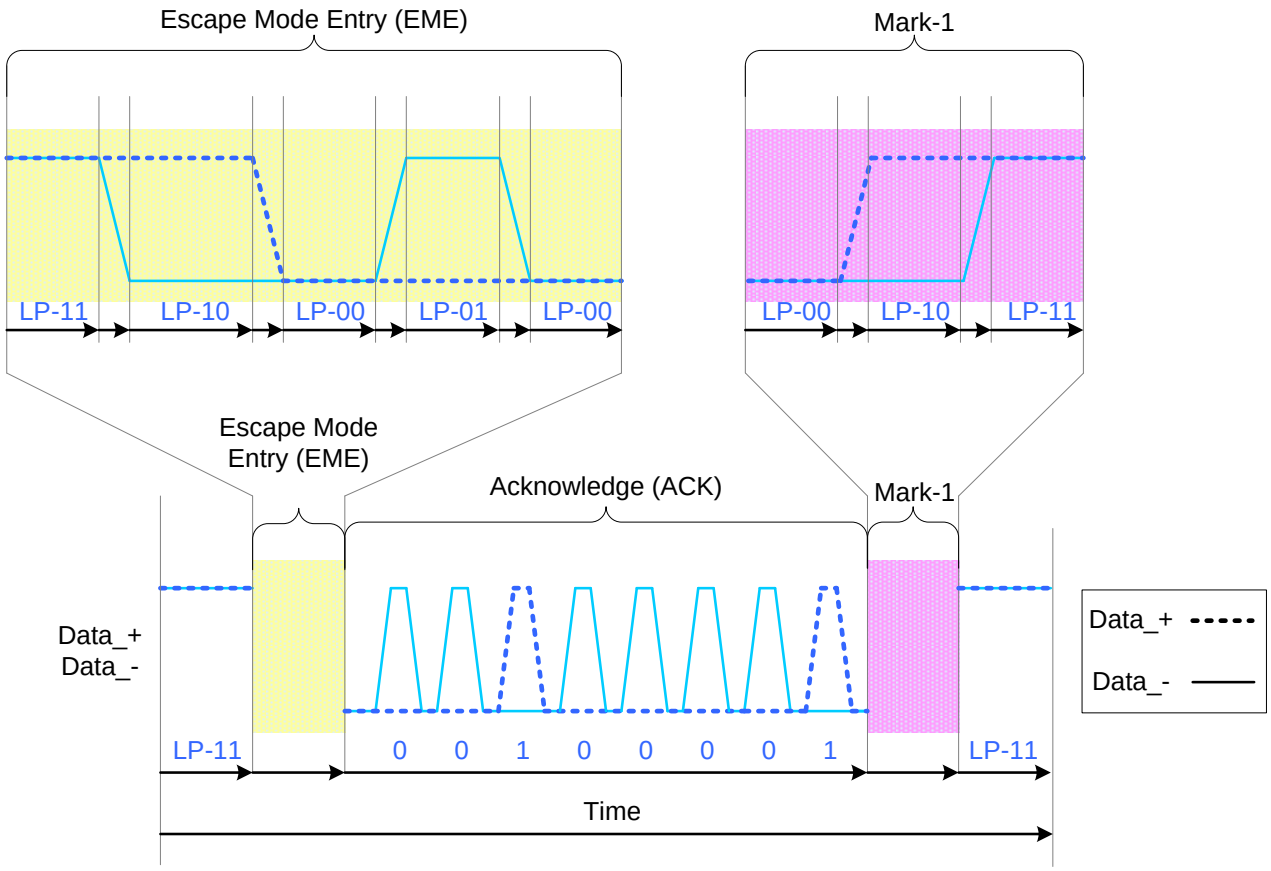
Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The display module is sending the Acknowledge (ACK) what is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Acknowledge (ACK)

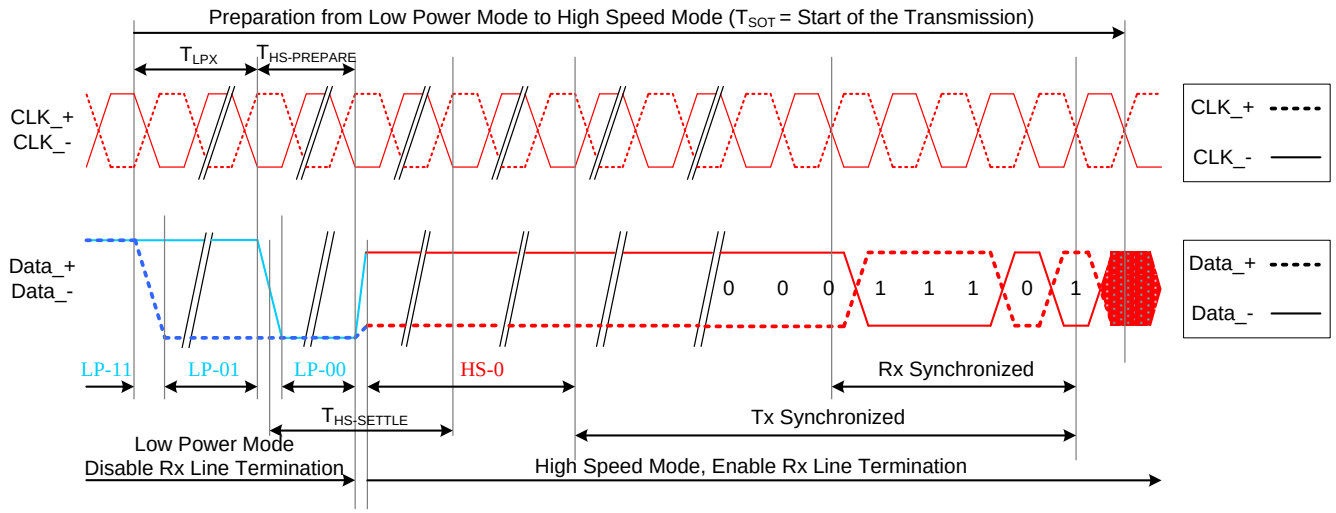
2. **High-Speed Data Transmission**

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes RX_CP/N have already been entered in the High-Speed Clock Mode (HSCM) by the MCU.

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below



Entering High-Speed Data Transmission (T_{SOT} of HSDT)

Leaving High-Speed Data Transmission

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes RX_CP/N are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode.

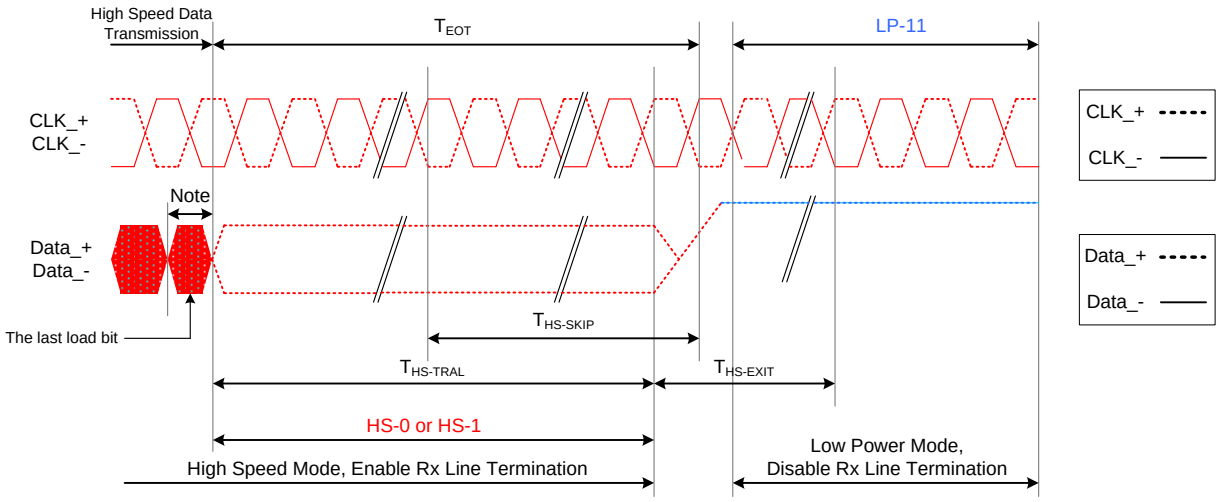
Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission

  MCU changes to HS-1, if the last load bit is HS-0

  MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below

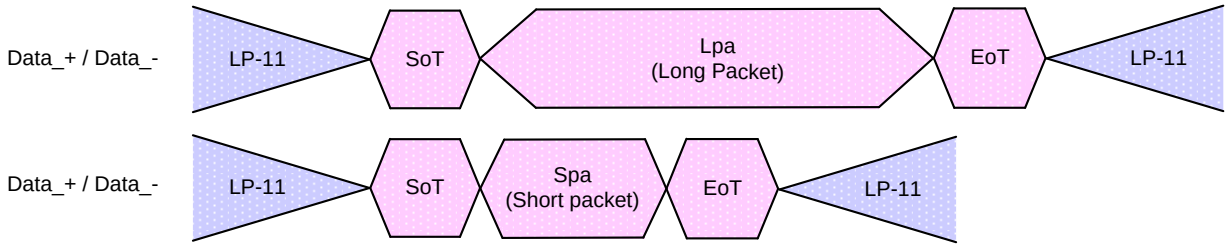


Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

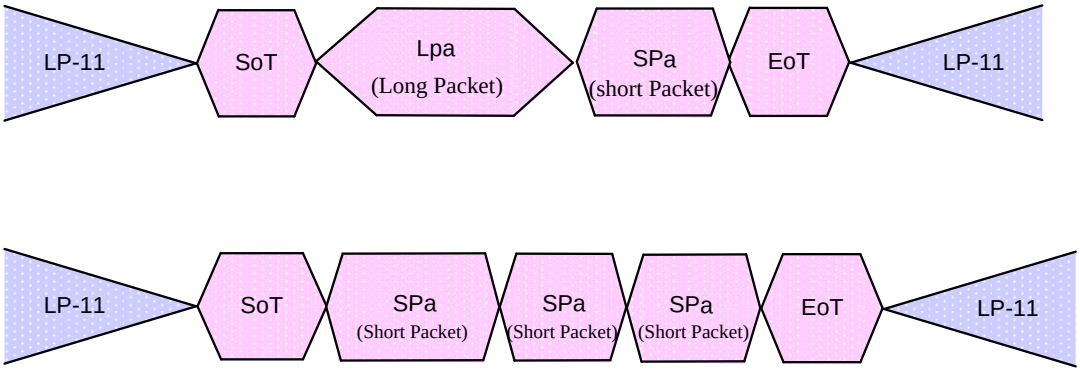
Burst of the High-Speed Data Transmission

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (Lpa) or Short (Spa) packets.

The single packet in High-Speed Data Transmission is illustrated for reference purposes below:

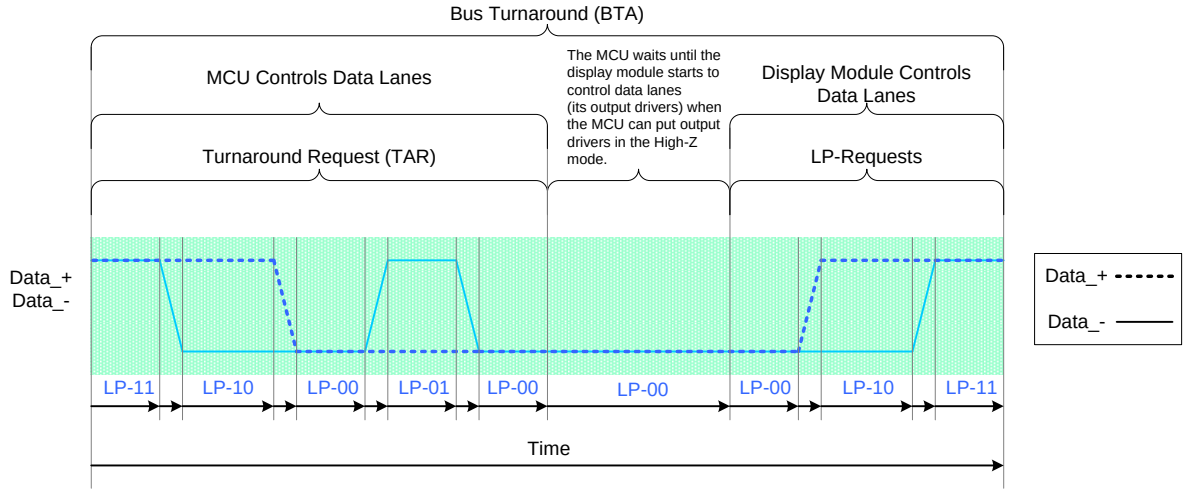


The multiple packets in High-Speed Data Transmission is illustrated for reference purposes below:



3. Bus Turnaround Request

The MCU which is controlling DSI-DATA_P/N Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or Display Module. The MCU and Display Module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to Display Module, as follows.

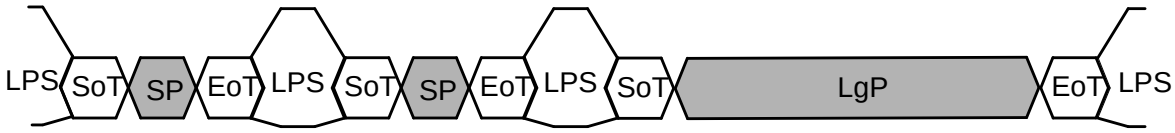


8.5.2 DSI protocol

The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY. Packets are serialized by the PHY and sent across the serial Link. The receiver side of a DSI Link performs the coverse of the transmitter side, decomposing the packet into parallel data, signal events and commands.

8.5.2.1 Multiple Packets per Transmission

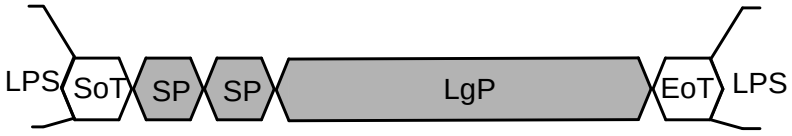
There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS transmission can be started, the transmitter PHY issues a SoT sequence to the receiver. After that, data or command packets can be transmitted in HS mode. Multiple packets may exist within a single HS transmission and the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. In order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp can be enabled or disabled.



Separate Transimssions

Key:

LPS -- Low power state
SoT -- Start of Transmission
EoT -- End of Transmission
SP -- Short Packet
LgP -- Long Packet



Single Transimssions

8.5.2.2 Packet Composition

The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. For example, in Video Mode systems in a display application the logical unit for a packet may be one horizontal display line. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

Packet sizes fall into two categories:

- **Short packets** are four bytes in length including the ECC. Short packets are used for most Command Mode commands and associated parameters. Other Short packets convey events like H Sync and V Sync edges. Because they are Short packets they can convey accurate timing information to logic at the peripheral.

➢**Long packets** specify the payload length using a two-byte Word Count field. Payloads may be from 0 to 2^{16}-1 bytes long. Therefore, a Long packet may be up to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.

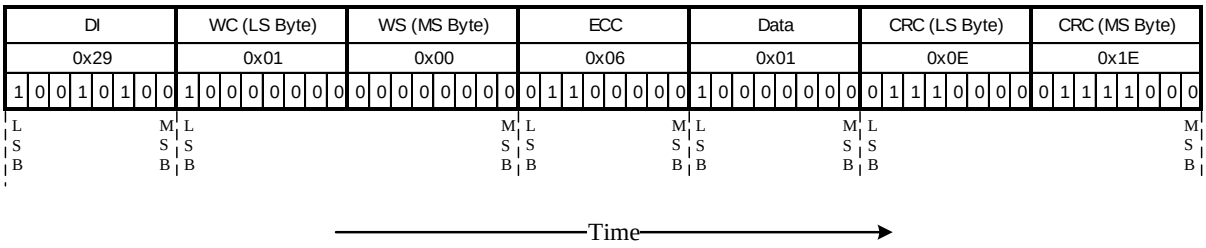
A special case of Command Mode operation is video-rate (update) streaming, which takes the form of an arbitrarily long stream of pixel or other data transmitted to the peripheral. As all DSI transactions use packets, the video stream shall be broken into separate packets. This “packetization” may be done by hardware or software. The peripheral may then reassemble the packets into a continuous video stream for display.

The Set Maximum Return Packet Size command allows the host processor to limit the size of response packets coming from a peripheral.

8.5.2.3 Endian Policy

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

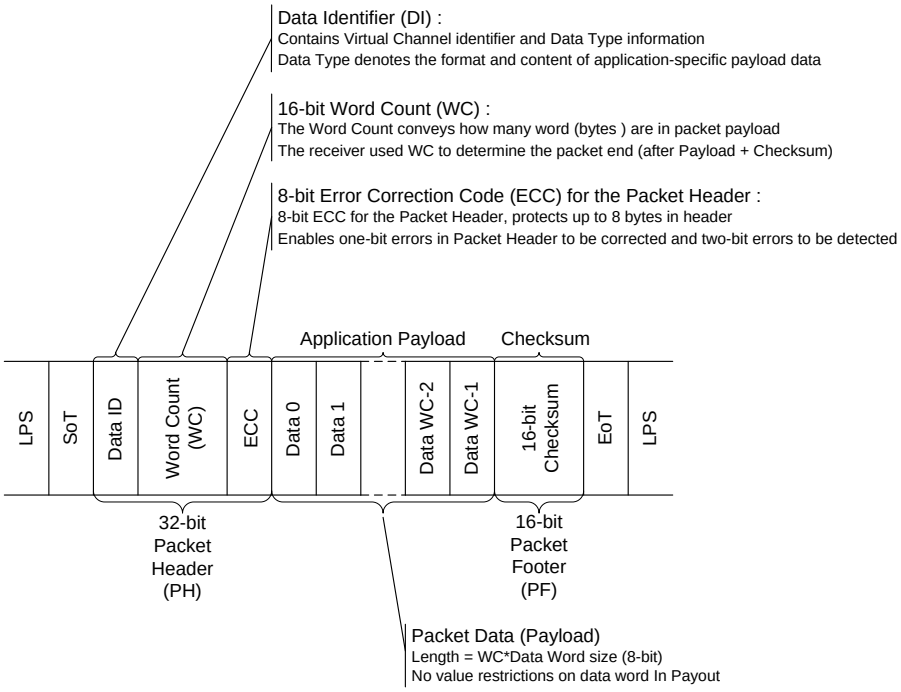
Figure 12 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.



Endian Example (Long Packet)

8.5.2.4 General Packet Structure(Long Packet Format)

A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.



Long Packet Structure

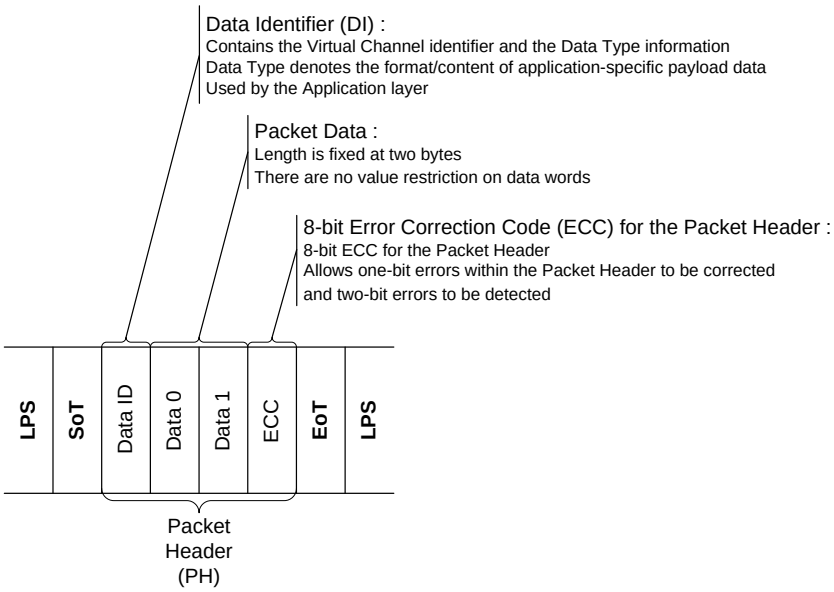
The Data Identifier defines the Virtual Channel for the data and the Data Type for the application specific payload data. See sections 8.8 through 8.10 for descriptions of Data Types. The Word Count defines the number of bytes in the Data Payload between the end of the Packet Header and the start of the Packet Footer. Neither the Packet Header nor the Packet Footer shall be included in the Word Count. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. This includes both the Data Identifier and Word Count fields. After the end of the Packet Header, the receiver reads the next Word Count * bytes of the Data Payload. Within the Data Payload block, there are no limitations on the value of a data word, i.e. no embedded codes are used. Once the receiver has read the Data Payload it reads the Checksum in the Packet Footer. The host processor shall always calculate and transmit a Checksum in the Packet Footer. Peripherals are not required to calculate a Checksum. Also note the special case of zero-byte Data Payload: if the payload has length 0, then the Checksum calculation results in (FFFFh). If the Checksum is not calculated, the Packet Footer shall consist of two bytes of all zeros (0000h). See section 9 for more information on calculating the Checksum. In the generic case, the length of the Data Payload shall be a multiple of bytes. In addition, each data format may impose additional restrictions on the length of the payload data, e.g. multiple of four bytes. Each byte shall be transmitted least significant bit first. Payload data may be transmitted in any byte order restricted only by data format requirements. Multi-byte elements such as Word Count and Checksum shall be transmitted least significant byte first

.

8.5.2.5 General Packet Structure(Short Packet Format)

A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a

Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.



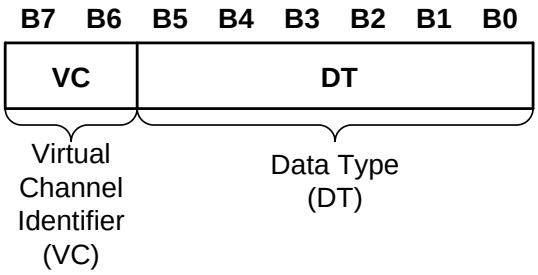
Short Packet Structure

8.5.2.6 Common Packet Elements

Long and Short packets have several common elements that are described in this section.

➢Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte. Figure 15 shows the composition of the Data Identifier (DI) byte. DI[7:6]: These two bits identify the data as directed to one of four virtual channels.DI[5:0]: These six bits specify the Data Type.

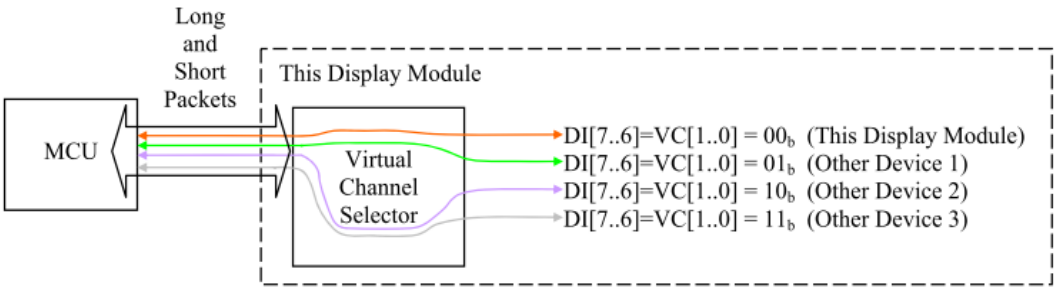


Data Identifier Byte

Virtual Channel Identifier – VC field, DI[7:6]

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel. Note that packets sent in a single transmission each have their own Virtual Channel assignment and can be directed to different peripherals. Although the DSI protocol permits communication

with multiple peripherals, this specification only addresses the connection of a host processor to a single peripheral. Implementation details for connection to more than one physical peripheral are beyond the scope of this document.



Virtual Channel (VC) Configuration

Data Type Field DT[5:0]

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start / end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet. When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

8.5.2.7 Error Correction Code

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

P7 = 0

P6 = 0

P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

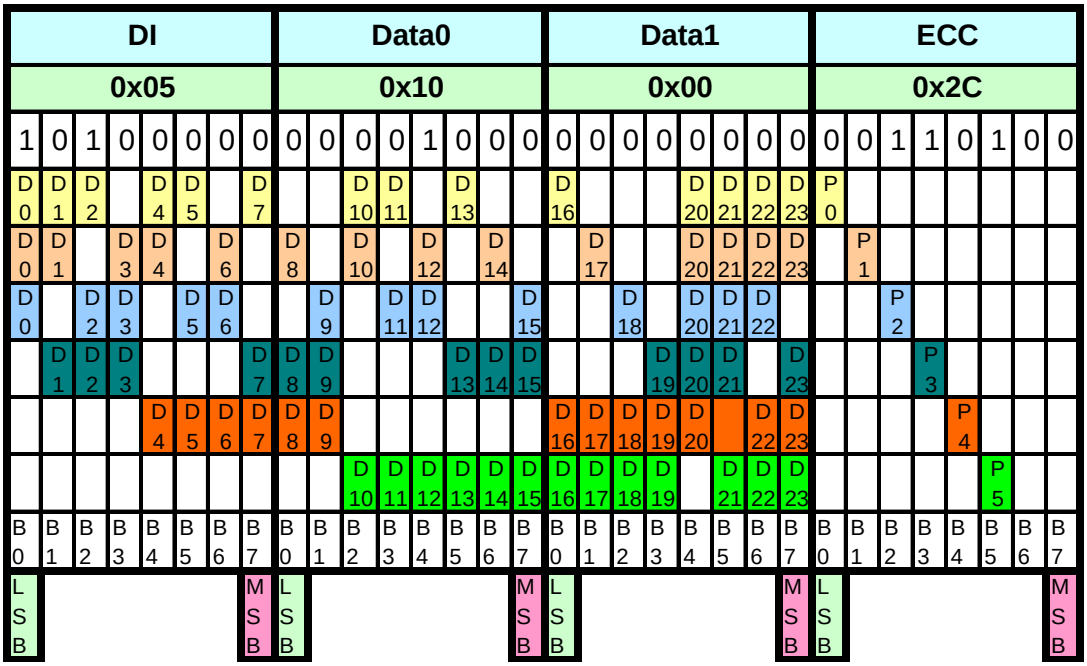
P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

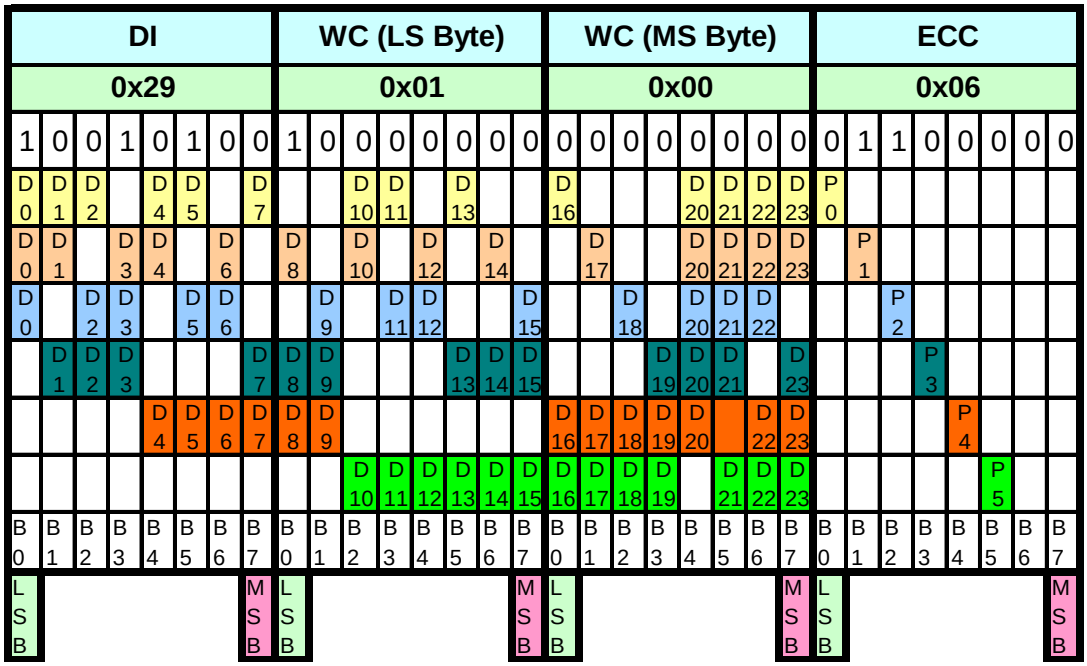
P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, there is only needed 6 bits (P [5…0]) for Error Correction Code (ECC).



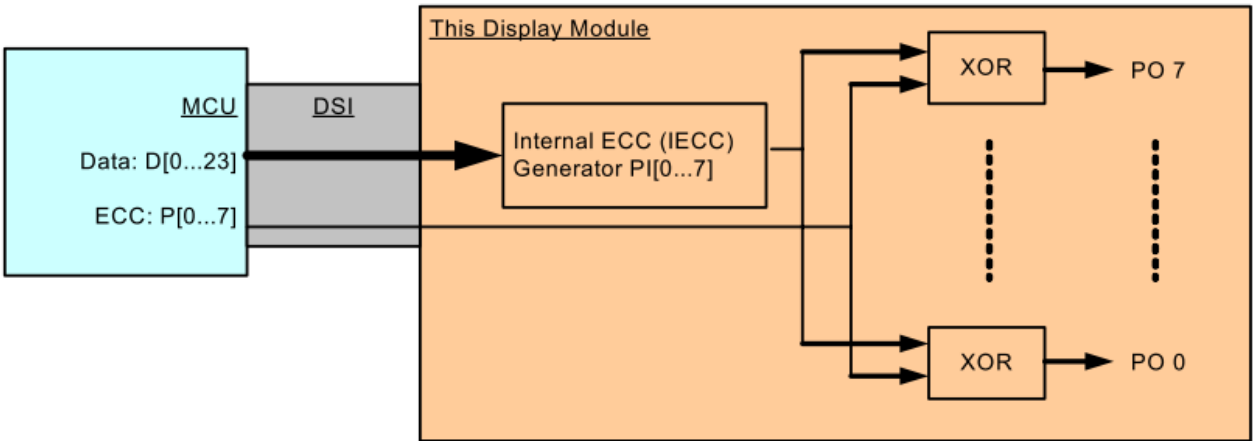
XOR Functionality on the Short Packet (Spa)



XOR Functionality on the Long Packet (Lpa)

The transmitter (The MCU or the Display Module) is sending data bits D[23:0] and Error Correction Code (ECC) P[7:0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction

Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7:0].



Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23:0]) and ECC (P[7:0]) are received correctly, if a value of the PO[7:0]) is 00h.
The sent data bits (D[23:0]) and ECC (P[7:0]) are not received correctly, if a value of the PO[7:0]) is not 00h.

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC	0	0	0	0	0	0	0	0	=00h => No Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC	0	0	1	1	0	0	0	0	=0Ch => Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values – Error

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

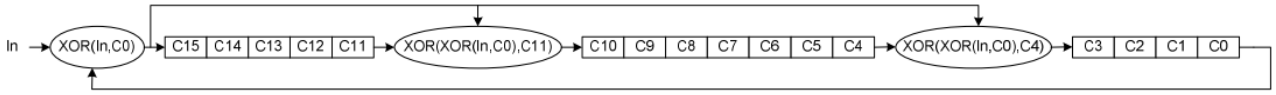
One error is detected if the value of the PO[7:0] is on the above table : One it Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO [7…0] = 0Eh
- The bit of the data (D [23:0]), what is not correct, is D[3]

More than one error is detected if the value of the PO [7…0] is not on the above table: One Bit Error Value of the Error Correction Code (ECC) e.g. PO [7…0] = 0Ch.

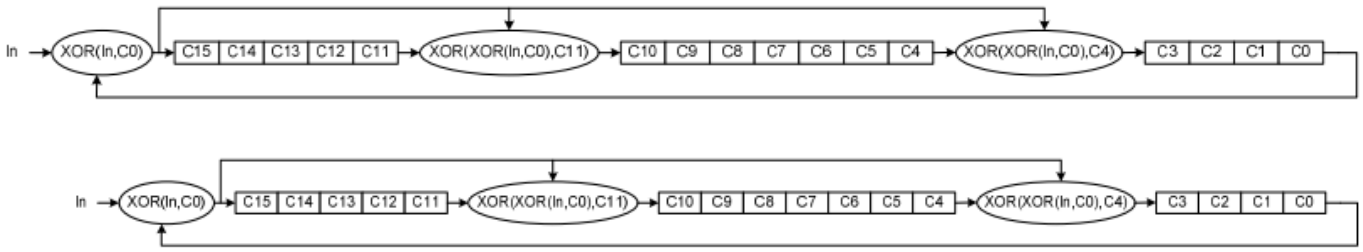
8.5.2.8 Packet Footer on the Long Packet

Packet Footer (PF) of the Long Packet (Lpa) is defined after the Packet Data (PD) of the Long Packet (Lpa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (Lpa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X_{16} + X_{12} + X_5 + X_0$ as it is illustrated below.



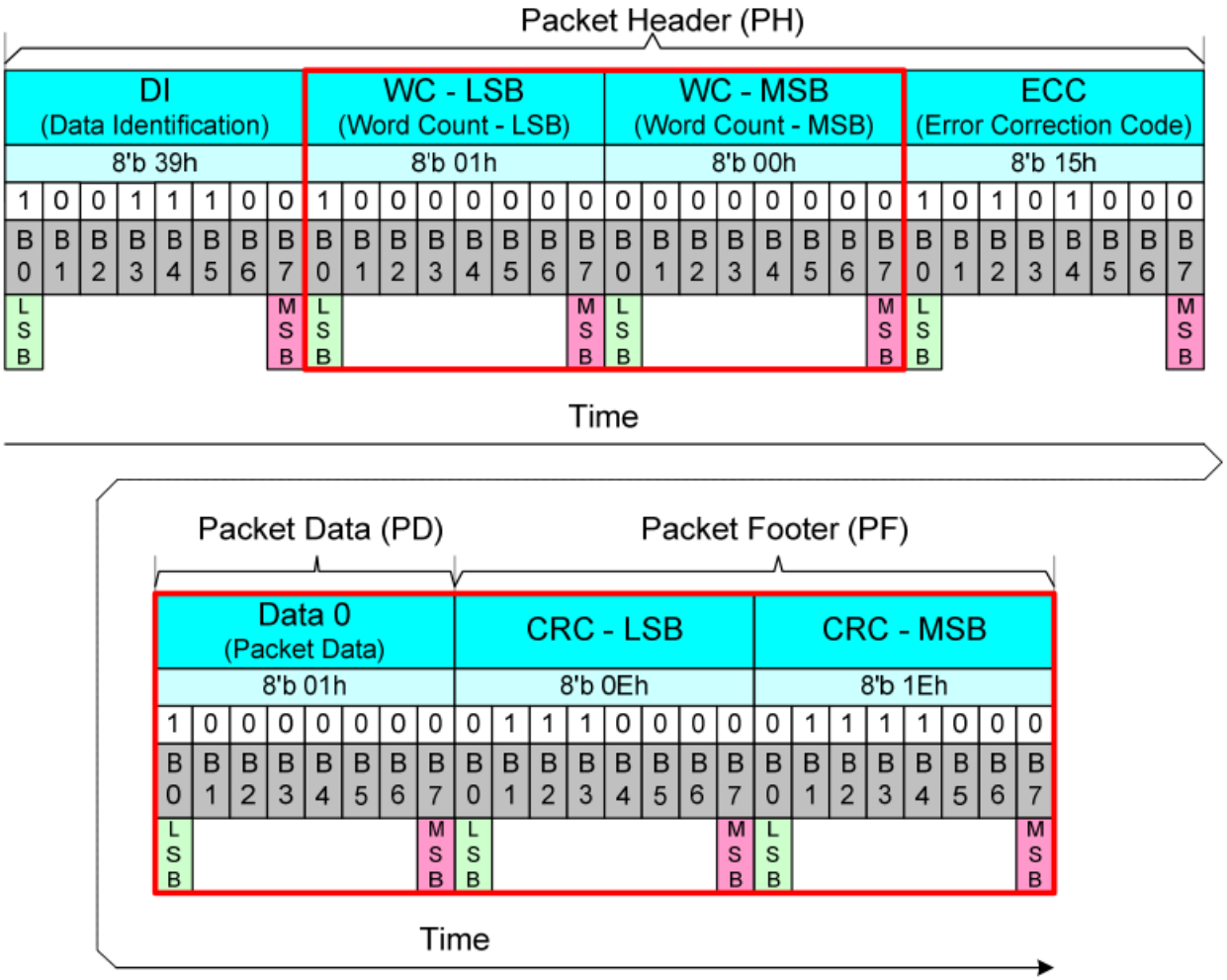
The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (Lpa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) is equal and vice versa the received Packet Data (PD) and Packet Footer(PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

8.5.2.9 Processor to Peripheral Direction Packet Data Types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are show as below table.

Data type	Data type, binary	Description packet	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	Generic READ, no parameters	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h / XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

Data Types for Processor-sourced Packets

All detail function of data types is as below：

Sync event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type, hex	**Function description**	**Number of bytes**
01h	Sync Event, V Sync Start	Short
11h	Sync Event, V Sync End	Short
21h	Sync Event, H Sync Start	Short
31h	Sync Event, H Sync End	Short
Note: In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA.		

Color mode status (Color Mode On, Color Mode Off)		
Data type, hex	**Function description**	**Number of bytes**
02h	Color Mode On that switches a Video Mode display module to a low-color mode for power saving.	Short
12h	Color Mode Off that switches a Video Mode display module from low-color display to normal display.	Short

Display status (shutdown command, turn-on command)		
Data type, hex	**Function description**	**Number of bytes**
22h	Shutdown Peripheral command that turns off the display in a Video Mode display for power saving.	Short
32h	Turn On Peripheral command that turns on the display in Video Mode display for normal display.	Short
Note: When use shutdown command, interface shall remain powered in order to receive the turn-on, or wake-up, command.		

DCS command setting		
Data type, hex	**Function description**	**Number of bytes**
05/15h	DCS Short Write command is used to write a single data byte to a peripheral such as a display module. If a parameter is not required, the parameter byte shall be 00h.	Short
06h	DCS Read command, the returned data may be of Short or	Short

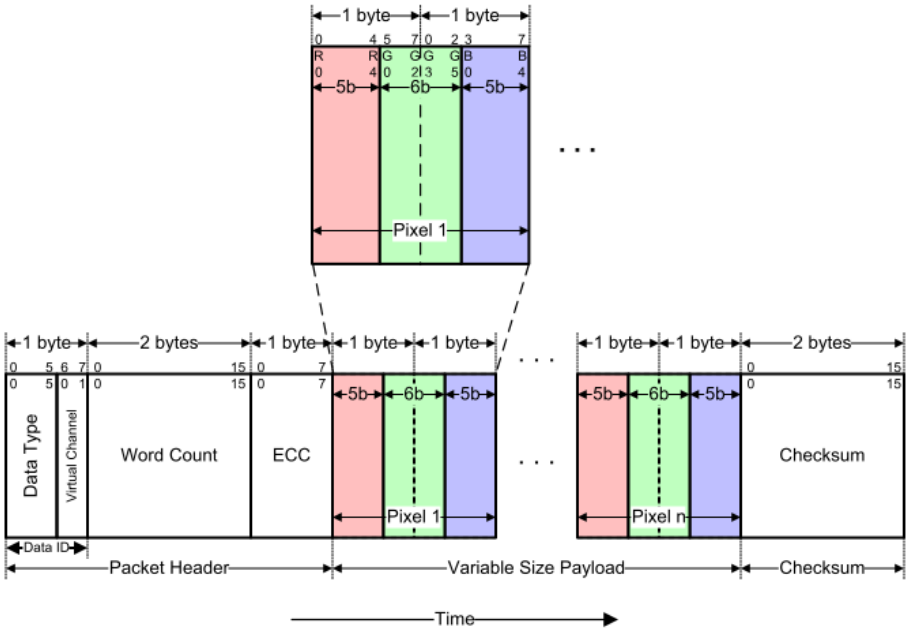
	Long packet format.	
39h	DCS Long Write/ Write _ LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Long

Return packet size setting		
Data type, hex	**Function description**	**Number of bytes**
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	Short
Note: The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.		

Variable data packet		
Data type, hex	**Function description**	**Number of bytes**
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Short
19h	Blanking packet is used to convey blanking timing information in a Long packet.	Short
Note: (1) When Null Packet, the Payload Data belong “null” Data, actual data values sent are irrelevant because the peripheral does not capture or store the data. (2) When Blanking packet, the packet represents a period between active scan lines of a Video Mode display,		

Data stream format – 16bit Format

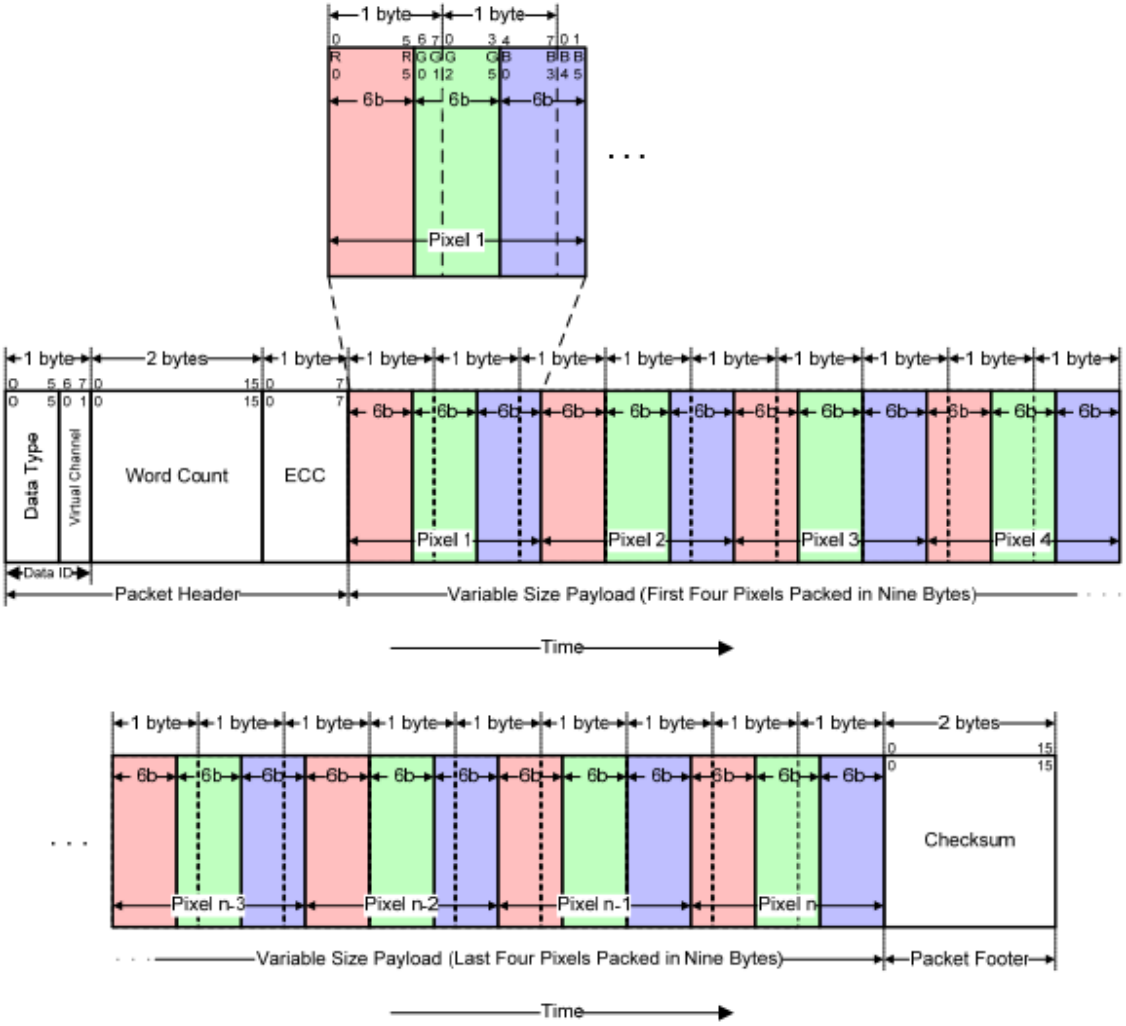
Data stream format – 16bit Format		
Data type, hex	**Function description**	**Number of bytes**
0Eh	Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is five bits red, six bits green, five bits blue, in that order.	Long



Note: That the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

Data stream format – 18bit Format (mode1)

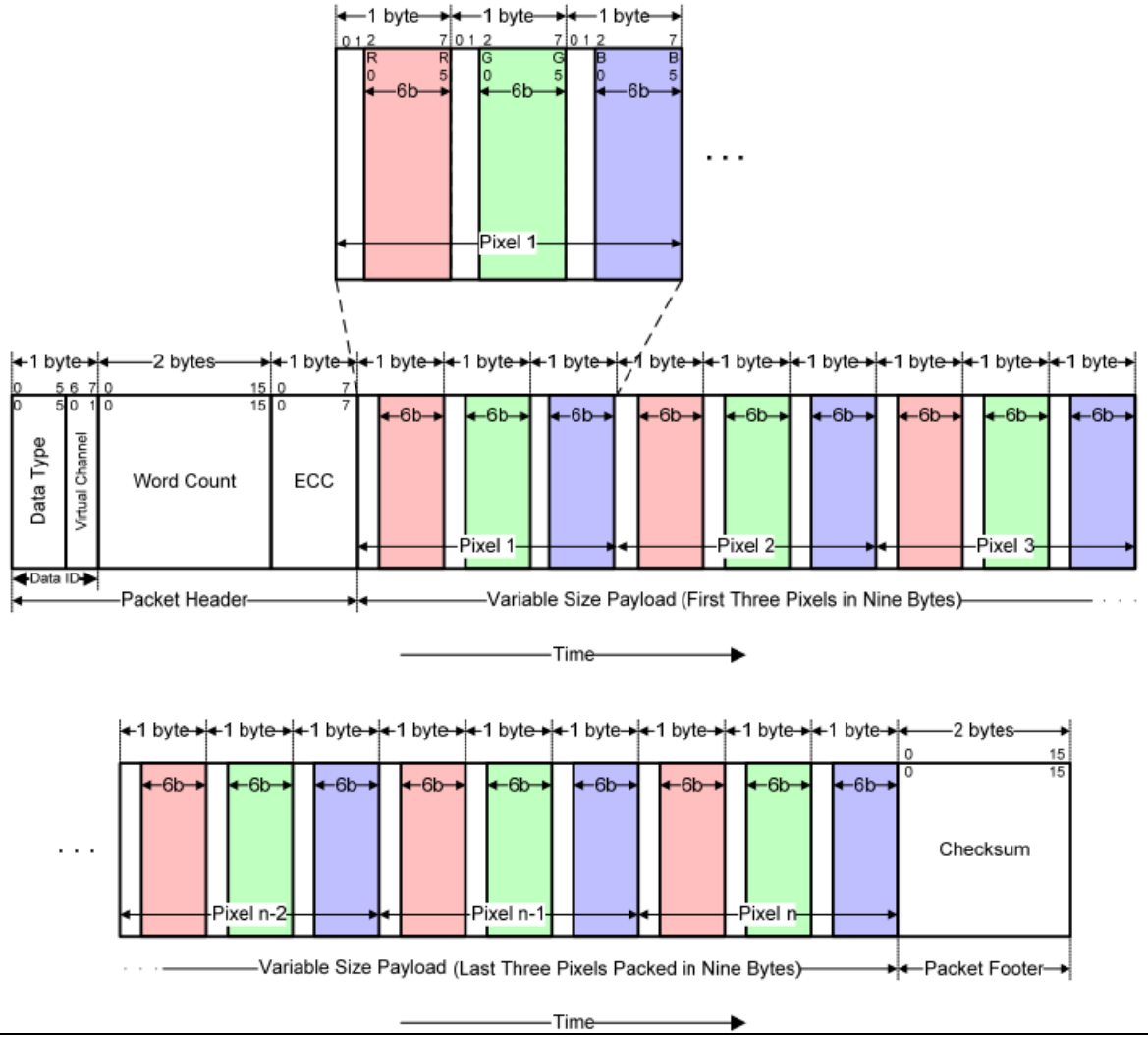
Data stream format – 18bit Format(Mode1)		
Data type, hex	**Function description**	**Number of bytes**
1Eh	Packed Pixel Stream 18-Bit Format is a Long packet used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is six bits red, six bits green, six bits blue, in that order.	Long



Note: Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a “clean start” for the next line.

Data stream format – 18bit Format(mode2)

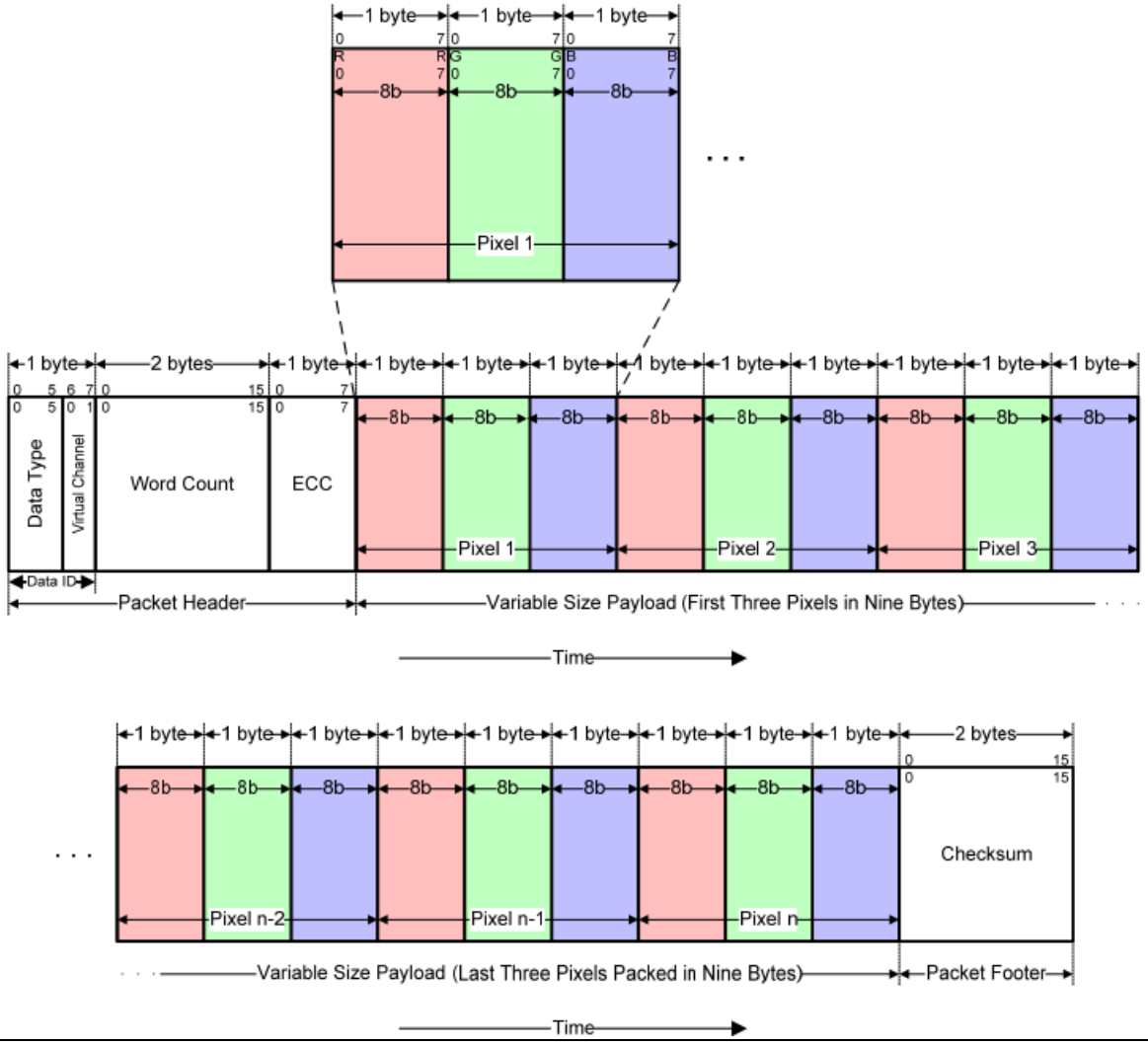
Data stream format – 18bit Format(Mode2)		
Data type, hex	**Function description**	**Number of bytes**
2Eh	In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits[1:0] of each payload byte representing active pixels are ignored.	Long



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

Data stream forma – 24bit Format

Data stream format –24bit Format		
Data type, hex	**Function description**	**Number of bytes**
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue.	Long



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

8.5.2.10 Peripheral-to-Processor (Reverse Direction) LP Transmissions

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions; other Lanes shall be unidirectional. Reverse-direction signaling shall only use LP (Low Power) mode of transmission.

Peripheral-to-processor transactions are of four basic types:

- Tearing Effect is a Trigger message sent to convey display timing information to the host processor. Trigger messages ate signal byte packets sent by a peripheral's PHY layer in response to a signal form the DSI protocol layer.
- Acknowledge is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.
- Acknowledge and Error Report is a Short packet sent if any errors were detected in preceding transmission from the host processor. Once reported, accumulated errors in the error register are cleared.
- Response to Read Request may be Short or Long packet that returns data requested by the preceding READ command from the processor.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or error information back to the host processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

- Following a non-Read command in which no error was detected, the peripheral shall respond with Acknowledge.
- Following a Read request in which no error was detected, the peripheral shall send the requested READ data.
- Following a Read request in which the ECC error was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (Acknowledge with Error Report) packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
- Following a non-Read command in which the ECC error was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (Acknowledge with Error Report) packet, the Error Report shall have the ECC Error flag set.
- Following any command in which SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid was detected, or the DSI command was not

recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

An error report is a Short packet comprised of two bytes following the DI byte, with an ECC byte following the Error Report bytes. By convention, detection and reporting of each error type is signified by setting the corresponding bit to “1”. Table 18 shows the bit assignment for all error reporting.

Bit	Error Report Bit Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

The table as below presents the complete set of peripheral-to-processor Data Types

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge and Error Report	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
11h	01 0001	Generic Short READ Response, 1 byte returned	Short
12h	01 0010	Generic Short READ Response, 2 bytes returned	Short
1Ah	01 1010	Generic Long READ Response	Short
1Ch	01 1100	DCS Long READ Response	Short
21h	10 0001	DCS Short READ Response, 1 byte returned	Short
22h	10 0010	DCS Short READ Response, 2 bytes returned	Short

Data Types for Peripheral-sourced Packets

Acknowledge types		
Data type, hex	**Function description**	**Number of bytes**
02h	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes
Note: When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor. With error Acknowledge with error report, Without error Acknowledge.		

Generic Read types		
Data type, hex	**Function description**	**Number of bytes**
11h, 12h	This is the Generic Short Read Response, 1 or 2bytes, respectively.	4 bytes
1Ah	This is the long-packet response to Generic Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD + Payload DATA + PF)
Note: If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h.If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent.		

DCS Read types		
Data type, hex	**Function description**	**Number of bytes**
21h, 22h	This is the DCS Short Read Response, 1 or 2bytes, respectively..	4 bytes
1Ch	This is the long-packet response to DCS Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD + Payload DATA + PF)
Note: If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h.If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent.		

9 COMMAND

9.1.. Command Table List

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**D17-8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No operation
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read display ID
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
Read Number of the Errors on DSI	0	↑	1		0	0	0	0	0	1	0	1	(05h)	Read DSI
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		D7	D6	D5	D4	D3	D2	D1	D0		
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read display status
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	ST25	ST24		-
	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
	1	1	↑	-	Vscroll	ST14	INVON	ALLON	ALLOFF	DISON	TEON	GCS2		-
	1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read display power
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	0	0		
RDD MADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read display
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	MY	MX	MV	ML	RGB	DISDL	0	0		-
RDD Interface Pixel Format	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read display pixel
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	R3	R2	R1	R0	0	D2	D1	D0		-

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**D17-8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read display image
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	VSSON	0	INVON	0	0	GC2	GC1	GC0		-
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read display signal
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	TEON	TEM	HSYN	VSYN	PIXCLK	DATEN	0	DSIER		-
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read display self-diagnostic result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	0	0	0	0	0	D0		-
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: 0≦ XS≦ X
	1	↑	1		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
	1	↑	1		XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address start: S≦ XE≦ X
	1	↑	1		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**D17-8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: 0≦ YS≦ Y
	1	↑	1		YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
	1	↑	1		YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address start: S≦ YE≦ Y
	1	↑	1		YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Read data
	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial sart/end address set
	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address: (0, 1,2, ..P)
	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0, 1,2, 3, , P)
	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Vertical scrolling definition
	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		
	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		
	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		
	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**D17-8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect line on
	1	↑	1	-	-	-	-	-	-	-	-	TEM		
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
	1	↑	1	-	MY	MX	MV	ML	RGB	MH	0	0		-
VSCRSADD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Vertical scrolling start address
	1	↑	1	-	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8		
	1	↑	1	-	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0		
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
Interface Pixel Format	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
	1	↑	1	-	0	D6	D5	D4	0	D2	D1	D0		Interface format
RAMWRC	0	↑	1	-	0	0	1	1	1	1	0	0	(3Ch)	Memory write continue
	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		
	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRDC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)	Memory read continue
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		
	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
TESCAN	0	↑	1	-	0	1	0	0	0	1	0	0	(44h)	Set tear scanline
	1	↑	1	-	N15	N14	N13	N12	N11	N10	N9	N8		
	1	↑	1	-	N7	N6	N5	N4	N3	N2	N1	N0		

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**D17-8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
RDTESCAN	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)	Get scanline
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	N15	N14	N13	N12	N11	N10	N9	N8		
	1	1	↑	-	N7	N6	N5	N4	N3	N2	N1	N0		
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)	Write display brightness
	1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)	Read display brightness value
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)	Write CTRL display
	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0		
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)	Read CTRL value dsiplay
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0		
WRCABC	0	↑	1	-	0	1	0	1	0	1	0	1	(55h)	Write content adaptive brightness control
	1	↑	1	-	CECTRL	0	CE1	CE0	0	0	C1	C0		
RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	(56h)	Read content adaptive brightness control
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	0	0	0	0	0	C1	C0		
WRCABCMB	0	↑	1	-	0	1	0	1	1	1	1	0	(5Eh)	Write CABC minimum brightness
	1	↑	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		

COMMAND Table 1														
Instruction	**D/CX**	**WRX**	**RDX**	**D17-8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
RDCABCMB	0	↑	1	-	0	1	0	1	1	1	1	1	(5Fh)	Read CABC minimum brightness
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDFCHKSUM	0	↑	1		1	0	1	0	1	0	1	0	(Aah)	Read First Checksum
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0		
RDCCHKSUM	0	↑	1		1	0	1	0	1	0	1	0	(Afh)	Read Continue Checksum
	1	1	↑		-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0		
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(Dah)	Read ID1
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

Register List

COMMAND Table 2														
Instruction	**D/CX**	**WRX**	**RDX**	**D17-8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
IFMODE	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)	Interface Mode Control
	1	↑	1		SPI_EN	0	0	0	VSCP	HSCP	PKP	DEP		
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	Frame Rate Control（In Normal Mode/Full Colors）
	1	↑	1	-	FRS[3:0]				0	0	DIVA[1:0]			
	1	↑	1	-	0	0	0	RTNA[4:0]						
FRMCTR2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	Frame Rate Control（In Idle Mode/8 colors）
	1	↑	1	-	0	0	0	0	0	0	0	0		
	1	↑	1	-	0	0	0	RTNB[4:0]						
FRMCTR3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	Frame Rate Control（In Partial Mode/Full colors）
	1	↑	1	-	0	0	0	0	0	0	0	0	XX	
	1	↑	1	-	0	0	0	RTNC[4:0]					XX	
INVTR	0	↑	1	-	0	0	0	0	1	0	0	1	(B4h)	Display Inversion Control
	1	↑	1	-	-	-	-	-	-	-	DINV			
BPC	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)	Blanking Porch Control
	1	↑	1	-	VFP[7:0]									
	1	↑	1	-	VBP[7:0]									
	1	↑	1	-	0	0	0	0	0	0	0	0		
	1	↑	1	-	HBP[7:0]									
DFC	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)	Display Function Control
	1	↑	1	-	BYPASS	RCM	RM	0	PTG[1:0]		PT[1:0]			
	1	↑	1	-	0	GS	SS	SM	ISC[3:0]					
	1	↑	1	-	0	0	NL[5:0]							
EM	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)	Entry Mode Set
	1	↑	1	-	EPF[1:0]		0	0	DSTB	GON	DTE	0		
MS	0	↑	1	-	1	0	1	1	1	0	0	1	(B9h)	Mode Selection
	1	↑	1	-	0	0	0	0	0	0	1	0		
PWR1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)	Power Control 1
	1	↑	1		AVDD[1:0]		AVCL[1:0]		0	0	0	0		
	1	↑	1	-	VGHS [2:0]			0	VGLS [2:0]			0		
PWR2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)	Power Control 2

COMMAND Table 2

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	1	-	0	VRH[6:0]								
PWR3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)	Power Control 3
	1	↑	1	-	1	0	1	0	SOP		GOP			
VCMPCTL	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)	Vcom Control
	1	↑	1	-	0	0	VCMP[5:0]							
VCM Offset	0	↑	1	-	1	1	0	0	0	1	1	0	(C6h)	Vcom Offset Register
	1	↑	1	-	VMFSEL	0	VMF_REG [5:0]							
NVMADW	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)	NVM Address/Data
	1	↑	1	-	0	0	0	PROG_ADDR[4:0]						
	1	↑	1	-	PROG_DATA[7:0]									
NVMBPROG	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)	NVM Byte Program Control
	1	↑	1	-	PROGCODE[23:16]									
	1	↑	1	-	PROGCODE[15:8]									
	1	↑	1	-	PROGCODE[7:0]									
NVMSTRD	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	NVM Status Read
	1	1	↑	-	-									
	1	1	↑	-	ID2CNT[3:0]				ID1CNT[3:0]					
	1	1	↑	-	VMFCNT[3:0]				ID3CNT[3:0]					
	1	1	↑	-	BUSY	-	-	-	-	-	-	-		
	1	1	↑		-	-	VMF[5:0]							
RDID4	0	↑	1	-	1	1	0	1	0	0	1	1	(D3h)	Read ID4
	1	1	↑	-	-	-	-	-	-	-	-	-	-	
	1	1	↑	-	ID41[7:0]									
	1	1	↑	-	ID42[7:0]									
	1	1	↑	-	ID41[7:0]									
PGC	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Positive Gamma Control
	1	↑	1	-	V63P[3:0]				V0P[3:0]					
	1	↑	1	-	0	0	V1P[5:0]							
	1	↑	1	-	0	0	V2P[5:0]							
	1	↑	1	-	0	0	0	V4P[4:0]						
	1	↑	1	-	0	0	0	V6P[4:0]						
	1	↑	1	-	0	0	J0P[1:0]		V13P[3:0]					
	1	↑	1	-	0	V20P[6:0]								
	1	↑	1	-	0	V36P[2:0]			0	V27P[2:0]				

COMMAND Table 2

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	1	-	0	V43P[6:0]								
	1	↑	1	-	0	0	J1P[1:0]		V50P[3:0]					
	1	↑	1	-	0	0	0	V57P[4:0]						
	1	↑	1	-	0	0	0	V59P[4:0]						
	1	↑	1	-	0	0	V61P[5:0]							
	1	↑	1	-	0	0	V62P[5:0]							
NGC	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Negative Gamma Control
	1	↑	1	-	V63N[3:0]				V0N[3:0]					
	1	↑	1	-	0	0	V1N[5:0]							
	1	↑	1	-	0	0	V2N[5:0]							
	1	↑	1	-	0	0	0	V4P[4:0]						
	1	↑	1	-	0	0	0	V6N[4:0]						
	1	↑	1	-	0	0	J0N[1:0]		V13N[3:0]					
	1	↑	1		0	V20N[6:0]								
	1	↑	1		0	V36N[2:0]			0	V27N[2:0]				
	1	↑	1		0	0	V43P[5:0]							
	1	↑	1		0	0	J1N[1:0]		V50N[3:0]					
	1	↑	1	-	0	0	0	V57N[4:0]						
	1	↑	1	-	0	0	0	V59N[4:0]						
	1	↑	1	-	0	0	V61N[5:0]							
	1	↑	1	-	0	0	V62N[5:0]							
DGC1	0	↑	1	-	1	1	1	0	0	0	1	0	(E2h)	Digital Gamma Control1
	1	↑	1	-	DGAM_R00									
	1	↑	1	-	DGAM_R01									
	1	↑	1	-	:									
	1	↑	1	-	DGAM_R62									
	1	↑	1	-	DGAM_R63									
DGC2	0	↑	1	-	1	1	1	0	0	0	1	1	(E3h)	Digital Gamma Control2
	1	↑	1	-	DGAM_B00									
	1	↑	1	-	DGAM_B01									
	1	↑	1	-	:									

COMMAND Table 2														
Instruction	**D/CX**	**WRX**	**RDX**	**D17-8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**	**Function**
	1	↑	1	-	DGAM_B62									
	1	↑	1	-	DGAM_B63									
DOCA	0	↑	1	-	1	1	1	0	1	0	0	0	(E8h)	Display Output CTRL Adjust
	1	↑	1	-	0	1	0	0	0	0	0	0		
	1	↑	1	-	1	0	0	0	1	0	1	0		
	1	↑	1	-	0	0	0	0	0	0	0	0		
	1	↑	1	-	0	0	0	0	0	0	0	0		
	1	↑	1	-	0	0	1	0	S_END					
	1	↑	1	-	0	0	G_START							
	1	↑	1		G_EQ	0	G_END							
	1	↑	1		0	0	1	1	0	0	1	1		
CSCON	0	↑	1	-	1	1	1	1	0	0	0	0	(F0h)	Command Set Control
	1	↑	1	-	D[7:0]									
SPIRC	0	↑	1	-	1	1	1	1	1	0	1	1	(FBh)	SPI Read Control
	1	1	↑	-	0	0	0	SPI_REN	SPI_CNT[3:0]					

9.2.. Command Table 1

9.2.1 NOP (00h)

00H	NOP (No Operation)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-
Description	This command is empty command. “-“ Don’t care												
Restriction													

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

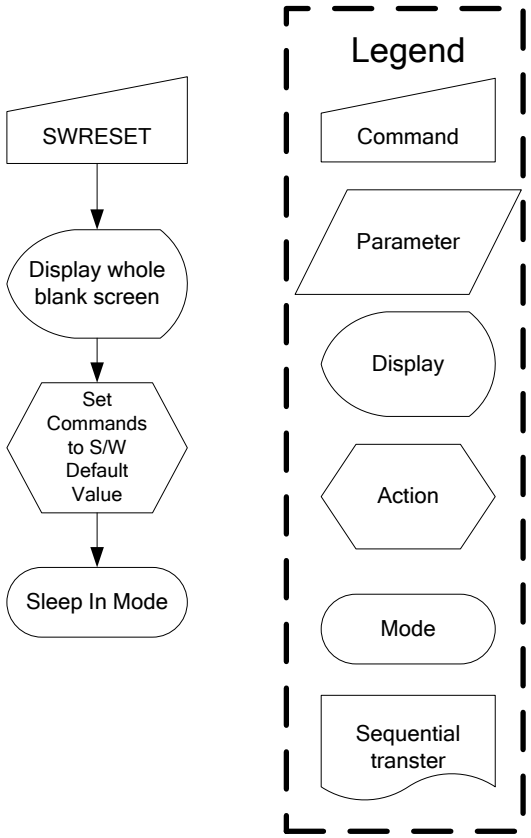
Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart

9.2.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-
Description	“-“ Don’t care - When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. - Frame memory contents are unaffected by this command.												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers’ factory default values to the registers during this 5msec.												

<table>
<tr><td></td><td>If software reset is sent during sleep in mode, it will be necessary to wait 120msec before sending sleep out command.
Software reset command cannot be sent during sleep out sequence.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>N/A</td></tr>
<tr><td>S/W Reset</td><td>N/A</td></tr>
<tr><td>H/W Reset</td><td>N/A</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

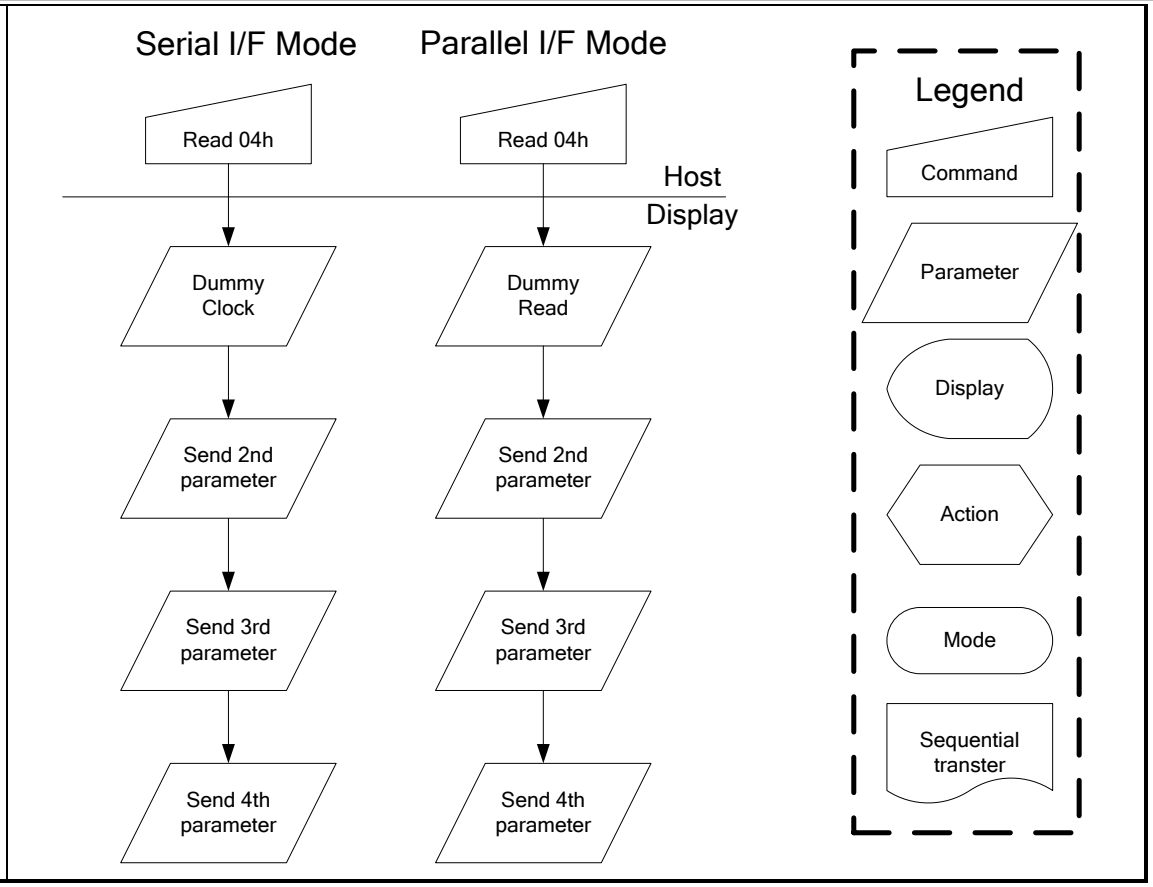
9.2.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	FFh
3rd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	FFh
4th parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	FFh
Description	- -The 1st parameter is dummy data -The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID. -The 3rd parameter (ID26 to ID20): LCD module/driver version ID -The 4th parameter (ID37 to ID30): LCD module/driver ID. -Commands RDID1/2/3(Dah, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively. "-" Don't care												
Restriction													
Register availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	FFh	FFh	FFh
S/W Reset	FFh	FFh	FFh
H/W Reset	FFh	FFh	FFh

Flow Chart



9.2.4 Read Number of the Errors on DSI (05h)

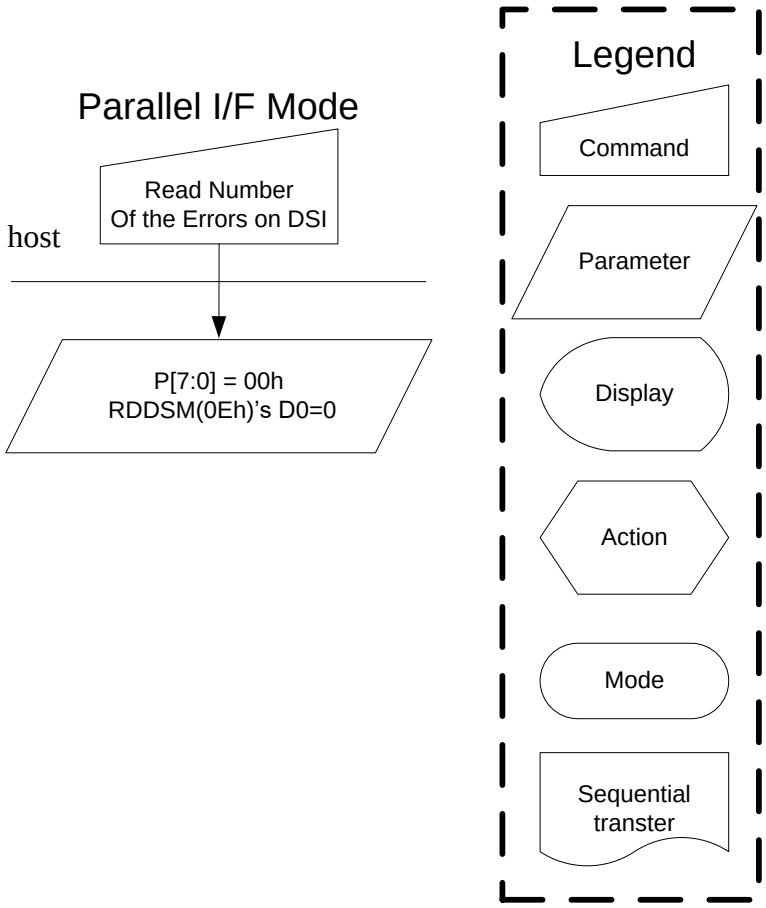
00H	RDNUMED (Read Number of the Errors on DSI)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	1	0	1	(05h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd Parameter	1	1	↑	-	P7	P6	P5	P4	P3	P2	P1	P0	
Parameter	No Parameter												-
Description	The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the errors. P[7] is set to '1' if there is overflow with P[6..0] bits. P[7..0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (= The read function is completed). "-" Don't care												
Restriction	This command is available in MIPI interface. In the other interface, P[7:0] bits are set to "0"s.												
Register Availability	Status | Availability												

		Normal Mode On, Idle Mode Off, Sleep Out	Yes
		Normal Mode On, Idle Mode On, Sleep Out	Yes
		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



9.2.5 RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	ST25	ST24	
3rd parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	
4th parameter	1	1	↑	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	
5th parameter	1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON (D31)	Booster Voltage Status	'1' =Booster on, '0' =Booster off
MY(D30)	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX(D29)	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='0')
MV(D28)	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0'
ML(D27)	Scan Address Order (ML)	'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')
RGB(D26)	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
ST245(D25)	For Future Use	'0'
ST24(D24)	For Future Use	'0'
ST23(D23)	For Future Use	'0'
IFPF2(D22)	Interface Color Pixel Format Definition	"101" = 16-bit / pixel, "110" = 18-bit / pixel, "111" = 24-bit / pixel, others are no define
IFPF1(D21)		
IFPF0(D20)		
IDMON(D19)	Idle Mode On/Off	'1' = On, "0" = Off
PTLON(D18)	Partial Mode On/Off	'1' = On, "0" = Off
SLPOUT(D17)	Sleep In/Out	'1' = Out, "0" = In

	NORON(D16)	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display
	ST15(D15)	Vertical Scrolling Status	'1' = Scroll on,"0" = Scroll off
	ST14(D14)	Not used	'0'
	INVON(D13)	Inversion Status	'1' = On, "0" = Off
	ST12(D12)	All Pixels On (Not Used)	'0'
	ST11(D11)	All Pixels Off (Not Used)	'0'
	DISON(D10)	Display On/Off	'1' = On, "0" = Off
	TEON(D9)	Tearing effect line on/off	'1' = On, "0" = Off
	GCSEL2(D8)	Gamma Curve Selection	"000" = GC0
	GCSEL1(D7)		"001" = GC1
	GCSEL0(D6)		"010" = GC2 "011" = GC3 "100" to "111" = Not defined
	TEM(D5)	Tearing effect line mode	'0' = mode1, '1' = mode2
	ST4(D4)	For Future Use	'0'
	ST3(D3)	For Future Use	'0'
	ST2(D2)	For Future Use	'0'
	ST1(D1)	For Future Use	'0'
	ST0(D0)	For Future Use	'0'

"-" Don't care

Restriction

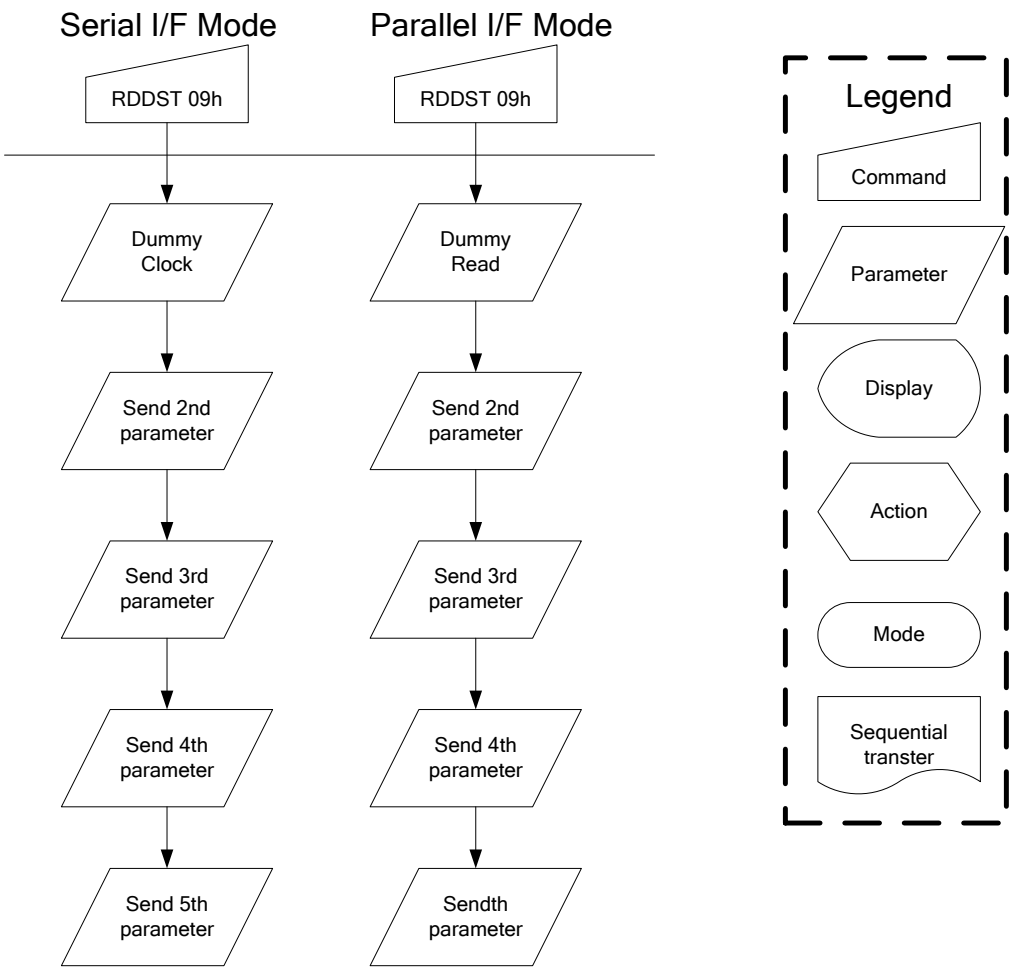
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (ST31 to ST0)			
	ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]
Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000
S/W Reset	0xxx-xx00	0110-0001	0000-0000	0000-0000
H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000

Flow Chart



9.2.6 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off
IDMON	Idle mode on/off	*'1' = Idle Mode On,* *'0' = Idle Mode Off*
PTLON	Partial mode on/off	'1' =Partial mode on, '0' =Partial mode off,
SLPOUT	Sleep in/out	'1' =Sleep out, '0' =Sleep in,
NORON	Display normal mode on/off	'1' = Normal display, '0' = Partial display,
DISON	Display on/off	'1' =Display on, '0' =Display off,
D1	Not Used	"0"
D0	Not Used	"0"

"-" Don't care

Restriction

There is one dummy parameter when using Parallel interface.

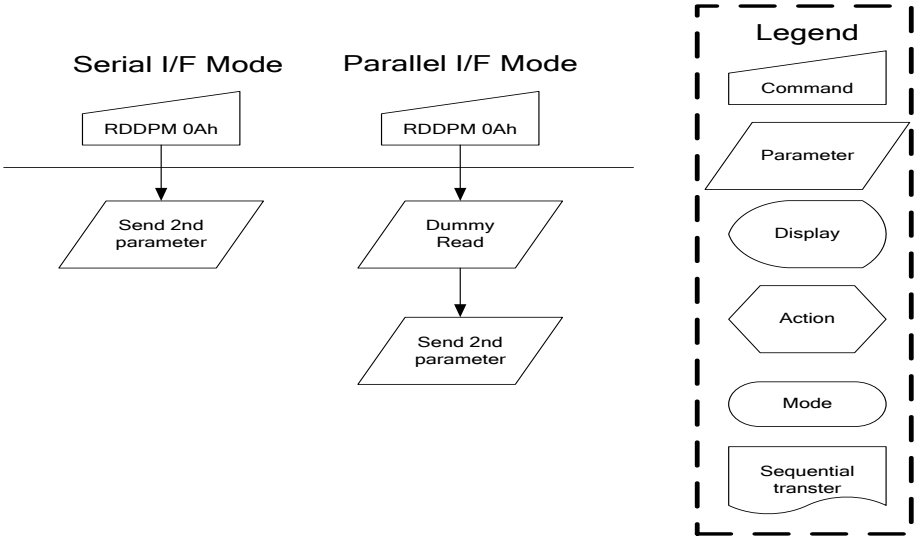
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000-1000(08h)
S/W Reset	0000-1000(08h)
H/W Reset	0000-1000(08h)

Flow Chart



9.2.7 RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	MY	MX	MV	ML	RGB	MH	D1	D0	

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='0')
MV	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0'
ML	Scan Address Order (ML)	'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')
RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
MH	Horizontal Order	'0' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1')
D1	Not used	'0'
D0	Not used	'0'

"-" Don't care

Restriction: There is one dummy parameter when using Parallel interface.

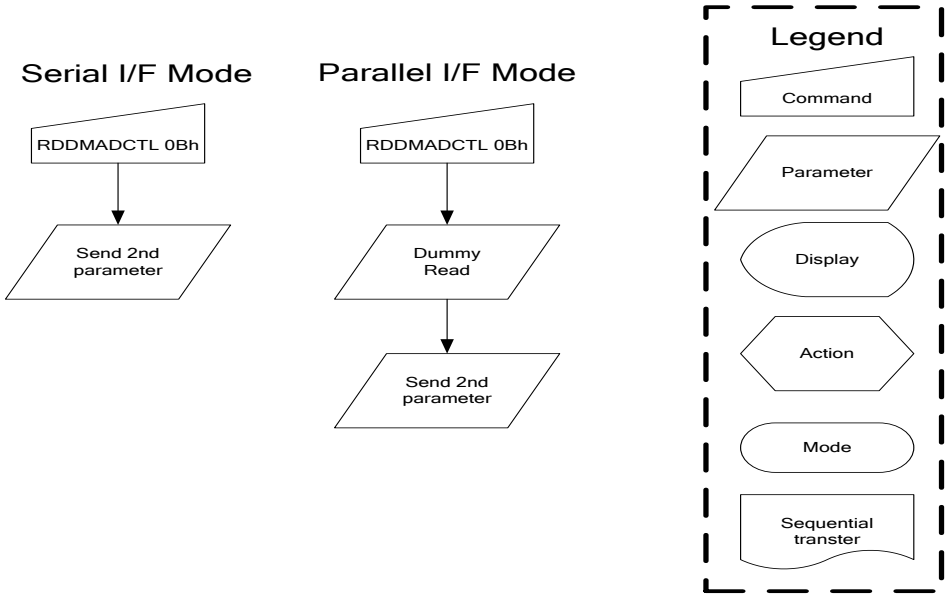
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	0000-0000 (00h)
S/W Reset	No change
H/W Reset	0000-0000 (00h)

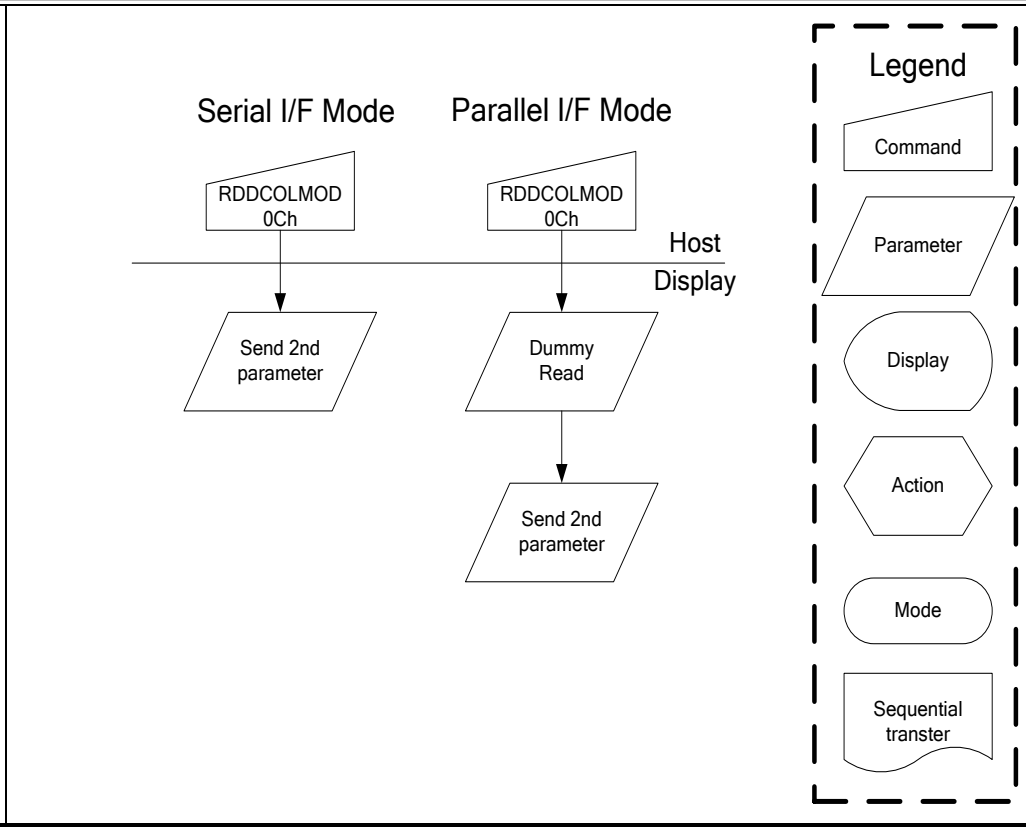
Flow Chart



9.2.8 RDDCOLMOD (0Ch): Read Display Pixel Format

<table>
<tr><td>0CH</td><td colspan="13">RDDCOLMOD (Read Display Pixel Format)</td></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>RDDCOLMOD</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>(0Ch)</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>D6</td><td>D5</td><td>D4</td><td>0</td><td>D2</td><td>D1</td><td>D0</td><td></td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D6</td><td rowspan="3">RGB interface color format</td><td rowspan="3">‘101’ = 16 bit/pixel
‘110’ = 18 bit/pixel</td></tr>
<tr><td>D5</td></tr>
<tr><td>D4</td></tr>
<tr><td>D3</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D2</td><td rowspan="3">Control interface color format</td><td rowspan="3">‘101’ = 16 bit/pixel
‘110’ = 18 bit/pixel
‘111’ = 24 bit/pixel</td></tr>
<tr><td>D1</td></tr>
<tr><td>D0</td></tr>
</table>
Others are no define and invalid
“-“ Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">There is one dummy parameter when using Parallel interface.</td></tr>
<tr><td>Register availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000-0110 (18 bit/pixel)</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>0000-0110 (18 bit/pixel)</td></tr>
</table>
</td></tr>
</table>

Flow Chart



9.2.9 RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	VSSON	0	INVON	0	0	GC2	GC1	GC0	

Description

This command indicates the current status of the display as described in the table below:

-VSSON: Vertical scrolling on/off

-INVON: Inversion on/off

Gamma Curve Selection	GC2	GC1	GC0	Gamma set (26h) Parameter
Gamma curve 1	0	0	0	GC0
Gamma curve 2	0	0	1	GC1
Gamma curve 3	0	1	0	GC2
Gamma curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Others are no define and invalid

"-" Don't care

Restriction

There is one dummy parameter when using Parallel interface.

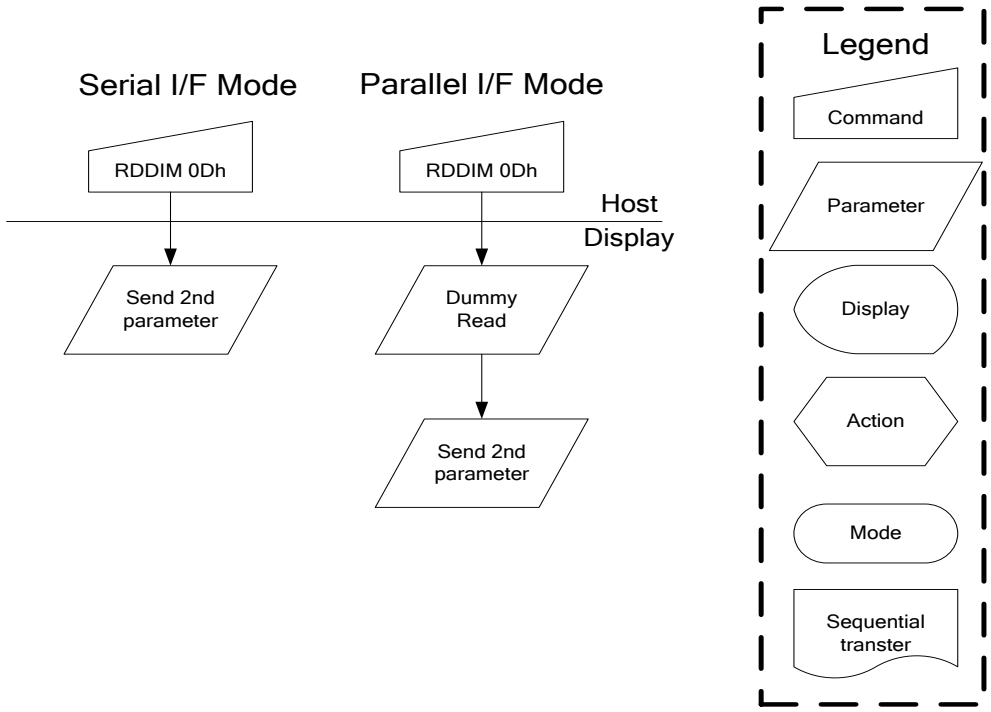
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

Flow Chart



9.2.10 RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	TEON	TEM	HS	VS	PixelClk	DataEn	0	ErrorDSI	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing effect line on/off	'1' = ON, '0' = OFF,
TEM	Tearing effect line mode	'1' = mode2, '0' = mode1,
HS	Horizontal Sync (RGB interface)	'1' = ON, '0' = OFF,
VS	Vertical Sync (RGB interface)	'1' = ON, '0' = OFF,
PixelClk	Pixel Clock (DOTCLK, RGB interface)	'1' = ON, '0' = OFF,
DataEn	Data Enable (DE, RGB interface)	'1' = ON, '0' = OFF,
ErrorDSI	Error On DSI (MIPI Interface)	'1' = Error, '0' = No Error

"-" Don't care

Restriction	There is one dummy parameter when using Parallel interface.

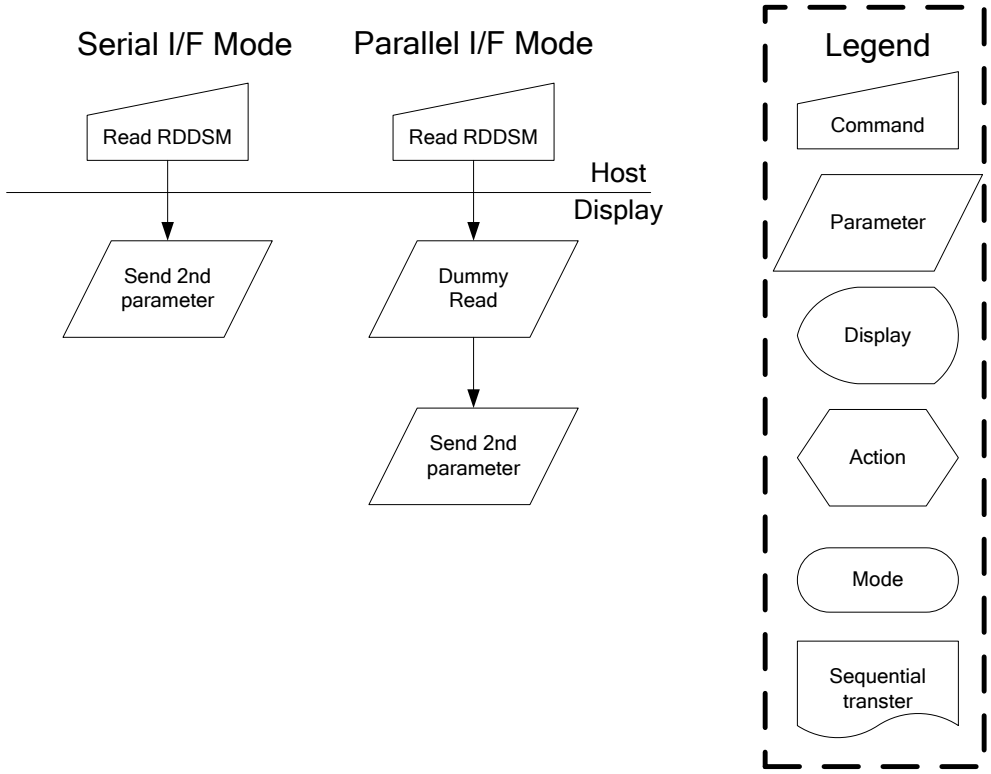
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

Flow Chart



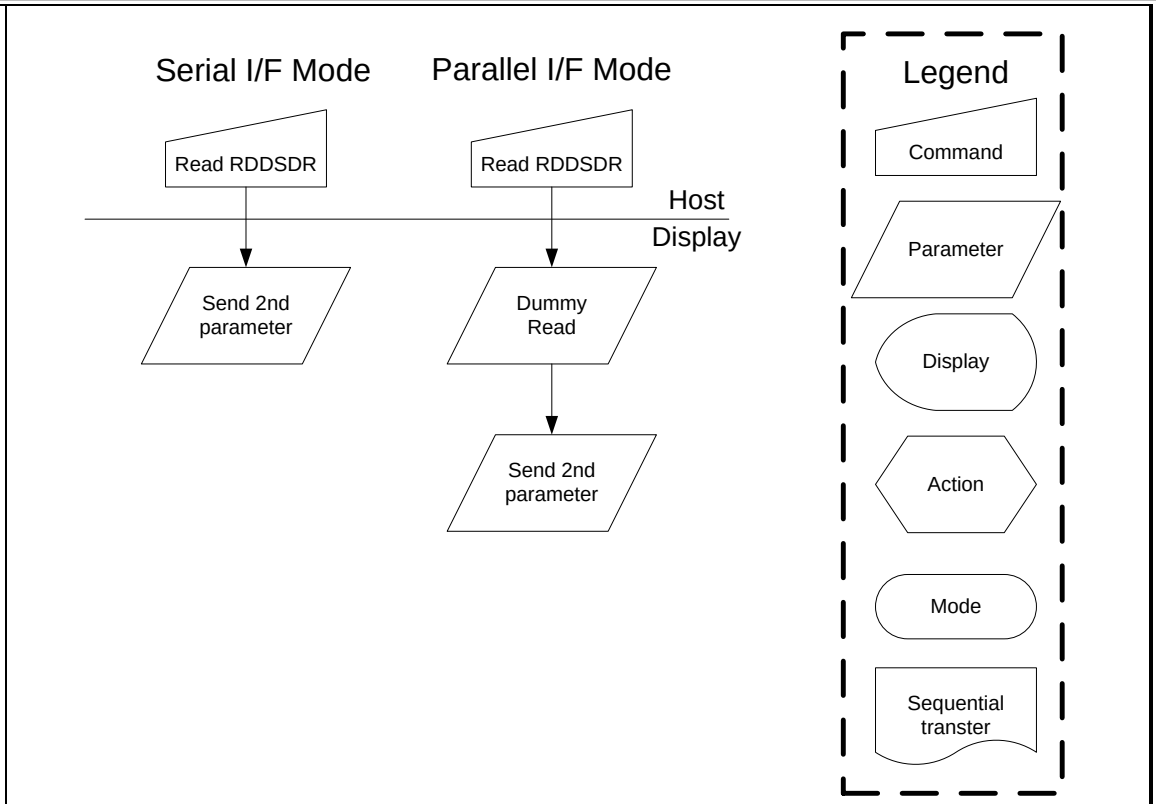
9.2.11 RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDDSDR (Read Display Self-Diagnostic Result)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	0	0	0	0	0	D0	-
Description	This command indicates the current status of the display self-diagnostic result after sleep out command as described below: -D7: Register loading detection -D6: Functionality detection -D0: Checksums Comparison, '0' = Checksums are same , '1' = Checksums are not same See sections: "Read First Checksum (Aah)" and "Read Continue Checksum (Afh)" "-" Don't care												
Restriction	There is one dummy parameter when using Parallel interface.												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000-0000
S/W Reset	0000-0000
H/W Reset	0000-0000

Flow Chart	

9.2.12 SLPIN (10h): Sleep in

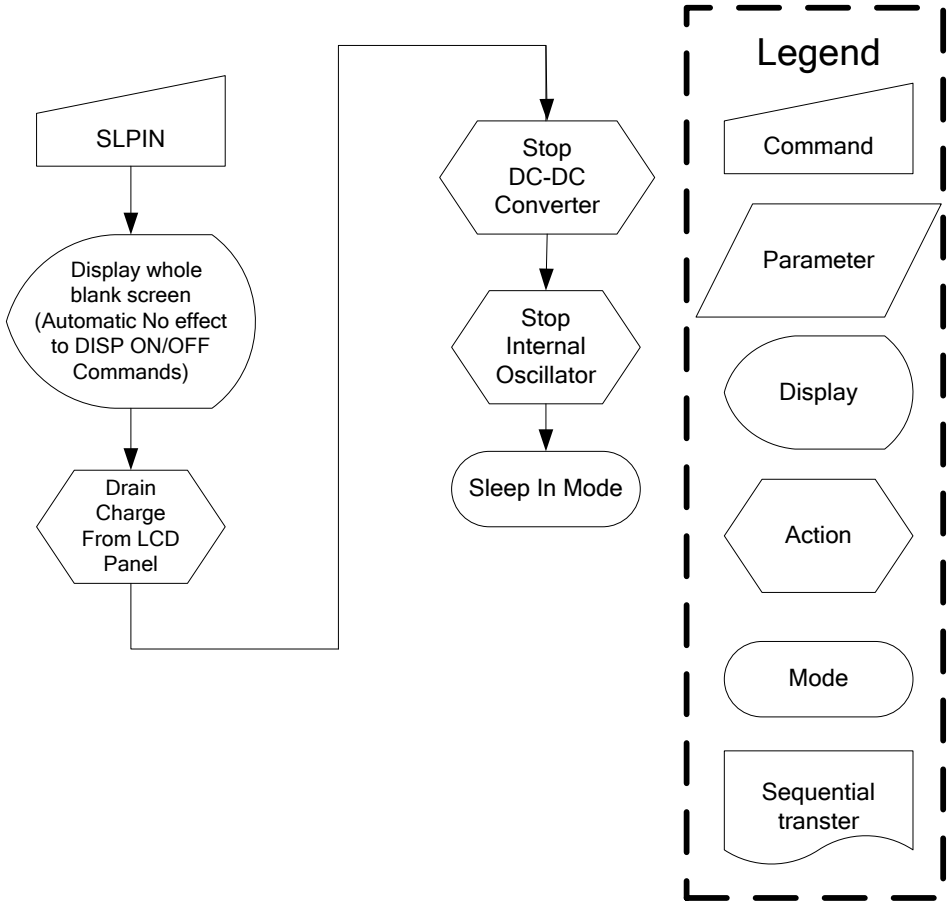
10H	SLPIN (Sleep In)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)
parameter	No Parameter												
Description	-This command causes the LCD module to enter the minimum power consumption mode. -In this mode the DC/DC converter is stopped, internal oscillator is stopped, and panel scanning is stopped. -MCU interface and memory are still working and the memory keeps its contents. -Dimming function does not work when there is changing mode from Sleep OUT to Sleep IN. "-" Don't care												
Restriction	-This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep in mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

Flow Chart

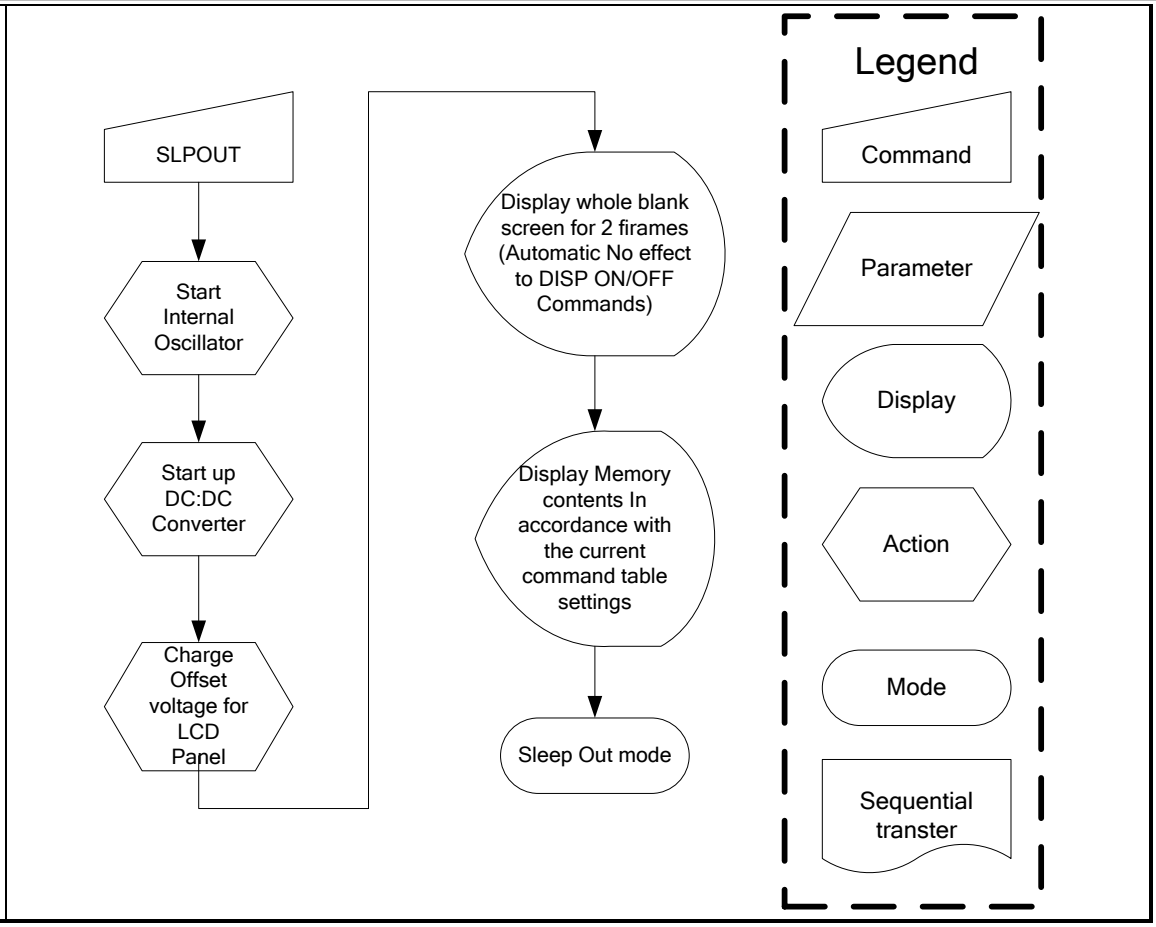


9.2.13 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)

<table>
<tr><td>parameter</td><td>No Parameter</td></tr>
<tr><td>Description</td><td>-This command turn off sleep mode.
-In this mode the DC/DC converter is enabled, internal display oscillator is started, and panel scanning is started.</td></tr>
<tr><td>Restriction</td><td>-This command has no effect when module is already in sleep out mode. Sleep out mode can only be left by the sleep in command (10h).
-It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize.
-It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.
-The display module runs the self-diagnostic functions after this command is received.</td></tr>
<tr><td>Register availability</td><td><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep in mode</td></tr><tr><td>S/W Reset</td><td>Sleep in mode</td></tr><tr><td>H/W Reset</td><td>Sleep in mode</td></tr></table></td></tr>
</table>

Flow Chart



9.2.14 PTLON (12h): Partial Display Mode On

12H	PTLON (Partial Display Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
parameter	No Parameter												
Description	-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h) -To leave Partial mode, the Normal Display Mode On command (13h) should be written. "-" Don't care												
Restriction	This command has no effect when partial mode is active.												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal display mode on
S/W Reset	Normal display mode on
H/W Reset	Normal display mode on

Flow Chart	See Partial Area (30h)

9.2.15 NORON (13h): Normal Display Mode On

12H	NORON (Normal Display Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)
parameter	No Parameter												
Description	-This command turns the display to normal mode. -Normal display mode on means partial mode off. -Exit from NORON by the partial mode on command. "-" Don't care												
Restriction	This command has no effect when normal display mode is active.												
Register availability													

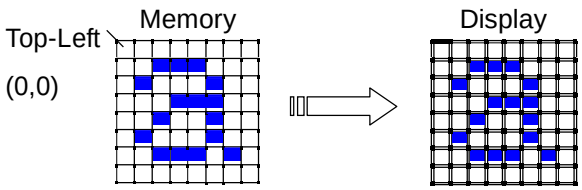
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal display mode on
S/W Reset	Normal display mode on
H/W Reset	Normal display mode on

Flow Chart	See partial area description for details of when to use this command.

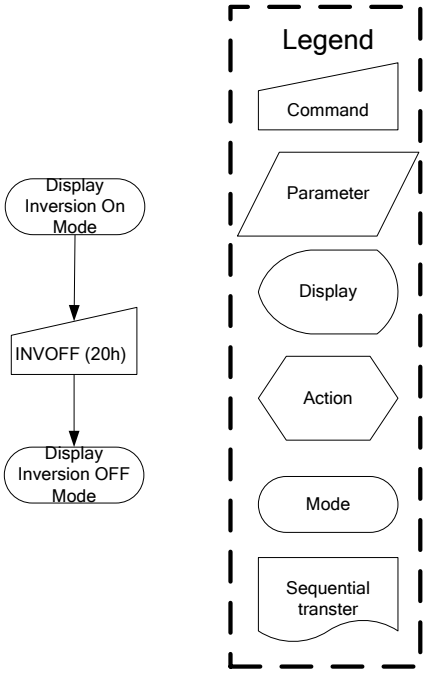
9.2.16 INVOFF (20h): Display Inversion Off

20H	INVOFF (Display Inversion Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
parameter	No Parameter												
Description	*-This command is used to recover from display inversion mode.* *"-" Don't care* (Example)  												
Restriction	This command has no effect when module is already in inversion off mode.												
Register availability													

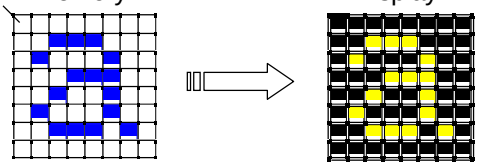
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display inversion off
S/W Reset	Display inversion off
H/W Reset	Display inversion off

Flow Chart	

9.2.17 INVON (21h): Display Inversion On

21H	INVON (Display Inversion On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
parameter	No Parameter												
Description	*-This command is used to recover from display inversion mode.* *"-" Don't care* (Example) Top-Left (0,0) Memory → Display 												
Restriction	This command has no effect when module is already in inversion on mode.												
Register availability													

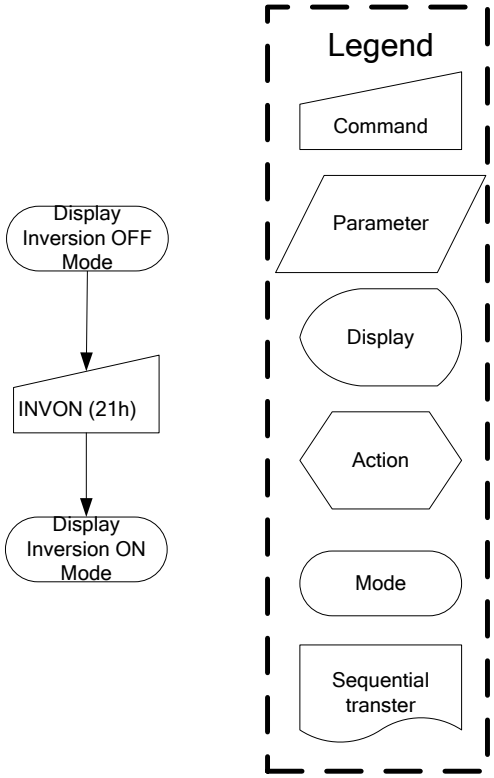
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

		Sleep In	Yes

Default

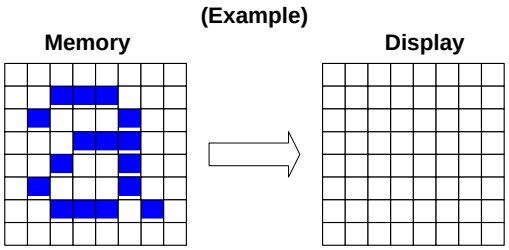
Status	Default Value
Power On Sequence	Display inversion off
S/W Reset	Display inversion off
H/W Reset	Display inversion off

Flow Chart



9.2.18 DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
parameter	No Parameter												
Description	*- This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.* *- This command makes no change of contents of frame memory.* *- This command does not change any other status.* *- There will be no abnormal visible effect on the display.* *- Exit from this command by Display On (29h)*												



Restriction: This command has no effect when module is already in display off mode.

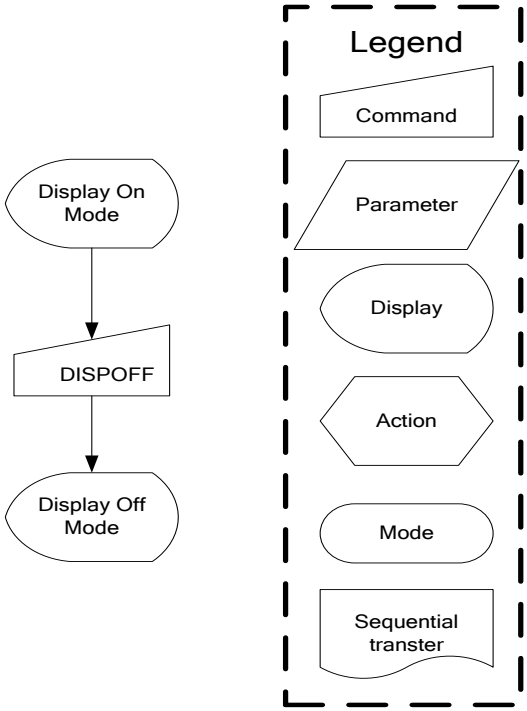
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

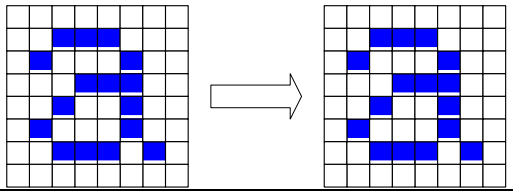
Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



9.2.19 DISPON (29h): Display On

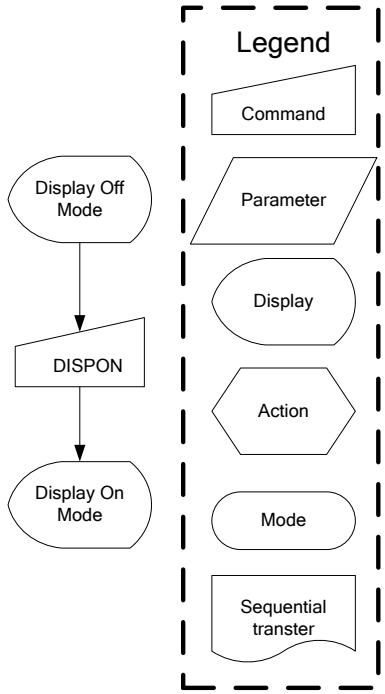
29H	DISPON (Display On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPO N	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)
parameter	No Parameter												
Description	*- This command is used to recover from DISPLAY OFF mode.* *- Output from the Frame Memory is enabled.* *- This command makes no change of contents of frame memory.* *- This command does not change any other status.* **(Example)** **Memory** **Display** 												
Restriction	This command has no effect when module is already in display on mode.												

Register availability

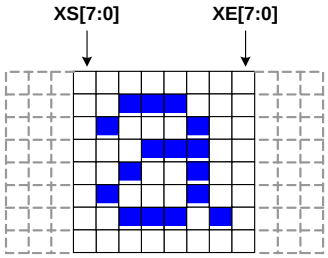
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart	

9.2.20 CASET (2Ah): Column Address Set

2AH	CASET (Column Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)
1st parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
2nd parameter	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
3rd parameter	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
4th parameter	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
1. Description	*-The value of XS [7:0] and XE [7:0] are referred when RAMWR command comes.* -Each value represents one column line in the Frame Memory. 												
Restriction	*XS [15:0] always must be equal to or less than XE [15:0]* *When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.* *(Parameter range: 0 < XS [15:0] < XE [15:0] < =(013Fh)): MV="0")* *(Parameter range: 0 < XS [15:0] < XE [15:0] < =(01DFh)): MV="1")*												

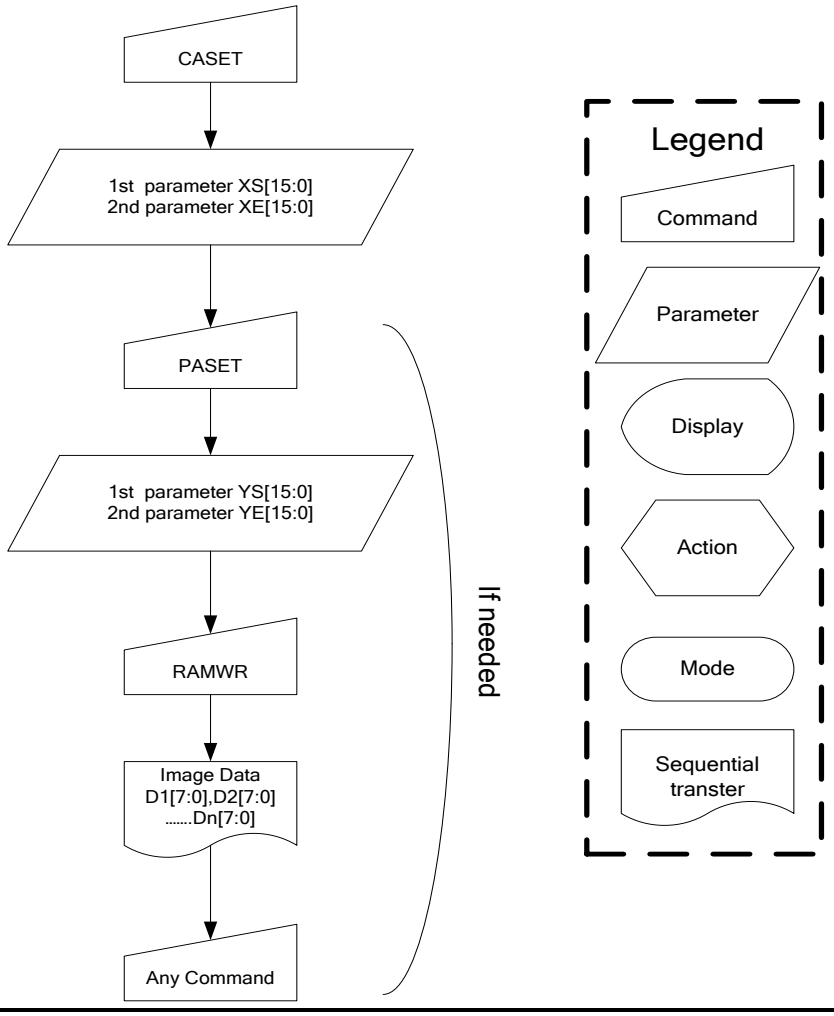
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	XS[15:0]=0x00	XE[15:0]=013F
S/W Reset	XS[15:0]=0x00	When MV=0: XE[15:0]=013Fh, When MV=1: XE[15:0]=01DFh
H/W Reset	XS[15:0]=0x00	XE[15:0]=013F

Flow Chart



9.2.21 RASET (2Bh): Row Address Set

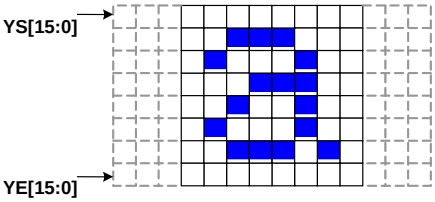
2BH	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1st parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
2nd parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
3rd parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
4th parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

2. Description

-This command is used to defined area of frame memory where MCU can access.

-The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes.

-Each value represents one page line in the Frame Memory.



Restriction

YS [15:0] always must be equal to or less than YE [15:0]

When YS [15:0] or YE [15:0] is greater than maximum address like below, data of out of range will be ignored.

(Parameter range: 0 < YS [15:0] < YE [15:0] < (01DFh)): MV="0")

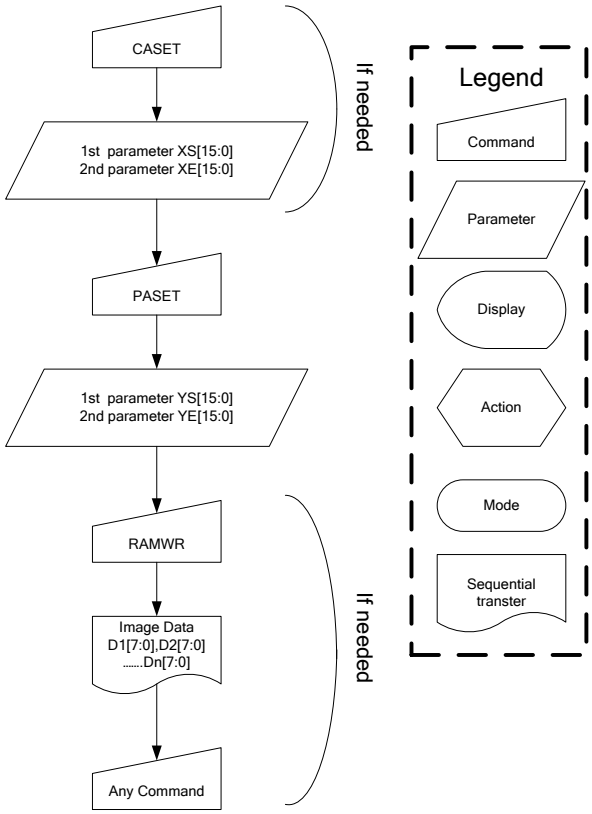
(Parameter range: 0 < YS [15:0] < YE [15:0] < (013Fh)): MV="1")

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	YS[15:0]=0000h	YE[15:0]=01DFh
S/W Reset	YS[15:0]=0000h	When MV=0: YE[15:0]=01DFh, When MV=1: YE[15:0]=013Fh

	H/W Reset | YS[15:0]=0000h | YE[15:0]=01DFh
Flow Chart	

9.2.22 RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1st parameter	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
…	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
N parameter	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	
Description	*-This command is used to transfer data from MCU to frame memory.* *-When this command is accepted, the column register and the page register are reset to the start column/start page positions.* *-The start column/start page positions are different in accordance with MADCTL setting.* *-Sending any other command can stop frame write.*												

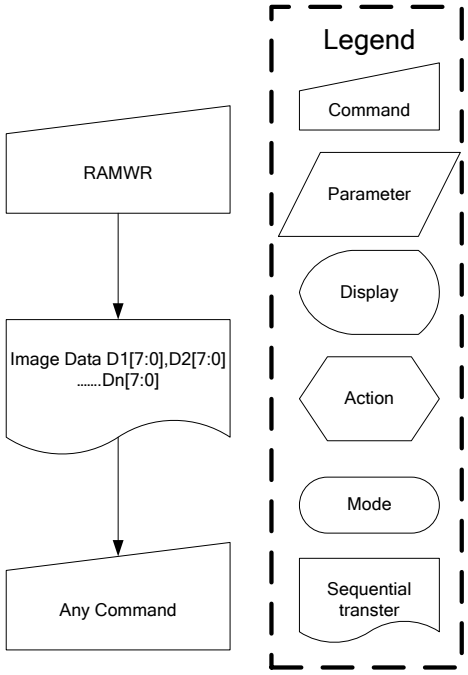
Restriction	*In all color modes, there is no restriction on length of parameters.*
Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



9.2.23 RAMRD (2Eh): Memory Read

2EH	RAMRD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	

:	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
(N+1)th parameter	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	

Description

-This command is used to transfer data from frame memory to MCU.

-When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.

-The Start Column/Start Row positions are different in accordance with MADCTL setting.

-Then D[17:0] is read back from the frame memory and the column register and the row register incremented

-Frame Read can be cancelled by sending any other command.

Restriction

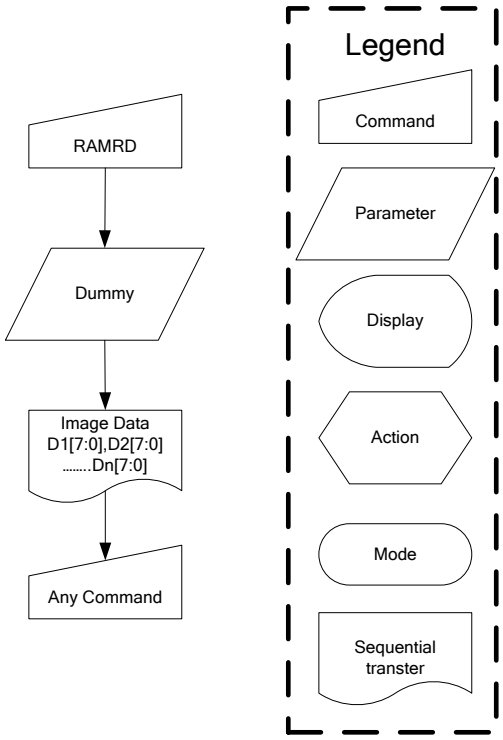
There is no restriction on length of parameters.

Register availability

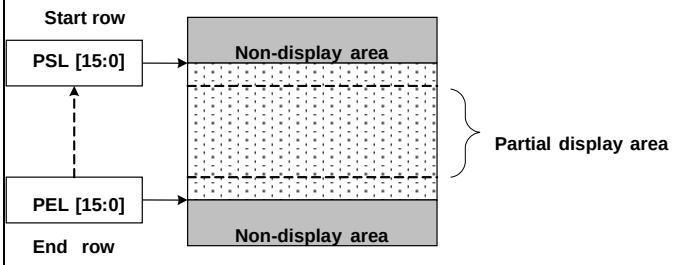
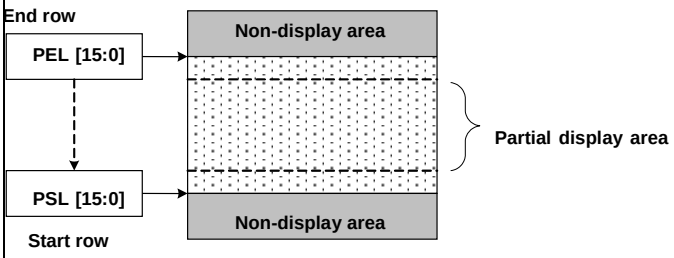
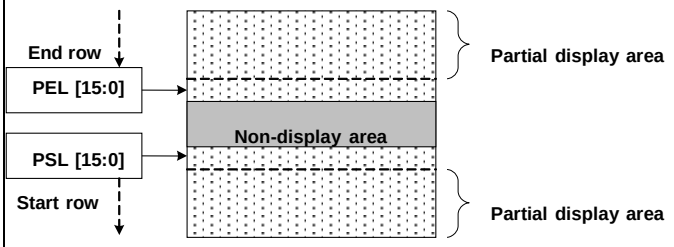
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart	

9.2.24 PTLAR (30h): Partial Area

30H	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1st parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	
2nd parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
3rd parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
4th parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	
Description	*-This command defines the partial mode's display area.* *-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.* *-If End Row > Start Row, when MADCTL ML='0'*  *-If End Row > Start Row, when MADCTL ML='1'*  *-If End Row < Start Row, when MADCTL ML='0'*  *-If End Row = Start Row then the Partial Area will be one row deep.*												
Restriction	*Each detail initial value by the display resolution will be updated.*												

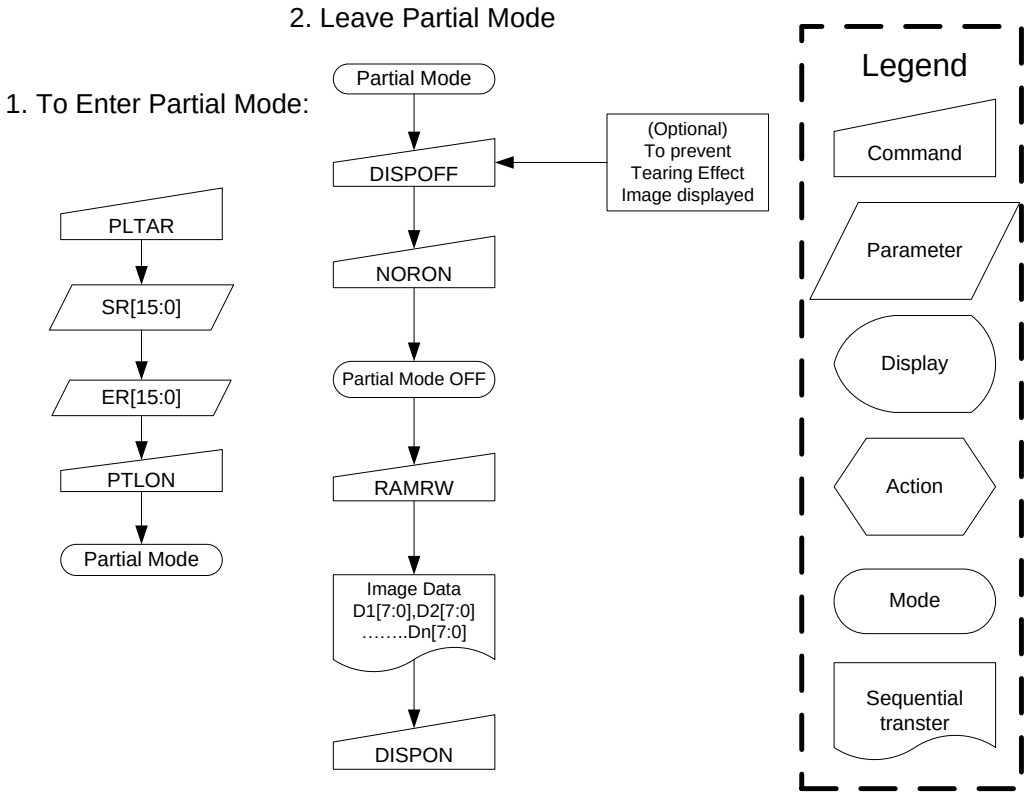
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	PSL[15:0]=0000h, PEL=01DFh
S/W Reset	PSL[15:0]=0000h, PEL=01DFh
H/W Reset	PSL[15:0]=0000h, PEL=01DFh

Flow Chart



9.2.25 VSCRDEF (33h): Vertical Scrolling Definition

33H	(Vertical Scrolling Definition)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)
1st parameter	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	
2nd parameter	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	
3rd parameter	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	
4th parameter	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
5th parameter	1	↑	1		BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	
6th parameter	1	↑	1		BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	

Description

-This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll

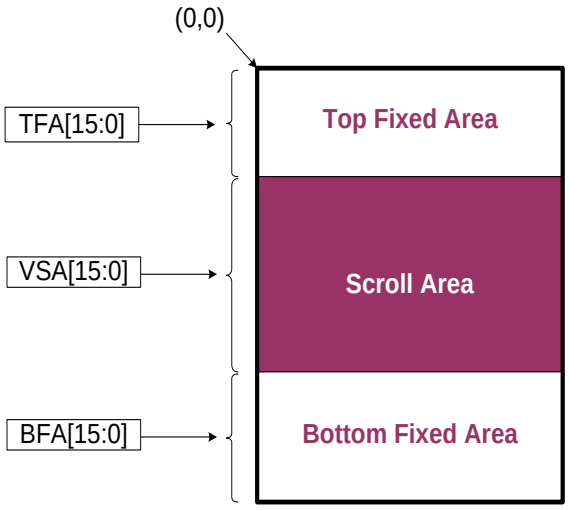
-When MADCTL MV=0

-The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

-The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area.

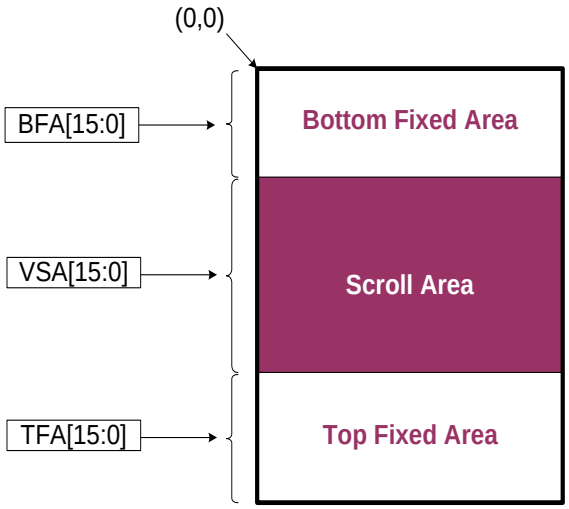
-The 4th & 5th parameter BFA [6:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer



-When MADCTL MV=1

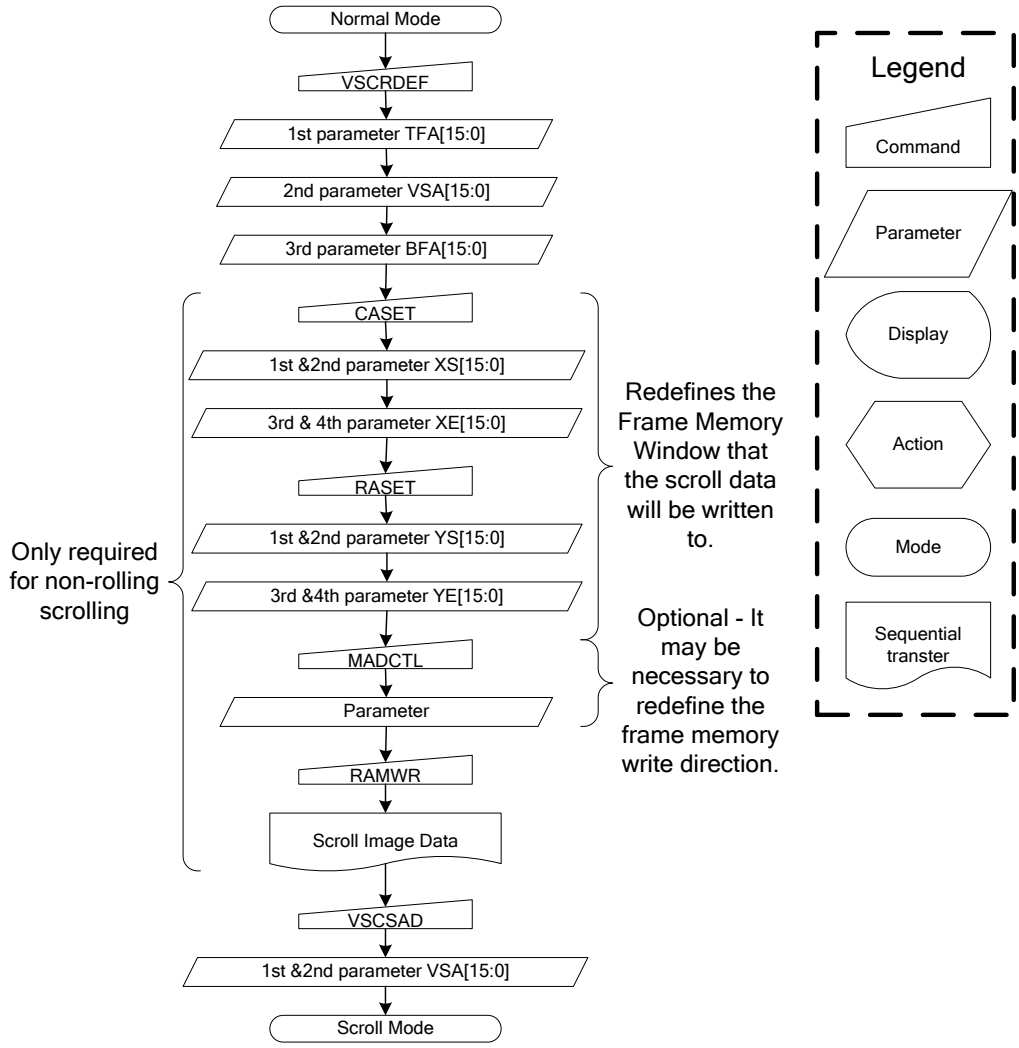
-The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display)

	-The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area. *-The 4th & 5th parameter BFA [6:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).* 
Restriction	*The sum of TFA, VSA and BFA must equal the number of the display device's horizontal lines (pages), otherwise Scrolling mode is undefined.* *In Vertical Scrolling Mode, MADCTL parameter MV should be set to '0' – this only affects the Frame Memory write.*
Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
Power On Sequence	TFA[15:0] = 0000h	VSA[0:15] = 01E0h	BFA[15:0] = 0000h
S/W Reset	TFA[15:0] = 0000h	VSA[0:15] = 01E0h	BFA[15:0] = 0000h
H/W Reset	TFA[15:0] = 0000h	VSA[0:15] = 01E0h	BFA[15:0] = 0000h

Flow Chart	1. TO Enter Vertical Scroll Mode: 

9.2.26 TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
parameter	No Parameter												
Description	*-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.*												
Restriction	This command has no effect when tearing effect output is already off..												
Register availability													

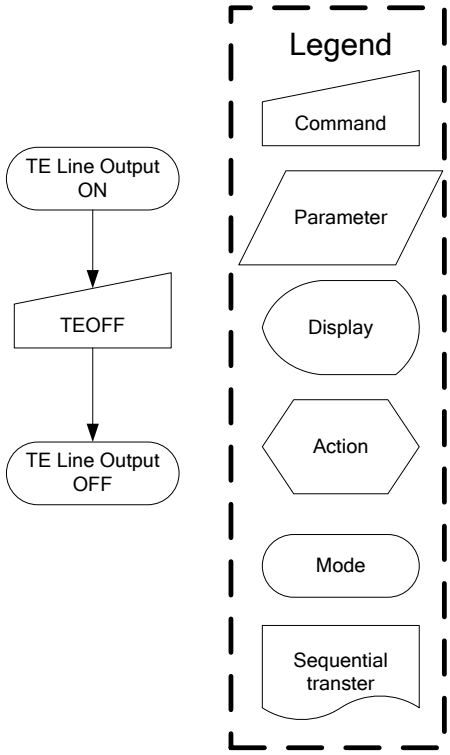
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes

		Normal Mode On, Idle Mode On, Sleep Out	Yes
		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes

Default

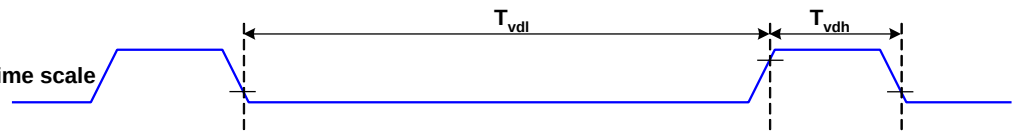
Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart

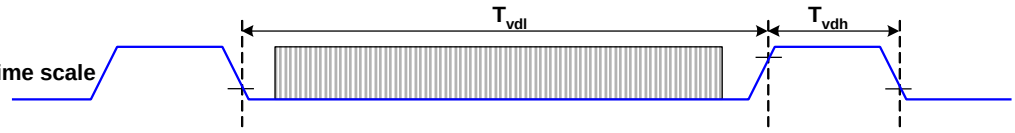


9.2.27 TEON (35h): Tearing Effect Line On

35H	TEON (Tearing Effect Line On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
parameter	1	↑	1	-	0	0	0	0	0	0	0	TEM	
Description	*-This command is used to turn ON the Tearing Effect output signal from the TE signal line.* *-This output is not affected by changing MADCTL bit ML.* *-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line:* -When TEM ='0': The Tearing Effect output line consists of V-Blanking information only												



-When TEM ='1': The Tearing Effect output Line consists of both V-Blanking and H-Blanking information



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction	*This command has no effect when tearing effect output is already on.*

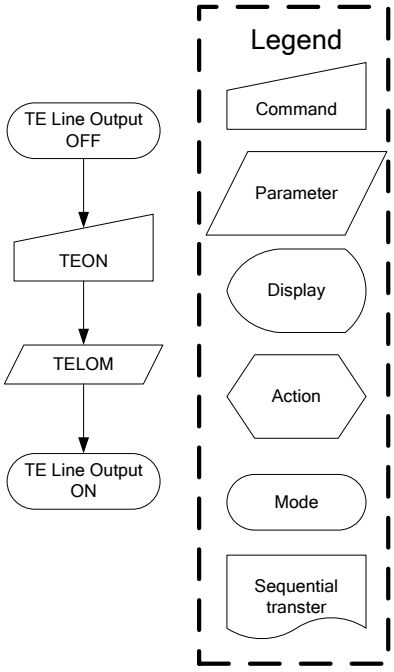
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



9.2.28 MADCTL (36h): Memory Data Access Control

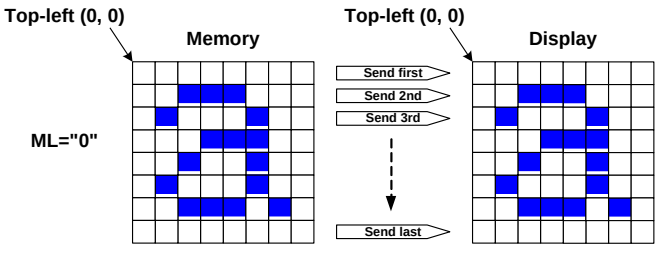
36H	MADCTL (Memory Data Access Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)
parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-	

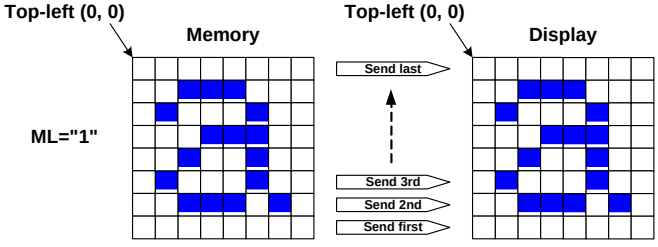
Description

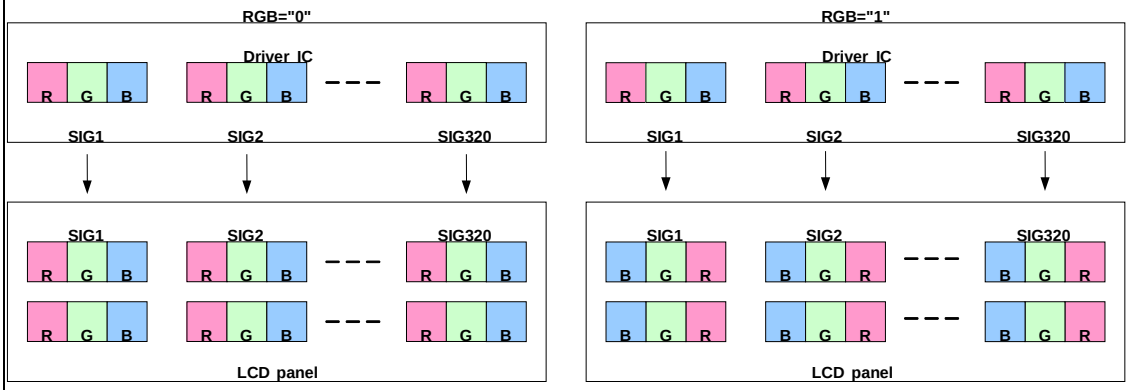
-This command defines read/ write scanning direction of frame memory.

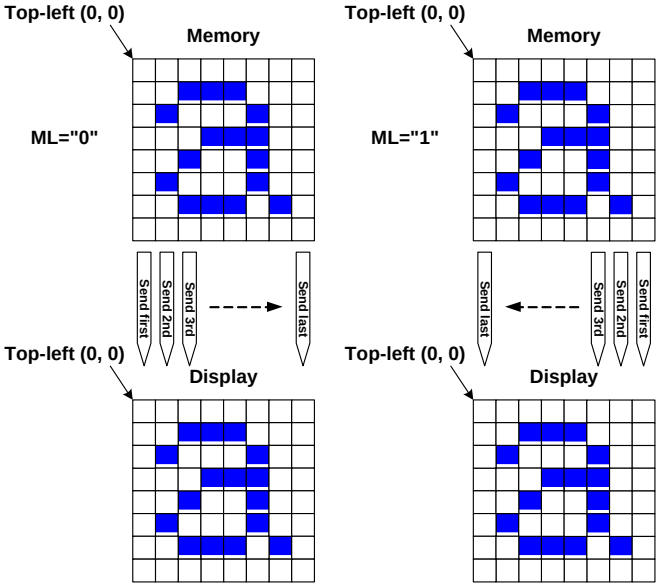
-Bit Assignment

Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3bits controls MCU to memory write/read direction.
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel
MH	Horizontal Refresh Order	Horizontal direction '0' = Left to Right '1' = Right to Left





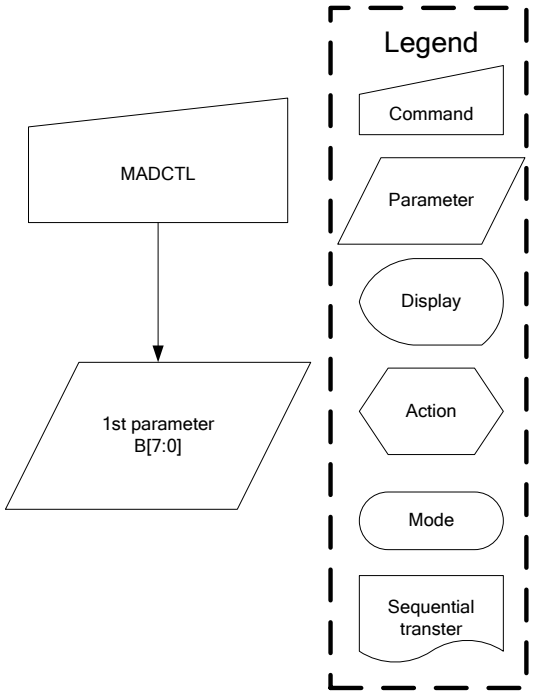




Restriction

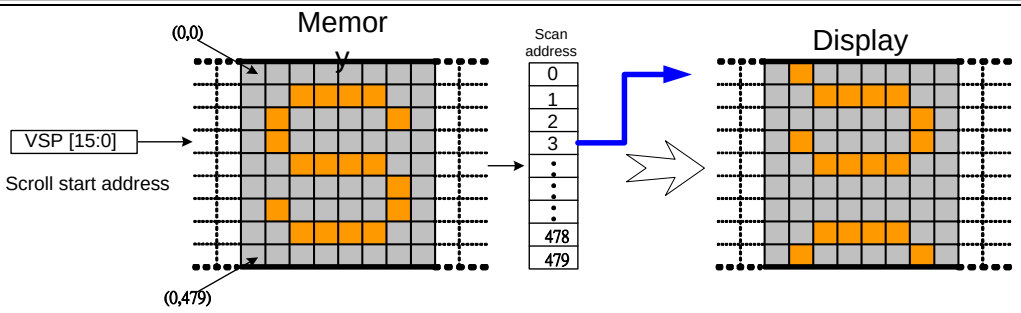
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>S/W Reset</td><td>No change</td></tr><tr><td>H/W Reset</td><td>0000h</td></tr></table>
Flow Chart	

9.2.29 VSCSAD (37h): Vertical Scroll Start Address of RAM

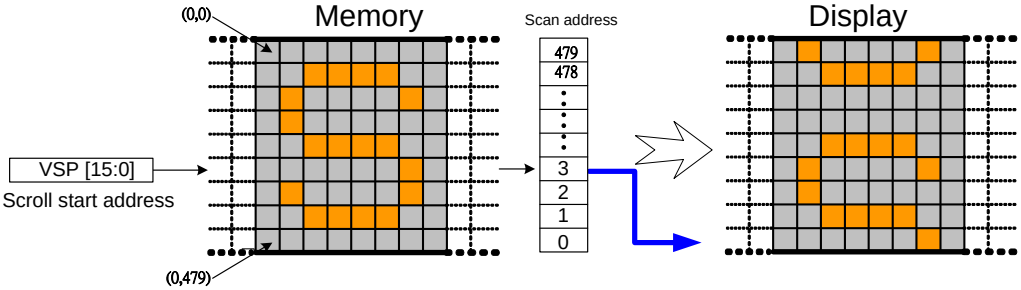
37H	VSCSAD (Vertical Scroll Start Address of RAM)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
1ST parameter	1	↑	1	-	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8	
2ND parameter	1	↑	1	-	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	
Description	*-This command is used together with Vertical Scrolling Definition (33h).* *-These two commands describe the scrolling area and the scrolling mode.* *-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:* *When ML=0* *Example:* *When Top Fixed Area = Bottom Fixed Area = 00, vertical Scrolling Area = 480 and VSP = '3'*												



When ML=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, vertical Scrolling Area = 480 and VSP = '3'



NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

VSP refers to the Frame Memory line Pointer

Restriction	*Since the value of the vertical scrolling start address is absolute (with reference to the frame memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)- otherwise undesirable image will be displayed on the panel)*

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	See Vertical Scrolling Definition (33h) description

9.2.30 IDMOFF (38h): Idle Mode Off

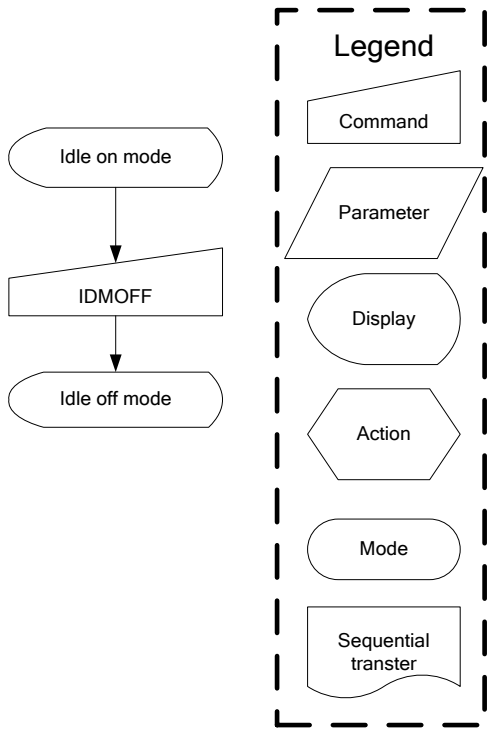
38H	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
parameter	No Parameter												
Description	*-This command is used to recover from Idle mode on.* *-In the idle off mode,* *1. LCD can display 65k, 262k or 16M colors.* *2. Normal frame frequency is applied.*												
Restriction	This command has no effect when module is already in idle off mode												

Register availability

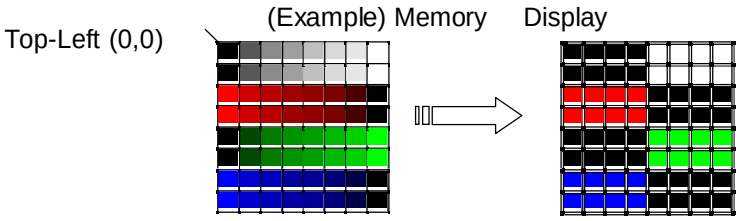
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode off
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Flow Chart	

9.2.31 IDMON (39h): Idle mode on

39H	IDMON (Idle Mode On)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)
parameter	No Parameter												
Description	*-This command is used to enter into Idle mode on.* *-There will be no abnormal visible effect on the display mode change transition.* *-In the idle on mode,* *1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.* *2. 8-Color mode frame frequency is applied.* *3. Exit from IDMON by Idle Mode Off (38h) command* 												

Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0
Black	0xxxxx	0xxxxx	0xxxxx
Blue	0xxxxx	0xxxxx	1xxxxx
Red	1xxxxx	0xxxxx	0xxxxx
Magenta	1xxxxx	0xxxxx	1xxxxx
Green	0xxxxx	1xxxxx	0xxxxx
Cyan	0xxxxx	1xxxxx	1xxxxx
Yellow	1xxxxx	1xxxxx	0xxxxx
White	1xxxxx	1xxxxx	1xxxxx

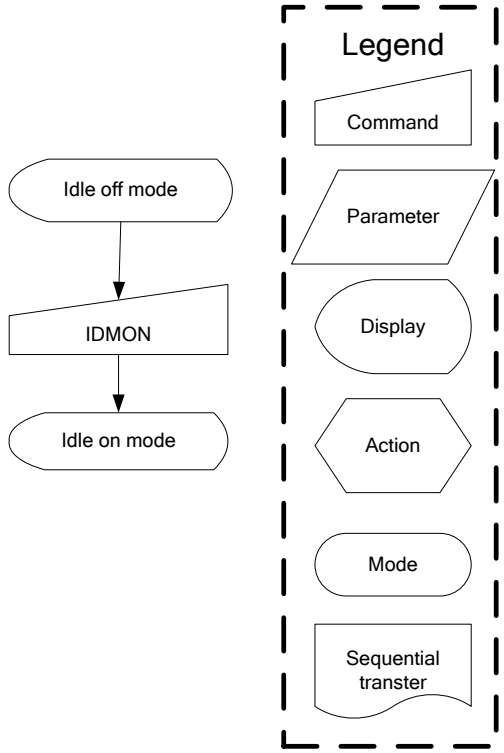
Restriction: This command has no effect when module is already in idle off mode

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode off
S/W Reset	Idle mode off
H/W Reset	Idle mode off

Flow Chart	

9.2.32 COLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (Interface Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
1st Parameter	1	↑	1	-	0	D6	D5	D4	0	D2	D1	D0	

Description

This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:

1st parameter:

Bit	Description	
D7	-	Set to '0'
D6	RGB interface color format	'101' = 16bit/pixel
D5		'110' = 18bit/pixel
D4		'111' = 24bit/pixel
D3	-	Set to '0'
D2	Control interface color format	'101' = 16bit/pixel
D1		'110' = 18bit/pixel
D0		'111' = 24 bit/pixel

Restriction

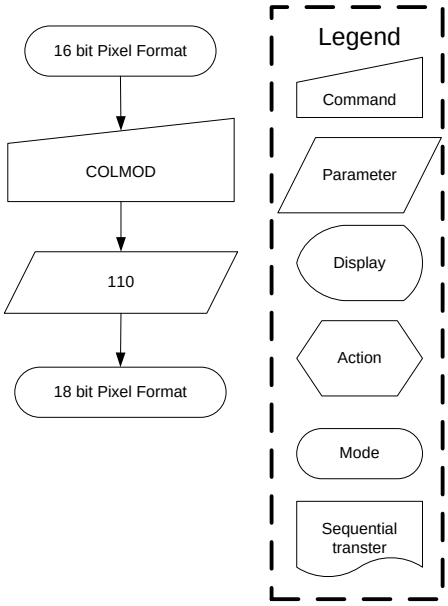
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	18bit/pixel
S/W Reset	No change
H/W Reset	18bit/pixel

Flow Chart



9.2.33 WRMEMC (3Ch): Write Memory Continue

3CH	WRMEMC (Write Memory Continue)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRMEMC	0	↑	1	-	0	0	1	1	1	1	0	0	(3Ch)
1ST parameter	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
⋮	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
Nth parameter	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	
Description	*-This command transfers image data from the host processor to the display module's frame memory continuing from*												

the pixel location following the previous write memory continue or memory write command.

-If MV=0:

Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)(YE-YS+1) the extra pixels are ignored.*

If MV=1:

Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are written to the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)(YE-YS+1) the extra pixels are ignored.*

Condition	Column	Page
Command 2C/2E is accepted	Return to “Start Column”	Return to “Start Page”
Read/Write RAM action	Increment by 1	No change
Column value is large than “End Column”	Return to “Start Column”	Increment by 1
Page value is large than “End Page”	Return to “Start Column”	Return to “Start Page”

Restriction

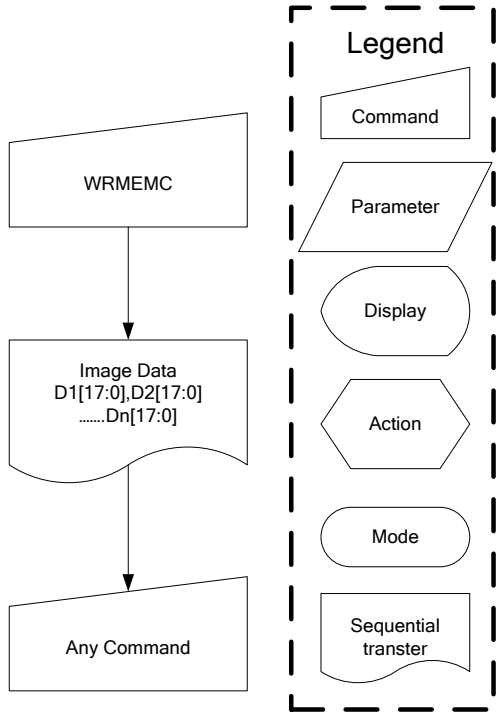
A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart	

9.2.34 RDMEMC (3Eh): Read Memory Continue

3EH	RDMEMC (Read Memory Continue)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDMEMC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)
1ST parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	
⋮	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	
Nth parameter	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	
Description	*-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous read memory continue or memory read command.* *-If MV=0:* *Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are read from the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command.* *If MV=1:* *Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The page register is then incremented and pixels are read from the frame memory until the page register*												

equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are read from the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command.

Condition	Column	Page
Command 2C/2E is accepted	Return to “Start Column”	Return to “Start Page”
Read/Write RAM action	Increment by 1	No change
Column value is large than “End Column”	Return to “Start Column”	Increment by 1
Page value is large than “End Page”	Return to “Start Column”	Return to “Start Page”

Restriction

Regardless of the color mode set in interface pixel format, the pixel format returned by read memory continue is always 18-bit so there is no restriction on the length of data

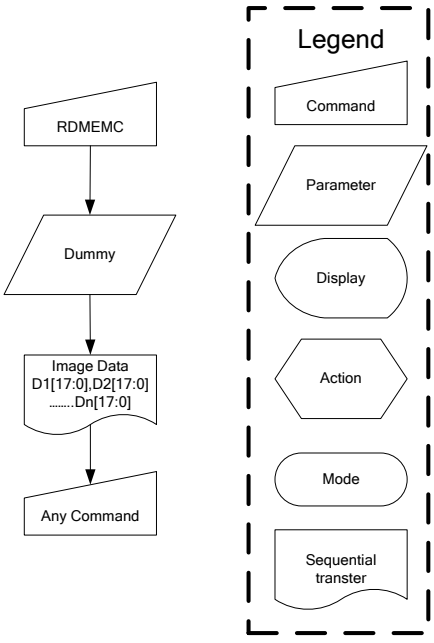
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



9.2.35 STE (44h): Set Tear Scanline

44H	STE (Set Tear ScanLine)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
STE	0	↑	1	-	0	1	0	0	0	1	0	0	(44h)
1st parameter	1	↑	1	-	N15	N14	N13	N12	N11	N10	N9	N8	
2nd parameter	1	↑	1	-	N7	N6	N5	N4	N3	N2	N1	N0	

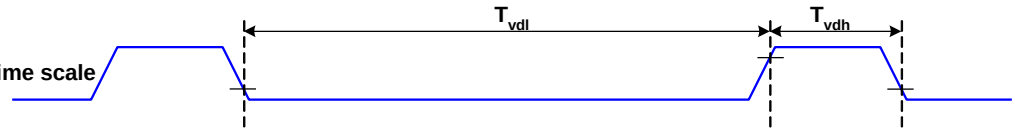
Description

-This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MV.

-The tearing effect line on has one parameter that describes the tearing effect output line mode.

-The tearing effect output line consist of V-blanking information only.

Vertical time scale



Note that set tear scanline with N=0 is equivalent to tearing effect line on with TEM=0.

The tearing effect output line shall be active low when the display module is in sleep mode

Restriction

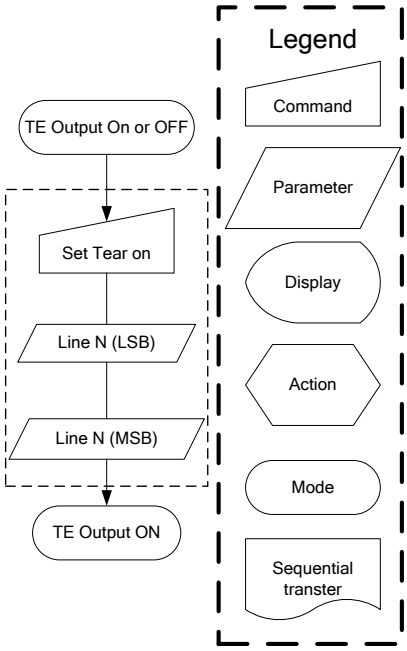
This command takes affect on the frame following the current frame. Therefore, if the tear effect (TE) output is already on, the TE output shall continue to operate as programmed by the previous tearing effect line on or set tear scanline command until the end of the frame

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

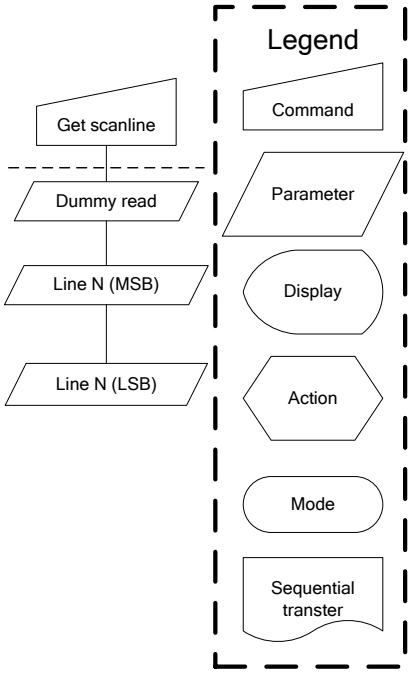
Flow Chart	

9.2.36 GSCAN (45h): Get Scanline

45H	GSCAN (Get ScanLine)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GSCAN	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	N15	N14	N13	N12	N11	N10	N9	N8	
3rd parameter	1	1	↑	-	N7	N6	N5	N4	N3	N2	N1	N0	
Description	*-The display module returns the current scanline ,N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.* *-When in sleep in mode, the value returned by get scanline is undefined.* *Note: that Set Tear Scan Line with N = 0 is equivalent to Tearing Effect Line ON with M = 0.*												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0000h</td></tr><tr><td>S/W Reset</td><td>0000h</td></tr><tr><td>H/W Reset</td><td>0000h</td></tr></table>
Flow Chart	

9.2.37 WRDISBV (51h): Write Display Brightness

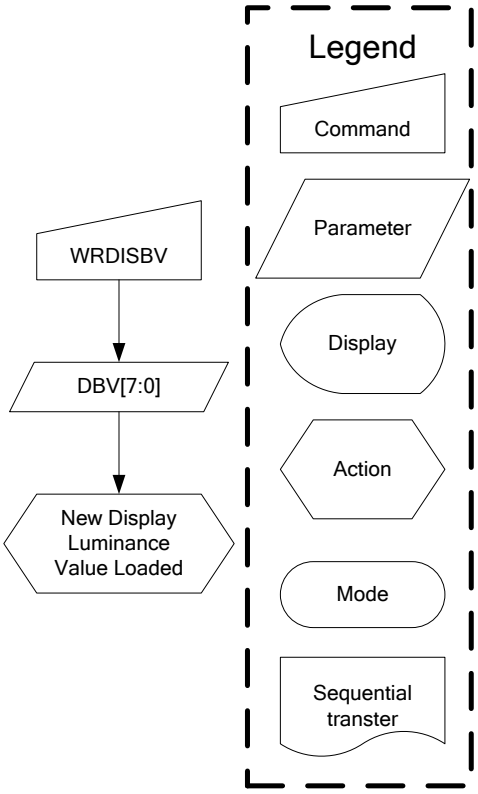
51H	WRDISBV (Write Display Brightness)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)
Parameter	1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	
Description	*-This command is used to adjust the brightness value of the display.* *-It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification.* *-In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.*												
Restriction													
Register availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr></table>												

		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



9.2.38 RDDISBV (52h): Read Display Brightness Value

52H	RDDISBV (Read Display Brightness Value)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	
Description	*-This command returns the brightness value of the display.* *-It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is.*												

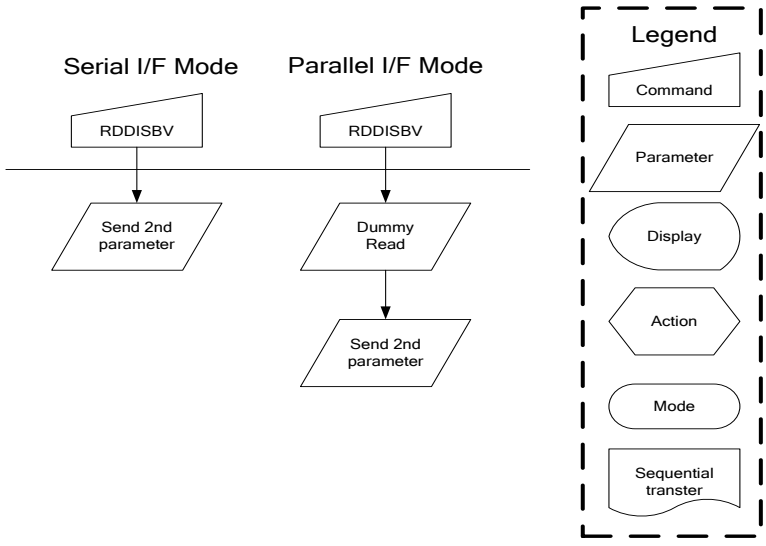
	-In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. *-DBV[7:0] is reset when display is in sleep in mode.* *-DBV[7:0] is '0' when bit BCTRL of write CTRL display command (53h) is '0'* *-DBV[7:0] is manual set brightness specified with write CTRL display command (53h) when bit BCTRL is '1'*
Restriction	-
Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



9.2.39 WRCTRLD (53h): Write CTRL Display

53H	WRCTRLD (Write CTRL Display)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)
Parameter	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0	

<table>
<tr><td>Description</td><td>

-This command is used to control display brightness.

*-**BCTRL**: Brightness Control Block On/Off, This bit is always used to switch brightness for display.*

0 = Off (Brightness register are 00h, DBV[7:0])

1 = On (Brightness register are active, according to the other parameters.)

*-**DD**: Display Dimming (Only for manual brightness setting)*

DD = 0: Display Dimming is off.

DD = 1: Display Dimming is on.

*-**BL**: Backlight Control On/Off*

0 = Off (Completely turn off backlight circuit. Control lines must be low.)

1 = On

-Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1.

-When BL bit changed from 'on' to 'off', backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.

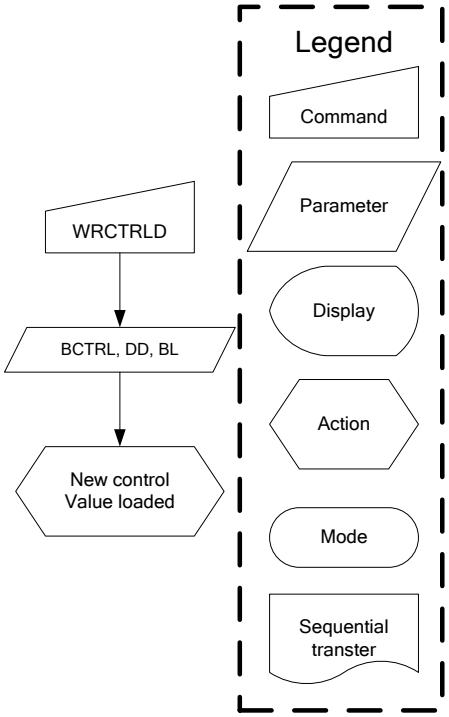
</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register availability</td><td>

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

</td></tr>
<tr><td>Default</td><td>

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

</td></tr>
</table>

Flow Chart	

9.2.40 RDCTRLD (54h): Read CTRL value Display

54H	RDCTRLD (Read CTRL value Display)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0	
Description	*-This command returns ambient light and brightness control values..* *-BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.* *0 = Off* *1 = On* *-DD: Display Dimming (Only for manual brightness setting)* *DD = 0* *DD = 1* *-BL: Backlight Control On/Off* *0 = Off* *1 = On*												

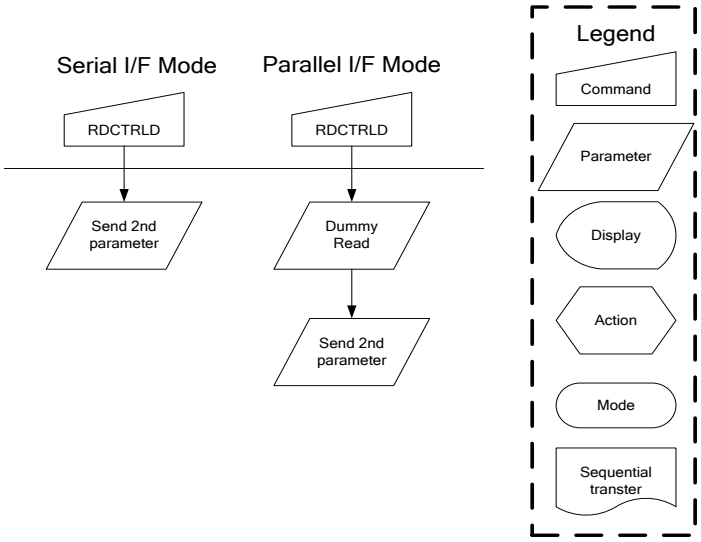
Restriction	-
Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



9.2.41 WRCABC (55h): Write Adaptive Brightness Control

55H	WRCABC (Write Adaptive Brightness Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCABC	0	↑	1	-	0	1	0	1	0	1	0	1	(55h)
Parameter	1	↑	1	-	CECTRL	0	CE1	CE0	0	0	C1	C0	

Description

-This command is used to set parameters for image content based adaptive brightness control functionality.

-There is possible to used 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	*C0*	*Function*

	0	*0*	*Off*
	0	*1*	*User Interface Mode*
	1	*0*	*Still Picture*
	1	*1*	*Moving Image*

-CECTRL: Color Enhancement Control Bit:

CECTRL=0: Color Enhancement Off.

CECTRL=1: Color Enhancement On.

-There are three color enhancement levels can be set.

CE1	*CE0*	*Color enhancement level*
0	*0*	*Low enhancement*
0	*1*	*Medium enhancement*
1	*1*	*High enhancement*

'-': Don't care

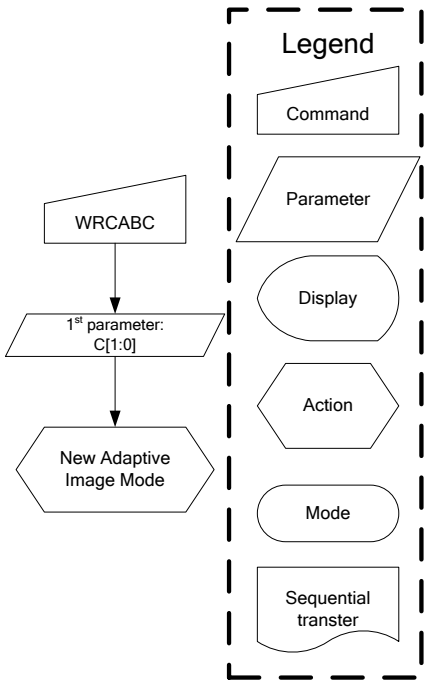
Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	

9.2.42 RDCABC (56h): Read Content Adaptive Brightness Control

56H	RDCABC (Read Content Adaptive Brightness Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	(56h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	0	0	0	0	0	0	C1	C0	

Description

-This command is used to read the settings for image content based adaptive brightness control functionality.

-There is possible to used 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	*C0*	*Function*
0	*0*	*Off*
0	*1*	*User Interface Mode*
1	*0*	*Still Picture*
1	*1*	*Moving Image*

'-': Don't care

Restriction: -

Register availability

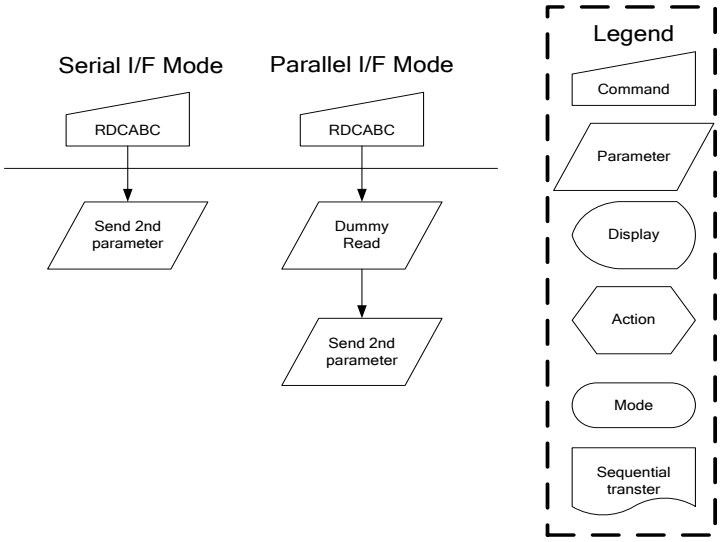
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes

		Normal Mode On, Idle Mode On, Sleep Out	Yes
		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



9.2.43 WRCABCMB (5Eh): Write CABC Minimum Brightness

5EH	WRCABCMB (Write CABC Minimum Brightness)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCABCMB	0	↑	1	-	0	1	0	1	1	1	1	0	(5Eh)
Parameter	1	↑	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	
Description	*-This command is used to set the minimum brightness value of the display for CABC function.* *-In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the brightness for CABC.* *'-': Don't care*												
Restriction													

Register availability

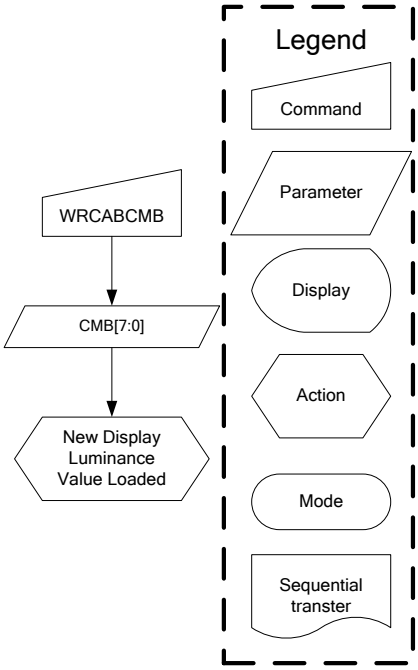
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes

		Normal Mode On, Idle Mode On, Sleep Out	Yes
		Partial Mode On, Idle Mode Off, Sleep Out	Yes
		Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



9.2.44 RDCABCMB (5Fh): Read CABC Minimum Brightness

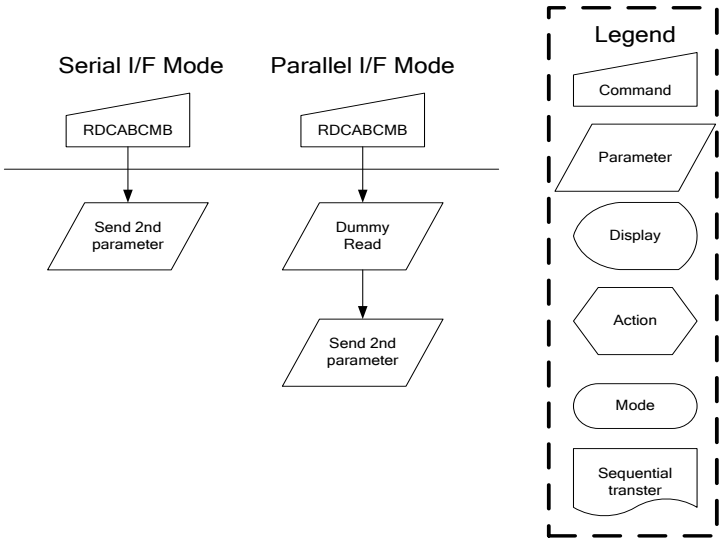
5FH	RDCABCMB (Read CABC Minimum Brightness)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCABCMB	0	↑	1	-	0	1	0	1	1	1	1	1	(5Fh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	
Description	*-This command returns the minimum brightness value of CABC function.* *-In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the brightness for CABC.* *'-': Don't care*												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart	

9.2.45 RDFCS (Aah): Read First Checksum

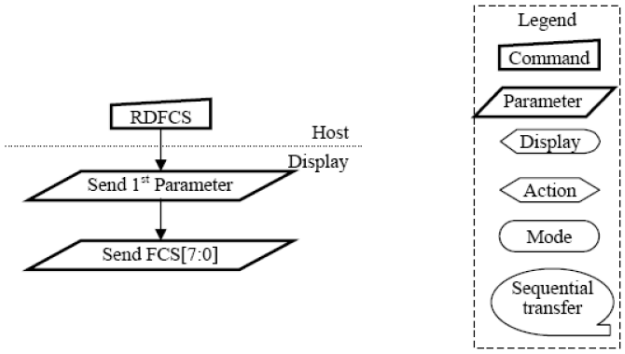
AAH	RDFCS (Read First Checksum)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	-	1	0	1	0	1	0	1	0	(Aah)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	FCS[7:0]								
Description	*- This command returns the first checksum what has been calculated from User's area registers and the frame memory after the write access to those registers and/or frame memory has been done.* *X = can be '0' or '1'*												
Restriction	*It will be necessary to wait 150ms after there is the last write access on User area registers before there can read this checksum value.*												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

9.2.46 RDCFCS (Afh): Read Continue Checksum

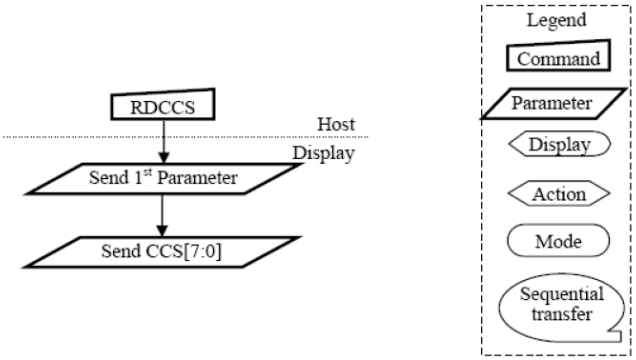
AFH	RDCFCS (Read Continue Checksum)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	-	1	0	1	0	1	1	1	1	(Afh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑		CCS[7:0]								
Description	*- This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from User's area registers and the frame memory after the write access to those registers and/or frame memory has been done.* *X = can be '0' or '1'*												
Restriction	*It will be necessary to wait 300ms after there is the last write access on User area registers before there can read this checksum value in the first time..*												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
H/W Reset	00h

Flow Chart	

9.2.47 RDID1 (Dah): Read ID1

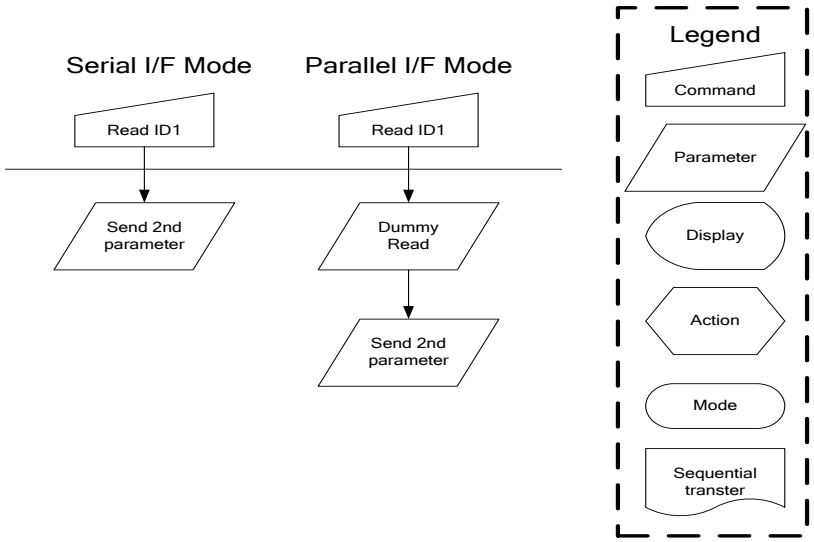
DAH	RDID1 (Read ID1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(Dah)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	FFh
Description	-*This read byte identifies the LCD module's manufacturer.* *'-': Don't care.*												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

Flow Chart	

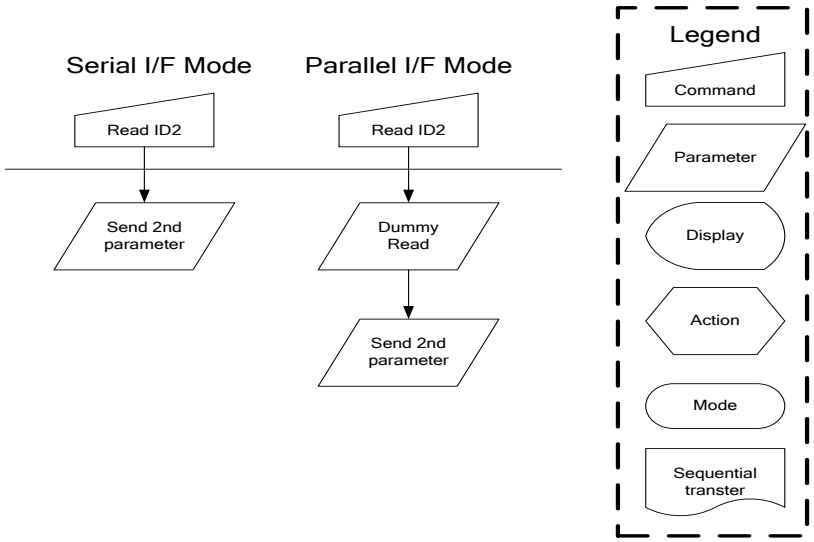
9.2.48 RDID2 (DBh): Read ID2

DBH	RDID2 (Read ID2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	FFh
Description	*This read byte is used to track the LCD module/driver IC version.* *'-': Don't care.*												
Restriction	-												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

Flow Chart	

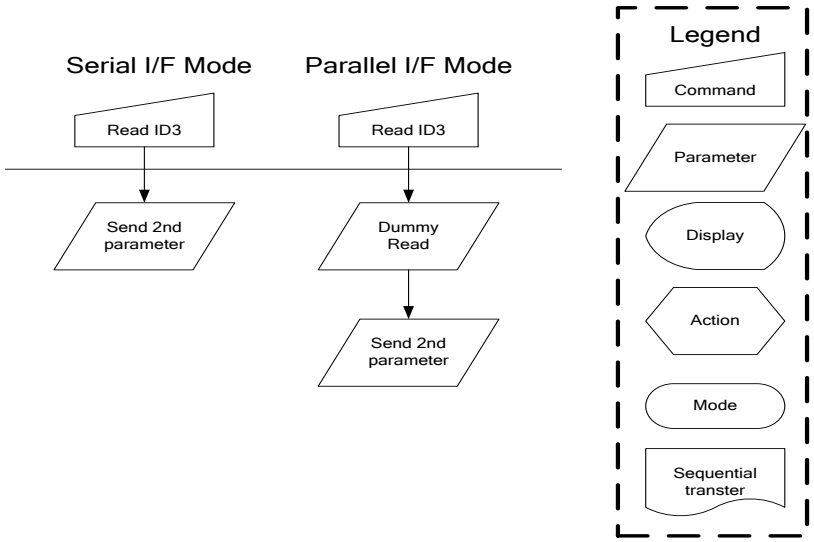
9.2.49 RDID3 (DCh): Read ID3

DCH	RDID3 (Read ID3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	FFh
Description	*This read byte identifies the LCD module/driver.* *'-': Don't care.*												
Restriction	-												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

Flow Chart	

9.3.. Command Table 2

9.3.1 IFMODE (B0h): Interface Mode Control

B0H	IFMODE (Interface Mode Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IFMODE	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)
1st parameter	1	↑	1	-	SPI_EN	0	0	0	VSCP	HSCP	PKP	DEP	00h
Description	*Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.* *DEP: DE polarity ("0"= High enable for RGB interface, "1"=Low enable for RGB interface)* *PKP: PCLK polarity set ("0"=data fetched at the rising time, "1"=data fetched at the falling time)* *HSCP: HSYNC polarity ("0"=Low level sync clock, "1"=High level sync clock)* *VSCP: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)* *SPI_EN: 3/4 wire serial interface selection* *SPI_EN = "0", DIN and DOUT pins are used for 3/4 wire serial interface.* *SPI_EN = "1", DIN/SDA pin is used for 3/4 wire serial interface and DOUT pin is not used.* *'-': Don't care.*												
Restriction	-												
Register availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

		Sleep In	Yes
Default			

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	

9.3.2 FRMCTR1 (B1h): Frame Rate Control (In Normal Mode/Full Colors)

B1H	FRMCTR1 (Frame Rate Control In Normal Mode/Full Colors)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1st parameter	1	↑	1	-	FRS[3:0]				0	0	DIVA[1:0]		A0h
2nd parameter	1	↑	1	-	0	0	0	RTNA[4:0]					10h

Description

FRS[3:0]: Sets the frame frequency of full color normal mode.

DIVA [1:0] : division ratio for internal clocks when Normal mode.

DIVA [1:0]	Inversion mode
2'b00	Fosc
2'b01	Fosc/2
2'b10	Fosc/4
2'b11	Fosc/8

RTNA [4:0] : RTNA[4:0] is used to set 1H (line) period of Normal mode at CPU interface.

Normal Display Mode On frame rate：

$$\text{Frame rate} = \frac{10^7}{(168 + RTNA[4:0] + 32X(15 - FRS[3:0]))(480 + VFP[7:0] + VBP[7:0])}$$

'-': Don't care.

Restriction	-

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

		Sleep In	Yes
Default			

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	

9.3.3 FRMCTR2 (B2h): Frame Rate Control 2 (In Idle Mode/8 colors)

B2H	Frame Rate Control 2 (In Idle Mode/8 colors)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRC IDLE	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1st parameter	1	↑	1	-	0	0	0	0	0	0	0	0	00h
2nd parameter	1	↑	1	-	0	0	0	RTNB[4:0]					10h
Description	*Sets the division ratio for internal clocks of Idle mode at CPU interface.* *RTNB [4:0] : RTNB[4:0] is used to set 1H (line) period of Idle mode at CPU interface.* *'-': Don't care.*												
Restriction	-												

Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	

9.3.4 FRMCTR3 (B3h): Frame Rate Control3 (In Partial Mode/Full Colors)

B3H	Frame Rate Control 3(In Partial Mode/Full Colors)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRC PTL	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)
1st parameter	1	↑	1	-	0	0	0	0	0	0	0	0	00h
2nd parameter	1	↑	1	-	0	0	0	RTNC[4:0]					10h
Description	*Sets the division ratio for internal clocks of Partial mode (Idle mode off) at CPU interface.* *RTNC [4:0] : RTNC[4:0] is used to set 1H (line) period of Partial mode at CPU interface.* *Note: B3 cmd needs to be set before Sleep Out.* *'-': Don't care.*												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart

9.3.5 DIC (B4): Display Inversion Control

B4H	Display Inversion Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DIC	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
1st parameter	1	↑	1	-	0	0	0	0	0	0	DINV		01h

Description	*DINV[1:0] : Set the inversion mode* DINV [1:0] / Inversion mode 2'b00 / Column inversion 2'b01 / 1-dot inversion 2'b10 / 2-dot inversion 2'b11 / Reserved *'-': Don't care.*
Restriction	-
Register availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes
Default	Status / Default Value Power On Sequence / N/A S/W Reset / N/A H/W Reset / N/A
Flow Chart	

9.3.6 BPC(B5): Blanking Porch Control

B5H	Blanking Porch Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BPC	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)
1st parameter	1	↑	1	-	VFP[7:0]								02h
2nd parameter	1	↑	1	-	VBP[7:0]								02h
3rd parameter	1	↑	1		0	0	0	0	0	0	0	0	00h
4th parameter	1	↑	1	-	HBP[7:0]								04h
Description	*VFP [7:0] / VBP[7:0]: The FP [7:0] and BP [7:0] bits specify the line number of vertical front and back porch period respectively.*												

VFP [7:0]	Front porch of Number lines
00h	Reserved
01h	Reserved
02h	2
:	:
:	:
FDh	253
Feh	254
FFh	255

VBP [7:0]	Front porch of Number lines
00h	Reserved
01h	Reserved
02h	2
:	:
:	:
FDh	253
Feh	254
FFh	255

HBP [7:0]: The HBP[7:0] bits specify the dotclk number of horizontal back porch period.

HBP [7:0]	Back porch of Number lines
00h	Reserved
01h	Reserved
02h	2
:	:
:	:
FDh	253
Feh	254
FFh	255

Note: B5 cmd needs to be set before Sleep Out.

'-': Don't care.

Restriction: -

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>
Flow Chart	

9.3.7 DFC(B6): Display Function Control

B6H	Blanking Porch Control												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DFC	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)
1st parameter	1	↑	1	-	BYPASS	RCM	RM	0	PTG[1:0]		PT[1:0]		80h
2nd parameter	1	↑	1	-	0	GS	SS	SM	ISC[3:0]				02h
3rd parameter	1	↑	1	-	0	0	NL[5:0]						3Bh

Description

***RM**: Select the interface to access the GRAM. When RM='0', the driver will write display data to GRAM via system interface and the driver will write display data to GRAM via RGB interface when RM='1'.*

RM	Interface for RAM access
0	System Interface
1	RGB interface

***RCM**: RGB interface selection (refer to the RGB interface section).*

RCM	RGB transfer mode
0	DE Mode
1	SYNC Mode

***BYPASS**: Select the display data path whether memory or direct to shift register when RGB interface is used.*

BYPASS	Display data path
0	Memory
1	Direct to shift register

Note: RGB input signal.

***PTG [1:0]**: Set the scan mode in non-display area.*

PTG [1:0]	Gate outputs in non-display area	Source outputs in non-display area

0	0	Normal scan	Set with the PT[2:0] bits
0	1	Setting prohibited	--
1	0	Interval scan	Set with the PT[2:0] bits
1	1	Setting prohibited	--

PT [1:0]*: Determine source/VCOM output in a non-display area in the partial display mode.*

PT[1:0]		Source output on non-display area
0	0	V63
0	1	V0
1	0	AGND
1	1	Hi-Z

SS*: Select the shift direction of outputs from the source driver.*

SS	Source Output Scan Direction
0	S1→ S960
1	S960 → S1

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S960, set SS = 0.

To assign R, G, B dots to the source driver pins from S960 to S1, set SS = 1.

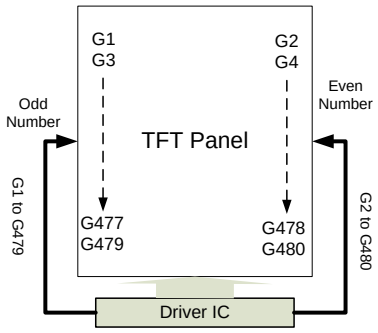
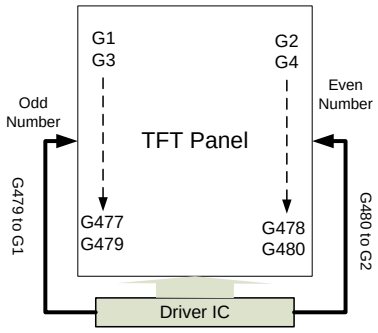
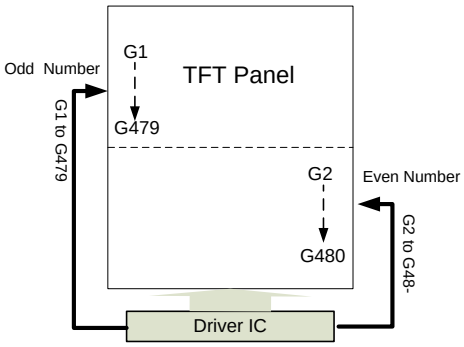
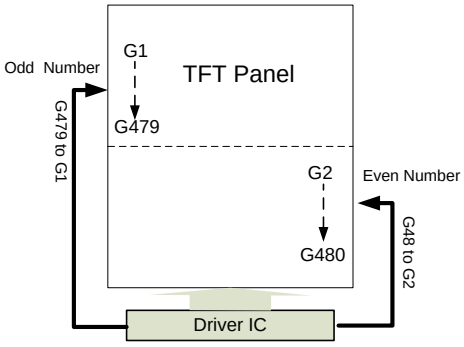
ICS[3:0] *: Set the scan cycle when PTG selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.*

GS*: Sets the direction of scan by the gate driver.*

GS	Gate Output Scan Direction
0	G1→ G480
1	G480 → G1

SM*: Sets the gate driver pin arrangement in combination with the GS to select the optimal scan mode for the module.*

SM	GS	Scan Direction	Gate Output Sequence

0	0		G1,G2,G3,G4…..,G476 G477,G478,G479, G480
0	1		G480,G479,……G8 G7,G6,G5,G4,G3,G2,G1
1	0		G1,G3,G5…….G471 G473,G475,G477,G479 G2,G4,G6…….G472 G474,G476,G478,G480
1	1		G480,G488,…….G14 G12,G10,G8,G6,G4,G2 G479,G477……G13 G11,G9,G7,G5,G3,G1

NL [5:0]*: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.*

NL[5:0]	LCD Drive Line
6'h00 ~ 6'h3B	8 * (NL5:0)+1) lines

	other | Setting inhibited *Note: B6 cmd needs to be set before Sleep Out.* *'-': Don't care.*
Restriction	-
Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart

9.3.8 EM(B7): Entry Mode Set

<table>
<tr><td>B7H</td><td colspan="12">Entry Mode Set</td></tr>
<tr><td>Inst / Para</td><td>D/CX</td><td>WRX</td><td>RDX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>EM</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>(B7h)</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td colspan="2">EPF[1:0]</td><td>0</td><td>0</td><td>DSTB</td><td>GON</td><td>DTE</td><td>0</td><td>06h</td></tr>
<tr><td>Description</td><td colspan="12">
DSTB: In Deep Standby mode (DSTB=1), both internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after the Deep Standby Mode is exited. Exit the Deep Standby Mode is as below,
1. Exit Deep Standby Mode by pull down CSX to low (“0”) 6 times.
2. Exit Deep Standby Mode by input RESX pulse.

GON/DTE: Set the output level of gate driver G1 ~ G480 as follows
<table>
<tr><th>GON</th><th>DTE</th><th>G1~G480 Gate Output</th></tr>
<tr><td>0</td><td>0</td><td>VGH</td></tr>
<tr><td>0</td><td>1</td><td>VGH</td></tr>
<tr><td>1</td><td>0</td><td>VGL</td></tr>
<tr><td>1</td><td>1</td><td>Normal display</td></tr>
</table>
EPF[1:0] Set the data format when 16bbp (R,G,B) to 18 bbp (r, g, b) is stored in the internal GRAM
<table>
<tr><th>EPF[1:0]</th><th>65k (R, G, B) to 262k (r, g, b)</th></tr>
<tr><td>00</td><td>r(0) = b(0) = “0”</td></tr>
<tr><td>01</td><td>r(0) = b(0) = “1”</td></tr>
<tr><td>10</td><td>The MSB value is written to the LSB.</td></tr>
<tr><td>11</td><td>r(0) = b(0) = G(0)</td></tr>
</table>
‘-’: Don’t care.
</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Register availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>
Flow Chart	

9.3.9 MODESEL(B9h): Mode Selection

B9H	MODESEL (Mode Selection)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	0	1	1	1	0	0	1	(B9h)
1st parameter	1	↑	1	-	0	0	0	0	0	0	1	0	02h
Description	*Mode Selection is dithering on. This parameter only take effect on 16.7M color input* *'-': Don't care.*												
Restriction	-												
Register availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>												
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>												
Flow Chart													

9.3.10 PWR1(C0h): Power Control 1

C0H	PWR1 (Power Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)
1st parameter	1	↑	1	-	AVDDS[1:0]		AVCLS[1:0]		0	0	0	0	80h
2nd parameter	1	↑	1	-	0	VGHS[2:0]			0	VGLS[2:0]			25h

Description

AVDDS[1:0]/ AVCLS[1:0] *: AVDD/AVCL setting is as below.*

AVDDS[1:0]	AVDD	AVDDS[1:0]	AVDD
0	6.20	2	6.60
1	6.40	3	6.80

AVCLS[1:0]	AVCL	AVCLS[1:0]	AVCL
0	-4.4	2	-4.8
1	-4.6	3	-5.0

VGHS/ VGLS[2:0]: VGH/L voltage setting,

VGHS[2:0]	VGH
0	12.541
1	12.889
2	13.257
3	13.647
4	14.061
5	14.500
6	14.968
7	15.467

VGLS[2:0]	VGL
0	-7.158
1	-7.667
2	-8.235
3	-8.875
4	-9.600
5	-10.429
6	-11.385
7	-12.500

'-': Don't care.

Restriction: -

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart

9.3.11 PWR2 (C1h): Power Control 2

C1H	PWR2 (Power Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
1st parameter	1	↑	1	-	0	VRH[6:0]							13h

Description

VRH[6:0]: Set GVDD/GVCL voltage level.

VRH[6:0]	VAP(GVDD) (V)	VRH[6:0]	VAP(GVDD) (V)
00h	3.55+(vcom+vcom offset)	15h	4.6+(vcom+vcom offset)
01h	3.6+(vcom+vcom offset)	16h	4.65+(vcom+vcom offset)
02h	3.65+(vcom+vcom offset)	17h	4.7+(vcom+vcom offset)
03h	3.7+(vcom+vcom offset)	18h	4.75+(vcom+vcom offset)
04h	3.75+(vcom+vcom offset)	19h	4.8+(vcom+vcom offset)
05h	3.8+(vcom+vcom offset)	1Ah	4.85+(vcom+vcom offset)
06h	3.85+(vcom+vcom offset)	1Bh	4.9+(vcom+vcom offset)
07h	3.9+(vcom+vcom offset)	1Ch	4.95+(vcom+vcom offset)
08h	3.95+(vcom+vcom offset)	1Dh	5+(vcom+vcom offset)
09h	4+(vcom+vcom offset)	1Eh	5.05+(vcom+vcom offset)
0Ah	4.05+(vcom+vcom offset)	1Fh	5.1+(vcom+vcom offset)
0Bh	4.1+(vcom+vcom offset)	20h	5.15+(vcom+vcom offset)
0Ch	4.15+(vcom+vcom offset)	21h	5.2+(vcom+vcom offset)
0Dh	4.2+(vcom+vcom offset)	22h	5.25+(vcom+vcom offset)
0Eh	4.25+(vcom+vcom offset)	23h	5.3+(vcom+vcom offset)
0Fh	4.3+(vcom+vcom offset)	24h	5.35+(vcom+vcom offset)
10h	4.35+(vcom+vcom offset)	25h	5.4+(vcom+vcom offset)
11h	4.4+(vcom+vcom offset)	26h	5.45+(vcom+vcom offset)
12h	4.45+(vcom+vcom offset)	27h	5.5+(vcom+vcom offset)
13h	4.5+(vcom+vcom offset)	28h~3Fh	Reserved
14h	4.55+(vcom+vcom offset)	--	--

VRH[5:0]	VAN(GVCL) (V)	VRH[5:0]	VAN(GVCL) (V)
00h	-3.55+(vcom+vcom offset)	15h	-4.6+(vcom+vcom offset)

	01h	-3.6+(vcom+vcom offset)	16h	-4.65+(vcom+vcom offset)
	02h	-3.65+(vcom+vcom offset)	17h	-4.7+(vcom+vcom offset)
	03h	-3.7+(vcom+vcom offset)	18h	-4.75+(vcom+vcom offset)
	04h	-3.75+(vcom+vcom offset)	19h	-4.8+(vcom+vcom offset)
	05h	-3.8+(vcom+vcom offset)	1Ah	-4.85+(vcom+vcom offset)
	06h	-3.85+(vcom+vcom offset)	1Bh	-4.9+(vcom+vcom offset)
	07h	-3.9+(vcom+vcom offset)	1Ch	-4.95+(vcom+vcom offset)
	08h	-3.95+(vcom+vcom offset)	1Dh	-5+(vcom+vcom offset)
	09h	-4+(vcom+vcom offset)	1Eh	-5.05+(vcom+vcom offset)
	0Ah	-4.05+(vcom+vcom offset)	1Fh	-5.1+(vcom+vcom offset)
	0Bh	-4.1+(vcom+vcom offset)	20h	-5.15+(vcom+vcom offset)
	0Ch	-4.15+(vcom+vcom offset)	21h	-5.2+(vcom+vcom offset)
	0Dh	-4.2+(vcom+vcom offset)	22h	-5.25+(vcom+vcom offset)
	0Eh	-4.25+(vcom+vcom offset)	23h	-5.3+(vcom+vcom offset)
	0Fh	-4.3+(vcom+vcom offset)	24h	-5.35+(vcom+vcom offset)
	10h	-4.35+(vcom+vcom offset)	25h	-5.4+(vcom+vcom offset)
	11h	-4.4+(vcom+vcom offset)	26h	-5.45+(vcom+vcom offset)
	12h	-4.45+(vcom+vcom offset)	27h	-5.5+(vcom+vcom offset)
	13h	-4.5+(vcom+vcom offset)	28h~3Fh	Reserved
	14h	-4.55+(vcom+vcom offset)	--	--

Note:

Vcom default value is 1ch(Vcom = 1.0V)

Vcom offset value is 00h(Vcom offset = 0 step)

'-': Don't care.

Restriction: -

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	

9.3.12 PWR3 (C2h): Power Control 3

C2H	PWR3 (Power Control 3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)
1st parameter	1	↑	1	-	1	0	1	0	SOP[1:0]		GOP[1:0]		A5h

Description

SOP[1:0]: Source driving current level

GOP[1:0]: Gamma driving current level

SOP	GOP	Current Level
00	00	no operation
01	01	Low
10	10	Medium
11	11	High

'-': Don't care.

Restriction	-

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	

9.3.13 VCMPCTL(C5h): VCOM Control

C5H	VCMPCTL (Vcom Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1st parameter	1	↑	1	-	-	-	VCMP[5:0]						1Ch

Description

VCMP[5:0]: Set the relative of VCOM

VCMP[5:0]	VCOM	VCMP[5:0]	VCOM	VCMP[5:0]	VCOM	VCMP[5:0]	VCOM
0	0.300	16	0.700	32	1.100	48	1.500
1	0.325	17	0.725	33	1.125	49	1.525
2	0.350	18	0.750	34	1.150	50	1.550
3	0.375	19	0.775	35	1.175	51	1.575
4	0.400	20	0.800	36	1.200	52	1.600
5	0.425	21	0.825	37	1.225	53	1.625
6	0.450	22	0.850	38	1.250	54	1.650
7	0.475	23	0.875	39	1.275	55	1.675
8	0.500	24	0.900	40	1.300	56	1.700
9	0.525	25	0.925	41	1.325	57	1.725
10	0.550	26	0.950	42	1.350	58	1.750
11	0.575	27	0.975	43	1.375	59	1.775
12	0.600	28	1.000	44	1.400	60	1.800
13	0.625	29	1.025	45	1.425	61	1.825
14	0.650	30	1.050	46	1.450	62	1.850
15	0.675	31	1.075	47	1.475	63	1.875

Note: VCOM = VCOMP + VMF_REG [5:0] < 1.875

'-': Don't care.

Restriction: -

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>
Flow Chart	

9.3.14 VCM Offset (C6h): Vcom Offset Register

C6H	VCM Offset (Vcom Offset Register)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	0	0	0	1	1	0	(C6h)
1st parameter	1	↑	1	-	VMFSEL	-	VMF_REG [5:0]						00h
Description	*VMFSEL: '0' from NV memory; '1': from VMF_REG[5:0] setting.* *VMF_REG[5:0]: add an offset to VCMP(for optimum display quality).* <table><tr><th>VMF_REG [5:0]</th><th>Offset</th></tr><tr><td>011111b</td><td>+31</td></tr><tr><td>011110b</td><td>+30</td></tr><tr><td>:</td><td>:</td></tr><tr><td>000010b</td><td>+2</td></tr><tr><td>000001b</td><td>+1</td></tr><tr><td>000000b</td><td>+0</td></tr><tr><td>111111b</td><td>-1</td></tr><tr><td>111110b</td><td>-2</td></tr><tr><td>:</td><td>:</td></tr><tr><td>100010b</td><td>-30</td></tr><tr><td>100001b</td><td>-31</td></tr><tr><td>100000b</td><td>-32</td></tr></table> *'-': Don't care.*												
Restriction	-												
Register availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr></table>												

	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	N/A
	S/W Reset	N/A
	H/W Reset	N/A

Flow Chart	

9.3.15 NVMADW (D0h): NVM Address/Data Write

D0H	NVMADW (NVM Address/Data Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)
1st parameter	1	↑	1	-	-	-	-	PROG_ADDR [4:0]					00h
2nd parameter	1	↑	1	-	PROG_DATA [7:0]								--

Description

- This command is used to program the NVM data.

- PROG_ADDR [4:0]: The select bits of ID1, ID2, ID3, VMF_REG[5:0] programming.

PROG_ADDR [4:0]	Description
00000	ID1 programming
00001	ID2 programming
00010	ID3 programming
00011	VMF_REG programming
00100	--
Others	Not allowed

PROG_DATA [7:0]: PROG_DATA is set by user for NVM data.

'-': Don't care.

Restriction: -

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes

	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	N/A
	S/W Reset	N/A
	H/W Reset	N/A

Flow Chart	

9.3.16 NVMBPROG (D1h): NVM Byte Program

D1H	NVMBPROG (NVM Byte Program)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)
1st parameter	1	↑	1	-	PROGCODE[23:16]								-
2nd parameter	1	↑	1		PROGCODE[15:8]								-
3rd parameter	1	↑	1	-	PROGCODE[7:0]								-
Description	*PROGCODE[23:0:] NVM program enable code. C3AA3Ch to start an auto byte program operation.* *'-': Don't care.*												
Restriction	-												

Register availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	N/A
	S/W Reset	N/A
	H/W Reset	N/A

Flow Chart	

9.3.17 NVM Status Read(D2h)

D2H	NVMSTRD (NVM Status Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	0	1	0	0	0	1	(D2h)
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	
2nd parameter	1	1	↑	-	ID2CNT[3:0]				ID1CNT[3:0]				00h
3rd parameter	1	1	↑	-	VMFCNT[3:0]				ID3CNT[3:0]				00h
4th parameter	1	1	↑	-	BUSY	-	-	-	-	-	-	-	-
5th parameter	1	1	↑	-	-	-	VMF[5:0]						00h

Description

ID1CNT[3:0], ID2CNT[3:0], ID3CNT[3:0], VMFCNT[3:0]: Programmed times status.

ID2CNT/ ID1CNT[3:0] VMFCNT/ ID3CNT[3:0]	Description
0000b	No Programmed
0001b	1 time
0011b	2 times
0111b	3 times
1111b	4 times

BUSY: This bit '1' means NVM is busy in programming. '0' is idle.

VMF[4:0]: This byte returns the VMF[4:0] value, which was programmed to NVM by command D0h.

'-': Don't care.

Restriction: -

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default		Status: Power On Sequence — Default Value: N/A Status: S/W Reset — Default Value: N/A Status: H/W Reset — Default Value: N/A
Flow Chart		

9.3.18 RDID4 (D3h): Read ID4

D3H	RDID4(Read ID4)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	0	1	1	0	1	1	1	(D3h)
1st parameter	1	1	↑	-	X	X	X	X	X	X	X	X	-
2nd parameter	1	1	↑	-	0	0	0	0	0	0	0	0	-
3rd parameter	1	1	↑	-	ID4_15	ID4_14	ID4_13	ID4_12	ID4_11	ID4_10	ID4_9	ID4_8	77h
4th parameter	1	1	↑	-	ID4_7	ID4_6	ID4_5	ID4_4	ID4_3	ID4_2	ID4_1	ID4_0	96h
Description	*Read IC device code.* *The 1st parameter is dummy read period.* *The 3rd and 4th parameter mean the IC model name.* *'-': Don't care.*												
Restriction	-												
Register availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	Status: Power On Sequence — Default Value: NA Status: S/W Reset — Default Value: NA Status: H/W Reset — Default Value: NA												
Flow Chart													

9.3.19 PGC (E0h): Positive Gamma Control

E0H	PGC (Positive Voltage Gamma Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PVGAMCTRL	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1st Parameter	1	↑	1	-	V63P3	V63P2	V63P1	V63P0	V0P3	V0P2	V0P1	V0P0	F0h
2nd Parameter	1	↑	1	-	0	0	V1P5	V1P4	V1P3	V1P2	V1P1	V1P0	03h
3rd Parameter	1	↑	1	-	0	0	V2P5	V2P4	V2P3	V2P2	V2P1	V2P0	05h
4th Parameter	1	↑	1	-	0	0	0	V4P4	V4P3	V4P2	V4P1	V4P0	09h
5th Parameter	1	↑	1	-	0	0	0	V6P4	V6P3	V6P2	V6P1	V6P0	0Ch
6th Parameter	1	↑	1	-	0	0	J0P1	J0P0	V13P3	V13P2	V13P1	V13P0	0Fh
7th Parameter	1	↑	1	-	0	V20P6	V20P5	V20P4	V20P3	V20P2	V20P1	V20P0	3Eh
8th Parameter	1	↑	1	-	0	V36P2	V36P1	V36P0	0	V27P2	V27P1	V27P0	77h
9th Parameter	1	↑	1	-	0	V43P6	V43P5	V43P4	V43P3	V43P2	V43P1	V43P0	4Fh
10th Parameter	1	↑	1	-	0	0	J1P1	J1P0	V50P3	V50P2	V50P1	V50P0	0Fh
11th Parameter	1	↑	1	-	0	0	0	V57P4	V57P3	V57P2	V57P1	V57P0	17h
12th Parameter	1	↑	1	-	0	0	0	V59P4	V59P3	V59P2	V59P1	V59P0	17h
13th Parameter	1	↑	1	-	0	0	V61P5	V61P4	V61P3	V61P2	V61P1	V61P0	21h
14th Parameter	1	↑	1	-	0	0	V62P5	V62P4	V62P3	V62P2	V62P1	V62P0	23h
Description	Adjust the gamma characteristics of the TFT panel. Positive Gamma Control												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

9.3.20 NGC (E1h): Negative Gamma Control

E1H	NGC (Negative Voltage Gamma Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVGAMCTRL	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)
1st Parameter	1	↑	1	-	V63N3	V63N2	V63N1	V63N0	V0N3	V0N2	V0N1	V0N0	F0h
2nd Parameter	1	↑	1	-	0	0	V1N5	V1N4	V1N3	V1N2	V1N1	V1N0	03h
3rd Parameter	1	↑	1	-	0	0	V2N5	V2N4	V2N3	V2N2	V2N1	V2N0	05h
4th Parameter	1	↑	1	-	0	0	0	V4N4	V4N3	V4N2	V4N1	V4N0	09h
5th Parameter	1	↑	1	-	0	0	0	V6N4	V6N3	V6N2	V6N1	V6N0	0Ch
6th Parameter	1	↑	1	-	0	0	J0N1	J0N0	V13N3	V13N2	V13N1	V13N0	0Fh
7th Parameter	1	↑	1	-	0	V20N6	V20N5	V20N4	V20N3	V20N2	V20N1	V20N0	3Eh
8th Parameter	1	↑	1	-	0	V36N2	V36N1	V36N0	0	V27N2	V27N1	V27N0	77h
9th Parameter	1	↑	1	-	0	V43N6	V43N5	V43N4	V43N3	V43N2	V43N1	V43N0	4Fh
10th Parameter	1	↑	1	-	0	0	J1N1	J1N0	V50N3	V50N2	V50N1	V50N0	0Fh
11th Parameter	1	↑	1	-	0	0	0	V57N4	V57N3	V57N2	V57N1	V57N0	17h
12th Parameter	1	↑	1	-	0	0	0	V59N4	V59N3	V59N2	V59N1	V59N0	17h
13th Parameter	1	↑	1	-	0	0	V61N5	V61N4	V61N3	V61N2	V61N1	V61N0	21h
14th Parameter	1	↑	1	-	0	0	V62N5	V62N4	V62N3	V62N2	V62N1	V62N0	23h

Description	1. Adjust the gamma characteristics of the TFT panel. 2. Negative Gamma Control
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

	Sleep In: Yes
Default	Status: Default Value Power On Sequence: Refer to description S/W Reset: Refer to description H/W Reset: Refer to description

9.3.21 DGC1(E2h): Digital Gamma Control 1

E2H	DGC1 (Digital Gamma Control 1)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	1	0	0	0	1	0	(E2h)
1st parameter	1	↑	1	-	DGAM_R00								--
2nd parameter	1	↑	1	-	DGAM_R01								--
	1	↑	1	-	:								--
63nd parameter	1	↑	1	-	DGAM_R62								--
64th parameter	1	↑	1	-	DGAM_R63								--
Description	*Digital Gamma adjustment registers for red gamma curve.* *'-': Don't care.*												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	

9.3.22 DGC2 (E3h): Digital Gamma Control 2

E3H	DGC2 (Digital Gamma Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	1	0	0	0	1	0	(E3h)
1st parameter	1	↑	1	-	DGAM_B00								--
2nd parameter	1	↑	1	-	DGAM_B01								--
	1	↑	1	-	:								--
63nd parameter	1	↑	1	-	DGAM_B62								--
64th parameter	1	↑	1	-	DGAM_B63								--
Description	*Digital Gamma adjustment register for blue gamma curve.* *'-': Don't care.*												
Restriction	-												

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	

9.3.23 DOCA (E8h): Display Output Ctrl Adjust

E8H	DOCA (Display Output Ctrl Adjust)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	1	0	1	0	0	0	(E8h)
1st parameter	1	↑	1	-	0	1	0	0	0	0	0	0	40h
2nd parameter	1	↑	1	-	1	0	0	0	1	0	1	0	8Ah
3rd parameter	1	↑	1	-	0	0	0	0	0	0	0	0	00h
4th parameter	1	↑	1	-	0	0	0	0	0	0	0	0	00h
5th parameter	1	↑	1	-	0	0	1	0	S_END[3:0]				25h
6th parameter	1	↑	1	-	0	0	G_START[5:0]						0Ah
7th parameter	1	↑	1	-	G_EQ	0	G_END[5:0]						38h
8th parameter	1	↑	1	-	0	0	1	1	0	0	1	1	33h

Description

S_END[3:0]: Set Source equalizing period time.

S_END [3:0]	Source timing Control(us)
00h	9
01h	10.5
02h	12
03h	13.5
:	
:	
0Eh	30
0Fh	31.5

G_START[5:0]: To determine the timing "Gate start".

G_END[5:0]: To determine the timing "Gate End".

G_START[5:0]	G_END[5:0]	Gate timing Control (Tclk)
00h	00h	1
01h	01h	2
02h	02h	3
03h	03h	4
:	:	:
:	:	:
3Eh	3Eh	62
3Fh	3Fh	63

	G_EQ: Gate driver EQ function ON/OFF. '0' → OFF, '1' →ON. Default is OFF. *Note:* *1. Tclk = 4/osc, Ta=25℃, Frame rate = 60Hz,VDDA=2.8V* *2. '-': Don't care.*
Restriction	-
Register availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart

9.3.24 CSCON (F0h): Command Set Control

F0h	CSCON (Command Set Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	1	1	0	0	0	0	(F0h)
1st parameter	1	↑	1	-	D[7:0]								00h
Description	*Enable command 2* *D[7:0] = C3h enable command 2 part I* *D[7:0] = 96h enable command 2 part II* *Disable command 2* *D[7:0] = 3Ch disable command 2 part I* *D[7:0] = 69h disable command 2 part II* *'-': Don't care.*												
Restriction	-												

Register availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>
Flow Chart	

9.3.25 SPI Read Control (FBh)

FBh	SPIRC (SPI Read Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0	↑	1	-	1	1	1	1	1	0	1	1	(FBh)
1st parameter	1	↑	1					SPI_REN	SPI_CNT[3:0]				00h
Description	*SPI_REN: SPI read enable* *SPI_CNT [3:0]: SPI read parameter number* *'-': Don't care.*												
Restriction	-												
Register availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>												

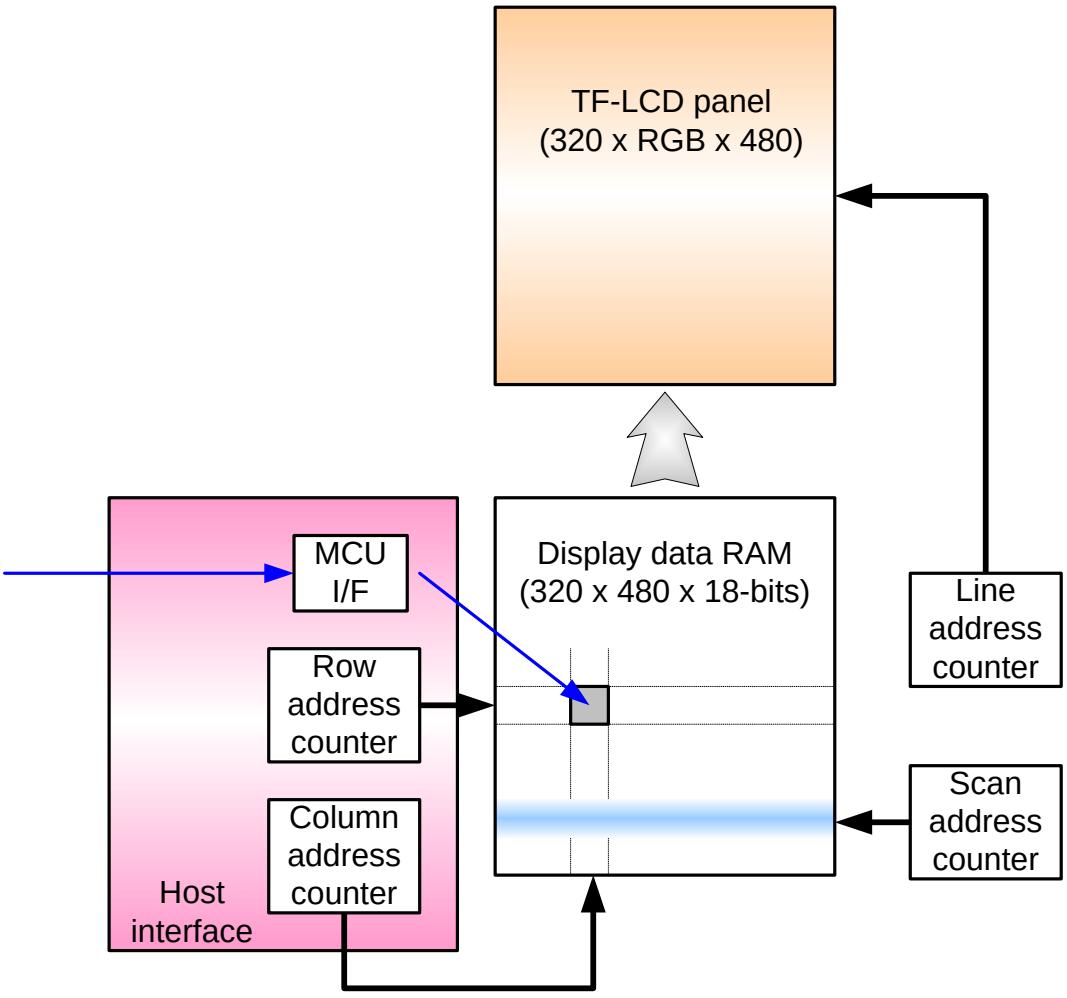
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>
Flow Chart	

10 Function Description

10.1.. Display Data RAM

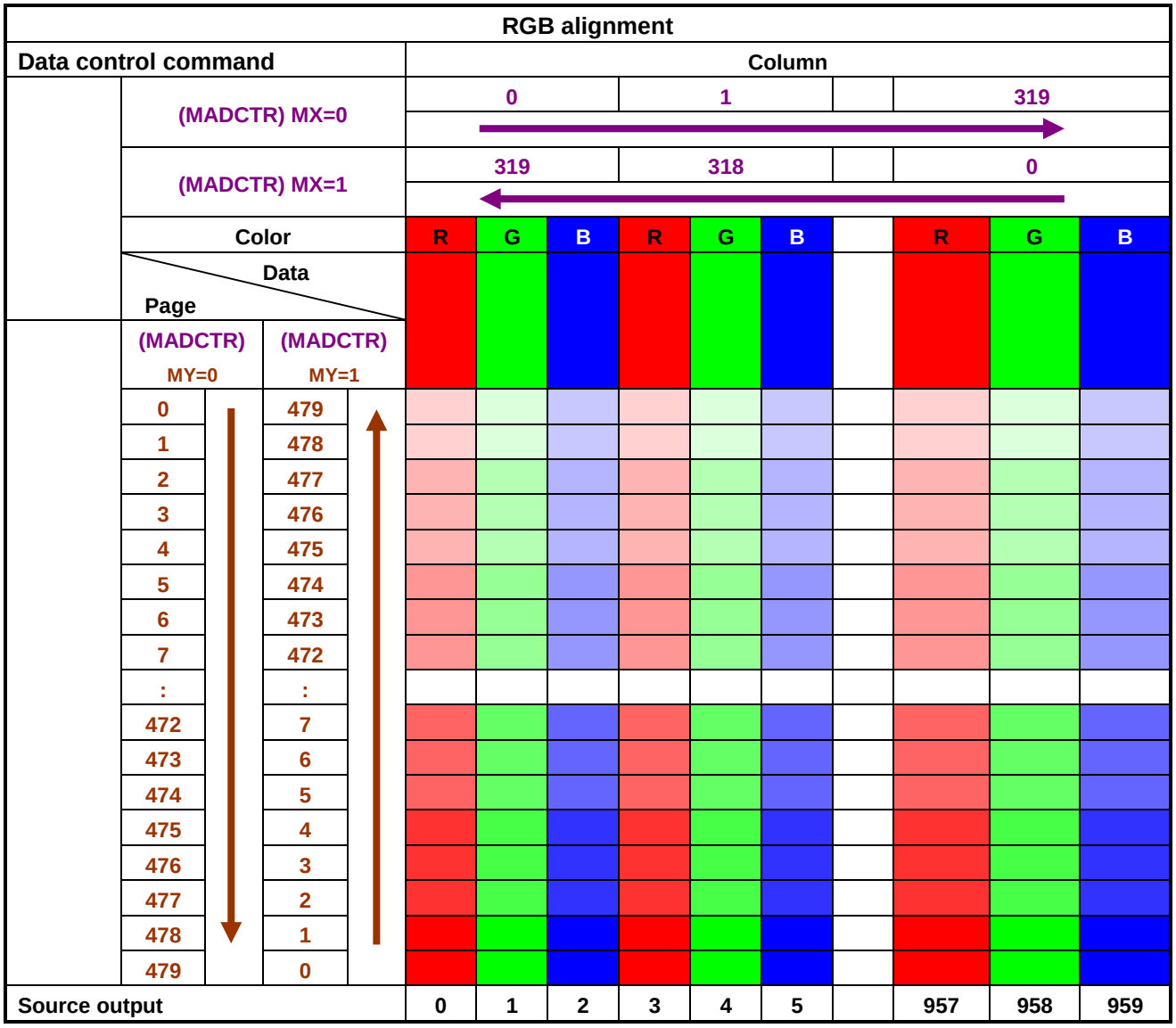
10.1.1 Configuration

The display module has an integrated 320x480x18-bit graphic type static RAM. This 2,764,800-bit memory allows storing on-chip a 320xRGBx480 image with an 18-bpp resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



Display data RAM organization

10.1.2 Memory to display address mapping



10.2.. Address Control

The address counter sets the addresses of the display data RAM for writing and reading. Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=319 and Y=0 to Y=479. Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

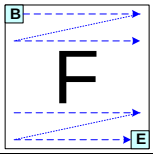
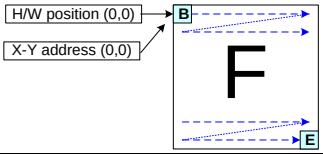
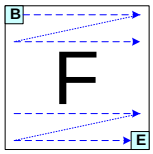
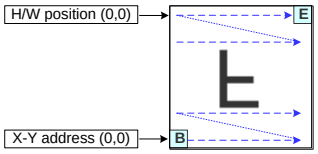
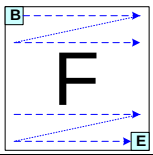
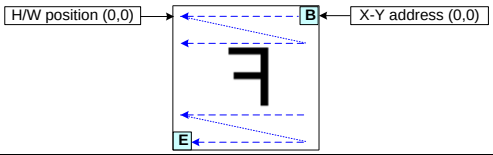
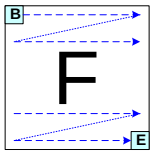
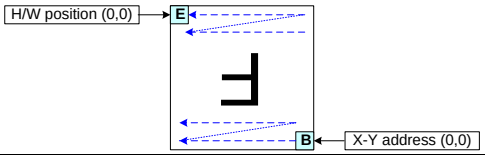
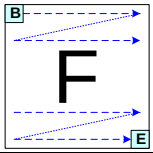
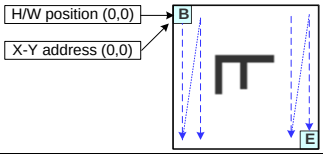
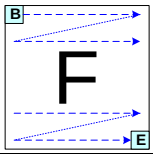
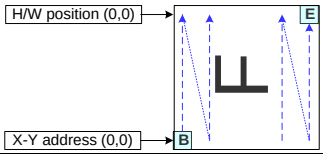
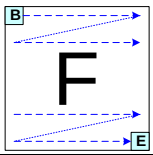
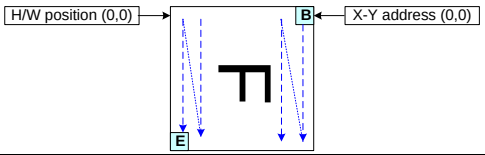
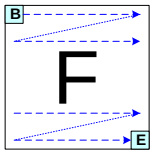
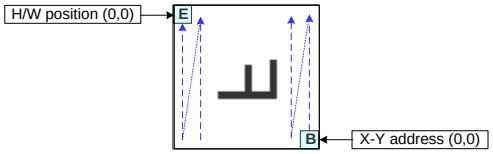
For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=319, YE=479.

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET and MADCTL”, define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed.

For each image condition, the controls for the column and row counters apply as below

Condition	Column	Page
Command 2C/2E is accepted	Return to “Start Column”	Return to “Start Page”
Read/Write RAM action	Increment by 1	No change
Column value is large than “End Column”	Return to “Start Column”	Increment by 1
Page value is large than “End Page”	Return to “Start Column”	Return to “Start Page”

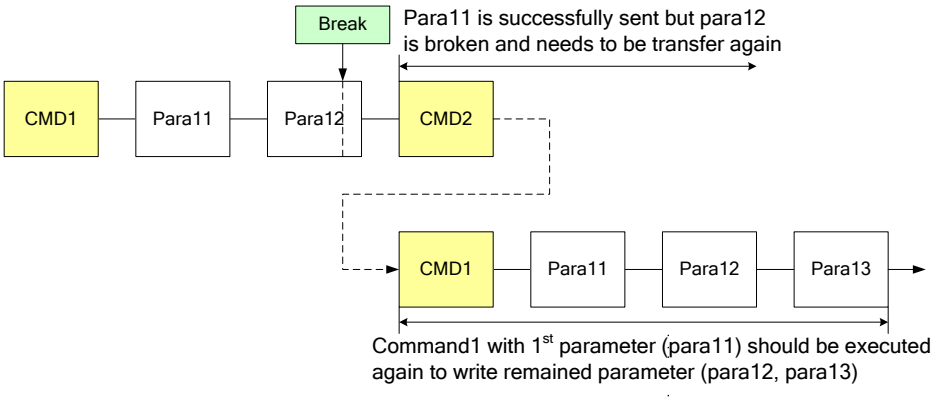
Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

10.3.. Data Transfer Break and Recovery

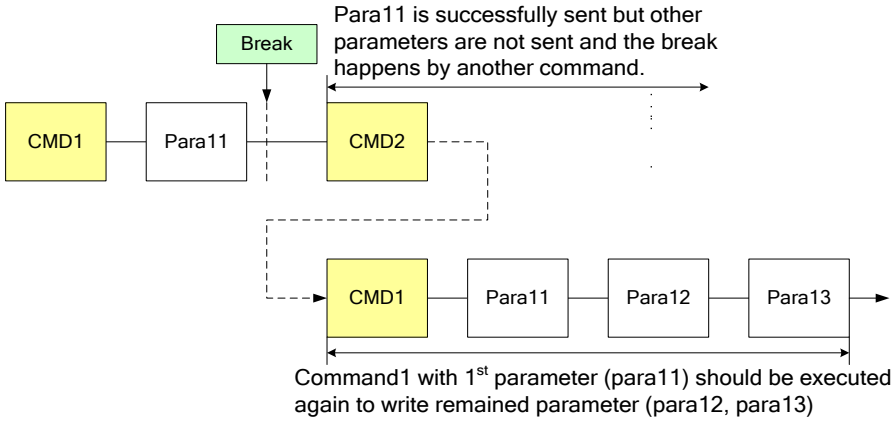
If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state.

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated.

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



Write interrupts recovery (serial interface)



Write interrupts recovery (both serial and parallel Interface)

10.4.. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select Line is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select line is next enabled as shown below.

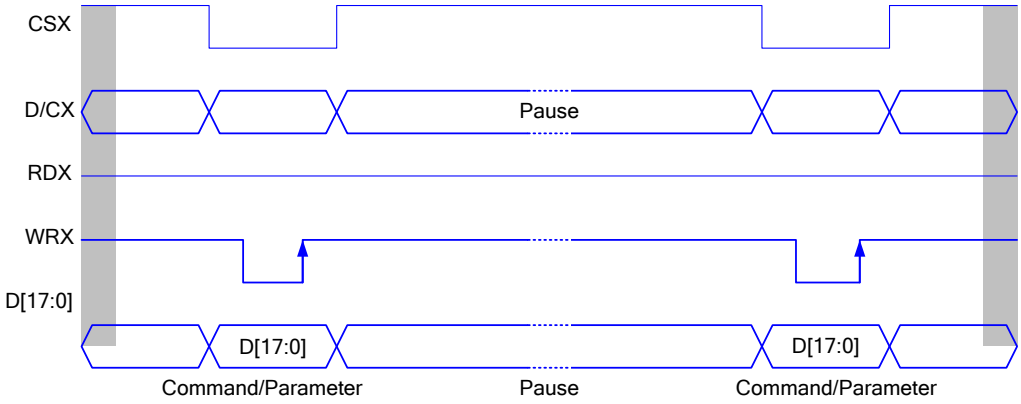
This applies to the following 4 conditions:

1) Command-Pause-Command

2) Command-Pause-Parameter

3) Parameter-Pause-Command

4) Parameter-Pause-Parameter



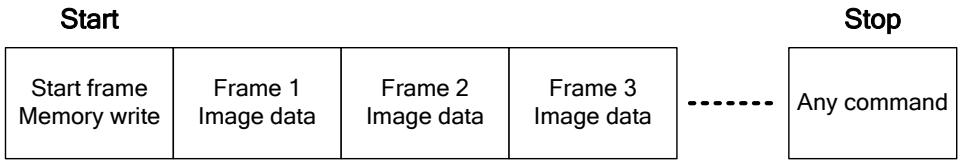
Parallel bus pause protocol (paused by CSX)

10.5.. Data Transfer Mode

The module has three kinds color modes for transferring data to the display RAM. These are 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

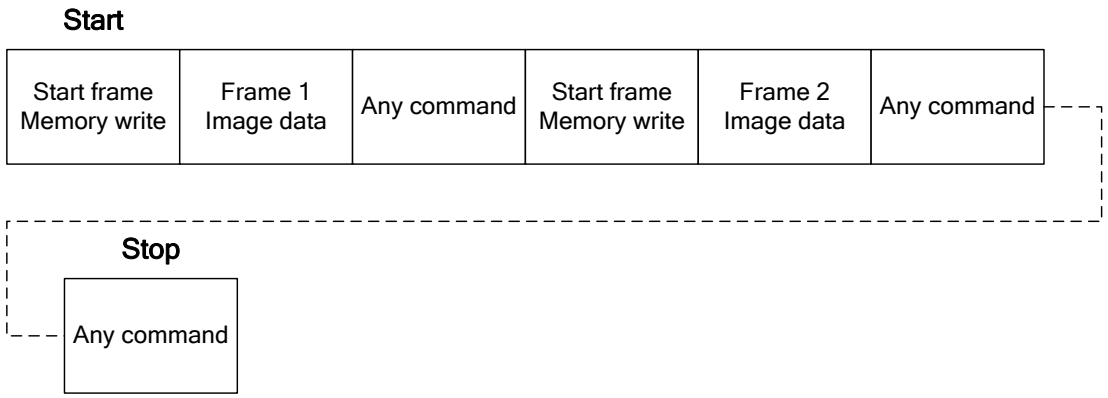
10.5.1 Method 1

The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.



10.5.2 Method 2

The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

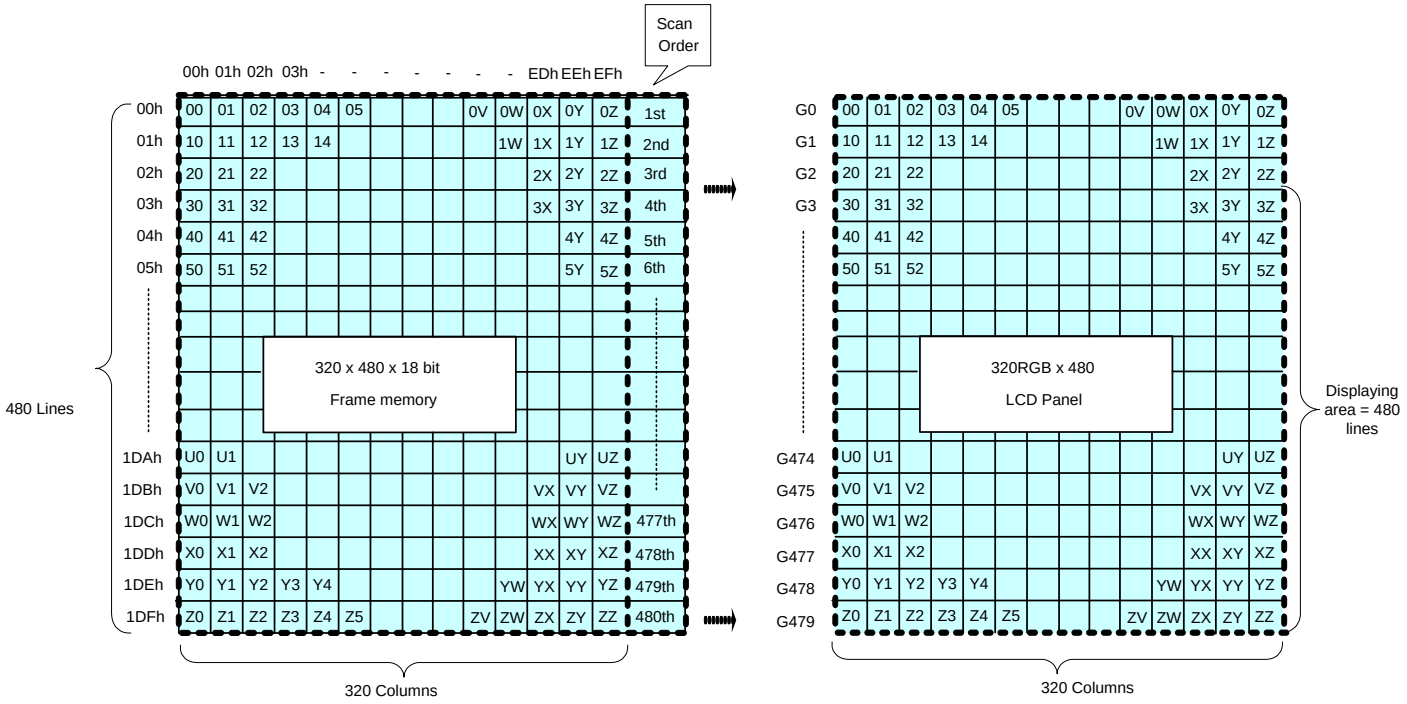
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

10.6.. Normal Display On or Partial Mode On, Vertical Scroll Off

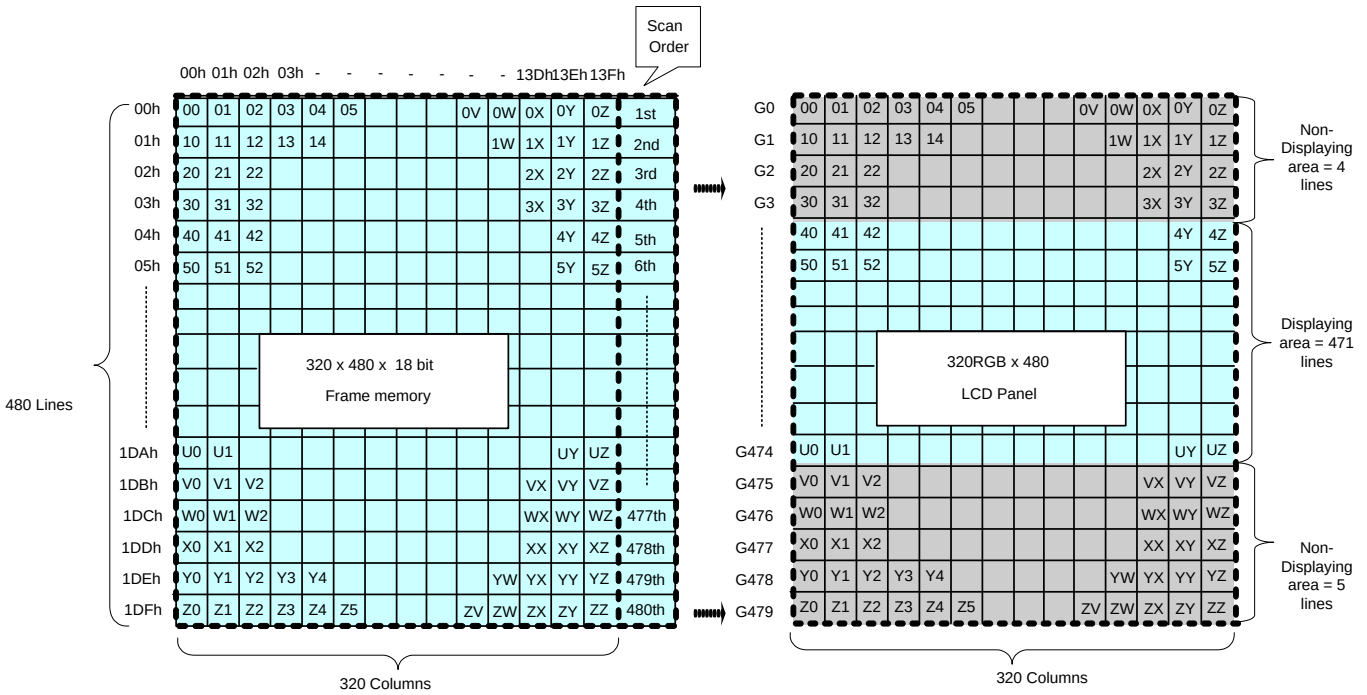
In this mode, contents of the frame memory within an area where column address is 00h to 83h and row address is 00h to 83h is displayed.

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).

Example1: Normal Display On



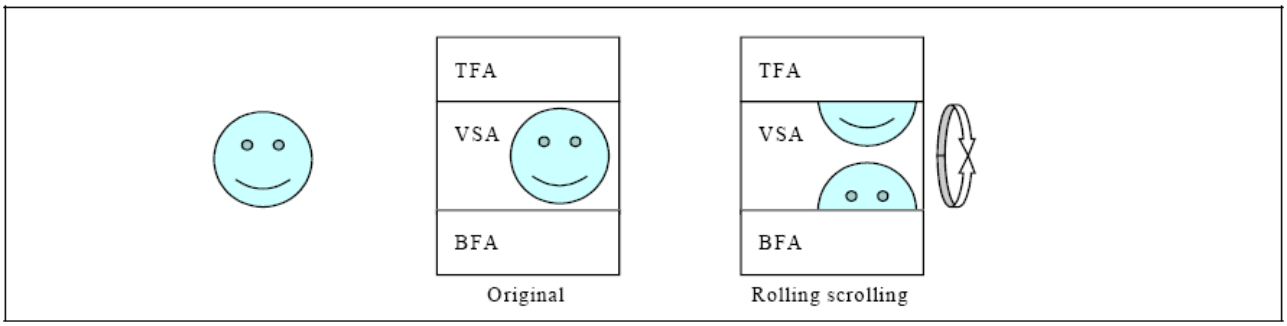
Example2) Partial Display On: PSL[15:0] = 0004h, PEL[15:0] = 01DBh, MADCTR (ML)=0



10.7.. Vertical Scroll Mode

10.7.1 Rolling scroll

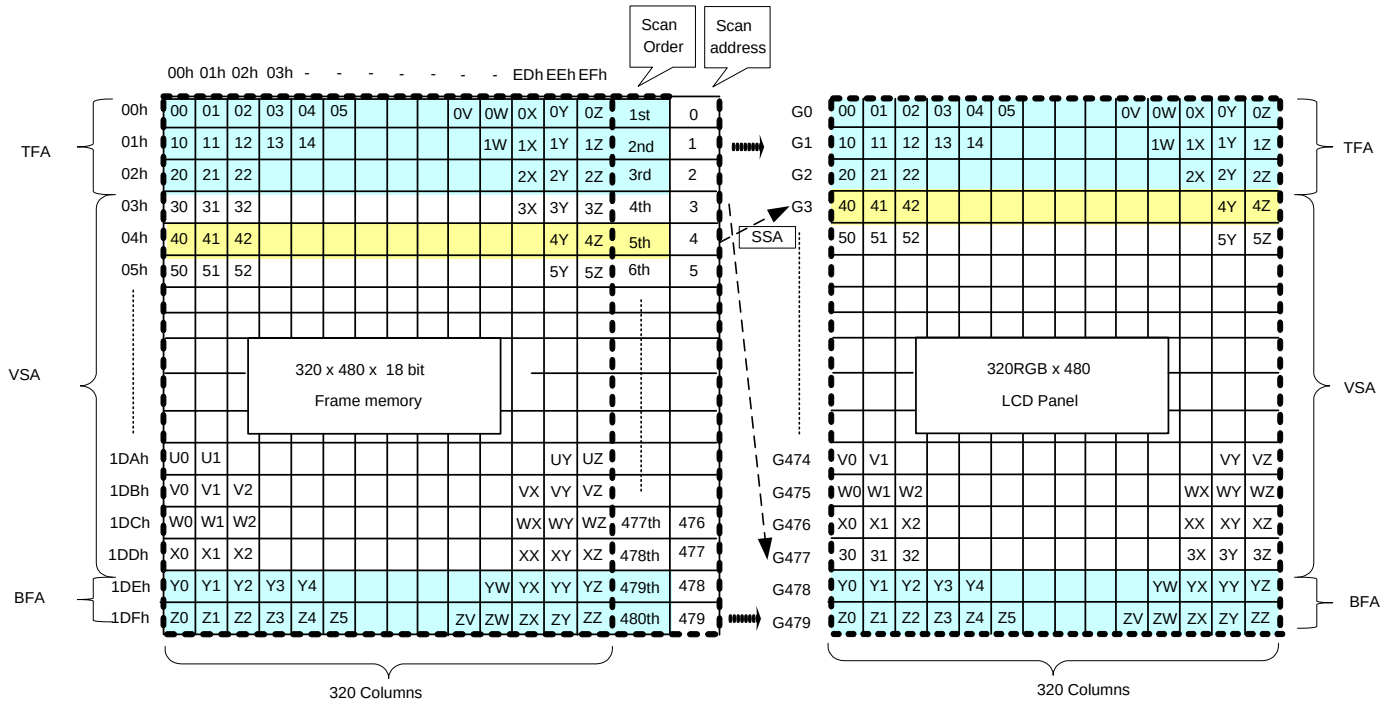
There is just one types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).



Rolling Scroll Definition

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =480. In this case, ‘rolling’ scrolling is applied as shown below. All the memory contents will be used.

Example: Panel size=320 x 480, TFA =3, VSA=475, BFA=2, SSA=4, MADCTR ML=0: Rolling Scroll



10.7.2 Vertical Scroll Example

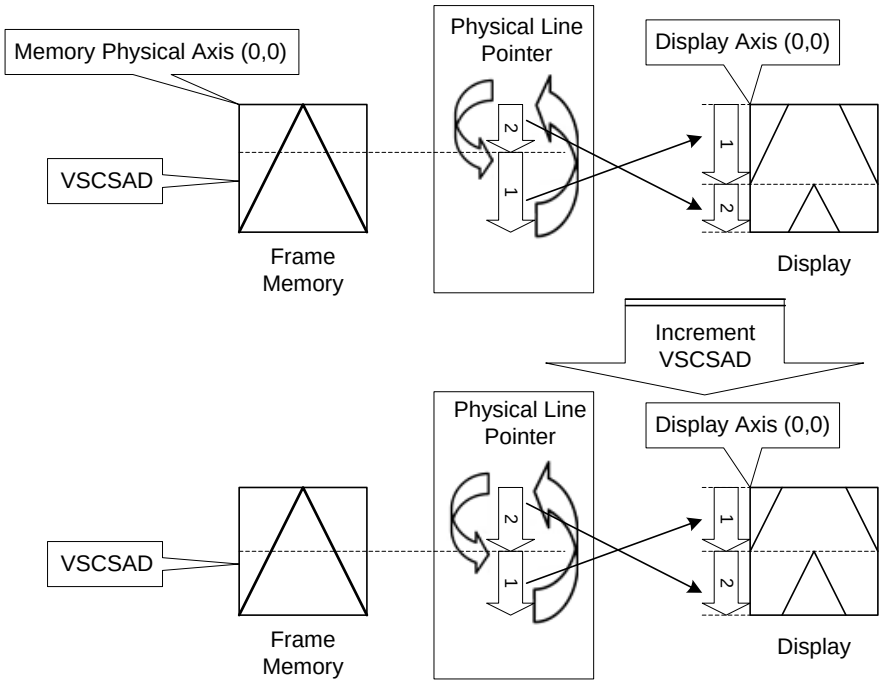
There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: TFA + VSA + BFA≠Panel total scan lines. In this case, scrolling is applied as shown below.

N/A. Do not set TFA + VSA + BFA≠Panel total scan lines. In that case, unexpected picture will be shown.

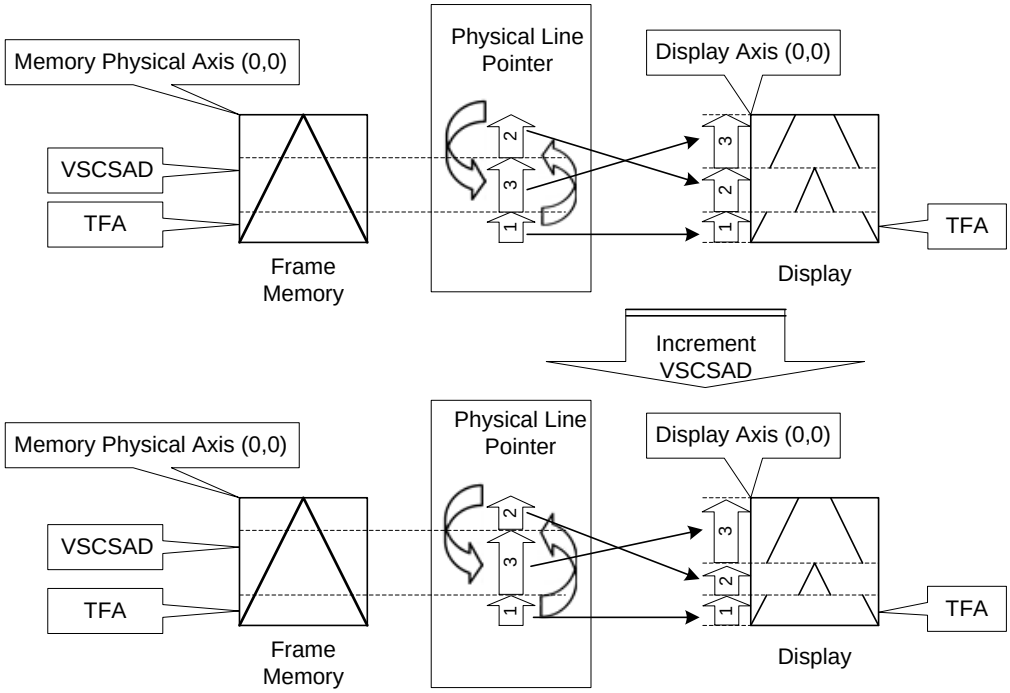
Case 2: TFA + VSA + BFA= Panel total scan lines

Example1) When MADCTR parameter ML=”0”, TFA=0, VSA=480, BFA=0 and VSCSAD=40.



Display of Vertical Scroll Example 1

Example2) When MADCTR parameter ML=”1”, TFA=60, VSA=420, BFA=0 and VSCSAD=160.



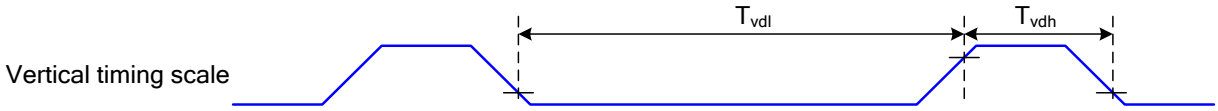
Display of Vertical Scroll Example 2

10.8.. Tearing Effect

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

10.8.1 Tearing effect line modes

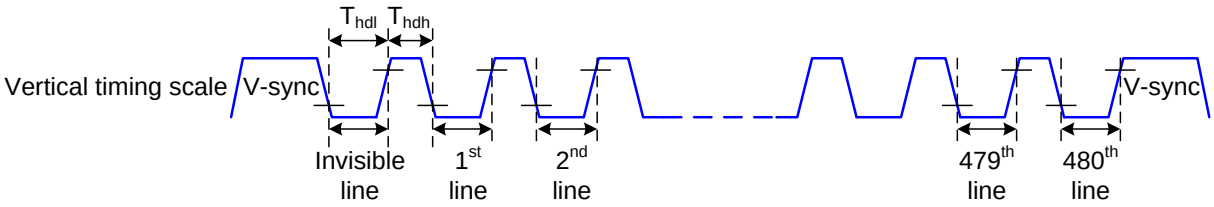
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



tvdh= The LCD display is not updated from the Frame Memory

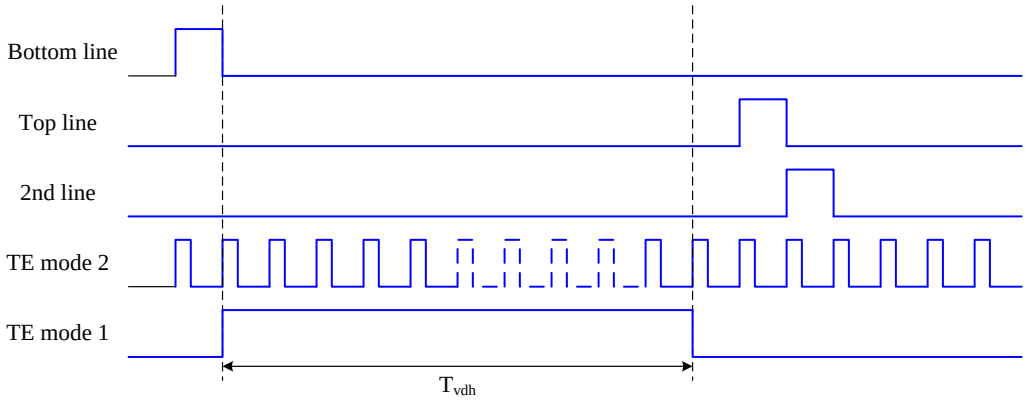
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 H-sync pulses per field.



thdh= The LCD display is not updated from the Frame Memory

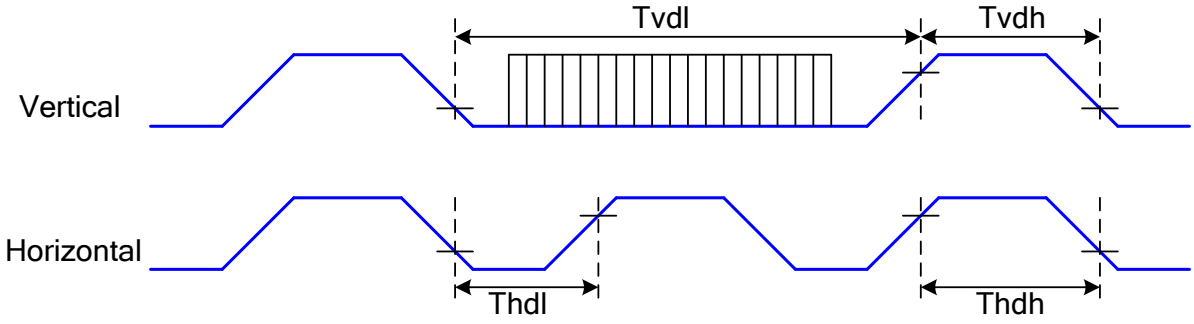
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

10.8.2 Tearign effect line timings

The Tearing Effect signal is described below:

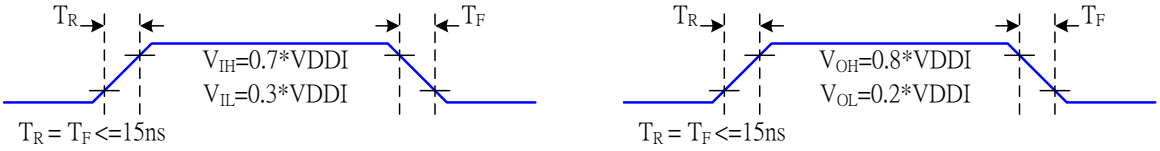


Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	16	-	µs	
thdh	Horizontal Timing Low Duration	-	500	µs	

Table AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25°C)

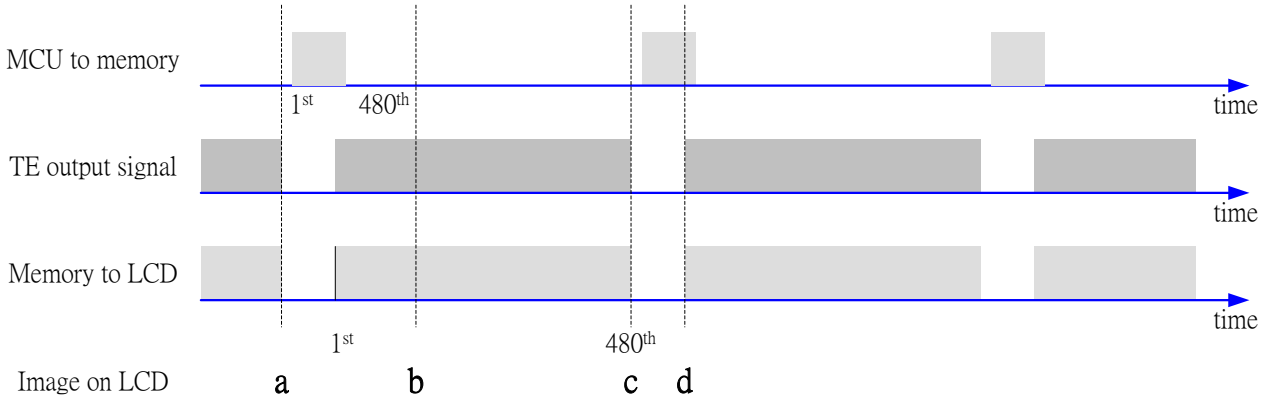
Note: The timings in Table 15 apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

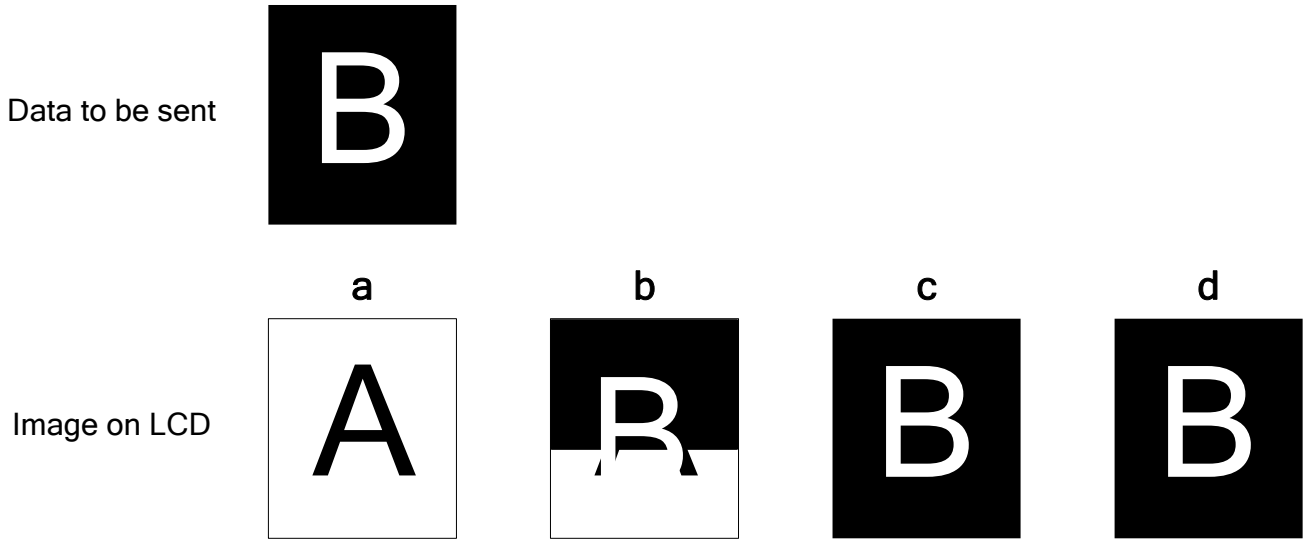


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

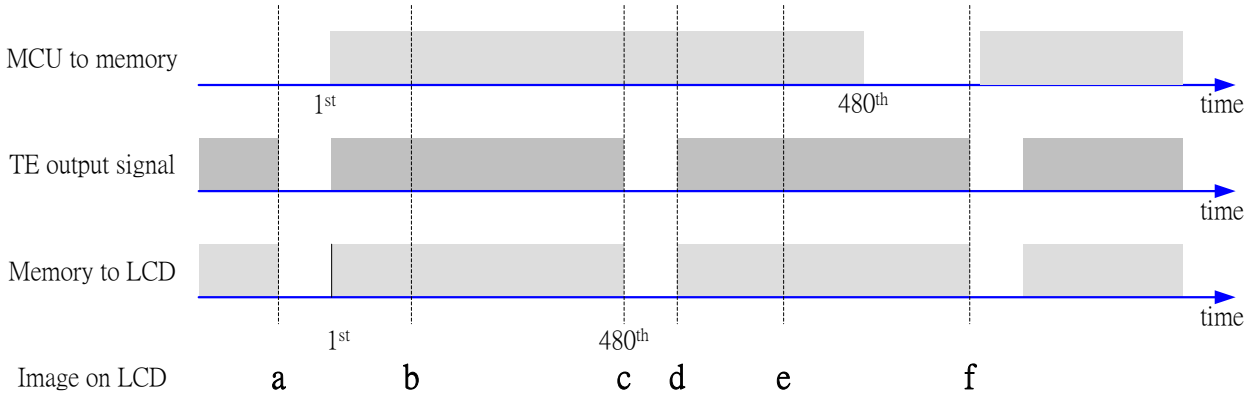
10.8.3 Example 1: MPU Write is faster than panel read



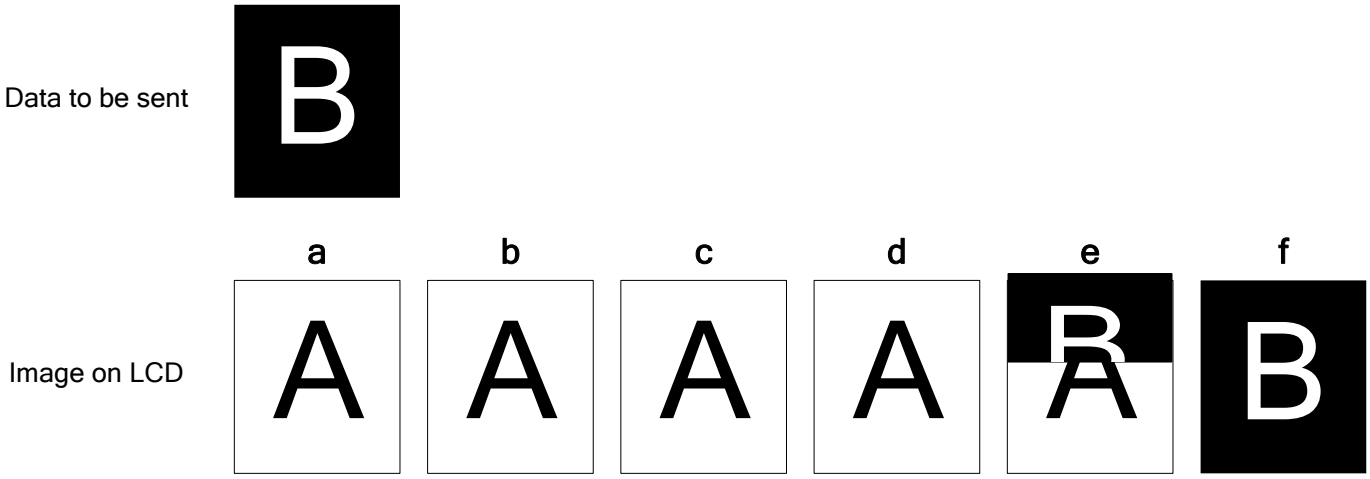
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



10.8.4 Example 2: MPU write is slower than panel read

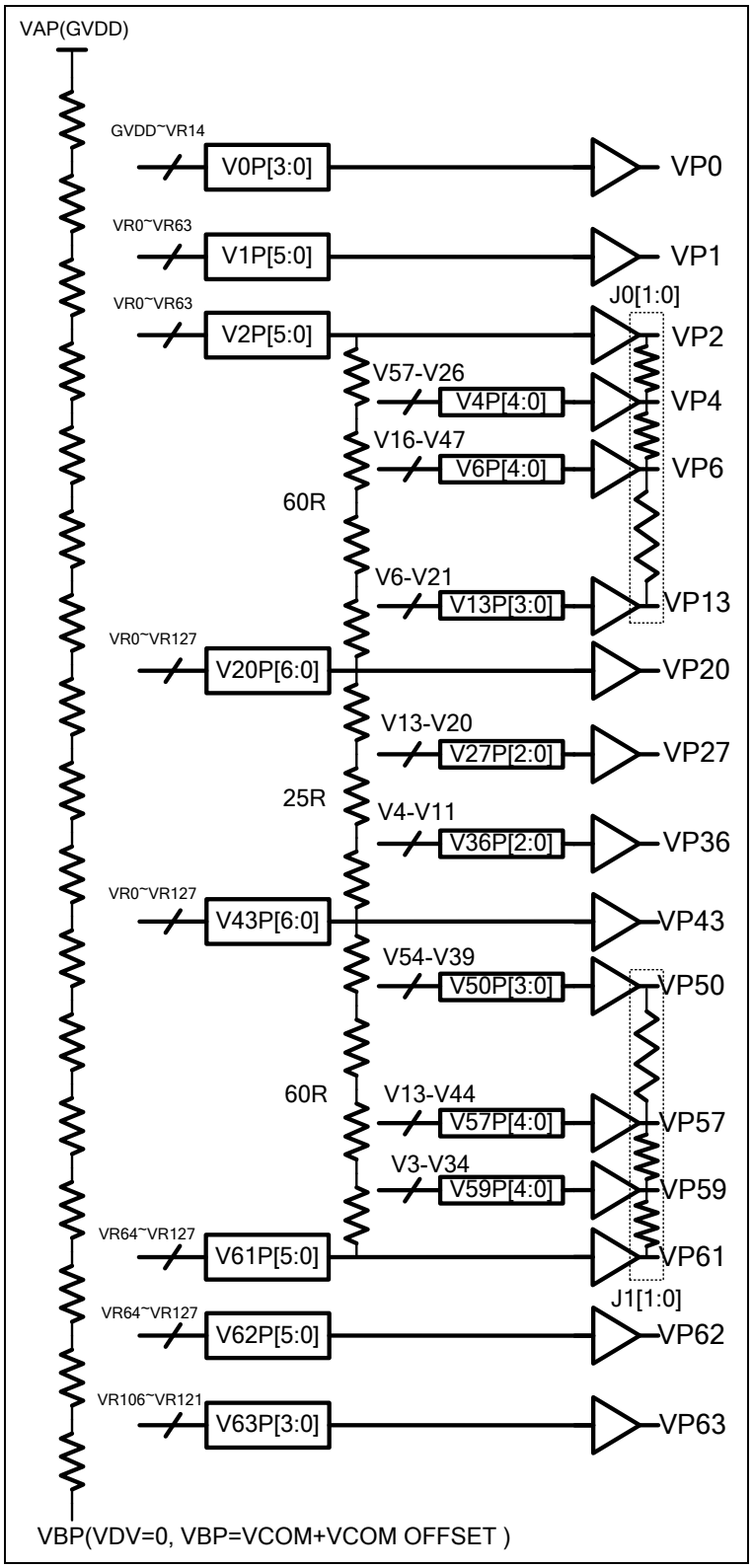


The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

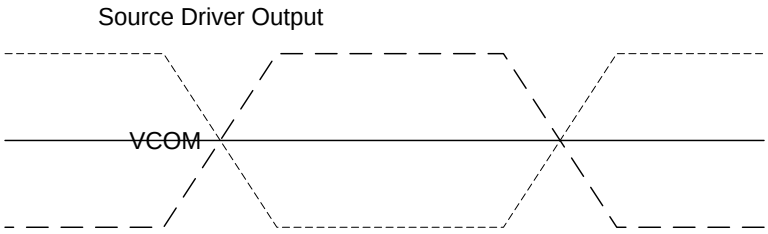


10.9.. Gamma Correction

ST7796U incorporate the gamma correction function to display 262,244 colors for the LCD panel. The gamma correction is performed with 3 groups of registers, which are gradient adjustment, contrast adjustment and fine- adjustment registers for positive and negative polarities, and RGB can be adjusted individually.



Gray scale Voltage Generation (Positive)



Relationship between Source Output and VCOM

Percentage adjustment:

J0P[1:0], J1P[1:0], J0N[1:0], J1N[1:0] these register are used to adjust the voltage level of interpolation point. The following table is the detail description.

J0P[1:0]/J0N[1:0]:

	00h	01h	02h	03h
VP3/VN3	50%	56%	50%	60%
VP5/VN5	50%	44%	50%	42%
VP7/VN7	86%	71%	80%	66%
VP8/VN8	71%	57%	63%	49%
VP9/VN9	57%	40%	49%	34%
VP10/VN10	43%	29%	34%	23%
VP11/VN11	29%	17%	20%	14%
VP12/VN12	14%	6%	9%	6%

J1P[1:0]/J1N[1:0]:

	00h	01h	02h	03h
VP51/VN51	86%	86%	86%	89%
VP52/VN52	71%	71%	77%	80%
VP53/VN53	57%	60%	63%	69%
VP54/VN54	43%	46%	46%	51%
VP55/VN55	29%	34%	31%	37%
VP56/VN56	14%	17%	14%	20%
VP58/VN58	50%	56%	47%	47%
VP60/VN60	50%	50%	50%	53%

voltage level percentage adjustment description

Source voltage of positive gamma level

Gamma level	Related Register	Formula
VP0	V0P[3:0]	(VAP-VBP)*(129R-V0P[3:0]R)/129R+VBP
VP1	V1P[5:0]	(VAP-VBP)*(128R-V1P[5:0]R)/129R+VBP
VP2	V2P[5:0]	(VAP-VBP)*(128R-V2P[5:0]R)/129R+VBP
VP3	J0P[1:0]	(VP2-VP4)*J0P[1:0]+VP4
VP4	V4P[4:0]	(VP2-VP20)*(57R-V4P[4:0])/60R+VP20
VP5	J0P[1:0]	(VP4-VP6)*J0P[1:0]+VP6
VP6	V6P[4:0]	(VP2-VP20)*(47R-V6P[4:0])/60R+VP20
VP7	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP8	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP9	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP10	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP11	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP12	J0P[1:0]	(VP6-VP13)*J0P[1:0]+VP13
VP13	V13P[3:0]	(VP2-VP20)*(21R-V13P[3:0])/60R+VP20
VP14	--	(VP13-VP20)/(20-13)*(20-14)+VP20
VP15	--	(VP13-VP20)/(20-13)*(20-15)+VP20
VP16	--	(VP13-VP20)/(20-13)*(20-16)+VP20
VP17	--	(VP13-VP20)/(20-13)*(20-17)+VP20
VP18	--	(VP13-VP20)/(20-13)*(20-18)+VP20
VP19	--	(VP13-VP20)/(20-13)*(20-19)+VP20
VP20	V20P[6:0]	(VAP-VBP)*(128R-V20P[6:0]R)/129R+VBP
VP21	--	(VP20-VP27)/(27-20)*(27-21)+VP27
VP22	--	(VP20-VP27)/(27-20)*(27-22)+VP27
VP23	--	(VP20-VP27)/(27-20)*(27-23)+VP27
VP24	--	(VP20-VP27)/(27-20)*(27-24)+VP27
VP25	--	(VP20-VP27)/(27-20)*(27-25)+VP27
VP26	--	(VP20-VP27)/(27-20)*(27-26)+VP27
VP27	V27P[2:0]	(VP20-VP43)*(20R-V27P[2:0])/25R+VP43
VP28	--	(VP27-VP36)/(36-27)*(36-28)+VP36
VP29	--	(VP27-VP36)/(36-27)*(36-29)+VP36
VP30	--	(VP27-VP36)/(36-27)*(36-30)+VP36
VP31	--	(VP27-VP36)/(36-27)*(36-31)+VP36
VP32	--	(VP27-VP36)/(36-27)*(36-32)+VP36
VP33	--	(VP27-VP36)/(36-27)*(36-33)+VP36
VP34	--	(VP27-VP36)/(36-27)*(36-34)+VP36
VP35	--	(VP27-VP36)/(36-27)*(36-35)+VP36
VP36	V36P[2:0]	(VP20-VP43)*(11R-V36P[2:0])/25R+VP43
VP37	--	(VP36-VP43)/(43-36)*(43-37)+VP43
VP38	--	(VP36-VP43)/(43-36)*(43-38)+VP43
VP39	--	(VP36-VP43)/(43-36)*(43-39)+VP43
VP40	--	(VP36-VP43)/(43-36)*(43-40)+VP43
VP41	--	(VP36-VP43)/(43-36)*(43-41)+VP43
VP42	--	(VP36-VP43)/(43-36)*(43-42)+VP43
VP43	V43P[6:0]	(VAP-VBP)*(128R-V43P[6:0]R)/129R+VBP
VP44	--	(VP43-VP50)/(50-43)*(50-44)+VP50
VP45	--	(VP43-VP50)/(50-43)*(50-45)+VP50
VP46	--	(VP43-VP50)/(50-43)*(50-46)+VP50
VP47	--	(VP43-VP50)/(50-43)*(50-47)+VP50
VP48	--	(VP43-VP50)/(50-43)*(50-48)+VP50
VP49	--	(VP43-VP50)/(50-43)*(50-49)+VP50
VP50	V50P[3:0]	(VP43-VP61)*(54R-V50P[3:0])/60R+VP61
VP51	J1P[1:0]	(V5P0-VP57)*J1P[1:0]+VP57

VP52	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP53	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP54	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP55	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP56	J1P[1:0]	(VP50-VP57)*J1P[1:0]+VP57
VP57	V57P[4:0]	(VP43-VP61)*(44R-V57P[4:0])/60R+VP61
VP58	J1P[1:0]	(VP57-VP59)*J1P[1:0]+VP59
VP59	V59P[4:0]	(VP43-VP61)*(34R-V59P[4:0])/60R+VP61
VP60	J1P[1:0]	(VP59-VP61)*J1P[1:0]+VP61
VP61	V61P[5:0]	(VAP-VBP)*(64R-V61P[5:0]R)/129R+VBP
VP62	V62P[5:0]	(VAP-VBP)*(64R-V62P[5:0]R)/129R+VBP
VP63	V63P[3:0]	(VAP-VBP)*(23R-V63P[3:0]R)/129R+VBP

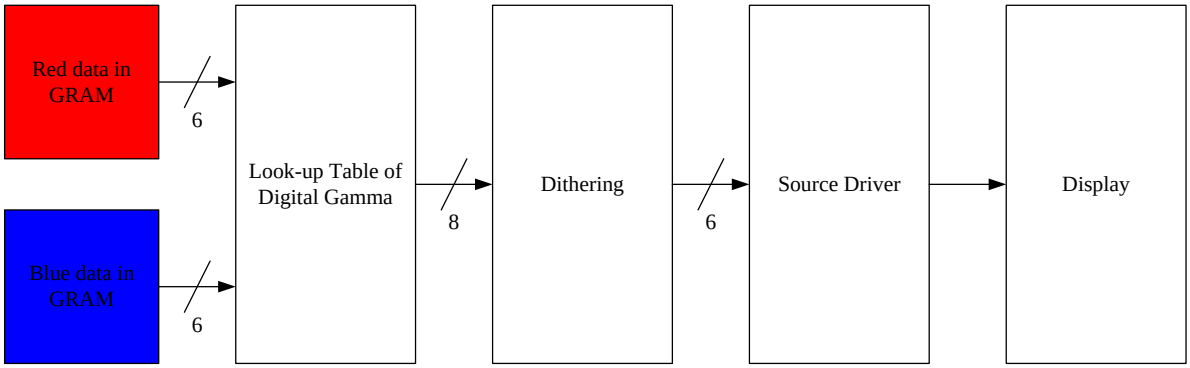
Source voltage of negative gamma level

Gamma level	Related Register	Formula
VN0	V0N[3:0]	VBN-(VBN-VAN)*(129R-V0N[3:0]R)/129R
VN1	V1N[5:0]	VBN-(VBN-VAN)*(128R-V1N[5:0]R)/129R
VN2	V2N[5:0]	VBN-(VBN-VAN)*(128R-V2N[5:0]R)/129R
VN3	J0N[1:0]	(VN2-VN4)*J0N[1:0]+VN4
VN4	V4N[4:0]	(VN2-VN20)*(57R-V4N[4:0])/60R+VN20
VN5	J0N[1:0]	(VN4-VN6)*J0N[1:0]+VN6
VN6	V6N[4:0]	(VN2-VN20)*(47R-V6N[4:0])/60R+VN20
VN7	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN8	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN9	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN10	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN11	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN12	J0N[1:0]	(VN6-VN13)*J0N[1:0]+VN13
VN13	V13N[3:0]	(VN2-VN20)*(21R-V13N[3:0])/60R+VN20
VN14	--	(VN13-VN20)/(20-13)*(20-14)+VN20
VN15	--	(VN13-VN20)/(20-13)*(20-15)+VN20
VN16	--	(VN13-VN20)/(20-13)*(20-16)+VN20
VN17	--	(VN13-VN20)/(20-13)*(20-17)+VN20
VN18	--	(VN13-VN20)/(20-13)*(20-18)+VN20
VN19	--	(VN13-VN20)/(20-13)*(20-19)+VN20
VN20	V20N[6:0]	VBN-(VBN-VAN)*(128R-V20N[6:0]R)/129R
VN21	--	(VN20-VN27)/(27-20)*(27-21)+VN27
VN22	--	(VN20-VN27)/(27-20)*(27-22)+VN27
VN23	--	(VN20-VN27)/(27-20)*(27-23)+VN27
VN24	--	(VN20-VN27)/(27-20)*(27-24)+VN27
VN25	--	(VN20-VN27)/(27-20)*(27-25)+VN27
VN26	--	(VN20-VN27)/(27-20)*(27-26)+VN27
VN27	V27N[2:0]	(VN20-VN43)*(20R-V27N[2:0])/25R+VN43
VN28	--	(VN27-VN36)/(36-27)*(36-28)+VN36
VN29	--	(VN27-VN36)/(36-27)*(36-29)+VN36
VN30	--	(VN27-VN36)/(36-27)*(36-30)+VN36
VN31	--	(VN27-VN36)/(36-27)*(36-31)+VN36
VN32	--	(VN27-VN36)/(36-27)*(36-32)+VN36
VN33	--	(VN27-VN36)/(36-27)*(36-33)+VN36
VN34	--	(VN27-VN36)/(36-27)*(36-34)+VN36
VN35	--	(VN27-VN36)/(36-27)*(36-35)+VN36
VN36	V36N[2:0]	(VN20-VN43)*(11R-V36N[2:0])/25R+VN43
VN37	--	(VN36-VN43)/(43-36)*(43-37)+VN43

VN38	--	(VN36-VN43)/(43-36)*(43-38)+VN43
VN39	--	(VN36-VN43)/(43-36)*(43-39)+VN43
VN40	--	(VN36-VN43)/(43-36)*(43-40)+VN43
VN41	--	(VN36-VN43)/(43-36)*(43-41)+VN43
VN42	--	(VN36-VN43)/(43-36)*(43-42)+VN43
VN43	V43N[6:0]	VBN-(VBN-VAN)*(128R-V43N[6:0]R)/129R
VN44	--	(VN43-VN50)/(50-43)*(50-44)+VN50
VN45	--	(VN43-VN50)/(50-43)*(50-45)+VN50
VN46	--	(VN43-VN50)/(50-43)*(50-46)+VN50
VN47	--	(VN43-VN50)/(50-43)*(50-47)+VN50
VN48	--	(VN43-VN50)/(50-43)*(50-48)+VN50
VN49	--	(VN43-VN50)/(50-43)*(50-49)+VN50
VN50	V50N[3:0]	(VN43-VN61)*(54R-V50N[3:0])/60R+VN61
VN51	J1N[1:0]	(V5N0-VN57)*J1N[1:0]+VN57
VN52	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN53	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN54	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN55	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN56	J1N[1:0]	(VN50-VN57)*J1N[1:0]+VN57
VN57	V57N[4:0]	(VN43-VN61)*(44R-V57N[4:0])/60R+VN61
VN58	J1N[1:0]	(VN57-VN59)*J1N[1:0]+VN59
VN59	V59N[4:0]	(VN43-VN61)*(34R-V59N[4:0])/60R+VN61
VN60	J1N[1:0]	(VN59-VN61)*J1N[1:0]+VN61
VN61	V61N[5:0]	VBN-(VBN-VAN)*(64R-V61N[5:0]R)/129R
VN62	V62N[5:0]	VBN-(VBN-VAN)*(64R-V62N[5:0]R)/129R
VN63	V63N[3:0]	VBN-(VBN-VAN)*(23R-V63N[3:0]R)/129R

10.10.. Gray voltage generator for digital gamma correction

ST7796U digital gamma function can implement the RGB gamma correction independently. ST7796U utilizes look-up table of digital gamma to change ram data, and then display the changed data from source driver. The following diagram shows the data flow of digital gamma.

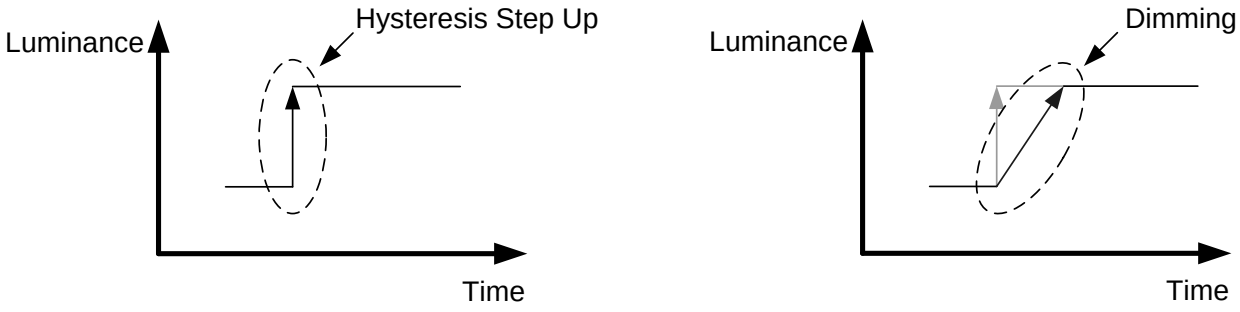


Block diagram of digital gamma

There are 2 registers and each register has 64 bytes to set R, G, B gamma independently. When bit DGMEN be set to 1, R and B gamma will be mapped via look-up table of digital gamma to gray level voltage.

10.11.. Display Dimming

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. This dimming function curve is the same in increment and decrement. The basic idea is described below.



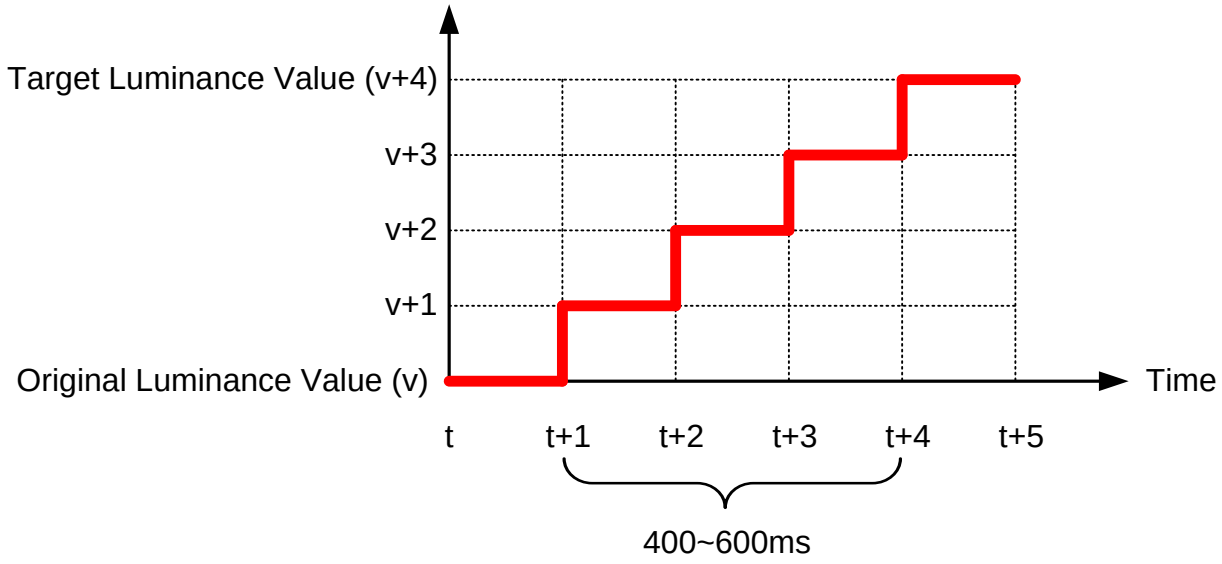
Dimming function can be enable and disable. See “Write CTRL Display (53h)” (bit DD) for more information.

10.11.1 Dimming Requirement

Dimming function in the display module should be implemented so that 400-600ms is used for the transition between the original brightness value and the target brightness value. The transferring time steps between these two brightness values are equal making the transition linear.

The dimming function is working similarly in both upward and downward directions.

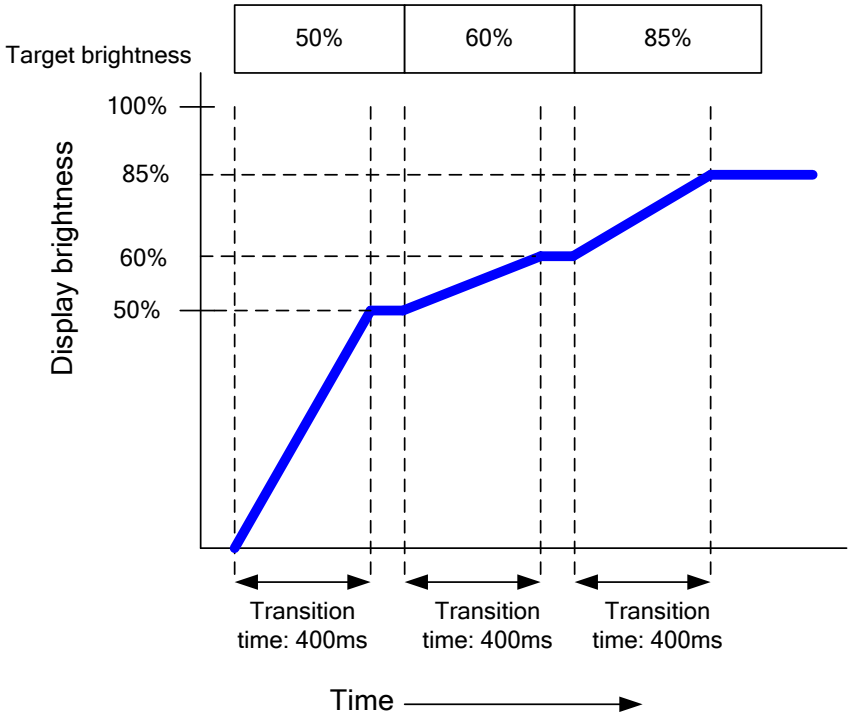
An upward example is illustrate below



10.11.2 Definition of brightness transition time

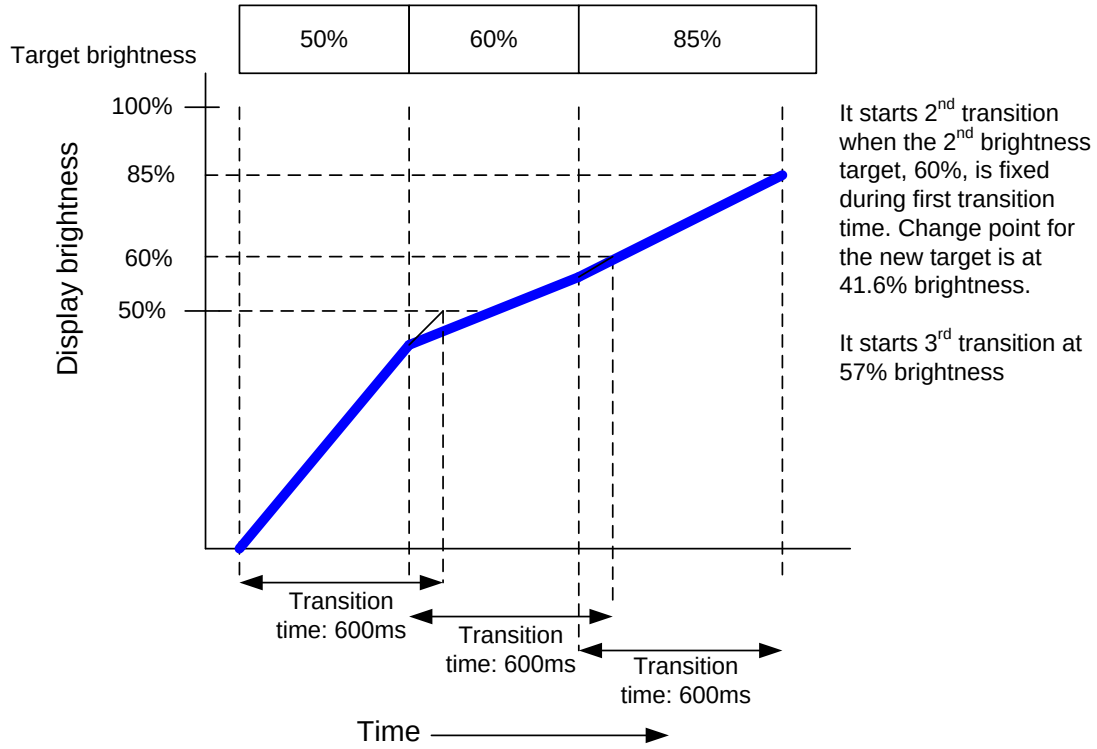
- Shorter transition time than 500ms.

There is some stable time between transitions. Below drawing is for transition time: 400ms.



- Longer transition time than 500ms

There is no any stable time between transitions. Below drawing is for transition time: 600ms.



10.12.. Content Adaptive Brightness Control (CABC)

10.12.1 Definition of CABC

A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content gray level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted gray level scale and thus the power consumption reduction

Definition of Modes and target power reduction ratio:

- Off mode: Content Adaptive Brightness Control functionality is totally off.
- UI [User interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less.
- Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%.
- Moving image mode: Optimized for moving image. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%.

Note 1: Updating partial area of the image data should be supported by CABC functionality.
Note 2: Processing power consumption of CABC should be minimized.

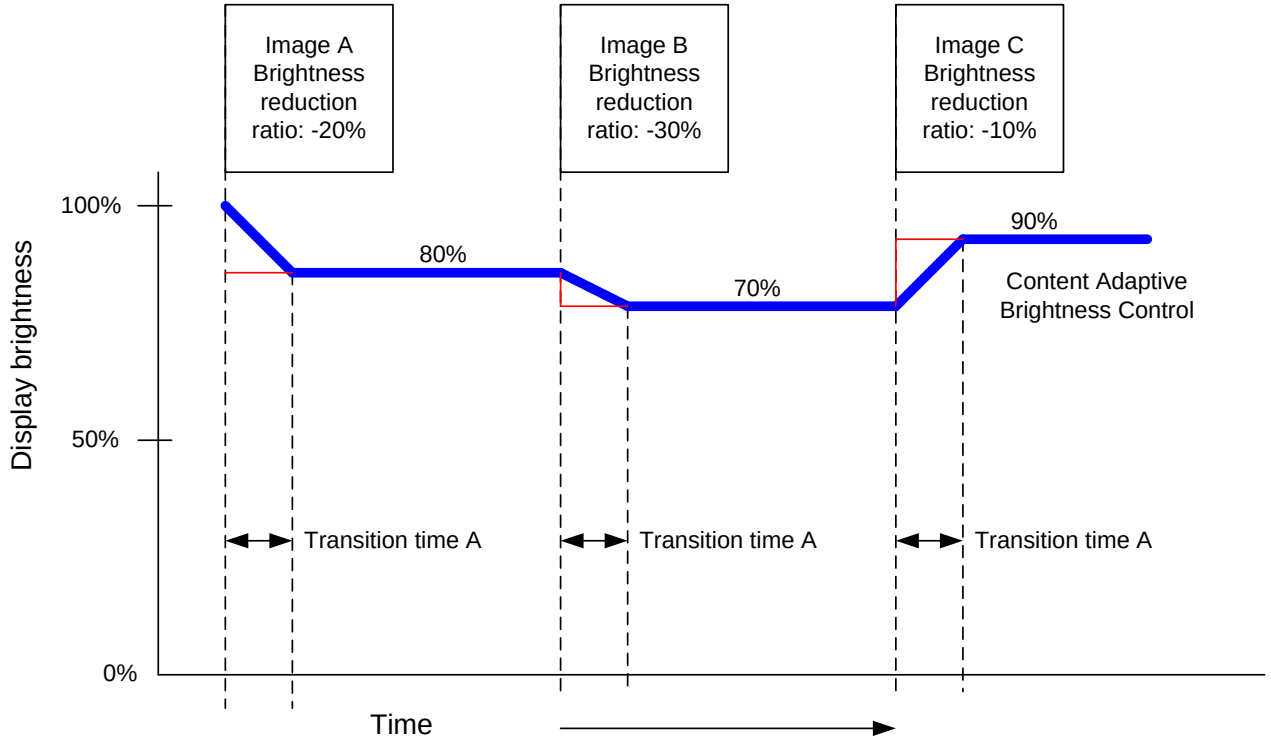
The transition time for dimming function is illustrated below.

- Content Adaptive Brightness Control

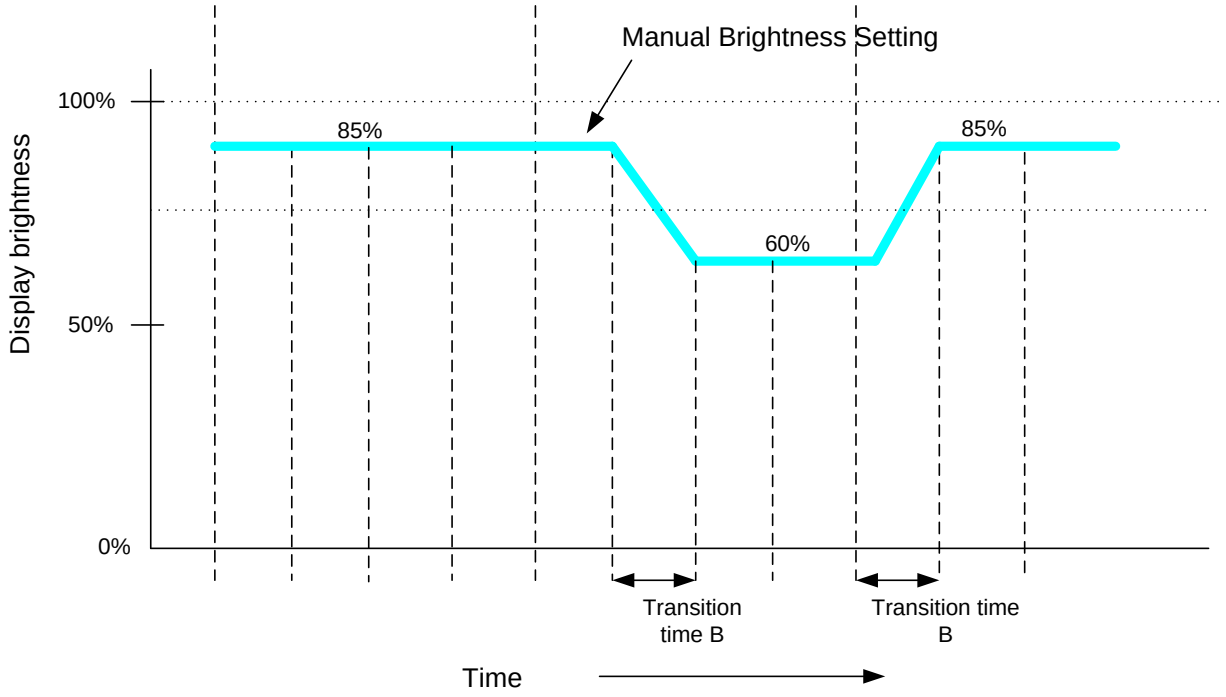
Display brightness is changed, according to the image contents. The following graph mentions the case of displaying three different images.

- Image A: -20% brightness reduction
- Image B: -30% brightness reduction
- Image C: -30% brightness reduction

Transition time from the previous image to the current displayed image is “transition time A”.



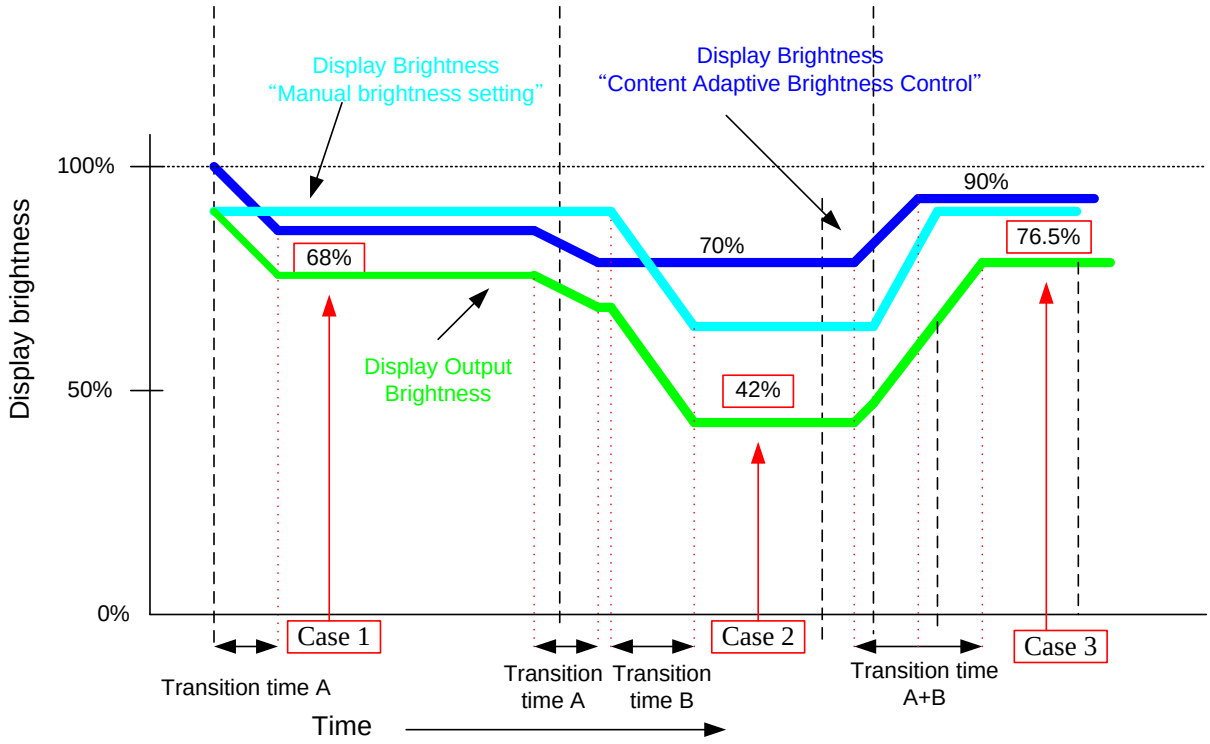
● Manual brightness setting and Dimming function



● Combine Display brightness

Green line in the following graph is for the output brightness of display. It is combined with both display brightness, which are defined in the above graphs.

Maximum transition time is transition time A+B.



Brightness level calculates with the following formula.

Display Output brightness = Manual Brightness setting * CABC brightness ratio

	Manual Brightness setting	Brightness ratio [CABC]	Display Output brightness
Case 1	85%	80%	68%
Case 2	60%	70%	42%
Case 3	85%	90%	76.5%

Transition time from the current brightness to target brightness is A+B in the worst case.

10.12.2 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the LABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting is to avoid too much brightness reduction. When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. If CABC algorithm works without any abnormal visual effect, image processing function can operate even when the brightness can not be changed.

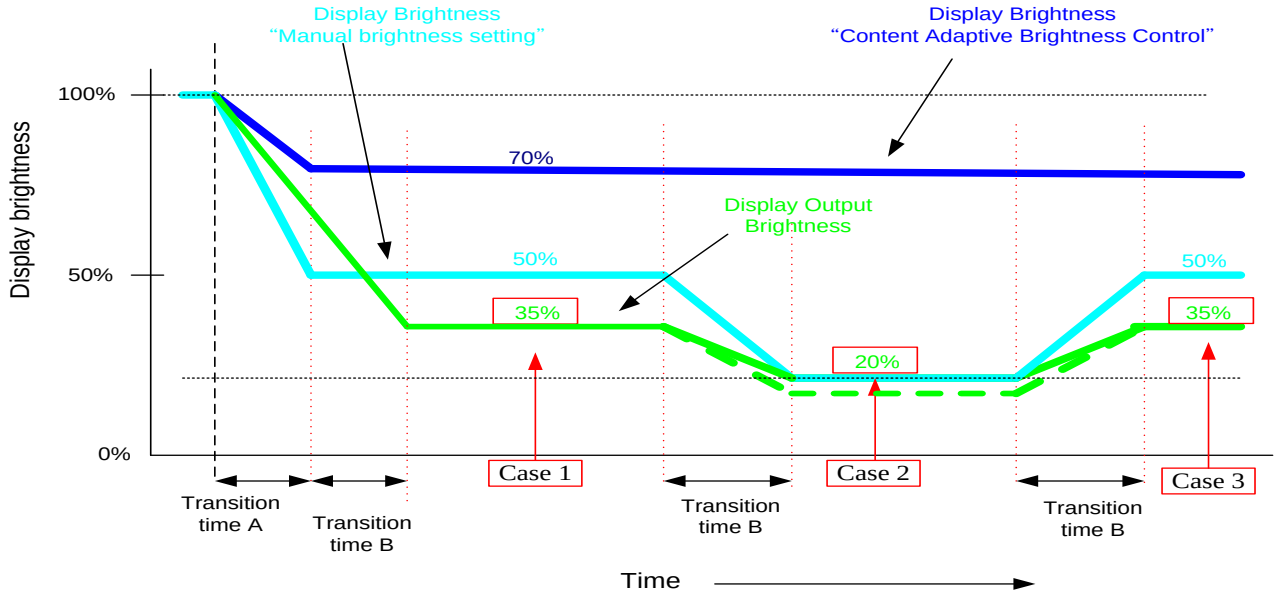
This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of “9.2.39 Write CTRL Display (53h)”), CABC minimum brightness setting is ignored. “9.2.44 Read CABC minimum brightness (5Fh)” always read the setting value of “9.2.43 Write CABC minimum brightness (5Eh)”.

	WRCABC (55h)	Function	RDCABCMB (5Fh)	Image
Sleep-in		NA	WRCABCMB (5Eh)	
CABC off	00b	Disable	WRCABCMB (5Eh)	Original
CABC on	01b/10b/11b	Enable	WRCABCMB (5Eh)	CABC modified

Brightness level calculates with the following formula.
Display Output Brightness = Manual brightness setting * CABC brightness ratio

Below drawing is for the explanation of the CABC minimum brightness setting.



CABC minimum brightness value = 51 (33h: 20% display brightness)

	Display Brightness [manual setting]	Brightness ratio [CABC]	Calculation result of the display brightness formula	Display Output Brightness	Image
Case 1	50%	70%	35%	35%	CABC modified
Case 2	20%	70%	14%	20%	CABC modified
Case 3	50%	70%	35%	35%	CABC modified

At the case 2, the calculation result of the display brightness is 14%. CABC minimum brightness value is set to 20% brightness. Actual display brightness is 20% as the CABC minimum brightness setting.

11 Power Definition

11.1.. Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

4. **Sleep In Mode**

In this mode, the DC: DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

1. Power Off Mode

In this mode, both VDD and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

11.2.. Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

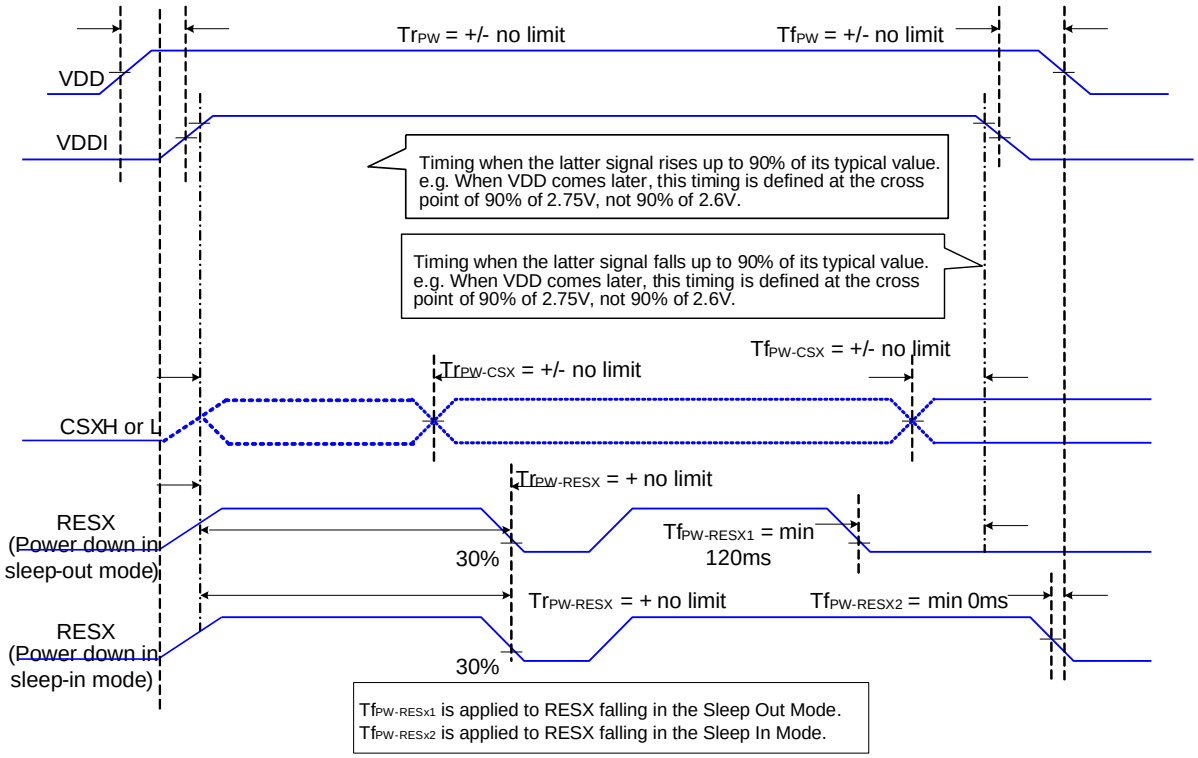
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

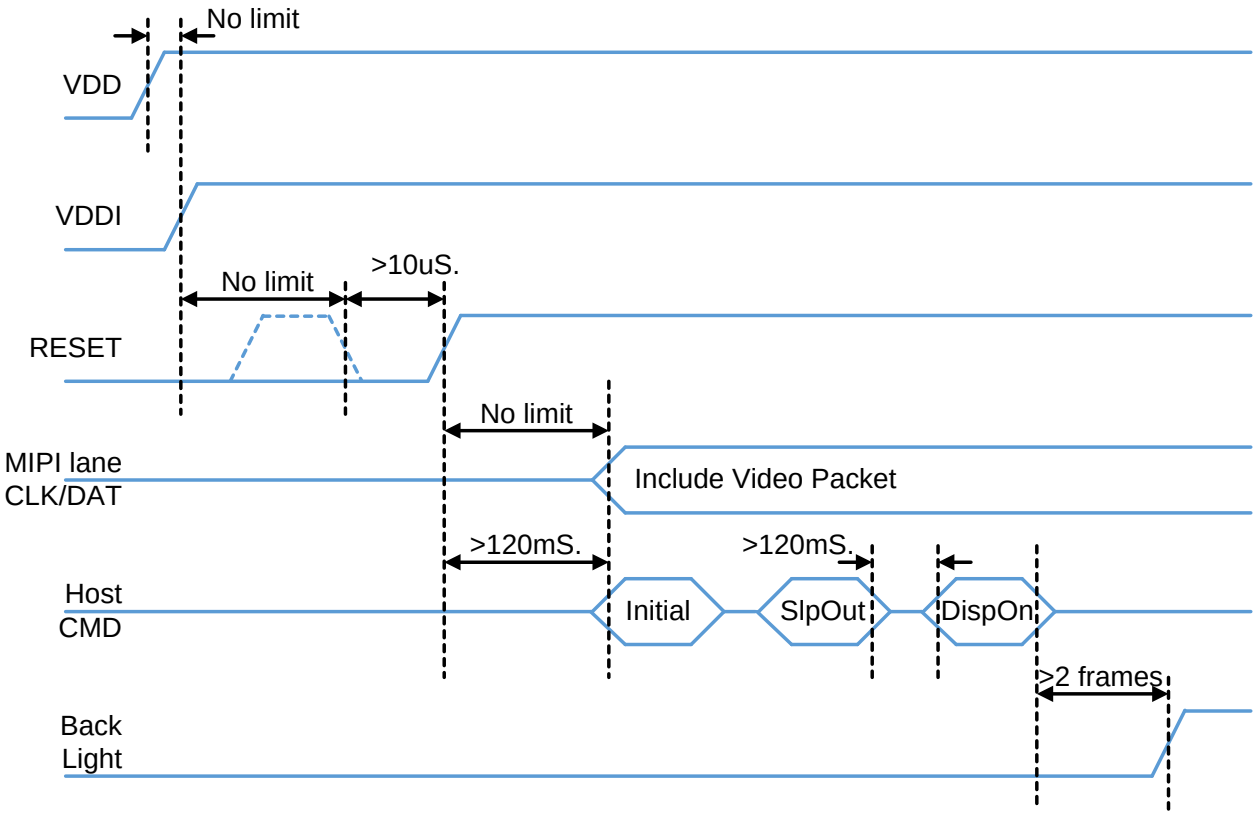
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below (320RGB x 480)



The power on/off sequence is illustrated below for other resolution (less than 320RGB x 480)

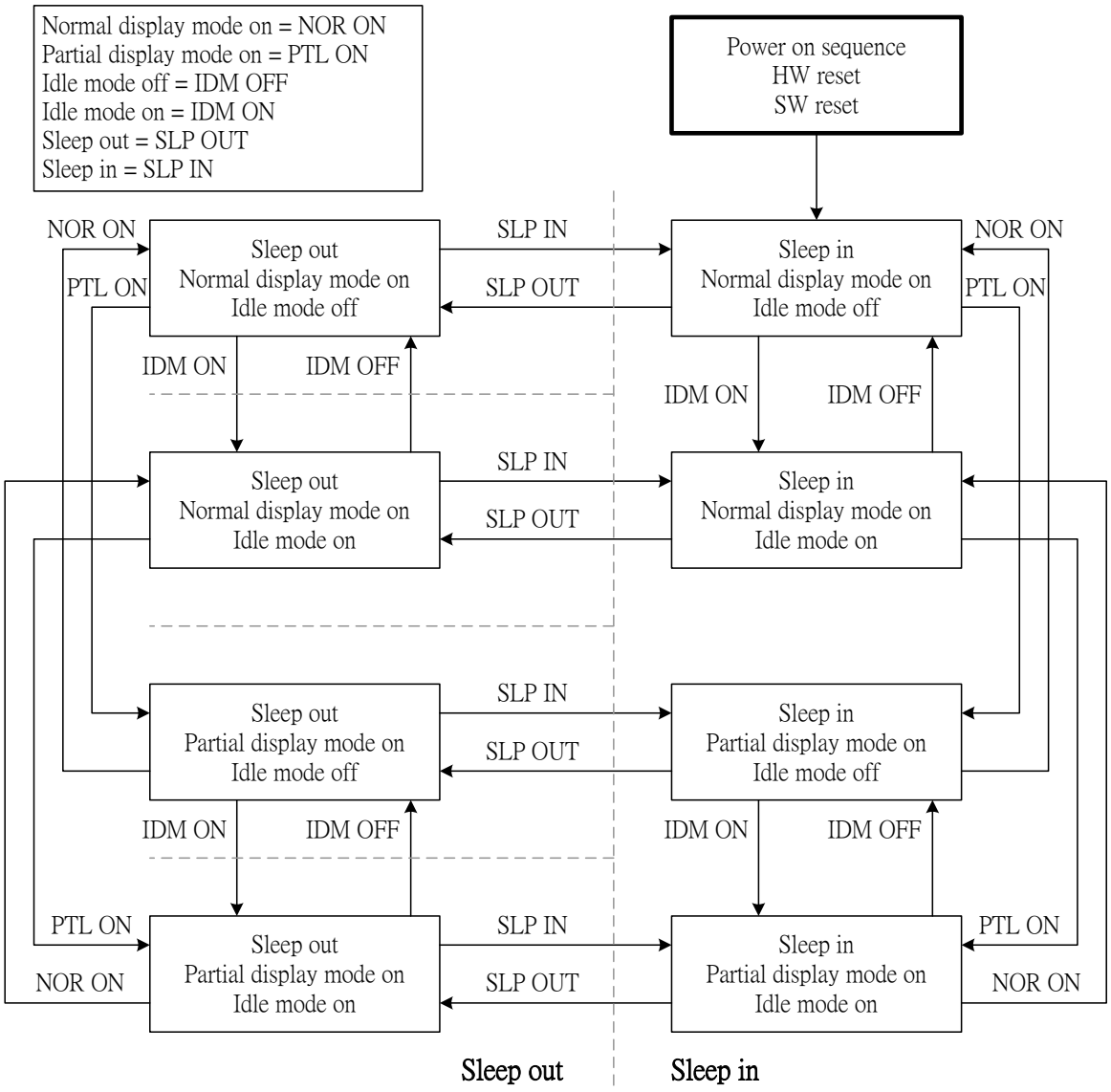


11.3.. Uncontrolled Power OFF

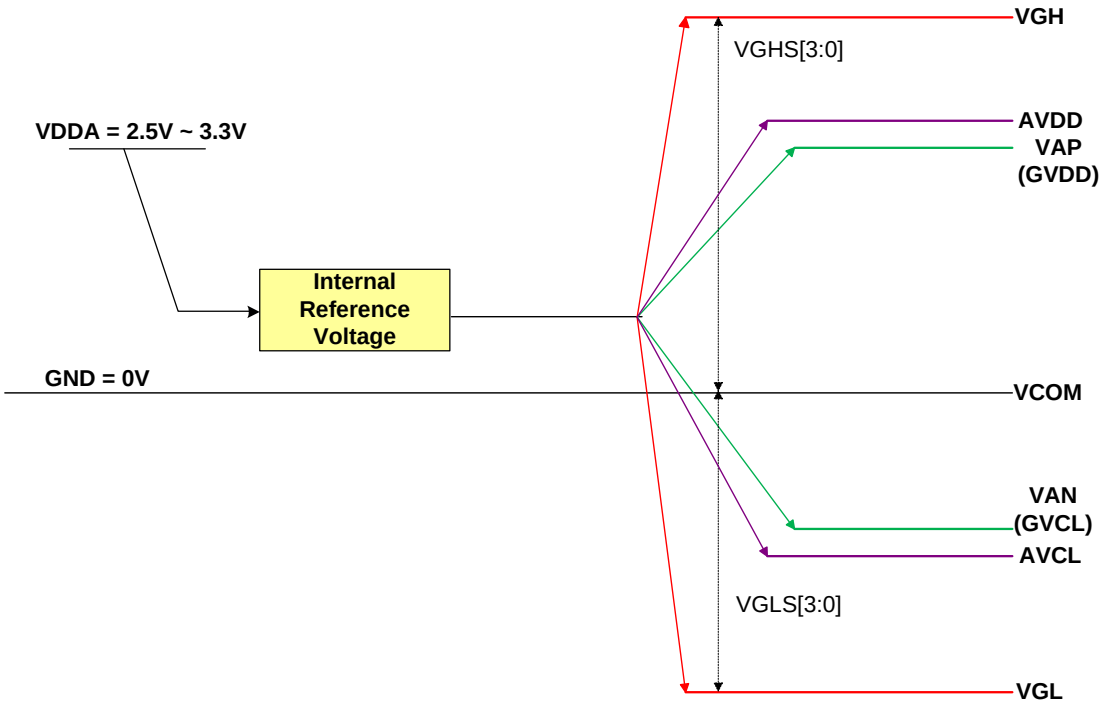
The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.

11.4.. Power Flow Chart

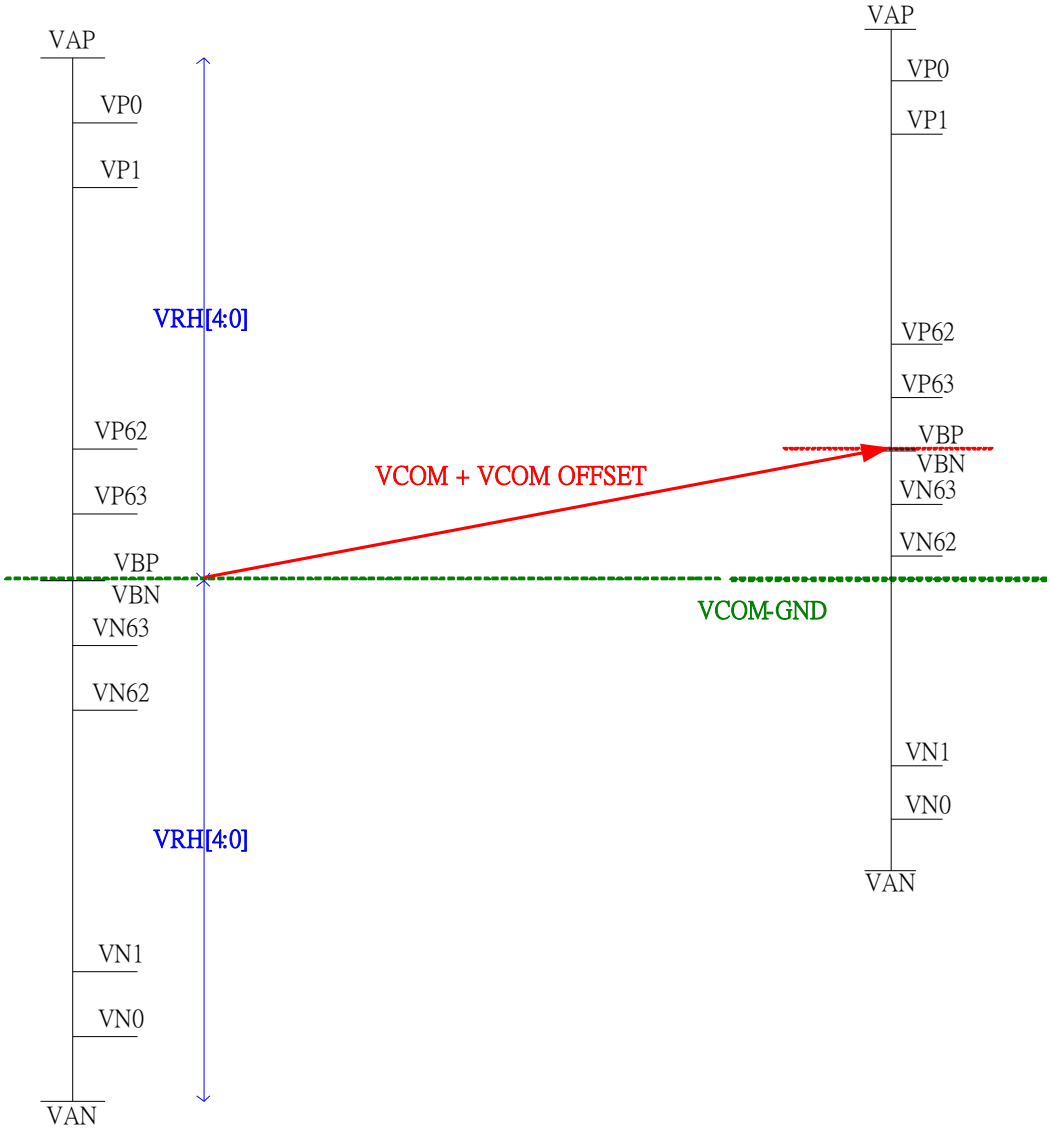


11.5.. Voltage Generation

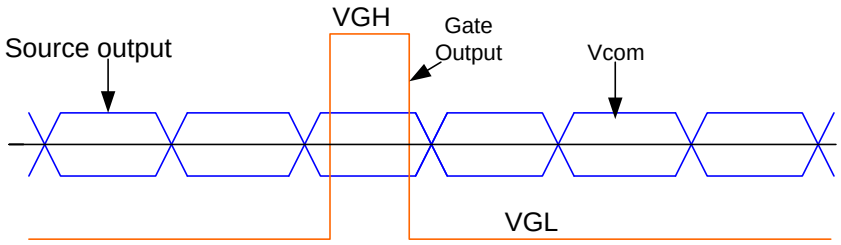


11.6.. Relationship about source voltage

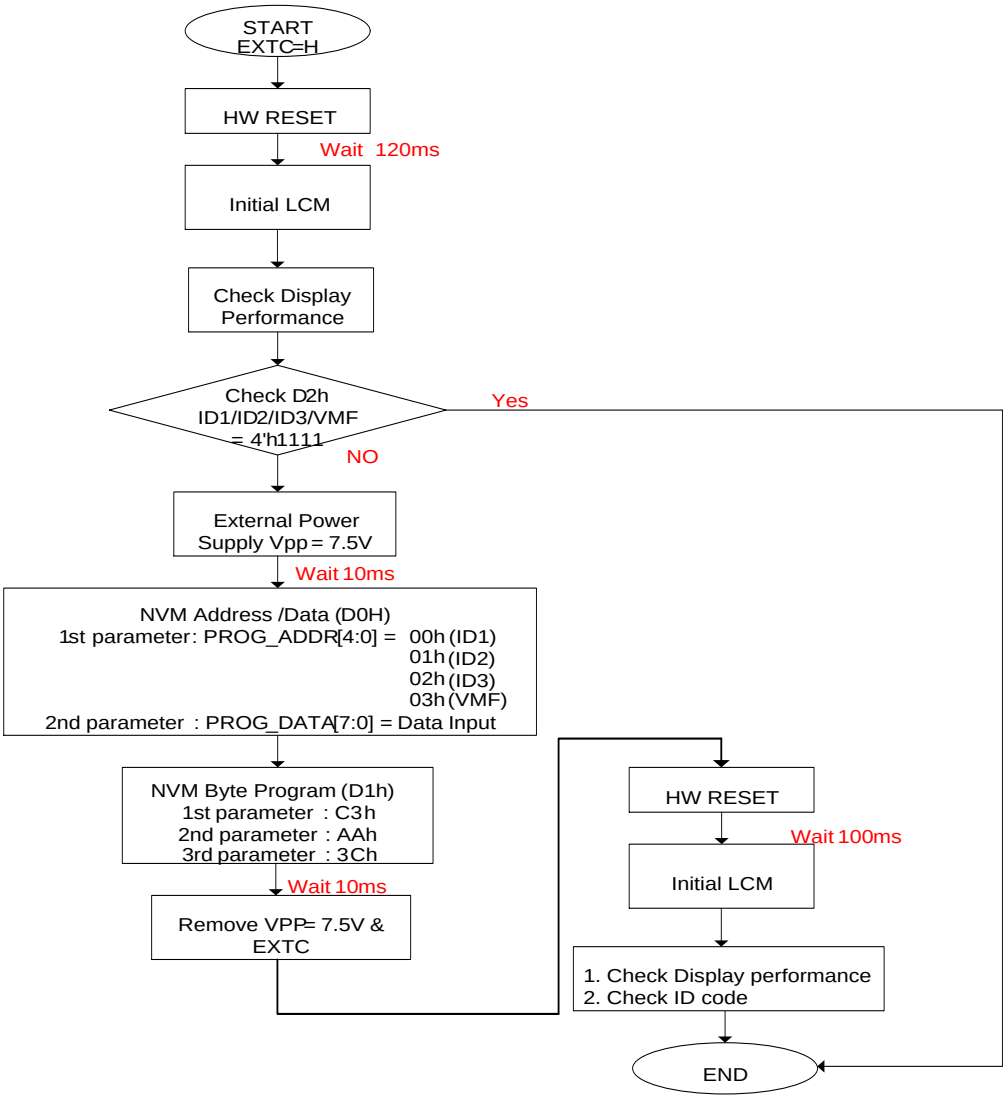
The relationship about source voltage is shown as below:



11.7.. Applied Voltage to the TFT panel

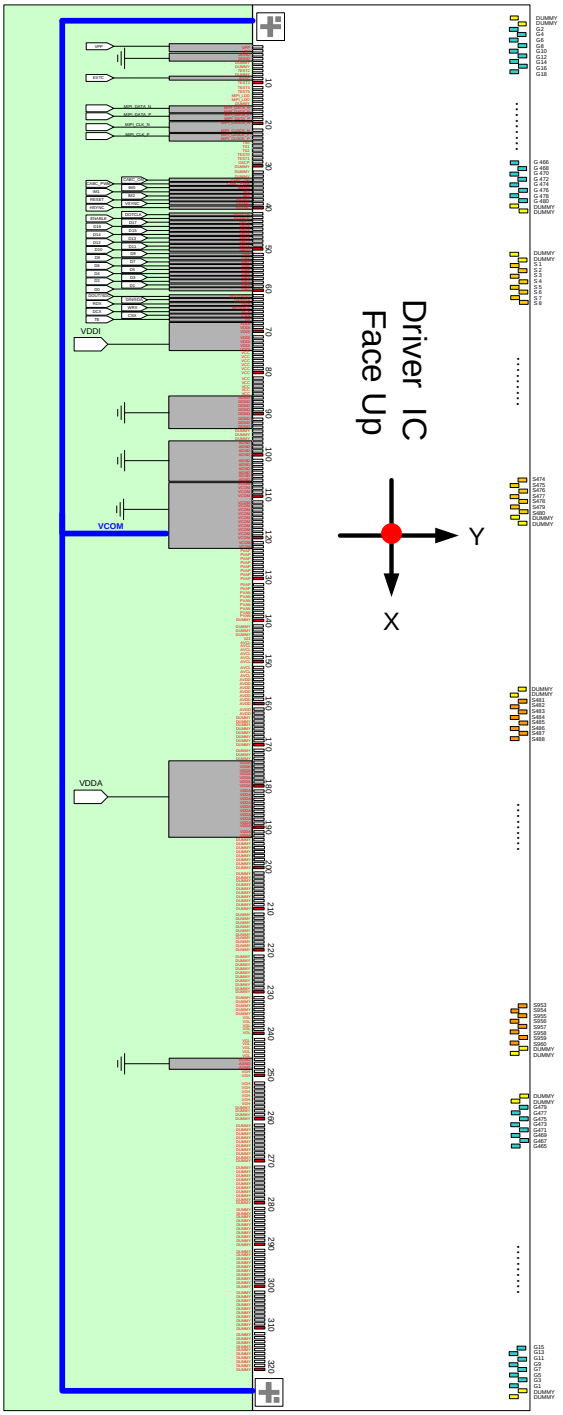


12 NVM Programming Flow



13 Application Note

13.1.. FPC Suggestion



13.2.. Layout Resistance Suggestion

Pin Name	Type	Maximum Resistance	
VDDI, VDDA, AGND, DGND	Power supply	10	Ω
VPP	Power supply	10	Ω
VCOM	Common Electrode	10	Ω
MIPI_CLK_P MIPI_CLK_N MIPI_DATA_P MIPI_DATA_N	MIPI	10	Ω
IM[2:0], RESET, CSX, DCX, RDX, WRX, VSYNC, HSYNC, ENABLE, DOTCLK	I	100	Ω
TE, CABC_PWM, CABC_ON, SDO	O	100	Ω
DB[17:0], SDA	I/O	100	Ω

14 REVISION HISTORY

Version	Date	Description
V1.0	2020/02	First Issue